Chapter

MRAM-Based FPGAs: A Survey

Peyton Chandarana, Mohammed Elbtity, Ronald F. DeMara and Ramtin Zand

Abstract

Over the last decade, field programmable gate arrays (FPGAs) have embraced heterogeneity in a transformative way by leveraging emerging memory devices along with conventional CMOS-based devices to realize technology-specific benefits. Memristive device technologies exhibit desirable characteristics such as non-volatility, scalability, near-zero leakage, radiation hardness, and more, making them promising alternatives for SRAM cells found in conventional SRAM-based FPGAs. In recent years, a significant amount of research has been performed to take advantage of these emerging technologies to develop fundamental building blocks of FPGAs like hybrid CMOS-memristive look-up tables (LUTs) and configurable logic blocks (CLBs). In this chapter, we will provide a brief overview of the previous work on hybrid CMOS-memristive FPGAs and their corresponding opportunities and challenges.

Keywords: magnetoresistive random-access memory (MRAM), non-volatile FPGA, MRAM-based look-up table, hybrid configurable logic block, heterogeneous technology reconfigurable fabric

1. Introduction

Since the advent of the first field programmable gate array (FPGAs), there has been a gradual transition from traditional homogeneous reconfigurable fabrics, designed with one type of logic block, to the now modern heterogeneous FPGAs with special-purpose co-processors to handle specific tasks such as floating point arithmetic [1, 2]. In recent years, a new type of heterogeneity has attracted the attention of both academia and industry which involves leveraging emerging logic and memory devices within FPGA fabrics to realize technology-specific advantages such as non-volatility, scalability, low leakage power, radiation hardness, etc. Some of the most promising technologies that have been proposed as alternatives for static random access memory (SRAM) cells in FPGAs are resistive random-access memory (RRAM) [3–6], phase-change memory (PCM) [7–9], and magnetoresistive random-access memory (MRAM) [10–14]. In this chapter, we specifically focus on MRAM-based FPGAs, but the underlying circuits and architectures discussed can be readily utilized for other resistive memory technologies.

Magnetic tunnel junctions (MTJs) are considered to be the primary component of MRAM devices. **Figure 1** shows an example of the MTJ stack structure [15], which includes two ferromagnetic (FM) layers (CoFeB), called the pinned and free layers,

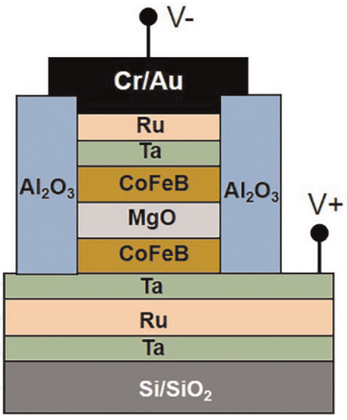

Figure 1.
MTJ stack structure [15].

that are separated by a thin oxide layer (MgO). The magnetization direction of the electrons in the pinned layers is fixed, while that of the free layer can switch to the parallel (P) or anti-parallel (AP) states with reference to the fixed layer. The resistance of an MTJ (R_{MTJ}) depends on the angle between the magnetization orientation of the FM layers (θ), as expressed in the below equation [16]:

$$R_{MTJ}(\theta) = \frac{2R_{Stack}(1+TMR)}{2+TMR(1+\cos\theta)} = \begin{cases} R_P = R_{Stack}, & \theta = 0 \\ R_{AP} = R_{Stack}(1+TMR), & \theta = \pi \end{cases} \quad (1)$$

where $R_{Stack} = \frac{RA}{Area}$, in which the resistance-area product (RA) value is determined by the material composition of MTJ's layers. Moreover, TMR is the tunneling magnetoresistance, which depends on the temperature (T) and bias voltage (V_b) as seen below [16]:

$$TMR(T, V_b) = \frac{2P^2\left(1-\alpha_{sp}T^{3/2}\right)^2}{1-P^2\left(1-\alpha_{sp}T^{3/2}\right)^2} \cdot \frac{1}{1+\left(\frac{V_b}{V_0}\right)^2} \quad (2)$$

where V_0 is a fitting parameter, α_{sp} is a material-dependent constant, and P is the spin polarization factor [16]. **Table 1** lists the experimental parameters used herein to model the MTJ devices. Spin transfer torque (STT) [18] is the conventional approach

Parameters	Description	Value
Area	MTJ surface	$65nm \times 65nm \times \pi/4$
RA	MTJ resistance-area product	$5\ \Omega.\mu m^2$
T	Temperature	358 K
P	Polarization	0.52
V_0	Fitting parameter	0.65
α_{sp}	Material-dependent constant	2e-5

Table 1.
Parameters of STT-MTJ device [16, 17].

to switch the resistance state of the MTJ, where a bidirectional charge current flows through the fixed layer of the MTJ. This, in turn, generates a spin-polarized current that switches the magnetization orientation of the electrons in the free layer. Recently, it has been shown that passing a charge current through a heavy metal can generate a spin-polarized current with a ratio greater than one [19]. This means the produced spin current can be larger than the applied charge current, and thus, lower energy switching can be achieved in the MRAM cells. Readers can refer to [20] for further details about the fundamentals and modeling of MRAM devices. Proceeding with this background information on MRAM cells, we can now introduce how MRAM technology can be used as an alternative for SRAM to realize the building blocks of FPGAs, such as look-up tables (LUTs) and configurable logic blocks (CLBs).

2. MRAM-based look-up table (LUT) circuits

Look-up tables (LUTs) are the main building blocks in FPGAs that allow combinational and sequential logic circuits to be realized. An n-input LUT circuit includes: (1) 2^n memory cells, containing a truth table of an n-input Boolean logic function, and (2) a select tree used to return the value stored in a specific memory cell specified by an address passed into the LUT circuit. Conventional LUT circuits consist of memory cells implemented using SRAM technology. This, however, introduces multiple challenges with respect to:

- *High static power*: Caused by the intrinsic leakage current which increases as the transistor size decreases.

- *Volatility*: SRAM's volatility limits the energy savings that could be achieved by power-gating in FPGAs. All functions must be reprogrammed upon each power-up, and therefore, external non-volatile memory is needed to reprogram all the functions upon each power-gating cycle.

- *Low logic density*: Each SRAM cell consists of six transistors which increases logic and memory footprint at scale.

In recent years, various MRAM-based LUT circuits have been proposed, where MRAM technology replaces SRAM. Similar to conventional SRAM-based LUTs, MRAM-LUTs have two operation phases: (1) the *configuration phase*, during which the states of the MTJs in MRAM cells are adjusted based on the Boolean logic function being stored in the LUT, and (2) the *read phase*, which involves reading the state of the MTJ devices in the MRAM-LUT to realize a Boolean function. The configuration operation of the MRAM cell requires special write circuitry to generate a sufficiently large spin current to switch the state of the MTJs. **Figure 2** Shows four well-known circuits introduced in the literature for the MRAM write operation.

The LUT read operation, on the other hand, involves sensing the resistive states of MRAM cells and generating the corresponding Boolean outputs, that is, "0" and "1". A commonly used circuit for reading the state of the MTJs is a pre-charge sense amplifier (PCSA) shown in **Figure 3**. The PCSA circuit reads the MTJ states in two steps that could be performed in one clock cycle: (1) the *pre-charge step*, in which the CLK signal is in a low state (GND) that leads to turning the MP0 and MP3 PMOS transistors on, and thus, the OUT and OUT' nodes are charged to VDD, and (2) the *discharge phase*,

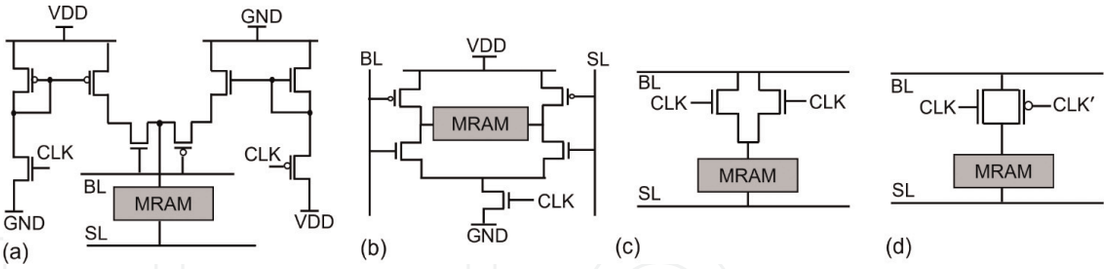

Figure 2.
Various MRAM write circuits circuit structure. (a) Current mirror write circuit [21], (b) proposed in [21], (c) proposed in [22], (d) proposed in [23].

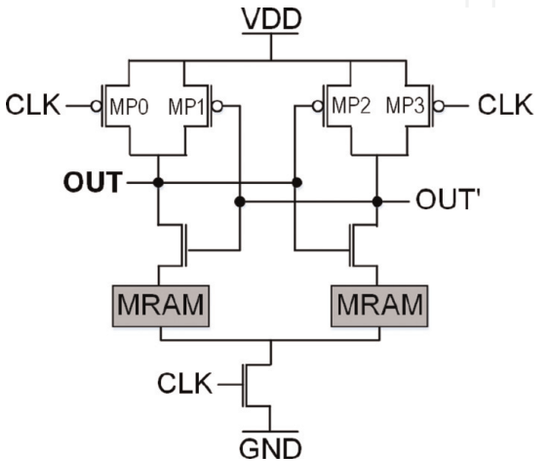

Figure 3.
PCSA circuit schematic.

where CLK signal is in a high state (VDD) which turns off all the PMOS transistors (MP0-MP3) and consequently disconnects the OUT and OUT' nodes from the voltage source (VDD). Therefore, the pre-charged OUT and OUT' nodes begin discharging. The discharge speed in each of the branches of the PCSA relies on the total resistance of each branch which, itself, depends on the resistance of the MRAM device connected to it. The branch of lower resistance discharges faster than the other and therefore turns on the PMOS transistor connected to the branch of higher resistance. This causes the opposite output node of the lower-resistance branch to connect to the VDD, while the output node connected to the lower-resistance branch discharges completely to GND. A comprehensive survey of various PCSA circuits designed for sensing MRAM cells is provided in [24].

One of the pioneering works on MRAM-LUT circuit design belongs to Zhao et al. [25], in which one PCSA circuit is used to sense each bit of the LUT, as shown in **Figure 4a**. The write circuits store each bit of the Boolean function in one MRAM cell and its inverse in another as a reference resistive memory that is used by the PCSA circuit to read the cells. A select tree is then used to read the corresponding MRAM cell, based on the input of the LUT circuit. However, the use of one PCSA per cell in the LUT for reading has led to significant energy and area overheads. Therefore, in 2012, Suzuki et al. [26] proposed an optimized MRAM-LUT design, in which only one PCSA is used in the LUT architecture as shown in **Figure 4b**. One branch of the PCSA is connected to the select tree and LUT MRAM cells, while the other branch is connected to a reference tree and a combination of MRAM devices. Reference tree

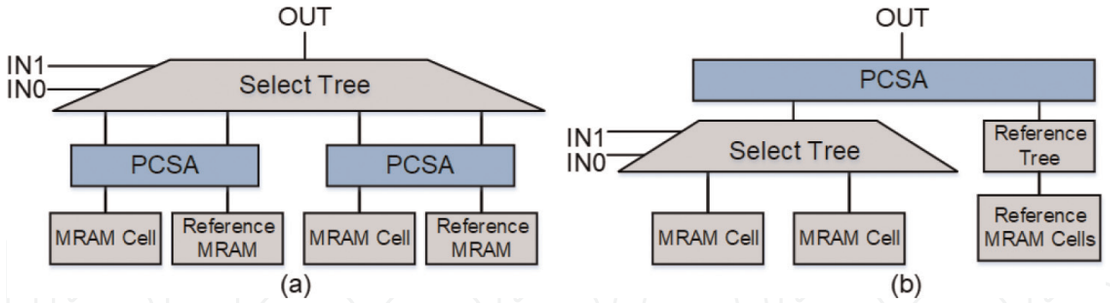

Figure 4.
Basic MRAM-LUT circuit structure: (a) proposed in [25], and (b) proposed in [26].

compensates for the resistance of the select tree and the reference MRAM cells provide a total resistance value between the high resistance (R_{AP}) and low resistance (R_P) of the LUT MRAM cells. With this modification in the circuit, Suzuki et al. [26] achieved a 44% reduction in active power compared to the MRAM-LUT designed in [25]. Another well-known MRAM-LUT circuit is proposed by Zand et al. in [27]. Instead of using multiple MRAM cells to form a reference MRAM cell, Zand et al. adjusted the area of a single MTJ such that its resistance in the parallel (P) state is between the high resistance (R_{AP}) and low resistance (R_P) of the main MRAM cells in the LUT circuit. This simple modification led to a 34% improvement in the power-delay-product (PDP) value compared to the MRAM-LUT design proposed by Suzuki et al. in [26].

2.1 Modern MRAM-LUT circuits

Most modern FPGAs utilize more versatile LUT structures in their architecture compared to the basic designs introduced in the previous subsection. Intel FPGAs, for example, the Arria®series, Cyclone®V, and Stratix®V, use adaptive logic modules (ALMs) as their building blocks. This can simultaneously realize various types of functions such as two independent 4-input functions, a 5-input and a 3-input function, two 5-input functions, which share two inputs, and so on [28]. Similarly, Xilinx FPGAs, for example, the Virtex-7 Family, employ fracturable 6-input LUTs in their design that can realize an independent 6-input function or two 5-input functions, if they share five inputs. Recently, there have been some efforts to design novel MRAM-LUT circuits that can support functionalities similar to those of modern LUT circuits. Here, we focus on two of the well-known designs in this area, that is, *adaptive MRAM-LUT* and *fracturable MRAM-LUT* proposed in [27, 29], respectively.

2.1.1 Adaptive MRAM-LUT design

Figure 5 shows a 4-input adaptive MRAM-LUT circuit proposed in [27], which can be configured to realize different functions. There are seven types of functions that can be implemented by the 4-input adaptive MRAM-LUT: four 2-input Boolean functions, two 3-input functions, and one 4-input function. The output of each configuration is individually connected to the PCSA circuit through a mode selector that includes pass transistors to choose between the different operational modes listed in **Table 2**. For example, in Mode 0, the adaptive MRAM-LUT is configured to operate as a 2-input LUT and realize the logic function stored in MRAM0 thru MRAM3.

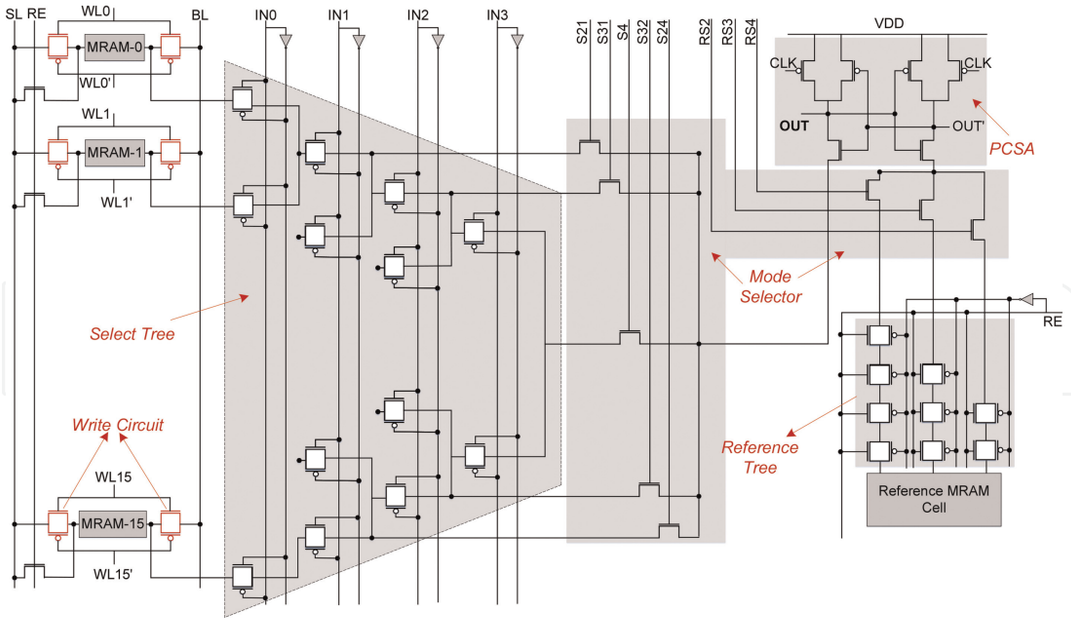

Figure 5.
The circuit diagram of a 4-input adaptive MRAM-LUT [27].

Mode	S21	S22	S23	S24	S31	S32	S4	RS2	RS3	RS4	MRAMs	Function
	1	0	0	0	0	0	0	1	0	0	0–3	2-input
	0	1	0	0	0	0	0	1	0	0	4–7	2-input
	0	0	1	0	0	0	0	1	0	0	8–11	2-input
	0	0	0	1	0	0	0	1	0	0	12–15	2-input
	0	0	0	0	1	0	0	0	1	0	0–7	3-input
	0	0	0	0	0	1	0	0	1	0	8–15	3-input
	0	0	0	0	0	0	1	0	0	1	0–15	4-input

Table 2.
Different operating modes in the 4-input adaptive MRAM-LUT.

2.1.2 Fracturable MRAM-LUT design

Figure 6 shows the structure of a six-input MRAM-LUT circuit proposed in [29], which includes MRAM-based storage cells, a select tree, a mode selector, and two PCSAs. The fracturable MRAM-LUT circuit is capable of implementing any six-input Boolean functions or two five-input Boolean functions if the inputs are shared. The M5 and M6 signals are used to select the 5-input or 6-input functional modes of the fracturable MRAM-LUT circuit, respectively. Zand and DeMara [30] have shown that fracturable MRAM-LUT circuits can achieve significant reductions in power consumption compared to their SRAM-based counterparts. However, they have also shown that MRAM-LUTs can be severely impacted by process variation (PV), while SRAM-LUTs exhibit no read errors in presence of PV.

There have been several efforts to address the PV challenges of MRAM-LUTs including the proposal of modular redundancy-based MRAM-LUT and clock-less MRAM-LUT circuits proposed in [30, 31], respectively. In [30], the authors identified the PCSA circuit as the most susceptible component of the MRAM-LUT and as a

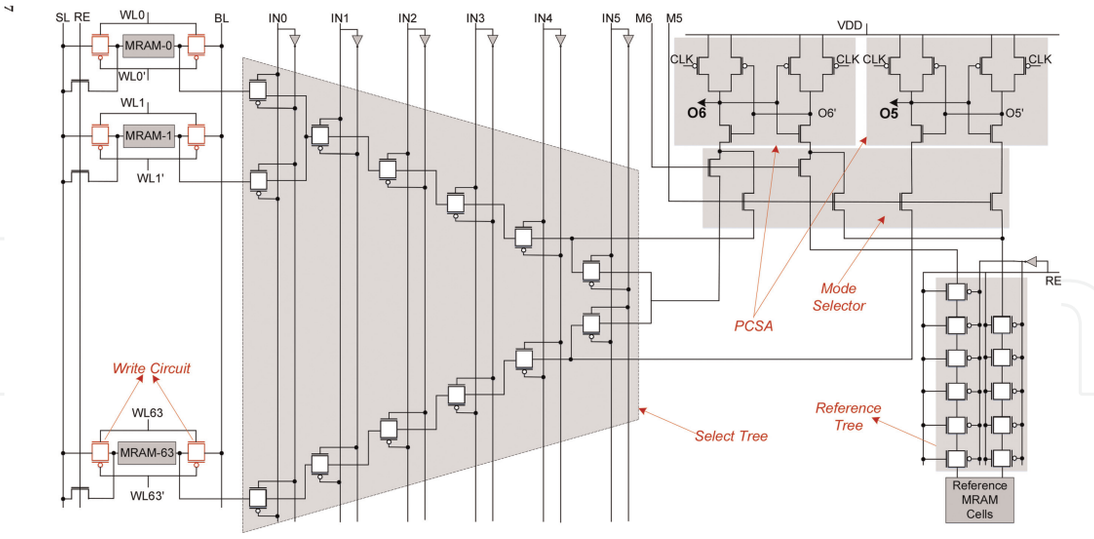

Figure 6.
The circuit diagram of a six-input fracturable MRAM-LUT [30].

result, proposed a triple modular redundancy method to alleviate the PV impacts. As shown in **Figure 7**, the proposed circuit includes three PCSAs and two voter circuits that determine the output of the LUT circuit based on the majority of the PCSA's outputs. The modular redundancy-based MRAM-LUT could successfully decrease the PV-induced read errors by more than 30% at the cost of a 24% and 6% increase in power consumption and area occupation, respectively.

In another effort to reduce the impact of PV on MRAM-LUT circuits, Salehi et al. [31] propose a fracturable MRAM-LUT design that uses two MRAM cells with differential magnetization polarities to represent each bit of the Boolean function stored in the LUT. This enables replacing the PCSA circuits, which are the main source of errors caused by PV in MRAM-LUTs, with a voltage divider circuit to read the states of the MTJs, as shown in **Figure 8**. Since the values stored in the MRAM cells are complementary, that is, one MRAM device is used to store the data value and the other as a reference, a wide read margin is realized, and this leads to a near zero error rate for the MRAM-LUT circuit in presence of various PV scenarios in both transistor and MRAM devices. However, as shown by Salehi et al. [31], PV-tolerance is achieved at the cost of increased power consumption compared to the PCSA-based MRAM-LUTs.

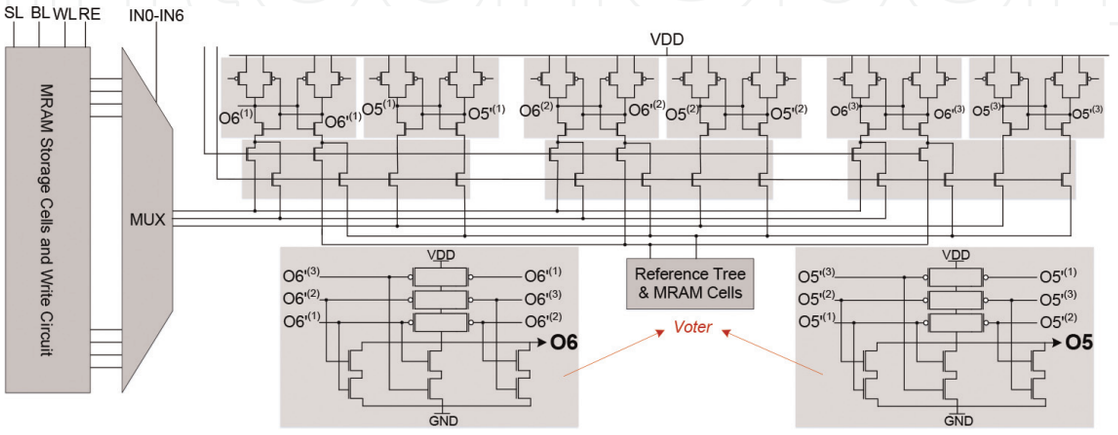

Figure 7.
The circuit diagram of a six-input modular redundancy-based fracturable MRAM-LUT [30].

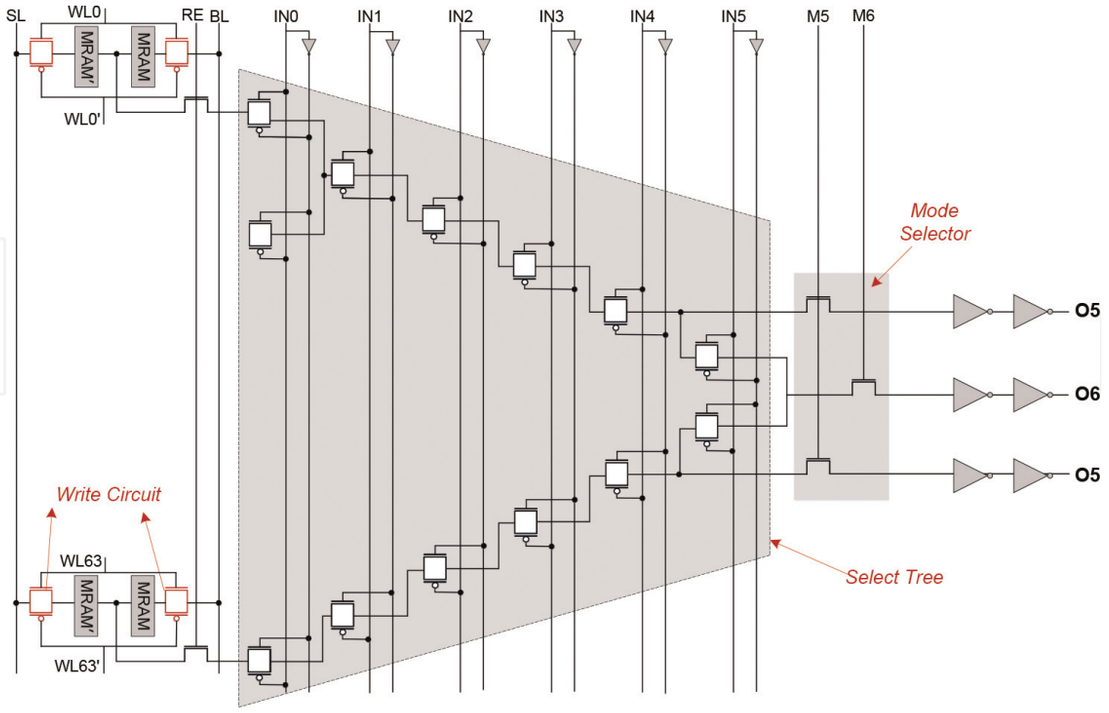

Figure 8.
The circuit diagram of a six-input fracturable MRAM-LUT that uses voltage divider circuits instead of PCSAs for the LUT's read operation [31].

3. MRAM-based FPGAs

Figure 9 shows the typical architecture of modern FPGAs, which include configurable logic blocks (CLBs), input–output blocks (IOBs), block RAMs, programmable switch matrices (SMs), and delay-locked loops (DLLs) for clock distribution. Bitstreams are used to store the logic functions in CLBs. Any new design of FPGAs that

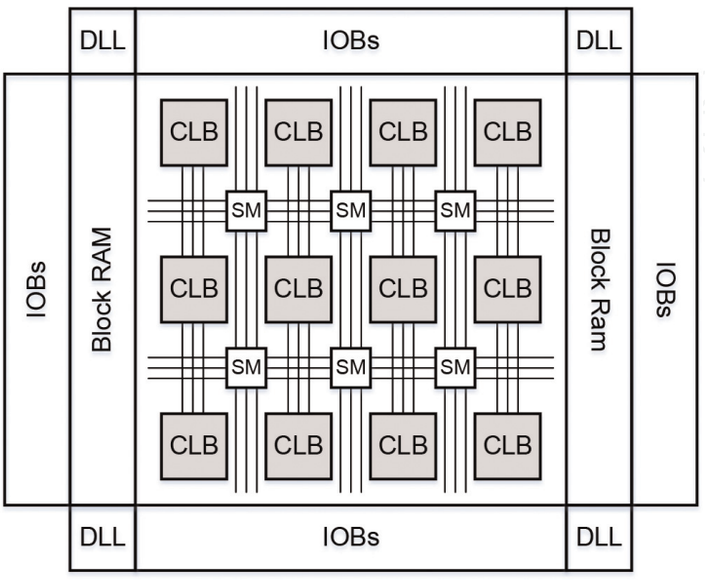

Figure 9.
A typical FPGA architecture.

intend to use MRAM-LUT circuits in their structure is desired to have the highest compatibility with modern FPGAs such that similar routing structures, programming paradigms, and toolchains can still be leveraged with minimal modifications. In [12], Zand and DeMara propose a hybrid spin/charge-based FPGA (HSC-FPGA) which is based on the architecture of Xilinx FPGAs, such as the Virtex 7 family.

Similar to the CLBs in modern Xilinx FPGAs, the CLBs in HSC-FPGA provide logic circuits including (1) six-input LUT circuit, (2) dual five-input LUTs with shared inputs, (3) distributed memory, (4) shift registers, and (5) dedicated carry logic for arithmetic operations. In particular, as shown in **Figure 10**, the HSC-FPGA's CLB architecture includes two slices to implement sequential and combinational logic functions, called Slice-S and Slice-C, respectively. Slice-C consists of SRAM-based LUT circuits that can also be used as shift registers and distributed RAM. Slice-S includes six-input fracturable MRAM-LUTs as well as latch and flip-flop circuits to realize sequential logic. Suzuki and Hanyu [32] have designed an MRAM-LUT circuit that can also operate as a shift register, however, they consume significantly higher energy compared to SRAM-based shift registers due to the high switching energy required to change the state of the MRAM cells. Overall, the simulation results, in [12], show that the HSC-FPGA can achieve more than 18% reduction in area occupation, in addition to a 70% and 15% decrease in standby power and read power dissipation, respectively, compared to conventional SRAM-based FPGAs.

Besides the designs discussed in this chapter, there are several important efforts in this area at different levels of design abstraction, from circuit and architecture to the fabrication of FPGA chips, with different design objectives including but not limited to: increasing performance, reducing power, area, and improving reliability and security. **Table 3** lists some of these efforts in the past two decades which have advanced the area of research, achieved promising results and set the foundation for future research and manufacturing of MRAM-based FPGAs.

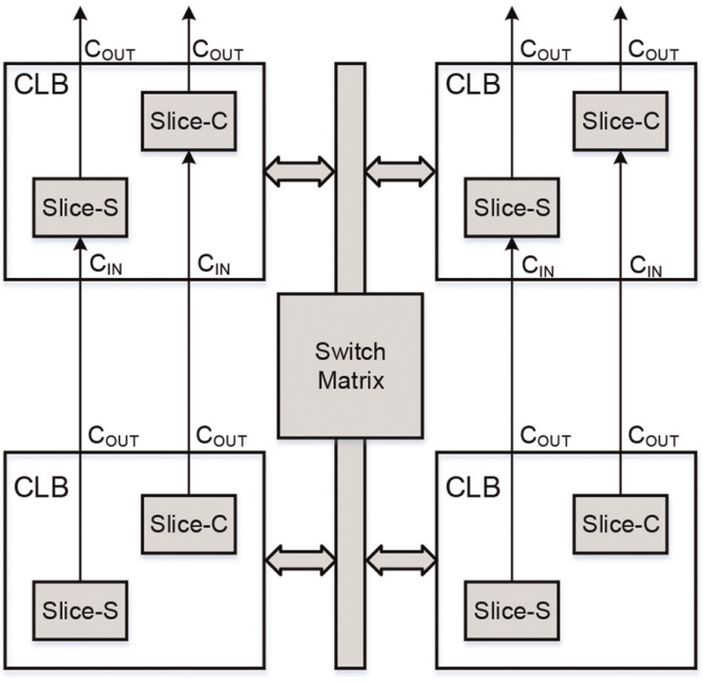

Figure 10.
The structure of the CLBs in hybrid spin-charge FPGA proposed in [12].

Paper	Design level			Design objective				
	Cir	Arch	Fab	Speed	Area	Power	Reliability	Security
[33]	✓					✓	✓	
[34]	✓	✓		✓	✓			
[35]	✓	✓	✓		✓	✓	✓	
[36]	✓		✓	✓		✓		
[37]	✓			✓	✓	✓		✓
[29]	✓			✓		✓	✓	
[38]	✓					✓		
[39]	✓		✓	✓				
[27]	✓			✓		✓		
[40]	✓		✓	✓	✓	✓		
[41]	✓			✓		✓	✓	
[26]	✓				✓			
[42]	✓	✓	✓			✓		
[10]	✓		✓		✓	✓		
[43]	✓		✓	✓		✓		
[44]	✓	✓	✓	✓		✓		
[30]	✓	✓			✓	✓	✓	
[45]		✓		✓		✓		
[46]	✓			✓		✓		
[47]	✓	✓		✓	✓	✓	✓	
[48]		✓			✓	✓	✓	
[49]				✓	✓	✓	✓	
[50]		✓		✓		✓		
[51]	✓		✓		✓	✓		✓
[52]	✓			✓		✓		
[13]	✓			✓		✓	✓	
[53]		✓			✓	✓	✓	✓
[11]	✓		✓	✓	✓	✓	✓	

Table 3.
An overview of the MRAM-based FPGA designs in the past two decades.

4. Conclusions

In this chapter, we provided an overview of the recent efforts in developing the next generation of FPGA fabrics which take advantage of the cooperating strengths of CMOS technology, such as fast and energy-efficient switching, and MRAM technology to attain characteristics such as non-volatility and low standby power. The prior research in this area shows that MRAM-based FPGAs can achieve significant

reductions in power consumption and chip area compared to conventional SRAM-based FPGAs. However, further research is required for addressing the reliability challenges of MRAM-based FPGAs including susceptibility to process variation, and endurance of memristive devices which can impact the reprogrammability of the FPGAs. Finally, this area of research provides several possibilities for future work, such as developing memristive-based in-memory computing co-processors to handle data-intensive applications such as machine learning and graph processing in hybrid memristive-CMOS FPGAs.

Abbreviations

FPGA	Field programmable gate array
CMOS	Complementary metal-oxide-semiconductor
SRAM	Static random-access memory
LUT	Look-up table
CLB	Configurable logic blocks
RRAM	Resistive random-access memory
PCM	Phase-change memory
MRAM	Magnetoresistive random-access memory
MTJ	Magnetic tunnel junctions
FM	Ferro-magnetic
CoFeB	Cobalt-ferrous-foron
MgO	Magnesium-oxide
P	Parallel
AP	Anti-parallel
RA	Resistance-area product
TMR	Tunneling magnetoresistance
STT	Spin transfer torque
PCSA	Pre-charge sense amplifier
PMOS	P-channel metal–oxide-semiconductor
PDP	Power-delay-product
ALM	Adaptive logic modules
PV	Process variation
IOB	Input–output block
SM	Switch matrix
DLL	Delay-locked loop
HSC	Hybrid spin/charge
EDA	Electronic design automation

Author details

Peyton Chandarana[1†], Mohammed Elbtity[1†], Ronald F. DeMara[2] and Ramtin Zand[1*]

1 University of South Carolina, Columbia, United States

2 University of Central Florida, Orlando, United States

*Address all correspondence to: ramtin@cse.sc.edu

† These authors contributed equally.

References

[1] DeMara RF, Roohi A, Zand R, Pyle SD. Heterogeneous technology configurable fabrics for field-programmable co-design of cmos and spin-based devices. In: 2017 IEEE International Conference on Rebooting Computing (ICRC). Washington, DC, USA: IEEE; 2017. pp. 1-4

[2] Kuon I, Tessier R, Rose J, et al. Fpga architecture: Survey and challenges. Foundations and Trends® in Electronic Design Automation. 2008;**2**(2):135-253

[3] Cong J, Xiao B. Fpga-rpi: A novel fpga architecture with rram-based programmable interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2013;**22**(4): 864-877

[4] Liauw YY, Zhang Z, Kim W, El Gamal A, Wong SS. Nonvolatile 3d-fpga with monolithically stacked rram-based configuration memory. In: 2012 IEEE International Solid-State Circuits Conference. San Francisco, California, USA: IEEE; 2012. pp. 406-408

[5] Tanachutiwat S, Liu M, Wang W. Fpga based on integration of cmos and rram. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2010; **19**(11):2023-2032

[6] Chen Y-C, Wang W, Li H, Zhang W. Non-volatile 3d stacking rram-based fpga. In: 22nd International Conference on Field Programmable Logic and Applications (FPL). Oslo, Norway: IEEE; 2012. pp. 367-372

[7] Huang K, Ha Y, Zhao R, Kumar A, Lian Y. A low active leakage and high reliability phase change memory (pcm) based non-volatile fpga storage element. IEEE Transactions on Circuits and Systems I: Regular Papers. 2014;**61**(9):2605-2613

[8] Chen Y, Zhao J, Xie Y. 3d-nonfar: Three-dimensional non-volatile fpga architecture using phase change memory. In: Proceedings of the 16th ACM/IEEE International Symposium on Low Power Electronics and Design. Austin, Texas, USA: Association for Computing Machinery (ACM); 2010. pp. 55-60

[9] Gaillardon P-E, Ben-Jamaa MH, Beneventi GB, Clermidy F, Perniola L. Emerging memory technologies for reconfigurable routing in fpga architecture. In: 2010 17th IEEE International Conference on Electronics, Circuits and Systems. IEEE; 2010. pp. 62-65

[10] Suzuki D, Natsui M, Mochizuki A, Miura S, Honjo H, Sato H, et al. Fabrication of a 3000-6-input-luts embedded and block-level power-gated nonvolatile fpga chip using p-mtj-based logic-in-memory structure. In: 2015 Symposium on VLSI Circuits (VLSI Circuits). Kyoto, Japan: IEEE; 2015. pp. C172-C173

[11] Zhao W, Belhaire E, Chappert C, Mazoyer P. Spin transfer torque (stt)-mram–based runtime reconfiguration fpga circuit. ACM Transactions on Embedded Computing Systems. 2009;**9**: 14:1-14:16

[12] Zand R, DeMara RF. Hsc-fpga: A hybrid spin/charge fpga leveraging the cooperating strengths of cmos and mtj devices. In: Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, Ser. FPGA'19. New York, NY, USA: Association for Computing Machinery; 2019. pp. 118-119. DOI: 10.1145/ 3289602.3293940

[13] Zand R, DeMara RF. Radiation-hardened mram-based lut for non-

volatile fpga soft error mitigation with multi-node upset tolerance. Journal of Physics D: Applied Physics. 2017;**50**(50): 505002

[14] Krishna MKG, Roohi A, Zand R, DeMara RF. Heterogeneous energy-sparing reconfigurable logic: Spin-based storage and cnfet-based multiplexing. IET Circuits, Devices & Systems. 2017; **11**(3):274-279

[15] Ikeda S, Miura K, Yamamoto H, Mizunuma K, Gan H, Endo M, et al. A perpendicular-anisotropy cofeb–mgo magnetic tunnel junction. Nature Materials. 2010;**9**(9):721

[16] Zhang Y, Zhao W, Lakys Y, Klein JO, Kim JV, Ravelosona D, et al. Compact modeling of perpendicular-anisotropy cofeb/mgo magnetic tunnel junctions. IEEE Transactions on Electron Devices. 2012;**59**(3):819-826

[17] Kim J, Chen A, Behin-Aein B, Kumar S, Wang J, Kim CH. A technology-agnostic mtj spice model with user-defined dimensions for stt-mram scalability studies. In: 2015 IEEE Custom Integrated Circuits Conference (CICC). San Jose, CA, United States: IEEE; 2015. pp. 1-4

[18] Slonczewski J. Current-driven excitation of magnetic multilayers. Journal of Magnetism and Magnetic Materials. 1996;**159**(1):L1-L7

[19] Liu L, Pai C, Li Y, Tseng HW, Ralph DC, Buhrman RA. Spin-torque switching with the giant spin hall effect of tantalum. Science. 2012;**336**(6081): 555-558

[20] Zand R, Roohi A, DeMara RF. Fundamentals, modeling, and application of magnetic tunnel junctions. In: Nanoscale Devices. Boca Raton, Florida: CRC Press; 2018. pp. 337-368

[21] Ben-Romdhane N, Zhao W, Zhang Y, Klein J-O, Wang Z, Ravelosona D. Design and analysis of racetrack memory based on magnetic domain wall motion in nanowires. In: 2014 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH). Paris, France: IEEE; 2014. pp. 71-76

[22] Gupta SK, Park SP, Mojumder NN, Roy K. Layout-aware optimization of stt mrams. In: 2012 Design, Automation & Test in Europe Conference & Exhibition (DATE). Dresden, Germany: IEEE; 2012. pp. 1455-1458

[23] Zand R, Roohi A, DeMara RF. Energy-efficient and process-variation-resilient write circuit schemes for spin hall effect mram device. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2017;**25**(9): 2394-2401

[24] Salehi S, Fan D, Demara RF. Survey of stt-mram cell design strategies: Taxonomy and sense amplifier tradeoffs for resiliency. ACM Journal on Emerging Technologies in Computing Systems (JETC). 2017;**13**(3):1-16

[25] Zhao W, Belhaire E, Chappert C, Jacquet F, Mazoyer P. New non-volatile logic based on spin-mtj. physica status solidi (a). 2008;**205**(6):1373-1377

[26] Suzuki D, Natsui M, Hanyu T. Area-efficient lut circuit design based on asymmetry of mtj's current switching for a nonvolatile fpga. In: 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS). Boise, Idaho, USA: IEEE; 2012. pp. 334-337

[27] Zand R, Roohi A, Salehi S, DeMara RF. Scalable adaptive spintronic reconfigurable logic using area-matched mtj design. IEEE Transactions on

Circuits and Systems II: Express Briefs. 2016;**63**(7):678-682

[28] Intel. Adaptive logic module (alm) definition. [Online]. Available from: h ttps://www.intel.com/content/www/us/en/programmable/quartushelp/17.0/reference/glossary/def_alm.htm

[29] Zand R, Roohi A, Fan D, DeMara RF. Energy-efficient nonvolatile reconfigurable logic using spin hall effect-based lookup tables. IEEE Transactions on Nanotechnology. 2017; **16**(1):32-43

[30] Zand R, Demara RF. Mram-enhanced low power reconfigurable fabric with multi-level variation tolerance. IEEE Transactions on Circuits and Systems I: Regular Papers. 2019;**66**: 4662-4672

[31] Salehi S, Zand R, DeMara RF. Clockless spin-based look-up tables with wide read margin. In: Proceedings of the 2019 on Great Lakes Symposium on VLSI. Washington, DC: ACM; 2019. pp. 363-366

[32] Suzuki D, Hanyu T. Design of a magnetic-tunnel-junction-oriented nonvolatile lookup table circuit with write-operation-minimized data shifting. Japanese Journal of Applied Physics. 2018;**57**(4S):04FE09

[33] Lakys Y, Zhao W, Klein J-O, Chappert C. Hardening techniques for mram-based nonvolatile latches and logic. IEEE Transactions on Nuclear Science. 2012;**59**:1136-1141

[34] Zhao W, Belhaire E, Javerliac V, Chappert C, Diény B. Evaluation Ofanon-volatile Fpgabased on Mram Technology. Padua, Italy: IEEE; 2006

[35] Goncalves O, Prenat G, di Pendina G, Diény B. Non-volatile fpgas based on spintronic devices. In: 2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC). Austin, TX, USA: IEEE; 2013. pp. 1-3

[36] Guillemenet Y, Torres L, Sassatelli G, Bruchon N, Hassoune I. A non-volatile run-time fpga using thermally assisted switching mrams. In: 2008 International Conference on Field Programmable Logic and Applications. Heidelberg, Germany: IEEE; 2008. pp. 421-426

[37] Zhao WS, Belhaire E, Mistral Q, Nicolle E, Devolder T, Chappert C. Integration of spin-ram technology in fpga circuits. In: 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings. Shanghai, China: IEEE; 2006. pp. 799-802

[38] Faber L-B, Zhao W, Klein J-O, Devolder T, Chappert C. Dynamic compact model of spin-transfer torque based magnetic tunnel junction (mtj). In: 2009 4th International Conference on Design & Technology of Integrated Systems in Nanoscal era. Cairo, Egypt: IEEE; 2009. pp. 130-135

[39] Silva V, Fernandes JR, Oliveira LB, Neto HC, Ferreira R, Freitas S, et al. Thermal assisted switching magnetic tunnel junctions as fpga memory elements. In: 2009 MIXDES-16th International Conference Mixed Design of Integrated Circuits & Systems. Lodz, Poland: IEEE; 2009. pp. 332-336

[40] Zhao W, Belhaire E, Chappert C, Mazoyer P. Power and area optimization for run-time reconfiguration system on programmable chip based on magnetic random access memory. IEEE Transactions on Magnetics. 2009;**45**:776-780

[41] Rajaei R, Gholipour A. Low power, reliable, and nonvolatile msram cell for

facilitating power gating and nonvolatile dynamically reconfiguration. IEEE Transactions on Nanotechnology. 2018; **17**:261-267

[42] Guillemenet Y, Torres L, Sassatelli G. Non-volatile run-time field-programmable gate arrays structures using thermally assisted switching magnetic random access memories. IET Computers and Digital Techniques. 2010;**4**:211-226

[43] Guillemenet Y, Torres L, Sassatelli G, Bruchon N. On the use of magnetic rams in field-programmable gate arrays. Int. J. Reconfigurable Comput. 2008;**2008**:723 950:1-723 950:9

[44] Bruchon N, Torres L, Sassatelli G, Cambon G. Magnetic tunnelling junction based fpga. In: FPGA'06. Monterey, California, USA: ACM; 2006

[45] Chaudhuri S, Zhao W, Klein J-O, Chappert C, Mazoyer P. High density asynchronous lut based on non-volatile mram technology. In: 2010 International Conference on Field Programmable Logic and Applications. Milan, Italy: IEEE; 2010. pp. 374-379

[46] Hāmsa S, Thangadurai N, Ananth A. Composition of magnetic tunnel junction-based magnetoresistive random access memory for field-programmable gate array. Current Science. Bangalore, India. 2020

[47] Cho K, Lee S, Lee CK, Yim T, Yoon H. Low power multi-context look-up table (lut) using spin-torque transfer magnetic ram for non-volatile fpga. In: 2017 International SoC Design Conference (ISOCC). Seoul, Korea (South): IEEE; 2017. pp. 107-108

[48] Goncalves O, Prenat G, Diény B. Radiation hardened mram-based fpga. IEEE Transactions on Magnetics. 2013; **49**:4355-4358

[49] Rajaei R. Radiation-hardened design of nonvolatile mram-based fpga. IEEE Transactions on Magnetics. 2016;**52**:1-10

[50] Kim J, Song Y, Cho K, Lee H, Yoon H, Chung E-Y. Stt-mram-based multicontext fpga for multithreading computing environment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2022; **41**:1330-1343

[51] Zhao W, Belhaire E, Chappert C, Diény B, Prenat G. Tas-mram-based low-power high-speed runtime reconfiguration (rtr) fpga. ACM Trans. Reconfigurable Technol. Syst. 2009;**2**:8: 1-8:19

[52] Bagheriye L, Toofan S, Saeidi R, Zeinali B, Moradi F. A reduced store/restore energy mram-based sram cell for a non-volatile dynamically reconfigurable fpga. IEEE Transactions on Circuits and Systems II: Express Briefs. 2018;**65**:1708-1712

[53] Goncalves O, Prenat G, Pendina GD, Layer C, Diény B. Nonvolatile runtime-reconfigurable fpga secured through mram-based periodic refresh. In: 2013 5th IEEE International Memory Workshop. Monterey, CA, USA: IEEE; 2013. pp. 170-173