Low-Noise, Low-Jitter, High Detection Efficiency InGaAs/InP Single-Photon Avalanche Diode

Alberto Tosi, *Member, IEEE*, Niccolò Calandri, Mirko Sanzaro, and Fabio Acerbi, *Member, IEEE*

I. INTRODUCTION

NEAR-INFRARED (NIR) single-photon detection is an enabling technology in many scientific and industrial fields and is driving many efforts worldwide. Among the different technologies available for photon counting and timing in the NIR, up to 1700 nm, InGaAs/InP single-photon avalanche diodes (SPADs) are one of the best choices for applications requiring not only high performance, but also high reliability and ease of implementation. Examples of such applications include quantum key distribution [1], eye-safe time-of-flight laser ranging (LIDAR) and 3-D imaging [2], time-resolved photoluminescence [3], optical time-domain reflectometry [4], singlet oxygen detection for dosimetry in photodynamic therapy [5], quantum experiments [6], integrated circuit characterization based on photon emission from hot-carriers in metal–oxide–semiconductor field-effect transistors [7]. All these applications benefit from high photon detection efficiency (PDE) and low dark count rate (DCR). Furthermore, other required performances are timing jitter, i.e. the precision in determining the photon arrival time, that has to be as low as possible, and afterpulsing probability, which introduces non-linearity and eventually limits the maximum count rate.
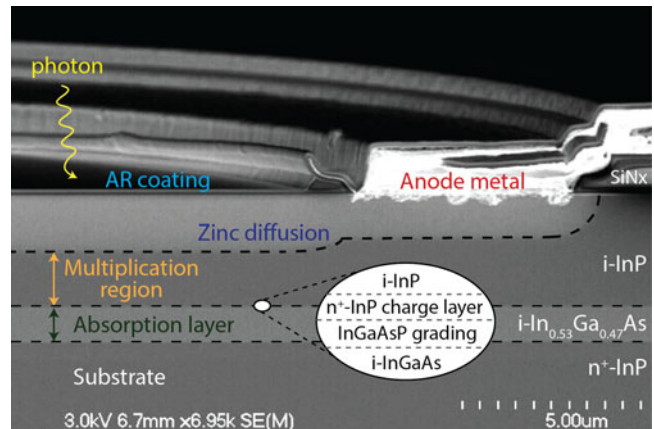

Fig. 1. Scanning electron microscope image of the InGaAs/InP SPAD cross-section, with layers structure and Zn diffusion profile.

In the last years, significant progress in InGaAs/InP SPADs was made to improve both semiconductors quality and heterostructure design. Detectors with DCR as low as few kilo-counts per seconds (cps) at 225 K (easy to reach by means of thermoelectric coolers) were demonstrated, with PDE higher than 20% at 1.55 μm [8], [9]. Others demonstrated low timing jitter, with lower than 100 ps full-width at half maximum (FWHM) and low afterpulsing probability, thus achieving 1 Mcps with standard square gate [10] and even 100 Mcps with GHz sinusoidal gating [11].

Here we present the design criteria for new InGaAs/InP SPADs with very low (few kilo-counts per seconds) DCR, high timing resolution (<100 ps FWHM), high PDE (30% at 1550 nm) and moderately low afterpulsing. The achieved performances are much better than those of previously developed detectors and successfully compare to state-of-the-art ones, mainly thanks to: i) optimized fabrication conditions during Zn diffusion; ii) optimized layer thicknesses and diffusion depths.

II. DEVICE DESCRIPTION

A. InGaAs/InP SPAD Structure

We designed an InGaAs/InP SPAD (see Fig. 1) with a separate absorption grading charge and multiplication structure, usually employed also for linear-mode avalache photodiodes (APDs) [12]. The confinement of the high electric field in the active area is achieved by means of double p-type Zinc diffusion: a central deep diffusion and a concentric shallow one. The latter has a larger diameter for reducing the electric field peaking at the edge of the active area, which would lead to premature edge

A. Tosi, N. Calandri, and M. Sanzaro are with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milano 20133, Italy (e-mail: alberto.tosi@polimi.it; niccolo.calandri@polimi.it; mirko.sanzaro@polimi.it).

F. Acerbi was with the Dipartimento di Elettronica, Informazione e Bioingeg-neria, Politecnico di Milano, Milano 20133, Italy. He is now with Fondazione Bruno Kessler, Trento 38123, Italy (e-mail: fabio.acerbi@polimi.it).

breakdown. The differences in depth and diameter between the two Zn diffusions proved to be important parameters that affect detector performance; hence, they must be properly tailored in order to get good electric field uniformity all over the active area [13] and sharp timing response.

A low-energy photon is absorbed in the intrinsic $In_{0.53}Ga_{0.47}As$ layer ($E_g \sim 0.75$ eV at room temperature) and the photo-generated hole drifts towards the InP ($E_g \sim 1.35$ eV at room temperature) multiplication layer, where the electric field is high enough to trigger an avalanche current process through impact ionization. The carrier multiplication process builds up and then self-sustains, thus leading to a macroscopic avalanche current, easy to be detected by the read-out circuitry. Between absorption and multiplication regions, an n+ doped InP charge layer shapes the electric field in order to lower it in the low energy-gap InGaAs absorbing region, for limiting tunneling and field-assisted thermal carrier generation [12], [13]. Three quaternary layers reduce the valence band discontinuity and avoid hole pile-up, thus speeding up the avalanche ignition.

B. Design Criteria and Fabrication

Design criteria for SPADs are different from APDs' ones [13]. The goals of our design were: i) low DCR at the lowest temperature easy to be reached by a compact thermo-electric cooler (i.e. ~ 225 K); ii) high PDE, more than 25% at the 1550 nm telecom wavelength; iii) low afterpulsing probability; iv) uniformity of detection efficiency all over the active area; v) low timing jitter, less than 100 ps FWHM. Starting from the good results obtained with previous designs and fabrication runs [10], we optimized: i) the fabrication processes, mainly for minimizing DCR; ii) the design of layers and diffusions.

Concerning fabrication processes, compared to previous runs we investigated the impact of Zn diffusion (p-dopant in InP) on the quality of the underlying semiconductors. Zinc is diffused using a metal-organic chemical vapor deposition reactor with dimethylzinc as the Zn source. After some adjustments in the fabrication runs, we found out that DCR depends on diffusion process parameters. Namely, Zn diffusion temperature, phosphine overpressure, and dimethylzinc source flow all impact on the concentration of mid-gap traps. Such defects, introduced during either epitaxial growth or successive processing, were associated with high dark current and noise [14]. Therefore, we selected the conditions to obtain both low DCR and high electric field uniformity. The latter directly influences PDE uniformity and is achieved with uniform Zn diffusion. In the InGaAs/InP SPAD from the last production run, we measured a very uniform Zn diffusion front, which guarantees also good reproducibility from device to device.

Concerning the design of layers and diffusions, in order to improve PDE and the timing response, while keeping the electric field in the InGaAs layer low, we tailored the electric field in the multiplication layer. High electric field gives higher avalanche triggering efficiency and lower timing jitter, but also higher tunneling contribution to DCR [13]. Compared to our previous design [10], higher charge in the charge layer causes the punch-through voltage to increase, the electric field in the InGaAs
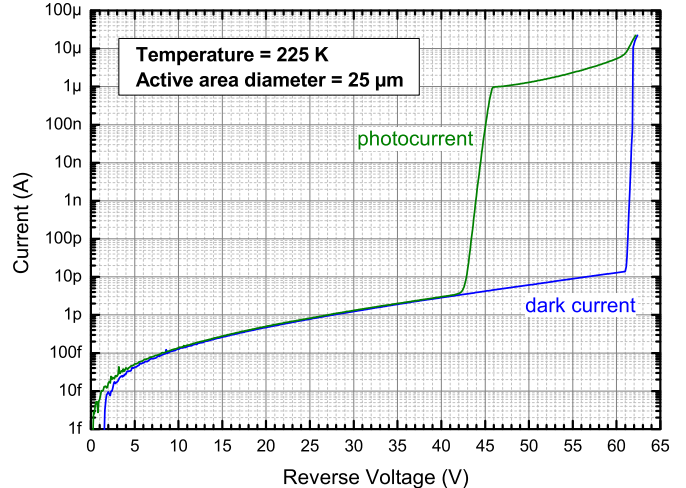

Fig. 2. Current-voltage characteristic of a 25 μm SPAD at 225 K: the dark current is just about 10 pA at 1 V below breakdown.

layer to slightly decrease (thus reducing field-assisted carrier generation in such low energy-gap layer), while the field in the multiplication region increases.

Measurements performed on devices with different layout show that PDE uniformity is very good over the whole active area, even with no floating guard rings. Therefore, in the new design we removed them, thus lowering stray capacitance, reaching smaller footprint (that is good for moving towards SPAD arrays) and having sharper transition from depleted region to neutral one.

III. EXPERIMENTAL RESULTS

We experimentally characterized the performance of our InGaAs/InP SPAD, with 25 μm active area diameter and no floating guard ring, operated in gated-mode with a passive quenching circuit similar to the one employed in [10]. During gate-OFF (T_{OFF}), the device is biased 0.5 V below its breakdown voltage, whereas during gate-ON (T_{ON}) it is driven to some volts above breakdown, by a value usually called excess bias, V_{EX}.

A. I-V Curve

At 225 K, we measured the current-voltage I-V characteristics shown in Fig. 2. The punch-through voltage, i.e. when the depleted region reaches the InGaAs absorption layer, is $V_{PT} \sim 43$ V. The breakdown voltage, defined as the knee between the "on" I-V characteristic during breakdown and the "off" (dark current) I-V characteristic below breakdown, is $V_{BD} \sim 60$ V. The difference $V_{BD} - V_{PT}$ of more than 15 V guarantees that the InGaAs layer is depleted even when the detector is operated at lower temperatures.

We also measured the dark current of SPAD detectors with larger active area diameters (up to 100 μm) and we verified that it scales with diameter, and not with active area. This is a clear signature that the dark current is dominated by peripheral leakage, and not by bulk leakage. Therefore, most of the dark
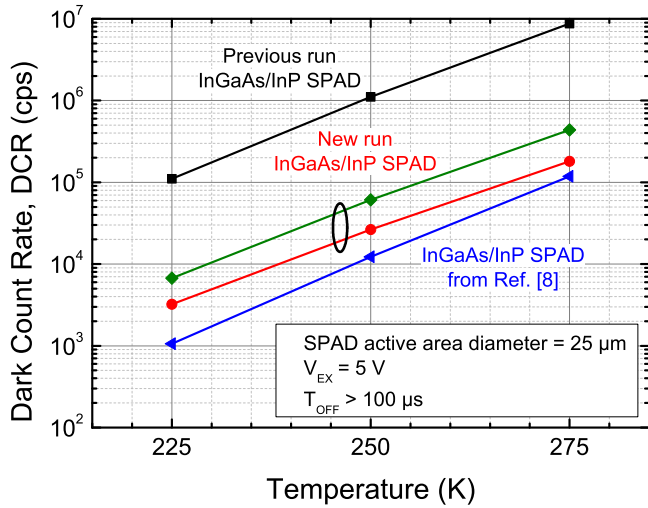
Fig. 3. Primary DCR of the new InGaAs/InP SPADs (a couple of examples are reported) as a function of temperature, compared with previous production run and state-of-the-art devices ([8]).
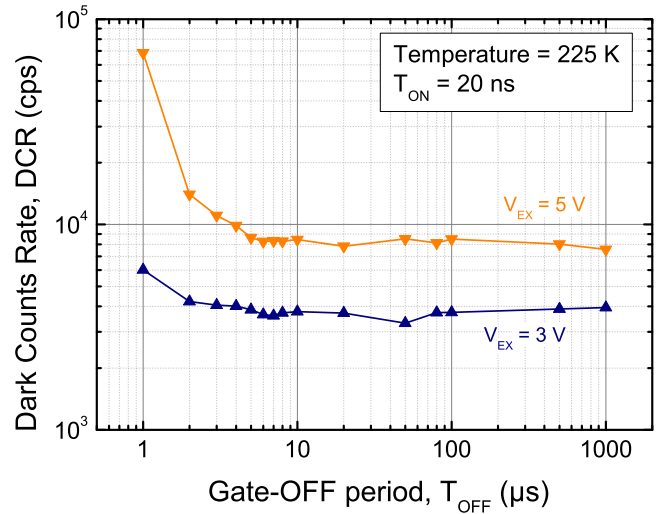

Fig. 4. Dependence of dark count rate on gate-OFF period, at two different excess bias voltages, when SPAD is operated in gated mode with $T_{ON} = 20$ns.

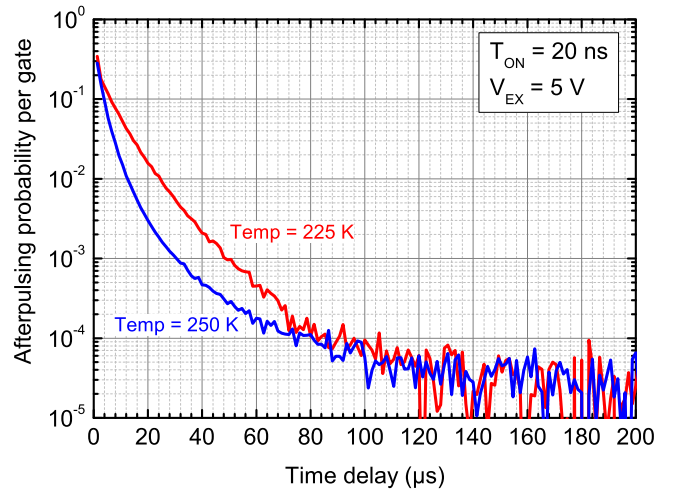current carriers do not contribute to DCR, since they do not succeed in triggering avalanche ignitions, because they leak through the low electric field periphery.

B. Dark Count Rate

At different temperatures and excess bias voltages, we characterized the primary DCR, due to thermal carrier generation and to field-assisted mechanisms, like trapped-assisted tunneling. In order to avoid distortions on DCR measurements due to afterpulsing, we enforced a long T_{OFF} time, longer than 100 μs, during pulse gating.

Fig. 3 compares the DCR dependence on temperature of our InGaAs/InP SPADs with our previous ones and those reported in [8], whose noise is the current state-of-the-art. Compared to our previous production run, the improvement is more than one order of magnitude and now DCR is similar to the best-in-class ones. In fact, DCR is just few kcps at 225 K, a temperature easily achievable with 3-stage thermo-electric coolers mounted in compact packages.

As we reported in Ref. [13], the slope of the curves depends on the dominant carrier generation mechanism: a slope of about one decade every 25 K generally shows that thermal generation is dominant, thus indicating a good electric field tailoring in multiplication region for avoiding tunneling.

C. Afterpulsing

SPADs suffer afterpulsing: during an avalanche process, some charge carriers flowing through the multiplication region are trapped in deep levels, then they are released with long time constants. If a carrier is de-trapped during a subsequent gate-ON period, it can trigger a new avalanche process, i.e. an 'afterpulsing event', which eventually impairs photon counting linearity. In order to reduce afterpulsing, it is compulsory to keep the SPAD OFF for a sufficiently long time (tens of microseconds)

Fig. 5. Afterpulsing probability per gate measured with the double pulse method [15], with $T_{ON} = 20$ns, $V_{EX} = 5V$ and two different operating temperatures.

after each avalanche ignition. The drawback is the reduced maximum count rate that can be achieved, whose saturated value is $1/(T_{ON}+T_{OFF})$.

Instead, when a short gate-OFF time is set, DCR increases because of afterpulsing. Fig. 4 shows such a DCR dependence on gate-OFF time, with a constant 20 ns gate-ON time. It can be noted that our new SPADs have afterpulsing comparable to state-of-the-art detectors operated in similar conditions [8]: very short T_{OFF} durations, as short as 10 μs, can be enforced, while still having negligible afterpulsing.

We also characterized the afterpulsing effect through the double-pulse method [15] at two temperatures, 225 and 250 K (see Fig. 5): as expected, afterpulsing is lower at higher temperature. By fitting the afterpulsing probability decay over the time delay after the original avalanche, we extracted three time constants (about 10, 20 and 320 μs at 225 K), which possibly
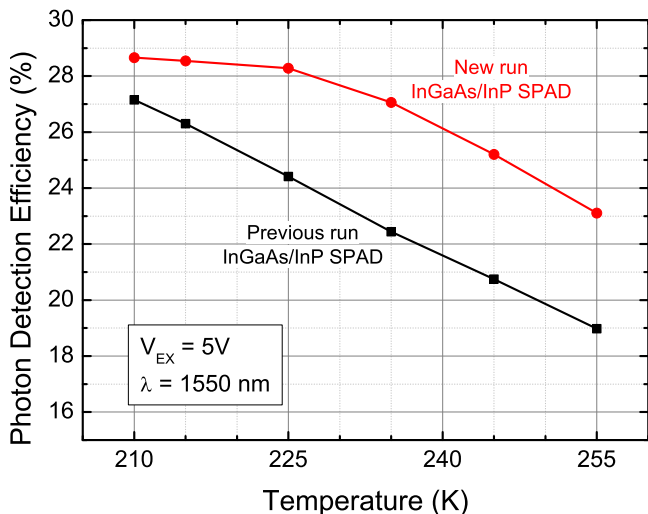
Fig. 6. Dependence of photon detection efficiency at 1550 nm on temperature, for SPADs of the new and the previous production run. Active area diameters are 25 μm and $V_{EX} = 5\ V$.
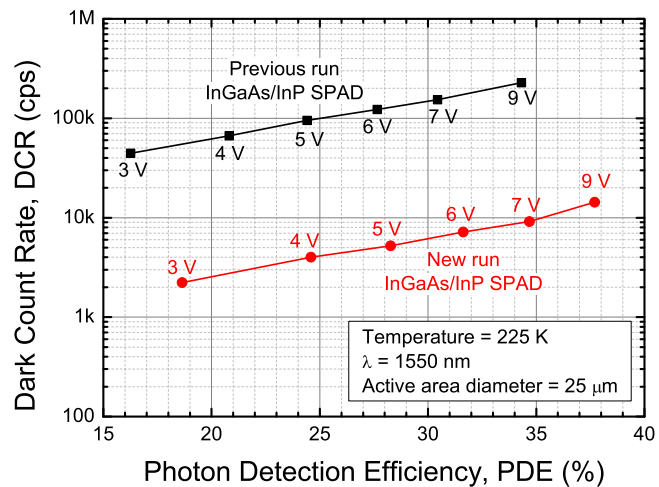

Fig. 7. Dark count rate as a function of the photon detection efficiency for SPADs of the new and the previous run, with corresponding excess bias voltages.

correspond to three main families of deep levels, responsible for trapping avalanche carriers.

Additionally, as demonstrated in literature [11], [17], [18], [19], when InGaAs/InP SPADs are employed with either GHz sinusoidal or sub-nanosecond gating, the avalanche charge is strongly reduced, thus afterpulsing lowers and a very high count rate can be reached.

D. Photon Detection Efficiency

PDE of SPAD results from the product of absorption efficiency and avalanche triggering probability. The former mainly depends on the thickness of the depleted region in the absorption InGaAs layer, which is equal to that of the previous production runs. The latter depends on the thickness of the multiplication InP layer and on the electric field therein. Fig. 6 reports the dependence of PDE on temperature, measured at 5 V excess bias: new devices show higher PDE, which tends to saturate at low temperatures, where values of new and previous runs are similar. PDE increases toward lower temperature because: i) at constant excess bias, since breakdown voltage lowers, the increase of electric field from OFF to ON in the multiplication region is stronger at lower temperatures, thus giving higher PDE; ii) triggering probability increases thanks to higher impact ionization coefficients at lower temperatures [20], [21].

Furthermore, the new devices have a lower breakdown voltage (at any temperature), hence for a given excess bias the electric field in the multiplication region is slightly higher than in the previous run, leading to higher triggering probability.

From a user point of view, it is often useful to compare SPADs in a plot with DCR vs. PDE, as shown in Fig. 7. InGaAs/InP SPADs from the new production run are more than one order of magnitude better in DCR: a PDE > 30% is achieved with DCR < 10 kcps.

E. Active Area Uniformity

We performed a two-dimensional scan over the active area to assess the PDE uniformity [16]. Data were acquired every 2 μm step, through a focused 1.55 μm laser beam with 5 μm spot size. The detector was operated at 225 K in gated-mode, with $T_{ON} = 20$ ns, a repetition rate of 20 kHz, and biased at different excess bias voltages. Since the laser power was kept constant (and at single-photon level) during the scan, the resulting photon-counting maps provide the variation of PDE across the area.

The results shown in Fig. 8 prove very high uniformity of the sensitivity over the whole active area. At low excess bias ($V_{EX} = 3V$), no edge effect is visible, and uniformity further improves at higher excess bias, because of the saturation of avalanche triggering efficiency [16]. These results prove that: i) the front of the double Zn diffusion is quite uniform (important to guarantee high reproducibility and reliability) and ii) the optimization of multiplication width and shallow Zn diffusion depths resulted in both uniform breakdown voltage in the active area and good smoothing of the electric field at its edge.

F. Timing Jitter

Timing jitter is the distribution of the measured single-photon arrival times. We illuminated the SPAD by means of a pulsed laser at 1550 nm with a pulse width of about 20 ps FWHM and we acquired the data with a standard time-correlated single-photon counting (TCSPC) setup.

As it can be seen in Fig. 9, the temporal response of the new SPAD is clean and sharp, with a main Gaussian distribution plus an exponentially decaying curve. At $V_{EX} = 7V$, the Gaussian shape has a standard deviation $\sigma = 28$ ps (i.e. FWHM = 67 ps), plus an exponential tail with a time constant of 58 ps. Fig. 10 shows the temporal response at different excess biases: FWHM is less than 100 ps even with $V_{EX} < 5V$. It can be noted that the time constant of the tail slightly decreases at higher excess bias, being 66 ps at 5 V and 56 ps at 9 V.
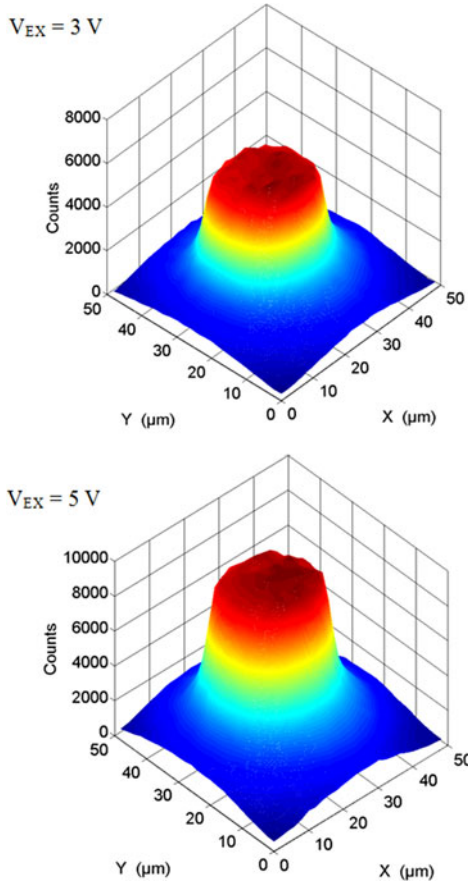
Fig. 8. Sensitivity map of our InGaAs/InP SPADs measured scanning the active area (and surroundings) with a CW laser beam at 1550 nm with 5 μm spot size. Note the good uniformity both at $V_{EX} = 3\,V$ and at $V_{EX} = 5\,V$. Data have been processed with bilinear interpolation for representation purposes.
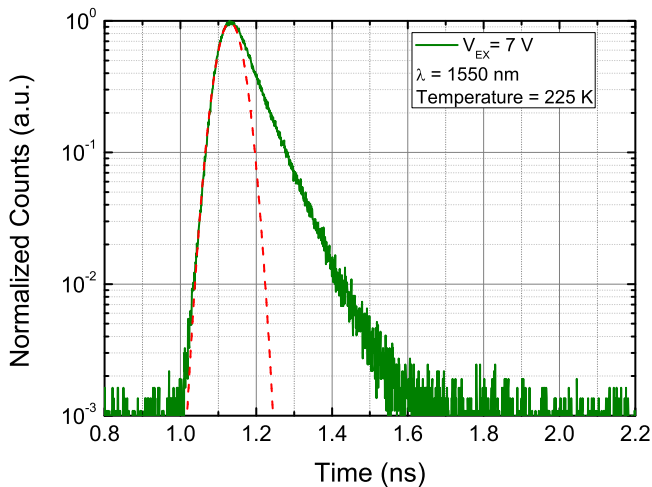

Fig. 9. Temporal response of the new InGaAs/InP SPADs when illuminated by a pulsed laser at 1550 nm. The response closely approaches a Gaussian distribution with standard deviation $\sigma = 28\,\mathrm{ps}$ (i.e. 67 ps FWHM), plus a minor exponential tail with 58 ps time constant, better than state-of-the-art InGaAs/InP SPADs.
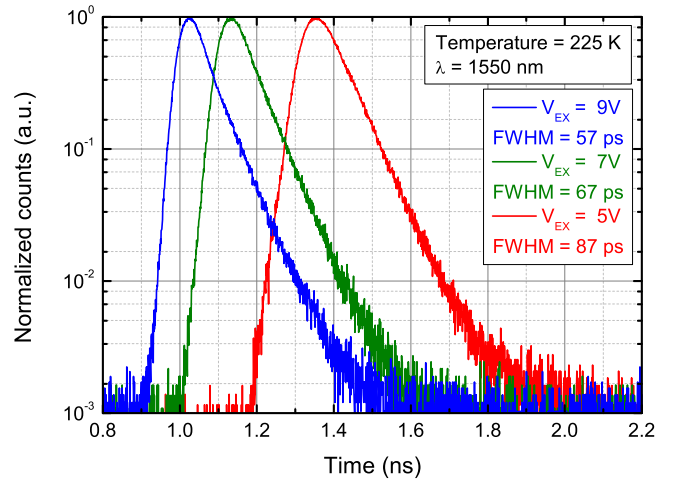

Fig. 10. Temporal response at different excess bias, when the SPAD is cooled at 225 K.

IV. CONCLUSION

In this paper, we presented the design criteria and the performance of a novel InGaAs/InP SPAD with low noise, high detection efficiency, and low timing jitter. SPAD with 25 μm active area diameter, cooled at 225 K and biased at 5 V excess bias, shows a DCR of just few kilo-counts per second, a 28% PDE at 1550 nm (with good uniformity over the active area), a timing jitter of about 87 ps (FWHM) and moderately low afterpulsing effect.

Compared to our previously design, we identified the critical design parameters and we optimized the fabrication processes and the device cross-section. In detail, we optimized the Zinc diffusion conditions into InP, in order to lower the defect concentration in the multiplication region. Additionally, tailoring of Zinc diffusion depths and total charge layer dose leads to lower electric field in the InGaAs layer, thus decreasing field-enhanced carrier generation, and increased triggering efficiency, leading to higher PDE.

This performance makes the presented InGaAs/InP SPADs excellent candidates for advanced TCSPC applications up to 1700 nm.

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