Analysis and Conceptualization of a Single-Phase Buck-Boost Integrated EV On-Board Charger Based on a Double Bridge Inverter Drive System

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1st Davide Cittanti
Dipartimento Energia "G. Ferraris"
Politecnico di Torino
Torino, Italy
davide.cittanti@polito.it

2nd Enrico Vico
Dipartimento Energia "G. Ferraris"
Politecnico di Torino
Torino, Italy
enrico.vico@polito.it

3rd Fabio Mandrile
Dipartimento Energia "G. Ferraris"
Politecnico di Torino
Torino, Italy
fabio.mandrile@polito.it

4th Eric Armando
Dipartimento Energia "G. Ferraris"
Politecnico di Torino
Torino, Italy
eric.armando@polito.it

5th Radu Bojoi
Dipartimento Energia "G. Ferraris"
Politecnico di Torino
Torino, Italy
radu.bojoi@polito.it

***Abstract*—Integrated on-board chargers (iOBCs) typically exploit the traction drive system (i.e., inverter and motor) of an electric vehicle (EV) as a battery charging interface. The main goal of iOBCs is to reduce cost and footprint of the EV charging system by leveraging existing powertrain components. However, this integration comes with unique challenges (e.g., limited efficiency, torque production, EMI, electrical safety, etc.), which currently represent an active research topic for both industry and academia. The main shortcoming of most existing iOBC solutions is that they only provide voltage step-up (boost) or voltage step-down (buck) capability, thus requiring an additional DC/DC conversion stage to address the full battery voltage range. This paper introduces a novel single-phase iOBC topology with inherent buck-boost capability, exploiting a next-generation 400 V double bridge inverter EV drive system. This topology allows for universal mains interface charging (i.e., 230 V EU, 120 V/240 V USA, etc.) and can exploit all kinds of synchronous/asynchronous electrical machines with an open-end winding configuration. The proposed iOBC structure only requires an additional line-frequency diode bridge rated for the charging current (or an active synchronous rectifier, if bidirectional charging is desired), an input filter capacitor and two reconfiguration switches. In this paper, the operational basics of the proposed iOBC are described, the stresses on all system active and passive components are analyzed and the converter closed-loop control strategy is introduced and assessed in simulation. Furthermore, a novel control approach addressing the double-line frequency power pulsation (i.e., typical of single-phase chargers) is proposed, exploiting the magnetic energy storage capability of the electrical machine.**

***Index Terms*—integrated on-board charger (iOBC); double bridge inverter (DBI); drive inverter; electric vehicles (EVs)**

I. Introduction

Electric vehicles (EVs) typically feature a dedicated on-board charger (OBC) to charge the high-voltage battery from the single-phase and/or the three-phase AC grid. Since the OBC results in added cost, weight and volume, the exploitation of the EV drive system (i.e., inverter and motor) to provide the charging function is currently an active research topic [1], [2]. Integrated on-board chargers (iOBCs) allow for significant cost and volume savings, however they are characterized by unique challenges, such as limited conversion efficiency (being the typical charging power several times lower than the drive system power rating) [3], [4], possible torque production (leading to control complexity, depending on the magnetic field generated within the electrical machine) [5], EMI generation (as for conventional OBCs) [5], [6], and electrical safety (especially for non-isolated topologies) [6].

Even though several iOBC concepts have been proposed in literature, most of them only provide voltage step-up (boost) or voltage step-down (buck) capability with the drive system components [7]–[18], thus requiring an additional DC/DC conversion stage to comply with the full battery voltage range. In [19]–[21], the buck-boost functionality is obtained with a dual three-phase inverter connected to an open-end winding machine, however the proposed solutions require a split battery configuration, substantially increasing the EV drivetrain complexity. In [22], the two three-phase inverters of a six-phase traction drive system are reconnected in a boost-buck configuration and the machine windings are exploited to provide galvanic isolation between the grid and the battery. Nevertheless, the iOBC concept in [22] requires the addition of a three-phase diode bridge rectifier, bulky grid-side filter inductors and several reconfiguration switches rated for the full traction drive current, undermining the iOBC cost/volume reduction goal. Most recently, a non-isolated single-phase iOBC topology with intrinsic boost-buck capability has been proposed in [4], leveraging the two inverters and the two machine winding sets of a dual three-phase drive system by adding only two reconfiguration switches, a single-phase diode bridge and an input filter capacitor. Notably, the solution in [4] provides excellent performance in terms of efficiency, torque generation and input/output current quality.

In this context, this paper proposes a novel single-phase non-isolated iOBC concept with inherent buck-boost functionality, exploiting a next-generation 400 V double bridge inverter (DBI) EV drive system [23], [24]. In particular, the proposed topology is able to operate with a universal mains interface (i.e., 230 V EU, 120 V/240 V USA, etc.) and can exploit all kinds of synchronous/asynchronous electrical machines with an open-end winding configuration, independently of the rotor isotropic or

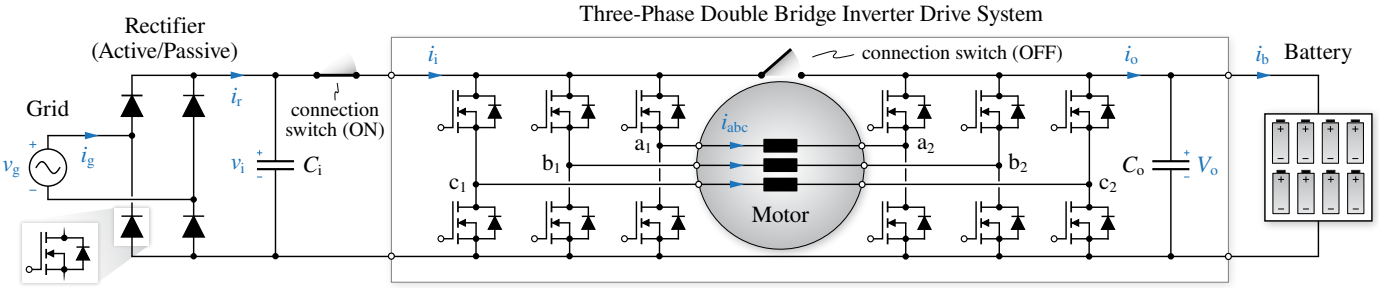

Fig. 1. Equivalent circuit schematic of the proposed single-phase buck-boost iOBC concept, based on a three-phase double bridge inverter drive system.

anisotropic structure. Remarkably, the proposed iOBC concept only requires the addition of a single-phase rectifier bridge rated for charging current, an input filter capacitor and two reconfiguration switches, as illustrated in Fig. 1: a line-frequency synchronous active rectifier may be adopted if bidirectional capability is desired. Furthermore, a novel control strategy aimed at addressing the double-line frequency power pulsation related to the single-phase operation of the system is introduced, providing an alternative to bulky output filter capacitors and/or to a dedicated active power pulsation buffer [25]–[30].

The main features of the proposed iOBC concept can be summarized as (1) intrinsic buck-boost capability, addressing the full battery voltage range, (2) sinusoidal AC input current shaping with very low ripple content (i.e., without requiring additional inductive components), (3) universal compatibility with all single-phase grid voltage/frequency levels, (4) wide applicability, being unaffected by the electrical machine kind, and (5) optional bidirectional charging capability. It is worth noting that galvanic isolation is not mandatory for OBCs, since double or reinforced insulation and/or the detection of residual currents with the automatic disconnection of the power supply are allowed alternatives to protect the end user against electrical shock [31].

This paper is structured as follows. In Section II the operational basics of the iOBC are described, introducing the buck and boost operating modes of the converter. In Section III the stresses on the semiconductor devices, the electrical machine and the input/output filter capacitors are analyzed in detail, providing the basis for the converter sizing and/or loss evaluation. In Section IV the iOBC closed-loop control is explained and a novel strategy to address the double-line frequency power pulsation is proposed. Finally, Section V summarizes and concludes this work.

II. Basics of Operation

The structure of the proposed iOBC is illustrated in Fig. 1 and consists of a grid-connected single-phase active/passive rectifier, an input filter capacitor, three paralleled buck-boost DC/DC converters adopting 600/650 V active switches and exploiting the motor as three mutually coupled inductors (i.e., the DBI drive system), and an output filter capacitor (i.e., the inverter DC-link). This topology resembles the voltage step-up single-phase Y-rectifier concept proposed in [32], however a different grid voltage rectification approach is adopted herein, to extend the charger operation in buck mode (i.e., when the battery voltage is below the grid peak voltage).

The drive system is reconfigured from traction mode to charging mode by means of the two connection switches illustrated in Fig. 1. The input rectifier bridge provides a unipolar voltage (i.e., a rectified sine-wave) across the input capacitor C_i. The three-phase DBI is controlled as three separate buck-boost converter units, exploiting the electrical machine mutually-coupled windings as inductive components. The three motor phase currents are controlled to be equal (i.e., not to produce torque) and are regulated to transfer the desired battery charging power, meanwhile ensuring sinusoidal input current shaping. Due to the single-phase operation of the system, the output capacitor C_o is subject to the inherent double-line frequency power pulsation, therefore, depending on the output system impedance and the acceptable output current ripple, either electrolytic capacitors and/or an active power pulsation buffer could be required [25], [26]. It is worth noting that the suppression of the double-line frequency voltage oscillation (i.e., the power pulsation buffer feature) can be obtained by leveraging the EV auxiliary DC/DC converter, i.e. without requiring additional power electronics, as reported in [27]–[30]. Remarkably, an alternative to the mentioned solutions is proposed and described in Section IV, exploiting the magnetic energy storage capability of the electrical machine to compensate the single-phase power pulsation.

The bridge-leg PWM switch signals s_{x_1}, s_{x_2} ($\mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}$) are generated from the comparison between the bridge-leg duty cycles d_{x_1}, d_{x_2} and the modulation carrier, as illustrated in Fig. 2. Defining the bridge-leg modulation reference as

$$m_\mathrm{x} = \frac{v_\mathrm{i}}{V_\mathrm{o}} = M\,|\sin\vartheta| \qquad \mathrm{x} = \mathrm{a},\ \mathrm{b},\ \mathrm{c}, \tag{1}$$

where ϑ is the grid phase angle (i.e., $v_\mathrm{g} = V_\mathrm{g}\sin\vartheta$, $v_\mathrm{i} \approx V_\mathrm{i}\,|\sin\vartheta|$ with $V_\mathrm{i} \approx V_\mathrm{g}$) and $M = V_\mathrm{i}/V_\mathrm{o}$ is the modulation index (i.e., $M > 1$ when operating in buck-boost mode, $M \leq 1$ when operating in boost-only mode), the primary and secondary-side bridge-leg duty cycles are obtained as

$$d_{\mathrm{x}_1} = \begin{cases} 1 & v_\mathrm{i} < V_\mathrm{o} \\ 1/m_\mathrm{x} & v_\mathrm{i} \geq V_\mathrm{o} \end{cases}, \qquad d_{\mathrm{x}_2} = \begin{cases} m_\mathrm{x} & v_\mathrm{i} \leq V_\mathrm{o} \\ 1 & v_\mathrm{i} > V_\mathrm{o} \end{cases}. \tag{2}$$

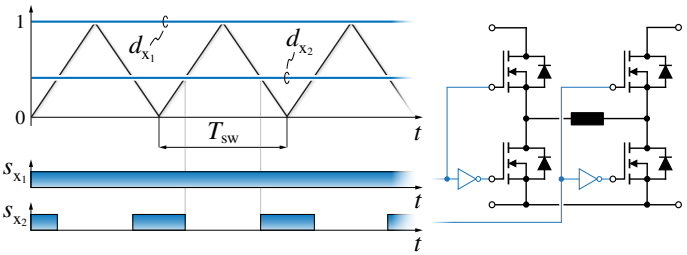

Fig. 2. Generation of the bridge-leg PWM switch signals s_{x_1}, s_{x_2} (boost mode).

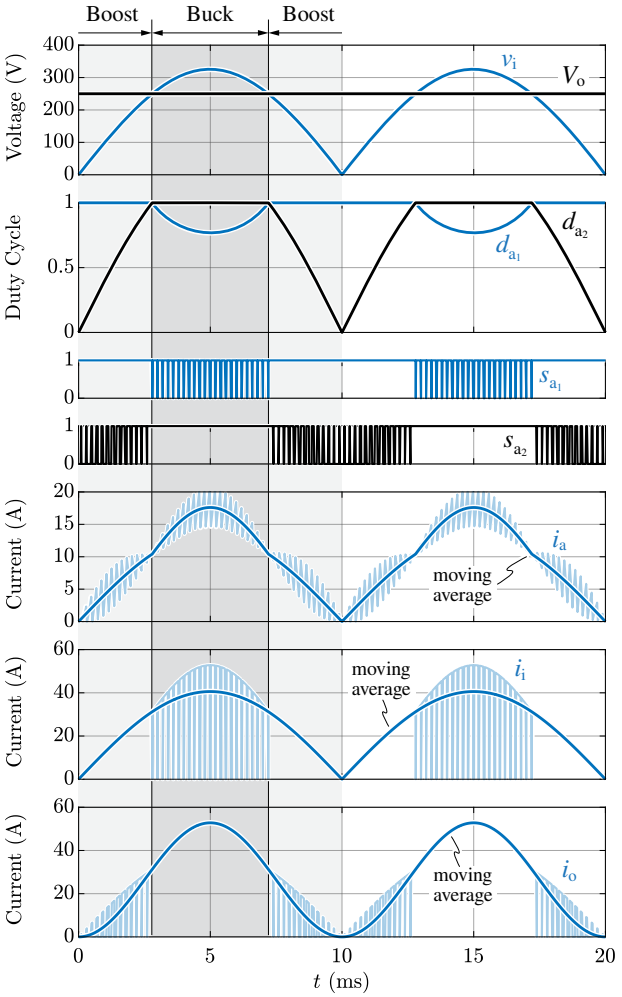

Fig. 3. iOBC simplified characteristic waveforms with $V_g = 325\,\mathrm{V}$ (i.e., European single-phase low-voltage grid), $V_o = 250\,\mathrm{V}$ and $P = 6.6\,\mathrm{kW}$. The boost mode and buck mode operating intervals are highlighted.

It is worth noting that the three buck-boost DC/DC units can be modulated with in-phase carriers or with phase-shifted carriers. In general, carrier interleaving may improve the phase current ripple performance by converting part of the common-mode (CM) voltage into differential-mode (DM) voltage, which is applied across a much larger inductance [9]. Nevertheless, interleaved operation may lead to higher PWM-induced losses in the machine at high frequency [3], as the DM flux paths involve a larger portion of the machine stator and rotor iron [33]. In the following analysis (cf. Section III), both in-phase carriers and 120° phase-shifted carriers are considered.

Simplified characteristic waveforms of the proposed iOBC concept with in-phase PWM carriers are illustrated in Fig. 3, where the battery voltage level is selected to be below the grid peak voltage, thus allowing for both buck and boost operating modes to take place over a grid semi-period. Notably, only one bridge-leg within each buck-boost DC/DC converter unit is modulated at any given point in time [34], effectively reducing the total switching losses. It is worth highlighting that during buck mode operation the amplitude of the machine phase currents i_{abc} is increased according to the inverse of the primary-side bridge-leg duty cycle d_{x_1}, in order to maintain the sinusoidal shape of the input current i_{i} (cf. Section IV).

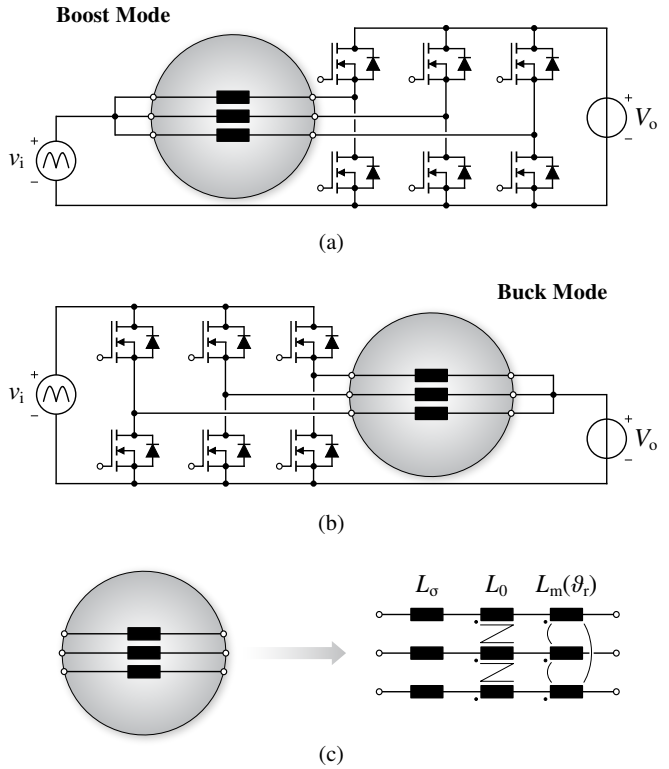

Fig. 4. Equivalent circuit schematic of (a) the iOBC in boost mode operation, (b) the iOBC in buck mode operation and (c) the generic electrical machine, represented as mutually coupled inductors (L_σ, L_0, L_m) [9].

The simplified equivalent circuits of the iOBC system operating in boost mode and buck mode are illustrated in Fig. 4(a) and (b), respectively, highlighting that the switching operation of the two three-phase inverters is mutually exclusive. Furthermore, Fig. 4(c) shows the equivalent circuit representation of a generic electrical machine, consisting of three sets of inductors [9]: the phase leakage inductance L_σ, the mutually-coupled zero-sequence inductance L_0 and the mutually-coupled magnetizing inductance L_m. This equivalent circuit representation addresses all kinds of synchronous and asynchronous electrical machines, such as induction machines, surface permanent magnet machines, interior permanent magnet machines, synchronous reluctance machines and electrically-excited synchronous machines (i.e., with rotor excitation). In particular, L_m is a 3x3 matrix and depends on the rotor angular position ϑ_r when the machine rotor is anisotropic [9]. It is worth noting that, for induction machines, the equivalent circuit in Fig. 4(c) approximately reduces to the stator leakage inductance from a CM perspective and to the sum of stator and rotor leakage inductances from a DM perspective, since the rotor cage/winding reacts to the pulsating stator flux similarly to a short-circuited transformer.

III. Component Stress Analysis

In this section, the stresses applied to the semiconductor devices, the machine phases and the input/output filter capacitors are analyzed, providing useful tools for the preliminary estimation of the system loss/efficiency and for the design/sizing of the components.

A. Semiconductor Losses

The diodes of the input rectifier are only characterized by conduction losses, i.e.

$$P_{\mathrm{D}} = P_{\mathrm{cond,D}} \approx V_{\mathrm{D}}\, I_{\mathrm{D,AVG}} + R_{\mathrm{D}}\, I^2_{\mathrm{D,RMS}}, \tag{3}$$

where V_{D} and R_{D} are the diode on-state threshold voltage and differential resistance, respectively, whereas $I_{\mathrm{D,AVG}}$ and $I_{\mathrm{D,RMS}}$ are the diode average and RMS current stresses, respectively. These stresses are obtained as

$$I_{\mathrm{D,AVG}} = \frac{I_{\mathrm{g}}}{\pi}, \quad I^2_{\mathrm{D,RMS}} = \frac{I^2_{\mathrm{g}}}{4}, \tag{4}$$

where I_{g} is the peak value of the grid phase current. The total rectifier losses are therefore obtained as $4\,P_{\mathrm{D}}$.

The active switches of the DBI are subject to both conduction and switching losses, which are independent of the PWM carrier interleaving. Assuming the adoption of unipolar semiconductor devices (e.g., MOSFETs, HEMTs), the average conduction losses of each transistor can be expressed as

$$P_{\mathrm{cond,T}} \approx R_{\mathrm{T}}\, I^2_{\mathrm{T,RMS}}, \tag{5}$$

where R_{T} is the transistor on-state resistance and $I_{\mathrm{T,RMS}}$ is the transistor RMS current stress. Assuming identical resistance values among the transistors, the total DBI conduction losses can be estimated as $6\,R_{\mathrm{T}}\, I^2_{\mathrm{x,RMS}}$, where $I_{\mathrm{x,RMS}}$ (i.e., $\mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c}$) is the RMS current flowing through each machine phase:

$$I^2_{\mathrm{x,RMS}} = \begin{cases} \dfrac{I^2_{\mathrm{g}}}{18} & M \leq 1 \\ \dfrac{I^2_{\mathrm{g}}}{12\pi}\left[\dfrac{\pi}{2}M^2 + \left(1 - \dfrac{2}{3}\dfrac{1}{M^2}\right)\sqrt{M^2-1} \right. \\ \qquad \left. + \left(\dfrac{4}{3} - M^2\right)\operatorname{asin}\left(\dfrac{1}{M}\right)\right] & M > 1 \end{cases} \tag{6}$$

where $I_{\mathrm{i}} \approx I_{\mathrm{g}}$ has been assumed and the machine phase current ripple has been neglected. Expression (6) is illustrated in Fig. 5 normalized with respect to I^2_{g}. In addition to the conduction losses, the instantaneous hard-switching losses of one transistor can be calculated as

$$p_{\mathrm{sw,T}} = f_{\mathrm{sw}}\left[E_{\mathrm{on}}\left(i_{\mathrm{sw}}\right) + E_{\mathrm{off}}\left(i_{\mathrm{sw}}\right)\right], \tag{7}$$

where f_{sw} is the switching frequency, E_{on} and E_{off} are the turn-on and turn-off switching energies, respectively, and i_{sw} is the instantaneous switched current (i.e., positive in the direction of the transistor). Since fast-switching unipolar devices are typically characterized by a linear dependence of the switching energies with respect to the switched current (i.e., $E_{\mathrm{on}} \approx k_{0,\mathrm{on}} + k_{1,\mathrm{on}}\, i_{\mathrm{sw}}$, $E_{\mathrm{off}} \approx k_{0,\mathrm{off}} + k_{1,\mathrm{off}}\, i_{\mathrm{sw}}$ for $i_{\mathrm{sw}} \geq 0$, and $E_{\mathrm{on}} = E_{\mathrm{off}} = 0$ for $i_{\mathrm{sw}} < 0$) [35], the average switching losses of one bridge-leg can be expressed as

$$P_{\mathrm{sw}} = f_{\mathrm{sw}}\left[\left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + I_{\mathrm{sw}}\left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right)\right], \tag{8}$$

where I_{sw} is the average switched current. Different expressions of I_{sw} are obtained for the primary-side and the secondary-side bridge-legs, respectively

$$I_{\mathrm{sw},1} = \begin{cases} 0 & M \leq 1 \\ \dfrac{I_{\mathrm{g}}}{3\pi}\left[\dfrac{1}{M}\sqrt{M^2-1} - M\left(\operatorname{asin}\left(\dfrac{1}{M}\right) - \dfrac{\pi}{2}\right)\right] & M > 1 \end{cases} \tag{9}$$

$$I_{\mathrm{sw},2} = \begin{cases} \dfrac{2I_{\mathrm{g}}}{3\pi} & M \leq 1 \\ \dfrac{2I_{\mathrm{g}}}{3\pi}\left(1 - \dfrac{1}{M}\sqrt{M^2-1}\right) & M > 1 \end{cases} \tag{10}$$

where $I_{\mathrm{i}} \approx I_{\mathrm{g}}$ has been assumed and the machine phase current ripple has been neglected. Expressions (9) and (10) are illustrated in Fig. 6 as functions of M and normalized with respect to I_{g}. The total DBI switching losses are therefore obtained as $6\, f_{\mathrm{sw}}\left(k_{0,\mathrm{on}} + k_{0,\mathrm{off}}\right) + 3\, f_{\mathrm{sw}}\left(I_{\mathrm{sw},1} + I_{\mathrm{sw},2}\right)\left(k_{1,\mathrm{on}} + k_{1,\mathrm{off}}\right)$.

B. Machine Phase Flux Ripple

The high-frequency voltage-time area applied to the machine phases generates a flux linkage ripple $\Delta\psi$ directly related to the magnetic flux density swing (and losses) within the machine stator/rotor cores and/or magnets. Furthermore, $\Delta\psi$ translates into a current ripple inversely proportional to the machine inductance, which generates additional winding losses. Therefore, $\Delta\psi$ is directly responsible for all PWM-induced high-frequency losses in the driven machine [33] and therefore represents a useful and comprehensive machine stress indicator.

Since the DBI drive system features an electrical machine with open-end windings (cf. Fig. 1), both DM and CM voltages

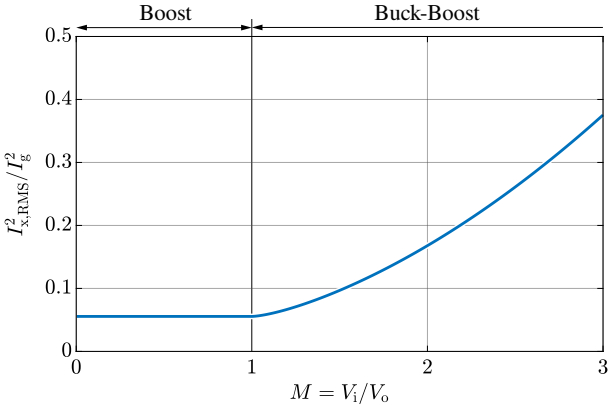

Fig. 5. Normalized RMS current stress $I^2_{\mathrm{x,RMS}}/I^2_{\mathrm{g}}$ affecting each machine phase and DBI bridge-leg as function of the modulation index M.

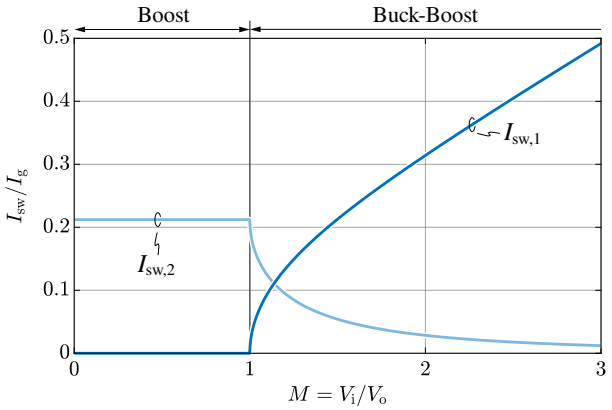

Fig. 6. Normalized primary-side and secondary-side bridge-leg average switched currents $I_{\mathrm{sw},1}/I_{\mathrm{g}}$, $I_{\mathrm{sw},2}/I_{\mathrm{g}}$ as functions of the modulation index M.

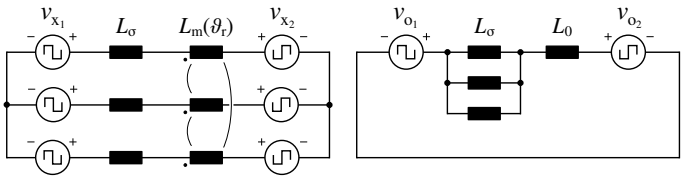

Fig. 7. (a) differential-mode (DM) and (b) common-mode (CM) equivalent circuits of the considered iOBC. v_{x_1}, v_{x_2}, v_{o_1}, v_{o_2} are defined in [24].

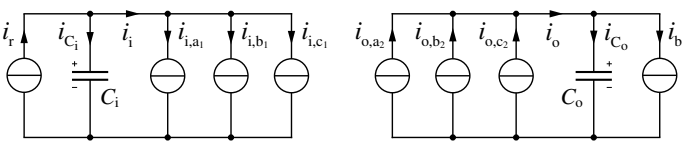

Fig. 9. (a) input-side and (b) output-side equivalent circuits of the considered iOBC.

are applied across the machine phases [24]. In particular, while the DM voltage sees the relatively large DM phase inductance $L_{\mathrm{DM}} \approx L_\sigma + L_\mathrm{m}(\vartheta_\mathrm{r})$ (cf. Fig. 7(a), where v_{x_1}, v_{x_2} are the primary-side and secondary-side DM voltages), the CM voltage is applied to the much lower common-mode inductance $L_{\mathrm{CM}} \approx L_\sigma/3 + L_0$ (cf. Fig. 7(b), where v_{o_1}, v_{o_2} are the primary-side and secondary-side CM voltages). Therefore, due to the different DM and CM flux paths within the machine (i.e., affecting core losses differently) and since $L_{\mathrm{DM}} \gg L_{\mathrm{CM}}$ (i.e., leading to very different current ripples and winding losses), the machine phase DM and CM flux ripple components must be analyzed independently. To take into account the flux ripple amplitude along the complete grid semi-period, the global DM and CM RMS flux ripples (i.e., $\Delta\Psi_{\mathrm{DM,RMS}}$, $\Delta\Psi_{\mathrm{CM,RMS}}$) are considered as performance indices, defined and calculated as in [24]. The results of the analysis are illustrated in Fig. 8, where $\Delta\Psi_{\mathrm{DM,RMS}}$ and $\Delta\Psi_{\mathrm{CM,RMS}}$ are reported in normalized form (i.e., with respect to $\Delta\Psi_\mathrm{n} = V_\mathrm{i}/f_\mathrm{sw}$) as functions of the modulation index M for both in-phase carriers and 120° phase-shifted carriers. It is observed that in-phase carriers lead to zero DM flux ripple, as the three buck-boost DC/DC units are synchronized and operated indentically, thus generating only CM voltage. On the other hand, the operation with 120° interleaved carriers shifts most of the voltage/flux stress to the DM component, thus minimizing the phase current ripple (i.e., $L_{\mathrm{DM}} \gg L_{\mathrm{CM}}$). It is worth noting that the piece-wise defined analytical expressions of $\Delta\Psi_{\mathrm{DM,RMS}}$ and $\Delta\Psi_{\mathrm{CM,RMS}}$ are not reported here for reasons of conciseness.

C. Input Capacitor RMS Current and Charge Ripple

The input capacitor C_i must filter the input current ripple to comply with the grid code and to reduce the current stress on the input diode bridge [36]. Therefore, C_i must be able to withstand the RMS current stress $I_{\mathrm{C_i,RMS}}$ and the peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{i,pp}}}$, which is directly proportional to the capacitor peak-to-peak voltage ripple and thus to the minimum required capacitance. Disregarding the machine phase current ripple, both stresses can be analytically calculated.

The equivalent circuit of the iOBC seen from the input side is reported in Fig. 9(a), where i_i is the sum of the DC-side bridge-leg currents of the first inverter unit (i.e., continuous in boost mode, discontinuous in buck mode, cf. Fig. 3) and i_r is the rectified grid-side current, assumed to be completely filtered and equal to the moving average of i_i (i.e., the line-frequency current in the capacitor is neglected, as it depends on the value of C_i). Therefore, the instantaneous current flowing into the input capacitor is obtained as difference between i_r and i_i and both the RMS current stress and the peak-to-peak charge ripple can be analytically calculated as explained in [24] (i.e., expressions not reported here for reasons of conciseness). The results of the analysis are illustrated in Fig. 10, where $I_{\mathrm{C_i,RMS}}$ and $\Delta Q_{\mathrm{C_i,pp}}$ are reported in normalized form (i.e., with respect to I_g and $\Delta Q_\mathrm{n} = I_\mathrm{g}/f_\mathrm{sw}$, respectively) as functions of the modulation index M for both in-phase carriers and 120° phase-shifted carriers. It is observed that in boost-only mode (i.e., $M \leq 1$) no switched current flows into C_i as $i_\mathrm{r} = i_\mathrm{i}$ (i.e., excluding the line-frequency current component), therefore $I_{\mathrm{C_i,RMS}} = 0$ and $\Delta Q_{\mathrm{C_i,pp}} = 0$. In buck-boost mode (i.e., $M > 1$), the 120° carrier interleaving provides significant benefits with respect to in-phase carriers, both in terms of $I_{\mathrm{C_i,RMS}}$ and $\Delta Q_{\mathrm{C_i,pp}}$.

D. Output Capacitor RMS Current and Charge Ripple

The output capacitor C_o must filter the output current ripple, so that it doesn't flow into the battery. Similarly to the input capacitor, C_o must be able to withstand the RMS current stress $I_{\mathrm{C_o,RMS}}$ and the peak-to-peak charge ripple $\Delta Q_{\mathrm{C_{o,pp}}}$. Disregarding the machine phase current ripple, both stresses can be analytically calculated. It is worth noting that, since the double-line frequency output current component can be compensated with an active power pulsation buffer or with the control strategy proposed in Section IV, only the high-frequency

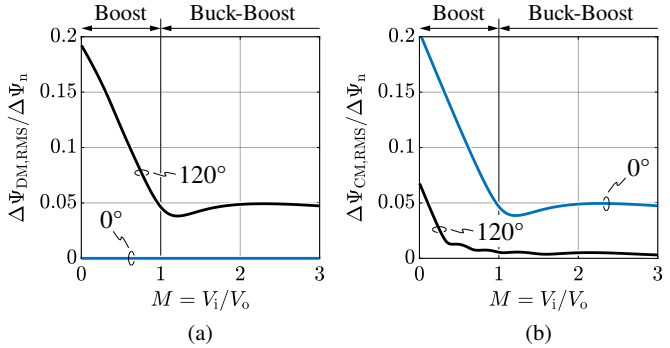

Fig. 8. Normalized machine phase (a) DM RMS flux ripple $\Delta\Psi_{\mathrm{DM,RMS}}$ and (b) CM RMS flux ripple $\Delta\Psi_{\mathrm{CM,RMS}}$ as functions of the modulation index M for in-phase PWM carriers (0°) and phase-shifted PWM carriers (120°).

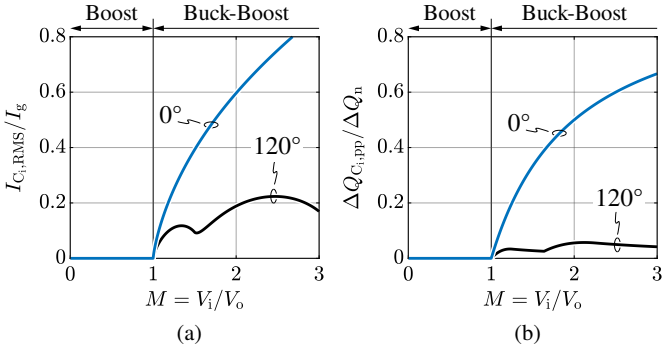

Fig. 10. Normalized input capacitor (a) RMS current stress $I_{\mathrm{C_i,RMS}}$ and (b) peak-to-peak charge ripple $\Delta Q_{\mathrm{C_i,pp}}$ as functions of the modulation index M for in-phase PWM carriers (0°) and phase-shifted PWM carriers (120°).

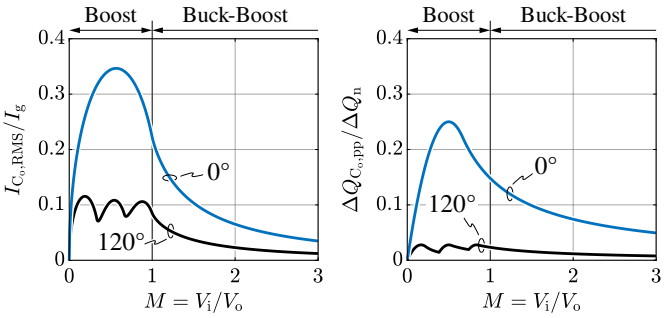

Fig. 11. Normalized output capacitor (a) RMS current stress $I_{C_o,RMS}$ and (b) peak-to-peak charge ripple $\Delta Q_{C_o,pp}$ as functions of the modulation index M for in-phase PWM carriers (0°) and phase-shifted PWM carriers (120°).

(i.e., switching frequency) current components are taken into account in the following.

The equivalent circuit of the iOBC seen from the output side is reported in Fig. 9(b), where i_o is the sum of the DC-side bridge-leg currents of the second inverter unit (i.e., continuous in buck mode, discontinuous in boost mode, cf. Fig. 3) and i_b is the battery-side current, assumed to be completely filtered and equal to the moving average of i_o. Therefore, the instantaneous current flowing into the output capacitor is obtained as difference between i_o and i_b and both the RMS current stress and the peak-to-peak charge ripple can be analytically calculated as explained in [24] (i.e., expressions not reported here for reasons of conciseness). The results of the analysis are illustrated in Fig. 11, where $I_{C_o,RMS}$ and $\Delta Q_{C_o,pp}$ are reported in normalized form (i.e., with respect to I_g and $\Delta Q_n = I_g/f_{sw}$, respectively) as functions of the modulation index M for both in-phase carriers and 120° phase-shifted carriers. Also in this case, it is observed that the 120° carrier interleaving provides significant benefits with respect to in-phase carriers, both in terms of $I_{C_o,RMS}$ and $\Delta Q_{C_o,pp}$.

IV. Closed-Loop Control

The control diagram of the proposed iOBC is illustrated in Fig. 12, where the measured quantities are indicated in blue (i.e., v_g, v_i, i_{abc}, V_o, ϑ_r). The synchronization with the grid, the output voltage control loop and the reference current shaper are implemented as in [36]. In particular, a moving average filter (MAF) is applied to V_o, in order not to react to the $2f$ voltage oscillation (if present). Due to the mutual coupling effect between the machine phases, the three phase currents i_a, i_b, i_c should not be controlled independently, therefore the dq0 reference frame is adopted as in [9], requiring the knowledge of the rotor angular position ϑ_r in anisotropic machines (i.e., with $L_d \neq L_q$) for proper loop tuning. In particular, i_d and i_q are continuously controlled to zero, ensuring equal phase current sharing and no torque production, whereas the zero-sequence current $i_0 = i_a + i_b + i_c$ regulates the power transfer (i.e., output of the V_o loop) and is controlled to provide sinusoidal input current shaping. The i_0 control loop is tuned according to the total zero-sequence/common-mode inductance $L_\sigma/3 + L_0$ (cf. Fig. 7(b)). To ensure the sinusoidal shape of i_g (i.e., the grid current), i_i must assume a rectified sine-wave shape, therefore the relation between i_i and i_0 (i.e., the controlled current) must be identified. Leveraging the definition of i_i,

$$i_i = d_{a_1} i_a + d_{b_1} i_b + d_{c_1} i_c, \tag{11}$$

and being $d_{a_1} \neq d_{b_1} \neq d_{c_1}$ in general, (11) can be expressed as

$$i_i = (d_{a_1} - d_{0_1})\, i_a + (d_{b_1} - d_{0_1})\, i_b + (d_{c_1} - d_{0_1})\, i_c + d_{0_1} i_0, \tag{12}$$

where $d_{0_1} = (d_{a_1} + d_{b_1} + d_{c_1})/3$ is the zero-sequence duty cycle of the primary-side inverter unit. Therefore, the zero-sequence current reference is obtained as

$$i_0^* = \frac{i_i^* - [(d_{a_1} - d_{0_1})\, i_a + (d_{b_1} - d_{0_1})\, i_b + (d_{c_1} - d_{0_1})]}{d_{0_1}}. \tag{13}$$

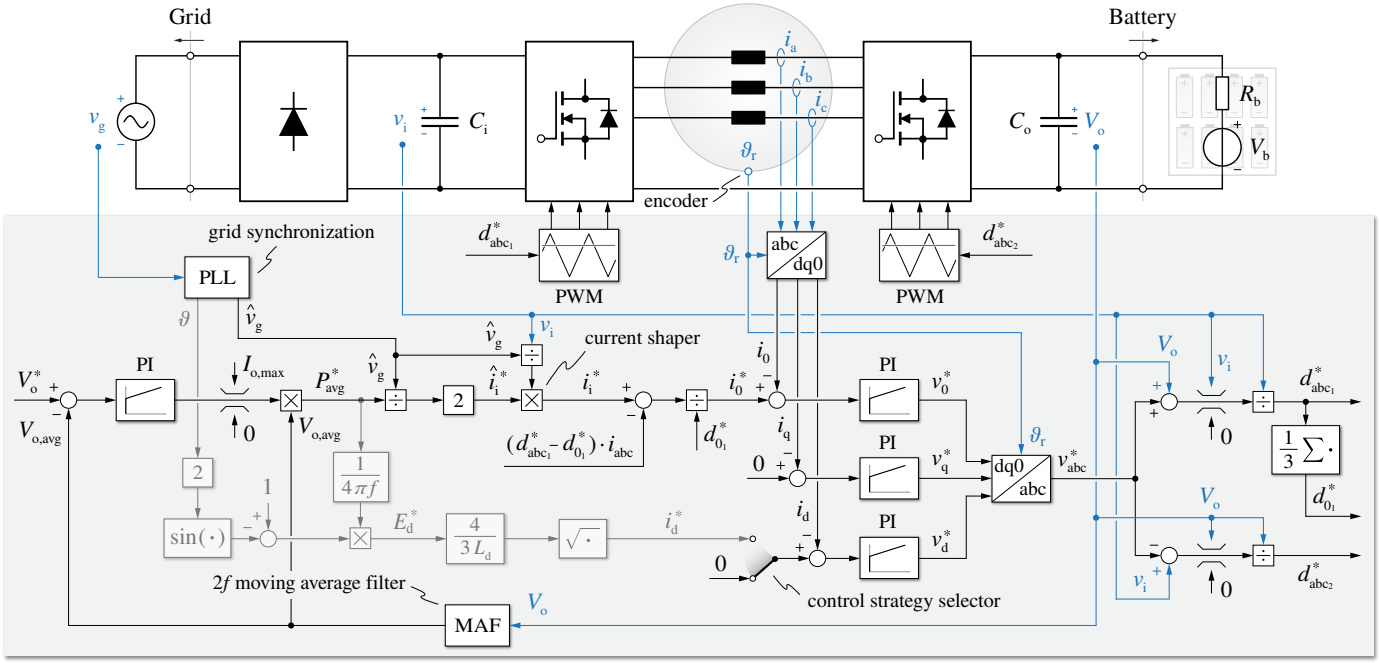

Fig. 12. Control diagram of the proposed iOBC, including the output voltage V_o, d-axis current i_d, q-axis current i_q and zero-sequence current i_0 control loops.

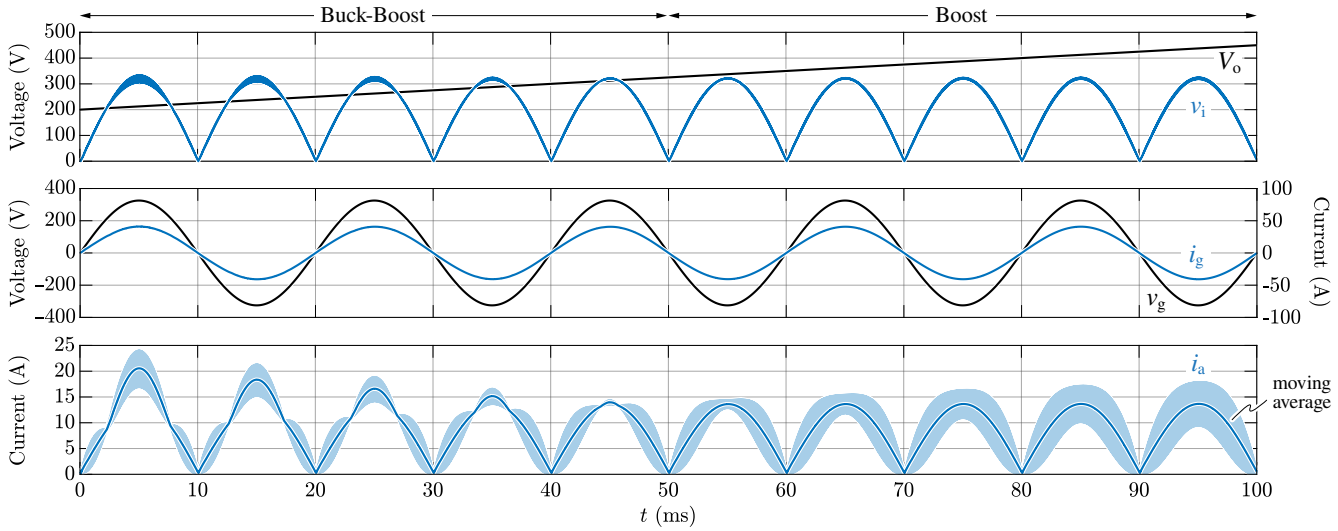

Fig. 13. Simulated closed-loop control waveforms of the proposed iOBC connected to the European low-voltage grid charging at 6.6 kW with variable battery voltage.

The most relevant simulated closed-loop control waveforms are illustrated in Fig. 13, assuming a 6.6 kW iOBC connected to the European low-voltage grid (i.e., 50 Hz, 230 V). The waveforms are obtained with in-phase PWM carriers and varying battery voltage between 200 V and 450 V. The following parameter values have been considered: $C_i = 5\,\mu F$, $C_o = 100\,\mu F$, $L_g = 500\,\mu H$ (i.e., 2 % inner grid inductance), $L_\sigma = 100\,\mu H$, $L_0 = 0$, $L_d = L_q = {}^3\!/_2\, L_m + L_\sigma = 3\,mH$ (i.e., isotropic machine) and $f_{sw} = 100\,kHz$ (i.e., exploiting the full-GaN 100 kVA DBI introduced in [24]). It is observed that in buck-boost mode, due to the switching operation of the primary-side inverter unit, the phase current $i_a = i_0/3$ is not a pure rectified sine-wave (i.e., according to (13)), nonetheless the grid current i_g remains purely sinusoidal.

The main drawback of the considered iOBC topology is related to the double-line frequency power pulsation, which is inherent to single-phase systems and, if not addressed, yields a typically unacceptable charging current ripple. This is illustrated on the left side of Fig. 14 (i.e., operation at $P = 6.6\,kW$, $V_o = 250\,V$), where the moving average of the output current i_o is a pure 100 Hz sine-wave with a DC offset equal to the average charging current. This large oscillation can be addressed either with bulky electrolytic capacitors, which must provide a lower impedance path with respect to the battery, or with an active power pulsation buffer, which can be obtained with a dedicated converter [25], [26], with the EV auxiliary DC/DC converter [27]–[30], or with a proper iOBC control strategy, as proposed here (cf. Fig. 12). Leveraging the magnetic energy storage capability of the machine along the axis with highest inductance (i.e., d-axis, to minimize the required current per unit of stored energy), the input power pulsation can be dynamically stored within the electrical machine by setting the d-axis current reference as

$$i_d^* = \sqrt{\frac{4}{3}\frac{E_d}{L_d}} \tag{14}$$

where E_d is the total magnetic energy stored in the machine

$$E_d = \frac{P_{avg}}{4\pi f}\left[1 - \sin(2\vartheta)\right] \tag{15}$$

and P_{avg} is the average transferred power.

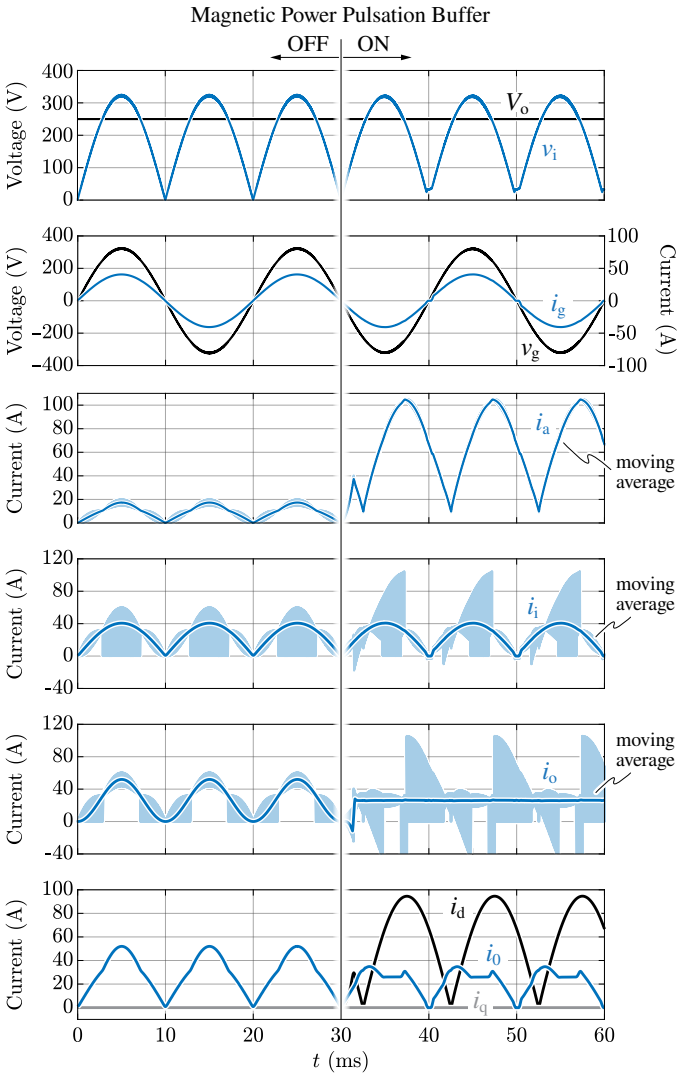

Fig. 14. Simulated control waveforms assuming $P = 6.6\,kW$, $V_o = 250\,V$, $\vartheta_r = 0$ highlighting the effect of the proposed magnetic power pulsation buffer.

The results are shown on the right side of Fig. 14. It is observed that the amplitude of the phase current i_a increases significantly due to the addition of the d-axis current component,

which allows to eliminate the $100\,\mathrm{Hz}$ oscillation from the output charging current i_o, however increasing the system losses. Notably, the zero-sequence current i_0 changes shape, as the active control of the d-axis current modifies the duty cycles d_{abc_1} in (13). Furthermore, it is worth noting that the grid-side current i_g remains sinusoidal, however a small zero-crossing distortion appears, since when $v_\mathrm{i} \approx 0$, the available input voltage is no longer sufficient to control both i_d and i_0, causing the premature saturation of the duty cycles.

V. Conclusion

This paper has introduced a novel single-phase buck-boost integrated on-board charger (iOBC) concept based on a next-generation $400\,\mathrm{V}$ double bridge inverter (DBI) electric vehicle (EV) drive system. The proposed topology is able to operate with a universal mains interface and can exploit all kinds of synchronous/asynchronous electrical machines with an open-end winding configuration, independently of the rotor isotropic or anisotropic structure. Moreover, the proposed iOBC concept only requires the addition of a line-frequency single-phase rectifier bridge rated for charging current, an input filter capacitor and two reconfiguration switches.

The basics of operation of the iOBC have been described and the stresses on all active and passive system components (i.e., semiconductor devices, electrical machine, input/output filter capacitors) have been analyzed in detail, providing useful tools for the loss/efficiency evaluation of the converter and the sizing of the components. Moreover, the closed-loop control of the iOBC has been explained and assessed in simulation. In particular, a novel control strategy aimed at addressing the double-line frequency power pulsation inherently related to single-phase systems has been proposed, exploiting the magnetic energy storage capability of the electrical machine to compensate the single-phase power pulsation.

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