# Channel doping concentration and cell program state dependence on random telegraph noise spatial and statistical distribution in 30 nm NAND flash memory 

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#### Abstract

The dependence of spatial and statistical distribution of random telegraph noise (RTN) in a 30 nm NAND flash memory on channel doping concentration $N_{\mathrm{A}}$ and cell program state $V_{\text {th }}$ is comprehensively investigated using three-dimensional Monte Carlo device simulation considering random dopant fluctuation (RDF). It is found that single trap RTN amplitude $\Delta V_{\mathrm{th}}$ is larger at the center of the channel region in the NAND flash memory, which is closer to the jellium (uniform) doping results since $N_{\mathrm{A}}$ is relatively low to suppress junction leakage current. In addition, $\Delta V_{\text {th }}$ peak at the center of the channel decreases in the higher $V_{\text {th }}$ state due to the current concentration at the shallow trench isolation (STI) edges induced by the high vertical electrical field through the fringing capacitance between the channel and control gate. In such cases, $\Delta V_{\text {th }}$ distribution slope $\lambda$ cannot be determined by only considering RDF and single trap.


## 1. Introduction

Random telegraph noise (RTN) is considered to be one of the major error/noise sources in ultra-scaled flash memory technology. ${ }^{1-8)}$ RTN is induced by capture/emission of single electron in a gate oxide trap, which is generated by fabrication process or program/erase cycling stress. Therefore, RTN results in threshold voltage ( $V_{\mathrm{th}}$ ) fluctuation as shown in Figure 1. RTN characteristics in the floating gate (FG) type NOR flash memories have been already extensively studied. ${ }^{2-8)}$ In these works, it is found that threshold voltage shift $\Delta V_{\text {th }}$ (RTN amplitude) depends on the channel doping profiles as well as the trap position and density at the gate oxide interface using three-dimensional (3D) Monte Carlo device simulation with random dopant fluctuation (RDF). ${ }^{9-12)}$ Also, assuming uniform doping profile with relatively high channel doping concentration $N_{\mathrm{A}}$ beyond $1 \times 10^{18} \mathrm{~cm}^{-3}, \Delta V_{\mathrm{th}}$ exhibits exponential distribution whose slope value is $\lambda$ and standard deviation is proportional to the square root of $N_{\mathrm{A}} \cdot{ }^{1,3-5)}$ Meanwhile, in FG type NAND flash memory, the cell design and operation are totally different from NOR in terms of the channel profiles and operating voltage as shown in Table I. $N_{\mathrm{A}}$ is expected to be kept as low as possible (< $1 \times 10^{18} \mathrm{~cm}^{-3}$ ) to suppress junction leakage current unless the short channel effect (SCE) becomes too significant. ${ }^{13-17)}$ Otherwise, the channel voltage $\left(V_{\mathrm{CH}}\right)$ cannot be maintained sufficiently high ( $\sim 8 \mathrm{~V}$ ) at the unselected cell during program inhibit operation using channel self-boosting technique ${ }^{18,19)}$ as shown in Figure 2. In this scheme, the NAND string channel potential is boosted utilizing capacitive coupling between the control gate (CG) and channel by turning off select gates. During channel self-boosting, the channel voltage drop by the leakage current at p-n junction results in unwanted electron injection to the floating gate (FG) called program disturbance.

On the other hand, there are also reports that focusing on RTN effects in NAND flash memories. ${ }^{20-26)}$ However in these reports, analyses are mainly based on measurement results, which are derived from macroscopic physical values. In other words, microscopic physics obtained from statistical 3D Monte Carlo device simulation would provide further understandings to the RTN in ultra-scaled NAND flash memory.

In this work, RTN characteristics in 30 nm NAND flash memory are analyzed through 3D Monte Carlo device simulation considering RDF. Two points are focused. First, single trap RTN amplitude $\Delta V_{\text {th }}$ and its distribution $\lambda$ are evaluated by widely varying $N_{\mathrm{A}}$ from
$1 \times 10^{17}$ to $3 \times 10^{18} \mathrm{~cm}^{-3}$. Cases for jellium and discrete doping are also compared. Figure 3 shows the differences between the jellium and discrete doping case. In the jellium doping case, dopants are uniformly distributed (no atomistic effect) while the discrete doping considers atomistic effect of the dopants. The results reveal that in NAND flash memory (low $N_{\mathrm{A}}$ ), RTN characteristics are more like the jellium doping case where drain current $I_{\mathrm{D}}$ flows at the center of the channel. Second, $\Delta V_{\text {th }}$ and its distribution $(\lambda)$ are evaluated with varying cell program state $\left(V_{\text {th }}\right)$ by changing charge amount in FG assuming 2 bit/cell multi-level cell (MLC) architecture. Simulations are also performed for different $N_{\mathrm{A}}$. As cell $V_{\mathrm{th}}$ increases in high $V_{\mathrm{th}}$ program state, $I_{\mathrm{D}}$ concentrates at the shallow trench isolation (STI) edges due to the high vertical electrical field by fringing capacitance resulting in different trends for both low and high $N_{\mathrm{A}}$.

This paper is organized as follows. In Sect. 2, device simulation conditions are explained. Sect. 3 shows and discusses the results of the $N_{\mathrm{A}}$ dependence of $\Delta V_{\text {th }}$ distribution for discrete doping and jellium case. Sect. 4 shows cell program state dependence of $\Delta V_{\text {th }}$ distribution. Finally, conclusions are given in Sect. 5.

## 2. 3D device simulation conditions

Figure 4(a) shows the 30 nm 2 bit/cell NAND flash memory cell structure for 3D device simulation used in this work. Figures 4(b) and 4(c) show the cross section view for x-z plane and y-z plane, respectively. $\mathrm{SiO}_{2}$ tunnel oxide thickness $t_{\mathrm{ox}}$, inter-poly dielectric thickness $t_{\mathrm{IPD}}$, and FG height $t_{\mathrm{FG}}$ are 7,10 , and 80 nm , respectively. Both channel width $W$ and length $L_{\mathrm{g}}$ are set to 30 nm , and source/drain junction depth $x_{\mathrm{j}}$ is set to 10 nm . In this work, $N_{\mathrm{A}}$ is widely varied from $1 \times 10^{17}$ to $3 \times 10^{18} \mathrm{~cm}^{-3}$ while punch-through stopper (PTS) layer is adopted at 30 nm below the source/drain junction to suppress excess SCE. PTS doping concentration is increased as $N_{\mathrm{A}}$ is increased.

Monte Carlo simulations over 100 NAND flash cells are performed including RDF effect. The threshold voltage difference between trapped and de-trapped states is extracted as $\Delta V_{\mathrm{th}}$ for each NAND cell having different discrete doping profiles based on methods in references. ${ }^{2,4-8)}$ Threshold voltage $V_{\mathrm{th}}$ is defined as the $V_{\mathrm{CG}}$ value when $I_{\mathrm{D}}$ reaches $W / L_{\mathrm{g}} \times 10^{-7} \mathrm{~A}$. To emulate the trapped states, $1 \mathrm{~nm}^{2}$ square negative surface charge is randomly placed at the channel surface (tunnel oxide/substrate interface) whose charge
amount equals to single electron. In this work, trap energy levels are not considered for simplicity. ${ }^{2)}$ Therefore, channel potential dependence on time constants and $\Delta V_{\text {th }}$ of the trap/de-trap phenomenon are not included. For changing cell program states, charge amount in the FG is changed to adjust the $V_{\text {th }}$ to the desired value for MLC operation, which will be explained in detail at Sect. 4.

## 3. $N_{\mathrm{A}}$ dependence of $\Delta V_{\text {th }}$ distribution

Simulation results of $\Delta V_{\text {th }}$ spatial distributions ( $\Delta V_{\text {th }}$ against trap position along $L_{\mathrm{g}}$ and $W$ for each $N_{\mathrm{A}}$ ) are shown in Figures 5(a)-5(j). At low $N_{\mathrm{A}}\left(1 \times 10^{17}\right.$ and $\left.3 \times 10^{17} \mathrm{~cm}^{-3}\right)$, it is found that $\Delta V_{\text {th }}$ is large at the center of the channel for both $L \mathrm{~g}$ and $W$ direction. $\Delta V_{\text {th }}$ distribution peak for position along $L_{\mathrm{g}}$ slightly locates near the source side since the drain voltage $V_{\mathrm{D}}$ of 0.5 V induces weak electrostatic potential asymmetry by drain-induced barrier lowering (DIBL). ${ }^{8}$ ) However, as $N_{\mathrm{A}}$ increases, $\Delta V_{\mathrm{th}}$ distribution peak along $W$ moves slightly towards the channel STI edges. Furthermore, extremely large $\Delta V_{\mathrm{th}}$ is observed at the highest $N_{\mathrm{A}}$ case. Figures 6(a) and 6(b) show current density distributions of the channel surface near $V_{\text {th }}$ for the low and high $N_{\mathrm{A}}$ devices, respectively. For the low $N_{\mathrm{A}}$ case [Fig. 6(a)], current widely flows at the center of the channel, corresponding to the $\Delta V_{\mathrm{th}}$ spatial distribution in Figures 5(b) and 5(d). On the other hand, in the high $N_{\mathrm{A}}$ case [Fig. 6(b)], huge RTN is observed when the trap locates above the percolation current path formed by the random discrete dopants. ${ }^{2,9,10)}$ Figures 7(a)-7(d) show $\Delta V_{\text {th }}$ spatial distribution in jellium doping case. When $N_{\mathrm{A}}$ is low, the $\Delta V_{\text {th }}$ spatial distribution of the discrete doping case [Figs. 5(c) and 5(d)] is nearly the same as the jellium doping case [Figs. 7(a) and 7(b)] indicating that very few dopants locate at the channel surface and hardly create percolation path. Considering 30 nm cubic area, only $2 \sim 3$ dopants exist on average in the region when $N_{\mathrm{A}}=1 \times 10^{17} \mathrm{~cm}^{-3}$. As for the high $N_{\mathrm{A}}$ case [Figs. 7(c) and 7(d)], slight $\Delta V_{\text {th }}$ peaks near the STI edges are also observed in the jellium case [Fig. 7(d)]. However, outlier sample is not observed in this case. It is also found that $\Delta V_{\text {th }}$ at high $N_{\mathrm{A}}$ is smaller than that at low $N_{\mathrm{A}}$ [Figs. 7(b) and 7(d)]. In order to clarify the origin of this difference, channel surface current density distributions along $W$ for the huge $\Delta V_{\text {th }}$ outlier sample in discrete dopant case and jellium case are extracted and compared as shown in Figure 8. Both trapped and de-trapped states are shown for the discrete and jellium doping
simulation results. From the current density distribution in the jellium case, current crowding is observed at the both sides of the STI edge, which is considered to be the electric field concentration by the corner effect at high $N_{\mathrm{A}}$ doping. ${ }^{27,28)}$ The slight $\Delta V_{\text {th }}$ peak shift towards the STI edge can be explained from this phenomenon for both jellium and discrete doping simulation results. However, two current peaks are symmetrical in the jellium case while in the outlier sample, the current peak only locates on one (the right) side. Since single trap is considered in this simulation, current can still flow at the opposite edge even when the trap locates at the either side of the STI edge in the jellium case. Therefore, $\Delta V_{\text {th }}$ is not huge compared to the outlier case where the current path is completely blocked when the trap site exactly locates above the single current path. The reason for smaller $\Delta V_{\text {th }}$ at higher $N_{\mathrm{A}}$ in the jellium doping case can be also explained from the current density distribution profiles along $W$ as shown in Figure 9. From Figures 9(a) and $9(\mathrm{~b}), \Delta V_{\text {th }}$ would be larger in the lower $N_{\mathrm{A}}$ case since the large portion of the current path is blocked and the maximum current density is reduced when the trap site locates above the channel center at low $N_{\mathrm{A}}$. It should be noted that the discussion is valid in the single trap case handled in this work and the result would be different in the multiple trap case. If two traps locate on both edges, the results above imply that large RTN would appear even in the jellium case.

Figures 10 (a) and $10(\mathrm{~b})$ show $\Delta V_{\text {th }}$ probability distributions for the jellium and discrete doping case, respectively. Distribution slope $\lambda$ cannot be determined below $N_{\mathrm{A}}=2 \times 10^{18}$ $\mathrm{cm}^{-3}$ [Fig. 10(b)] as well as in the jellium case [Fig. 10(a)], since $\Delta V_{\text {th }}$ tail bits do not exist due to the absence of the percolation path. Other physical origins should be considered such as multiple trap sites ${ }^{2,20,21)}$ or line edge roughness ${ }^{29-31)}$ to account for the $\Delta V_{\text {th }}$ tail bits found in the NAND flash memory measurement results in the other reports. ${ }^{20-26)}$ Figures 11(a) and 11 (b) show $N_{\mathrm{A}}$ dependence of the average and standard deviation of $\Delta V_{\mathrm{th}}$, respectively. Average $\Delta V_{\mathrm{th}}$ of the discrete doping case agrees well with the jellium, and continues to decrease as $N_{\mathrm{A}}$ increases. This is because channel current broadly flows in the low $N_{\mathrm{A}}$ cells and the current peak gradually becomes sharp as $N_{\mathrm{A}}$ increases by the electric field concentration at the STI edge (note that channel also becomes percolative in the discrete doping case). On the other hand, standard deviation of $\Delta V_{\text {th }}$ starts to increase above $N_{\mathrm{A}}=1 \times 10^{18} \mathrm{~cm}^{-3}$ in the discrete doping case as the percolation path starts to appear
in the channel.

## 4. Effect of cell program state

In this section, $\Delta V_{\text {th }}$ distribution is evaluated with varying cell program state by changing the charge amount in the FG. Figure 12 shows $V_{\text {th }}$ distribution and corresponding data symbols in MLC NAND flash memory. ${ }^{32)} N_{\mathrm{A}}$ is also varied where its value are $1 \times 10^{17}$, $3 \times 10^{17}$, and $3 \times 10^{18} \mathrm{~cm}^{-3}$, respectively. Here, fluctuation of the charge amount in the FG within each program state is not considered for simplicity. Figures 13(a)-13(d) show $\Delta V_{\text {th }}$ distribution along $L_{\mathrm{g}}$ and $W$ with cell data symbol for " 11 " (the lowest $V_{\text {th }}$ state corresponding to the erase state) and " 10 " (the highest $V_{\text {th }}$ state) when $N_{\mathrm{A}}=3 \times 10^{17} \mathrm{~cm}^{-3}$. Figures 13(e)-13(h) are those when $N_{\mathrm{A}}=3 \times 10^{18} \mathrm{~cm}^{-3}$. At low $N_{\mathrm{A}}\left(3 \times 10^{17} \mathrm{~cm}^{-3}\right), \Delta V_{\mathrm{th}}$ distribution of Figures 13(a) and 13(b) are basically the same as Figures 5(c) and 5(d) when data symbol is " 11 ". However, as $V_{\mathrm{th}}$ increases (data symbol " 10 "), maximum and minimum $\Delta V_{\text {th }}$ near the center of channel along $L_{\mathrm{g}}$ direction decreases [Fig. 13(c)]. Furthermore, $\Delta V_{\text {th }}$ peak along $W$ direction is diminished [Fig. 13(d)]. On the other hand, at high $N_{\mathrm{A}}\left(3 \times 10^{18} \mathrm{~cm}^{-3}\right)$ in Figures 13(e)-13(h), $\Delta V_{\mathrm{th}}$ distribution shape is less dependent on data symbols compared to the low $N_{\mathrm{A}}$ case, although $\Delta V_{\text {th }}$ peak slightly moves toward the channel STI edges along $W$ direction in Figure 13(h). Also, extremely large $\Delta V_{\mathrm{th}}$ is observed for both " 11 " and " 10 " data symbols. Figures 14(a) and 14(b) show channel surface current distribution at the center of the channel for low and high $N_{\mathrm{A}}$ in typical samples with discrete doping, respectively. As shown in Figure 14(a), when $N_{\mathrm{A}}$ is low, the current distribution shape is completely inverted for two program states. The current peak is at the center of the channel for the low $V_{\text {th }}$ state " 11 " while it is at the channel STI edges for the high $V_{\text {th }}$ state " 10 ". The reason for the current crowding at the STI edges at " 10 " state is due to the fringing electrical field from CG to channel, since higher voltage is applied to the CG to invert the channel. ${ }^{22)}$ Therefore, $\Delta V_{\text {th }}$ at the center of the channel is reduced in " 10 " state in Figure 13(d). Also, the reason why high $\Delta V_{\mathrm{th}}$ is not observed at the STI edge in "10" state in Figure 13(d) can be explained by the same mechanism discussed in Figure 8 jellium case, where two current peaks existing in single trap simulations. On the other hand, at high $N_{\mathrm{A}}$, current path concentrates at the STI edge region for both " 11 " and " 10 " state but not symmetry as shown in Figure 14(b). In particular, this trend is more
prominent in " 10 ", where the maximum current density surpasses $5 \times 10^{6} \mathrm{~A} / \mathrm{cm}^{2}$. Figures 15 (a) and 15 (b) show $\Delta V_{\text {th }}$ probability distributions for four data symbols at $N_{\mathrm{A}}=3 \times 10^{17}$ and $3 \times 10^{18} \mathrm{~cm}^{-3}$, respectively. Figure. 16 shows standard deviation of $\Delta V_{\mathrm{th}}$ as a function of $V_{\text {th }}$ of the program state. Distribution slope $\lambda$ is still not available at low $N_{\mathrm{A}}$ even if the program state changes. Furthermore, $\Delta V_{\text {th }}$ tail bits are reduced at " 10 " state, which can be seen from Figure 15(a) and the decrease in $\Delta V_{\text {th }}$ standard deviation in Figure 16. This is due to the current concentration at the both STI edges in the single trap condition as discussed before. On the other hand, $\lambda$ can be extracted at the high $N_{\mathrm{A}}$ case except for the "10" state due to the RDF induced percolation path as shown in Figure 15(b). It is interesting that three distribution tendencies are found in the " 10 " state according to the $\Delta V_{\text {th }}$ range as indicated by $\lambda_{1}, \lambda_{2}$ and $\lambda_{3}$ lines in Figure 15(b). The tail distribution $\lambda_{2}$ of $250 \mathrm{mV} / \mathrm{dec}$ is larger than $\lambda_{1}$ of $145 \mathrm{mV} / \mathrm{dec}$, since strong current concentration by the fringing electrical field and RDF induces large $\Delta V_{\text {th }}$ when a trap locates above the current path. However, $\lambda$ significantly reduces to $\lambda_{3}$ of $45 \mathrm{mV} / \mathrm{dec}$ for even higher $\Delta V_{\mathrm{th}}$. This is because the fringing electrical field from the CG tries to induce two current paths at the STI edges and $\Delta V_{\text {th }}$ is suppressed in the single trap condition.

From these results, the amplitude and distribution of RTN in NAND flash memory with low $N_{\mathrm{A}}$ strongly depends on the cell program state. The results also indicate that the number of trap sites would significantly affect the NAND flash memory RTN characteristics.

## 5. Conclusions

The spatial and statistical distributions of RTN in a 30 nm node NAND flash memory in terms of $N_{\mathrm{A}}$ and cell program state $V_{\text {th }}$ are studied using 3D Monte Carlo device simulation assuming single trap. Low $N_{\mathrm{A}}$ and low cell state $V_{\text {th }}$ in NAND flash memory result in large $\Delta V_{\text {th }}$ at the center of the channel region, showing jellium-like characteristics. On the other hand, as the programmed state $V_{\text {th }}$ increases, $\Delta V_{\text {th }}$ peak at the center of the channel decreases because $I_{\mathrm{D}}$ concentrates at the both STI edges due to the fringing electrical field from CG. Since single trap is considered in this work, $\Delta V_{\text {th }}$ is suppressed in spite of the high current concentration because alternative current path remains even if a trap locates
above either side of the STI edges. Therefore, exponential distribution $\lambda$ is only observed above $N_{\mathrm{A}}=1 \times 10^{18} \mathrm{~cm}^{-3}$ in this work, which is too high for NAND flash memory. In order to explain the $\Delta V_{\text {th }}$ tail bits in the NAND flash memory measurement results found in other reports, multiple trap sites or other physical origins will play an important role rather than RDF.

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## References

1) K. Takeuchi, T. Nagumo, S. Yokogawa, K. Imai, Y. Hayashi, Symp. VLSI Tech. Dig., 2009, p. 54.
2) A. Ghetti, C. M. Compagnoni, A. S. Spinelli, A. Visconti, IEEE Trans. Electron Devices 56, (2009) 1746.
3) S. M. Joe, M. K. Jung, W. Lee, M. S. Lee, B. S. Jo, J. H. Bae, S. K. Park, K. R. Han, J. H. Yi, G. S. Cho, J. H. Lee, Symp. VLSI Tech. Dig., 2011, p. 112.
4) C. M. Compagnoni, A. S. Spinelli, S. Beltrami, M. Bonanomi, A. Visconti, IEEE Electron Device Lett. 29, (2008) 941.
5) C. M. Compagnoni, R. Gusmeroli, A. S. Spinelli, A. Visconti, IEEE Trans. Electron Devices 55, (2008) 3192.
6) A. Ghetti, C. M. Compagnoni, F. biancardi, A. L. Lacaita, S. Beltrami, L. Chiavarone, A. S. Spinelli, A. Visconti, IEDM Tech. Dig., 2008, p. 1.
7) A. Ghetti, S. M. Amoroso, A. Mauri, C. M. Compagnoni, IMW Tech. Dig., 2011, p. 1.
8) A. Ghetti, S. M. Amoroso, A. Mauri, and C. M. Conpagnoni, IEEE Trans. Electron Devices 59, (2012) 309.
9) Y. Li, C. H. Hwang, T. Y. Li, M. H. Han, IEEE Trans. Electron Devices 57, (2010) 437
10) Y. Li, S. M. Yu, J. R. Hwang, F. L. Yang, IEEE Trans. Electron Devices 55, (2008) 1449.
11) S. Markov, A. S. M. Zain, B. Cheng, A. Asenov, SOI Conf., 2012 p. 1.
12) A. Asenov, IEEE Trans. Electron Devices 45, (1998) 2505.
13) Y. Taur, G. J. Hu, R. H. Dennand, L. M. Terman, Y. T. Chung, K. E. Petrillo, IEEE Trans. Electron Devices 32, (1985) 203.
14) R. R. Troutman, IEEE J. Solid-State Circuits 14, (1979) 383.
15) R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, IEEE Solid-State Integrated Circuits 9, (2003) 256.
16) D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, IEEE Trans. Electron Devices 47, (2002) 2320.
17) Z. H. Liu, H. Chenming, J. H. Huang, T. Y. Chan, M. C. Jeng, P. K. Ko, Y. C. Cheng, IEEE Trans. Electron Devices 40, (2002) 86.
18) A. Torsi, Y. Zhao, H. Liu, T. Tanzawa, A. Goda, P. Kalavade, K. Parat, IEEE Trans. Electron Devices 58, (2011) 11.
19) K. D. Suh, B. H. Suh, Y. H. Lim, J. K. Kim, Y. J. Choi, Y. N. Koh, S. S. Lee, S. C. Kwon, B. S. Choi, J. S. yum, J. H. Choi, J. R. Kim, and H. K. Lim, IEEE J. Solid-State Circuits. 30 (1995) 1149.
20) N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S. Kamohara, K. Tokami, Y. Ikeda, and R. Yamada, IEDM Tech. Dig., 2006, p. 1.
21) K. Fukuda, Y. Shimizu, K. Amemiya, M. Kamoshida, and C. Hu, IEDM Tech. Dig., 2007, p. 169.
22) T. Kim, D. He, R. Porter, D. Rivers, J. Kessenich, and A. Goda: IEEE Electron Device Lett. 31, (2010) 153.
23) T. Kim, N. Franklin, C. Srinivasan, P. Kalavade, and A. Goda: IEEE Electron Device Lett. 32, (2011) 1183.
24) D. Kang, S. Lee, H. M. Park, D. J. Lee, J. Kim, J. Seo, C. Lee, C. Song, C. S. Lee, H. Shin, J. Song, H. Lee, J. H. Choi, and Y. H. Jun: Symp. VLSI Tech. Dig., 2011, p. 206.
25) M. K. Jeong, S. M. Joe, H. J. Kang, K. R. Han, G. Cho, S. K. Park, B. G. Park, J. H. Lee: Symp. VLSI Tech. Dig., 2013, p. T154.
26) E. Nowak, J. H. Kim, H. Y. Kown, Y. G. Kim, J. S. Sim, S. H. Lim, D. S. Kim, K. H. Lee, Y. K. Park, J. H. Choi, C. Chung, Symp. VLSI Tech. Dig., 2012, p. 21.
27) W. Xiong, J. W. Park, J. P. Colinge, SOI Conf., 2003, p. 111.
28) T. Nagumo, and T. Hiramoto, IEEE Trans. Electron Devices 53, (2006) 3025.
29) F. L. Yang, J. R. Hwang, and Y. Li, IEEE CICC Tech. Dig., 2006, p. 691.
30) H. Fukutome, Y. Momiyama, T. Kubo, E. Yoshida, H. Morioka, M. Tajima, and T. Aoyama: IEDM Tech. Dig., 2006, p. 281.
31) A. Asenov, IEEE Trans. Electron Devices 50, (2003) 1837.
32) S. Tanakamaru, C. Hung, A. Esumi, M. Ito, K. Li, and K. Takeuchi, ISSCC Tech. Dig., 2011, p. 204.

## Figureure Captions

Fig. 1 (Color online) $I_{\mathrm{D}}-V_{\mathrm{CG}}$ characteristics for trapped and de-trapped states induced by RTN. Threshold voltage shifts by RTN.

Fig. 2 (Color online) Channel voltage ( $V_{\mathrm{CH}}$ ) self-boosting during program inhibit operation in NAND flash memory. $V_{\mathrm{CH}}$ in unselected NAND strings is self-boosted ( $\sim 8 \mathrm{~V}$ ) utilizing capacitance $C_{\mathrm{CG}}$ and $C_{\mathrm{CH}}$ by turning off select gates.

Fig. 3 (Color online) Schematics of dopants in the channel to show the differences between jellium and discrete doping. In jellium doping case, dopants are uniformly distributed while discrete doping considers atomistic effect of dopants.

Fig. 4 (Color online) Simulated 30 nm NAND flash memory cell structure. (a) NAND structure overall view, (b) the cross section view of channel gate length $L_{\mathrm{g}}$ direction at the center of channel width $W$, (c) the cross section view of $W$ direction at the center of $L_{\mathrm{g}}$.

Fig. 5 (Color online) $\Delta V_{\text {th }}$ against trap position along $L_{\mathrm{g}}$ and $W$ for each $N_{\mathrm{A}}$ in discrete doping case. (a, b) $N_{\mathrm{A}}=1 \times 10^{17} \mathrm{~cm}^{-3}$. (c, d) $N_{\mathrm{A}}=3 \times 10^{17} \mathrm{~cm}^{-3}$. (e, f) $N_{\mathrm{A}}=1 \times 10^{18} \mathrm{~cm}^{-3}$. (g, h) $N_{\mathrm{A}}=2 \times 10^{18} \mathrm{~cm}^{-3}$. (i, j) $N_{\mathrm{A}}=3 \times 10^{18} \mathrm{~cm}^{-3}$. For (a), (c), (e), (g), and (i), source edge is at 0 nm .

Fig. 6 (Color online) Current density distribution at the channel surface of the de-trapped state near $V_{\text {th. }}$. (a) $N_{\mathrm{A}}=1 \times 10^{17} \mathrm{~cm}^{-3}, V_{\mathrm{CG}}=-0.3 \mathrm{~V}$ (b) $N_{\mathrm{A}}=3 \times 10^{18} \mathrm{~cm}^{-3}, V_{\mathrm{CG}}=1.2 \mathrm{~V}$.

Fig. 7 (Color online) $\Delta V_{\text {th }}$ against trap position along $L_{\mathrm{g}}$ and $W$ for each $N_{\mathrm{A}}$ in jellium doping case. (a, b) $N_{\mathrm{A}}=1 \times 10^{17} \mathrm{~cm}^{-3}$. (c, d) $N_{\mathrm{A}}=3 \times 10^{18} \mathrm{~cm}^{-3}$.

Fig. 8 (Color online) Channel surface current density distribution profiles along $W$ for the huge $\Delta V_{\text {th }}$ outlier sample in the discrete dopant case and the jellium case. $V_{\mathrm{CG}}$ is 1.2 V for jellium doping case ( $V_{\mathrm{CG}}$ is same for both de-trapped and trapped states) and 1.3 V for discrete doping case.

Fig. 9 (Color online) Channel surface current density distribution profiles along $W$ between trapped and de-trapped state in the jellium doping case at (a) low and (b) high $N_{\mathrm{A}}$. $V_{\mathrm{CG}}$ is -0.15 and 1.3 V for low and high $N_{\mathrm{A}}$, respectively.

Fig. 10 (Color online) Statistical distribution of $\Delta V_{\text {th }}$. (a) Jellium doping and (b) discrete doping case.

Fig. 11 (Color online) (a) Average and (b) standard deviation of $\Delta V_{\text {th }}$ as a function of $N_{\mathrm{A}}$.

Fig. 12 (Color online) $V_{\text {th }}$ distribution and corresponding data symbols in MLC NAND flash memory. ${ }^{32)} V_{\text {th }}$ values for each program state used in this work are also shown.

Fig. 13 (Color online) $\Delta V_{\text {th }}$ distribution along $L_{\mathrm{g}}$ and $W$ with cell data symbol for "11" (lowest $V_{\text {th }}$ state representing erase state) and " 10 " (highest $V_{\text {th }}$ state). (a)-(d) $N_{\mathrm{A}}=3 \times 10^{17}$ $\mathrm{cm}^{-3}$. (e)-(h) $N_{\mathrm{A}}=3 \times 10^{18} \mathrm{~cm}^{-3}$.

Fig. 14 (Color online) Channel surface current distribution at the center of the channel for low and high $N_{\mathrm{A}}$ in typical samples with discrete doping (a) low $N_{\mathrm{A}}$ case and (b) high $N_{\mathrm{A}}$ case. $V_{\mathrm{CG}}$ is implied -2.5 and 3.5 V for data" 11 " and data " 10 " respectively.

Fig. 15 (Color online) $\Delta V_{\text {th }}$ probability distribution for four data symbol in (a) $N_{\mathrm{A}}=3 \times 10^{17}$ and (b) $3 \times 10^{18} \mathrm{~cm}^{-3}$.

Fig. 16 (Color online) Standard deviation of $\Delta V_{\mathrm{th}}$ as a function of $V_{\mathrm{th}}$ of the program state.

Table I Differences between NOR and NAND flash memory in terms of program voltage $V_{\text {PGM }}$, max channel voltage $V_{\text {Сн }}$ and channel doping concentration $N_{\mathrm{A}}$.

|  | NOR | NAND |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $V_{\text {PGM }}$ | 10 V | 20 V |  |  |
| $V_{\mathrm{CH}}$ | 5 V <br> (selected <br> cell) | 8 V <br> (inhibited <br> cell) |  |  |
| $N_{\mathrm{A}}$ | high <br> $>1 \times 10^{18}$ <br> $\mathrm{~cm}^{-3}$ | low <br> $\sim 3 \times 10^{17}$ <br> $\mathrm{~cm}^{-3}$ |  |  |
| $[4-8]$ |  |  |  | This work |



Fig. 1


Junction leakage must be suppressed $\rightarrow$ High $N_{\mathrm{A}}$ not available

Fig. 2


Fig. 3


Fig. 4


Fig. 5


Fig. 6


Fig. 7

#  

Fig. 8


Fig. 9


Fig. 10


Fig. 11


Fig. 12


Fig. 13


Fig. 14


Fig. 15


Fig. 16

