Electronically Tunable Voltage-Mode Multiphase Sinusoidal Oscillator with Low Output Impedance Nodes Employing VD-DIBAs

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Received 05 July 2022; received in revised form 15 September 2022; accepted 16 September 2022

DOI: https://doi.org/10.46604/ijeti.2022.10461

Abstract

The multiphase sinusoidal oscillator (MSO) is useful for various electrical and electronic applications. This study aims to design an MSO employing voltage differencing differential input buffered amplifiers (VD-DIBAs). The design procedure is based on cascading the first-order low-pass filter. Each phase consists of a VD-DIBA, two resistors, and a grounded capacitor. An odd-phase system without requiring an additional amplifier. The frequency is electronically controlled through the bias current without affecting the condition. The sinewave amplitudes and the phase difference between each waveform are identical. The proposed MSO is designed to obtain three-phase waveforms (n = 3). PSPICE simulation demonstrates the performance of the proposed oscillator with 0.18 μm TSMC CMOS parameters with ±0.9 V power supply. The feasibility of the proposed MSO is also verified with experiments using the VD-DIBA constructed from commercial integrated circuits (ICs) with a ±5 V power supply. The simulated and experimental results align with theoretical predictions.

Keywords: VD-DIBA, multiphase sinusoidal oscillator, voltage mode, odd-phase system

1. Introduction

Oscillator circuits are very important and are widely used in many electrical and electronic systems, such as control systems, power systems, communication systems, measurement systems, and instruments. The multiphase sinusoidal oscillator (MSO) is one important type of oscillator, which is useful for various electronic applications in communication systems, control systems, instruments, power electronics, single-sideband generators [1], etc. The MSO is designed by first-order circuits, such as an all-pass filter [2-6], a high-pass filter [7-8], and a low-pass filter [9-19]. To achieve the same magnitude and phase difference of each output sinusoidal waveform, the MSO should be designed from the same sub-circuit without an additional amplifier. Also, to adjust the frequency of the output sinusoidal waveform over the fulfilling oscillating state, the frequency of oscillation and condition of oscillation should be independently controlled by a separate element. Moreover, the frequency of the MSO should be electronically tuned for easy control by a microcomputer or microcontroller. This is the requirement of modern analog circuits.

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With the widespread utilization of active building blocks (ABB) in circuit network synthesis and design, it enables designers to create high-performance circuits with a minimal number of active components. Biolek et al. [20] introduced the concept of active building blocks for the synthesis and design of current-mode and voltage-mode circuits with the aforementioned properties. Biolek et al. [20] also proposed the voltage differencing differential input buffered amplifier (VD-DIBA) as an attractive active element. The transconductance (g_m) of VD-DIBA can be electronically controlled by adjusting the bias current. The terminals for input voltage and output current have high impedance, while the terminal for output voltage has low impedance. In addition, VD-DIBA includes a differential voltage amplifier with unity gain. This means it can be used to design voltage-mode circuits that can be electronically adjusted and do not require external voltage-difference devices. A system for processing analog signals that uses VD-DIBA as an active building block has been proposed in several different ways [20-22].

In the literature, numerous types of multiphase sinusoidal oscillators employing active building blocks have been proposed [2-5, 7-8, 10-19]. The proposed multiphase sinusoidal oscillators in [2-5] are based on the first-order all-pass (AP) filter, the high-pass (HP) filter [7-8], and the low-pass (LP) filter [10-19]. Each phase of the proposed sinusoidal oscillators in [3, 7-8, 13] requires two active elements. The control of the frequency and condition are not independently controlled [10-13, 15-17]. Some such MSOs require a floating capacitor, which is undesirable for integrated circuit implementation [3-4, 10, 12-13]. The frequency of the sinusoidal waveform obtained from the proposed MSOs in [5, 10-12, 15-17] is not electronically controllable. An additional amplifier is required in [2, 4, 11, 15]. The performance of the MSO proposed in [2-4, 7-8, 14-16, 18-19] is only validated via simulation. Table 1 presents the comparative table, which includes the advantages and disadvantages of the MSOs from the literature.

Table 1 Comparison of similar works in multiphase sinusoidal oscillator

Ref.	ABB	Number of ABB per phase	Number of R+C per phase	Design technique	Control of frequency and condition	Grounded capacitor/ Grounded resistor	Electronic control of frequency	No using additional amplifier	Supply voltage	power consumption	Cascade ability at an output node	Experiment
[2]	CCCDTA	1	1+1	AP	Independently	Yes/ No	Yes	Yes	±5 V	-	Yes	No
[3]	CDTA	2	0+1	AP	Independently	No/ No	Yes	No	±3 V	-	Yes	No
[4]	DO-VDBA	1	0+1	AP	Independently	No/ No	Yes	No	±1 V	-	Yes	No
[5]	OA	1	3+1	AP	Independently	Yes/ No	No	Yes	±12 V	-	Yes	Yes
[6]	Sinh-Domain	1	0+1	AP	Independently	Yes/ -	Yes	Yes	1.2 V	238.3 mW	Yes	No
[7]	CCCII	2	0+1	HP	Independently	Yes/ No	Yes	Yes	±2 V	-	Yes	No
[8]	OTA	2	0+1	HP	Independently	Yes/ No	Yes	Yes	±1.5 V	13.6 mW	Yes	No
[9]	S and SC cell	2	0+1	LP	Independently	Yes/ -	Yes	Yes	1.2 V	0.24 mW	Yes	No
[10]	OA	1	2+1	LP	Orthogonally	No/ No	No	Yes	±12 V	-	Yes	Yes
[11]	CCII	1	2+1	LP	Orthogonally	Yes/ Yes	No	No	±5 V	-	Yes	Yes
[12]	CFA	1	2+0	LP	Orthogonally	No/ Yes	No	Yes	±15 V	-	Yes	Yes
[13]	OA+OTA	3	1+0	LP	Orthogonally	No/ No	Yes	Yes	±1.5 V	-	Yes	Yes
[14]	CCCII	1	0+2	LP	Independently	Yes/ No	Yes	Yes	-	-	Yes	No
[15]	CBTA	1	0+1	LP	Orthogonally	Yes/ Yes	No	No	±1.5 V	-	Yes	No
[16]	FTFN	1	2+1	LP	Orthogonally	Yes/ Yes	No	Yes	±5 V	-	Yes	No
[17]	CFOA	1	2+1	LP	Orthogonally	Yes/ Yes	No	Yes	-	-	Yes	Yes
[18]	VDDDAs	1	2+1	LP	Independently	Yes/ No	Yes	Yes	±0.9 V	-	Yes	No
[19]	CBTAs	1	0+1	LP	Independently	Yes/ Yes	Yes	No	±1.5 V	-	Yes	No
This study	VD-DIBA	1	2+1	LP	Independently	Yes/ Yes	Yes	Yes	±5 V	1.44 mW	Yes	Yes

This paper proposes a VD-DIBA-based multiphase sinusoidal oscillator with low output impedance nodes. The proposed oscillator is realized by cascading the gain controllable first-order LP filter in a voltage-mode system. The proposed MSO is realized from a VD-DIBA, two resistors, and one grounded capacitor per phase. The condition and frequency of the proposed MSO are independently controlled. The proposed voltage-mode VD-DIBA low-pass filter-based MSO is verified using PSPICE simulations and experiments using commercial IC.

2. Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA) Overview

This section provides an overview of the VD-DIBA. Biolek et al. [20] proposed the fundamental principle of the VD-DIBA in 2008. The VD-DIBA contains a controllable differential transconductance amplifier and a differential voltage amplifier with unity gain. Fig. 1(a) depicts the electrical circuit symbol for the VD-DIBA. High impedance is found at the input voltage terminals, *v*+, *v*-, v, and the output current terminal, *z*. Low impedance is located at the output voltage terminal, *w*. The equivalent circuit diagram for the VD-DIBA is depicted in Fig. 1(b). The following matrix form in Eq. (1) describes the electrical behavior of the VD-DIBA.

$$\begin{bmatrix} I_{V_+} \\ I_{V_-} \\ I_z \\ I_v \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \\ V_z \\ V_v \\ I_w \end{bmatrix} \tag{1}$$

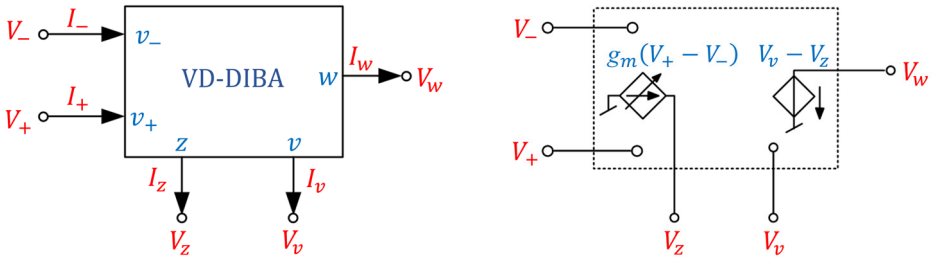
The transconductance, g_m of VD-DIBA constructed from CMOS technology and commercial ICs are as follows:

$$g_m = \sqrt{I_B(\mu_n C_{OX})(W/L)} \tag{2}$$

and

$$g_m = I_B / 2V_T \tag{3}$$

where I_B is the bias current, V_T is the thermal voltage, μ_n is the carrier mobility for MOS transistors, C_{OX} is the gate-oxide capacitance per unit area, W is the effective channel width, and L is the effective channel length.



(a) Schematic circuit symbol (b) Equivalent circuit

Fig. 1 The VD-DIBA

3. Circuit Description

In this design, the configuration of an odd-phase sinusoidal signal oscillator in voltage waveform is shown in Fig. 2. This configuration consists of the gain controllable first-order LP filter in cascading *n* stages (≥ 3 and *n* = 3, 5, 7, …). The variable *n* is the number of phases in the oscillator. The output voltage of the first LP filtering stage is fed to the input of the next LP filtering stage, and the output voltage of the last stage is fed back to the input of the first LP filtering stage. The voltages, V_{o1}, V_{o2}, …, and V_{on} are the output voltages of the first, second, and n^{th} LP filters, respectively.

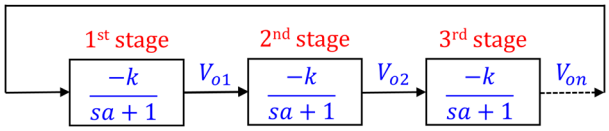


Fig. 2 Block diagram to design an odd-phase MSO using the gain controllable first-order LP filter [22]

From the structure of an odd-phase sinusoidal signal oscillator in Fig. 2, if each LP filter has identical properties, the system loop gain is given by:

$$\frac{V_{on}}{V_{in}} = \left(\frac{-k}{sa+1}\right)^n \tag{4}$$

where k is the voltage gain and $1/a$ is the pole frequency of the LP filter. Based on the Barkhausen criterion, the system loop gain is equal in absolute magnitude to one. Then, the system loop gain given in Eq. (4) becomes:

$$\left(\frac{-k}{sa+1}\right)^n = 1 \tag{5}$$

From Eq. (5), the characteristic equation of the proposed voltage-mode VD-DIBA integrator-based multiphase sinusoidal oscillator is given by:

$$(sa+1)^n + k^n = 0 \tag{6}$$

From Eq. (6), the frequency of oscillation (FO) of the proposed MSO and the condition of oscillation (CO) is given by:

$$\omega_{osc} = \frac{1}{a}\tan\left(\frac{\pi}{n}\right) \tag{7}$$

$$k \geq \sec\left(\frac{\pi}{n}\right) \tag{8}$$

Note that, according to Eqs. (7) and (8), the frequency and CO are independently adjustable. By changing the time constant of the integrator, the frequency is adjusted without effect on the condition. By changing the voltage gain of the amplifier, the condition is controlled without changing the frequency. Considering the block diagram depicted in Fig. 2, the phase difference for each output voltage waveform is given by:

$$\theta = \pi\left(\frac{n-1}{n}\right) \tag{9}$$

4. The Proposed Multiphase Sinusoidal Oscillator

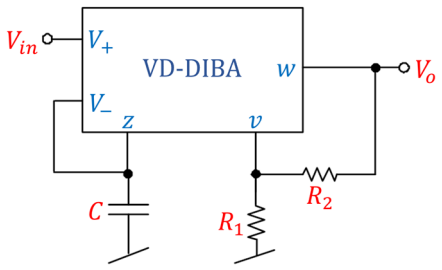


Fig. 3 The gain controllable first-order LP filter using VD-DIBA [23]

As stated above, the MSO proposed in this paper is based on the gain controllable first-order LP filter. Therefore, the gain controllable first-order LP filter employed in this design is given. Fig. 3 shows the VD-DIBA-based first-order filter [23]. It consists of one VD-DIBA, one grounded capacitor (C), and two resistors (R_1 and R_2). The input voltage node (V_{in}) has a high

impedance, while the output voltage node (V_o) has a low impedance. With this feature, it can be built as an MSO without needing voltage buffers. Using grounded capacitors is particularly advantageous for implementing ICs. The below voltage transfer function is the result of routine analysis of the gain controllable first-order voltage-mode filter shown in Fig. 3.

$$\frac{V_o}{V_{in}} = \frac{-\left(\frac{R_1}{R_2}+1\right)}{s\frac{C}{g_m}+1} \tag{10}$$

In this design, the proposed odd-phase sinusoidal signal oscillator using VD-DIBA-based gain controllable first-order LP filter is shown in Fig. 4. The proposed MSO is composed of a VD-DIBA, two resistors, and a capacitor per phase. The proposed MSO can provide an odd-phase sinusoidal waveform without an additional amplifier. From Fig. 4, if each gain controllable first-order LP filter has identical properties, the system loop gain is given by:

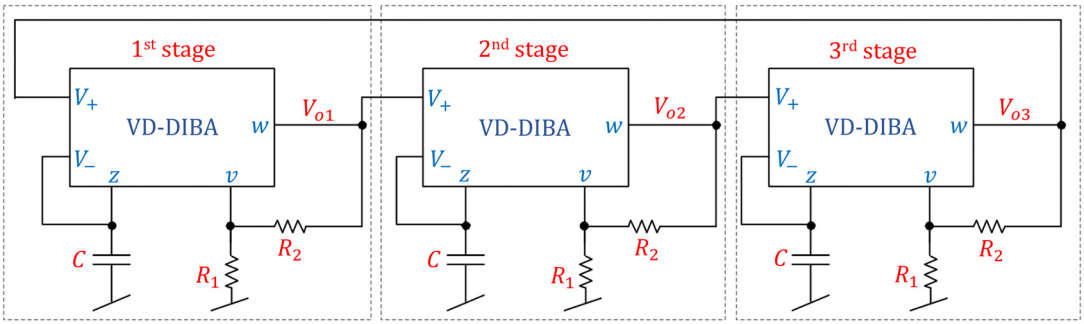


Fig. 4 The proposed electronically tunable voltage-mode MSO with low output impedance nodes

$$\frac{V_{on}}{V_{in}} = \left[\frac{-\left(\frac{R_1}{R_2}+1\right)}{s\frac{C}{g_m}+1}\right]^n \tag{11}$$

Based on the principle described above, the FO and the CO are given by:

$$\omega_{osc} = \frac{g_m}{C}\tan\left(\frac{\pi}{n}\right) \tag{12}$$

and

$$\frac{R_1}{R_2}+1 \geq \sec\left(\frac{\pi}{n}\right) \tag{13}$$

According to Eqs. (12) and (13), the frequency can be independently controlled without affecting the condition by electronically adjusting g_m, and the condition can be independently adjusted without effect on the frequency by adjusting R_1 or R_2. Thus, the proposed odd-phase sinusoidal oscillator shown in Fig. 4 provides a tuning law for the FO and CO that is completely decoupled. The electronic controllability of the sinusoidal oscillator is attractive for modern circuits using microcontrollers [24]. It is easy to construct resistor R_1 in each gain-controllable first-order LP filter from a photoresistor to stabilize the output amplitude level. This device is a component of the optocoupler with photoresistor 3WK16341 [25]. More information regarding amplitude stabilization utilizing 3WK16341 is available in [26-27]. Based on the circuit in Fig. 4, the three-phase sinusoidal oscillator is designed. The three-phase sinusoidal oscillator is used to directly produce the generator magnetomotive forces [28]. For n = 3, the FO in Eq. (12) and the CO in Eq. (13) becomes:

$$\omega_{osc} = 1.732\frac{g_m}{C} \tag{14}$$

and

$$R_1 \geq R_2 \tag{15}$$

From Eq. (9), the phase difference for each output voltage waveform is given by:

$$\theta = 120^{\circ} \tag{16}$$

5. Effect of VD-DIBA Non-Ideal Properties

This section will examine the non-ideal circuit model of VD-DIBA. The non-ideal terminal effects of VD-DIBA, including non-ideal voltage transfer errors and non-ideal parasitic elements at the input and output terminals of VD-DIBA, are investigated. The first analysis will focus on the voltage transfer errors in VD-DIBA, while the second will examine the parasitic elements in VD-DIBA. Eq. (17) gives the VD-DIBA properties with voltage transfer errors.

$$\begin{bmatrix} I_{V_+} \\ I_{V_-} \\ I_z \\ I_v \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\beta_z & \beta_v & 0 \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \\ V_z \\ V_v \\ I_w \end{bmatrix} \tag{17}$$

where β_z and β_v are the voltage transfer errors from z and v terminals to w terminal. According to Eq. (18), the non-ideal voltage transfer function of the gain controllable first-order LP filter with voltage transfer error is given by:

$$\frac{V_o^*}{V_{in}} = \frac{-1}{\beta_z\left(s\frac{C}{g_m}+1\right)}\left[\frac{R_1+R_2}{(R_1+R_2)\beta_v - R_1}\right] \tag{18}$$

From Eq. (18), for n = 3, the FO and the CO with voltage transfer error effect are given by:

$$\omega_{osc}^* = 1.732\frac{g_m}{C} \tag{19}$$

$$\frac{R_1+R_2}{(R_1+R_2)\beta_z\beta_v - \beta_z R_1} \geq 2 \tag{20}$$

As indicated by Eqs. (19) and (20), the voltage transfer errors do not affect the FO. However, these errors affect the CO.

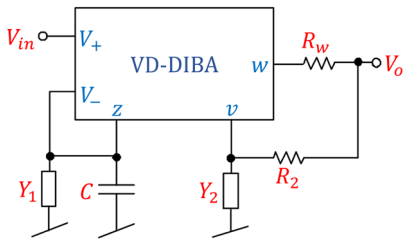


Fig. 5 Model of a non-ideal gain controllable first-order LP filter with the parasitic elements

The representation of the proposed multiphase sinusoidal oscillator with parasitic effect is depicted in Fig. 5. The admittances Y_1 and Y_2 in Fig. 5 can be defined as follows:

$$Y_1 = s(C + C_- + C_z) + G_- + G_z \tag{21}$$

$$Y_2 = sC_v + G_v + G_1 \tag{22}$$

where

$$G_{-} = 1/R_{-} \tag{23}$$

$$G_{Z} = 1/R_{z} \tag{24}$$

$$G_{V} = 1/R_{V} \tag{25}$$

$$G_{1} = 1/R_{1} \tag{26}$$

According to the circuit in Fig. 5, the non-ideal voltage transfer function of the gain controllable voltage-mode LP filter with parasitic effect is obtained by:

$$\frac{V_o^{**}}{V_{in}} = \frac{-g_m}{g_m + Y_1}\left(1 + \frac{1}{Y_2 R_2}\right) \tag{27}$$

If the operational frequency of the proposed voltage-mode VD-DIBA LP filter-based multiphase sinusoidal oscillator is less than Eq. (28), the non-ideal voltage transfer function in Eq. (27) is approximated as:

$$f_{op} \ll 1/\left\{2\pi C_V \left(R_1 // R_V\right)\right\} \tag{28}$$

$$\frac{V_o^{**}}{V_{in}} \approx \frac{-\left(1 + \frac{R_1 // R_v}{R_2}\right)}{s\left(\frac{C + C_{-} + C_z}{g_m}\right) + \frac{G_{-} + G_z}{g_m} + 1} \tag{29}$$

From Eq. (29), for $n = 3$, the FO and the CO with the parasitic effect are given by:

$$\omega_{osc}^{**} = \frac{1.732}{C + C_{-} + C_z}\left(\frac{1}{R_{-} // R_z} + g_m\right) \tag{30}$$

$$\frac{R_1 // R_v}{R_2} - \frac{2}{\left(R_{-} // R_z\right) g_m} \geq 1 \tag{31}$$

From Eqs. (30)-(31), the parasitic elements, R_{-}, R_z, C_{-}, and C_z affect the FO, while the parasitic resistances, R_v, R_{-}, and R_z affect the CO. It is also found that tuning the frequency by g_m will slightly affect the condition. Moreover, the frequency limitations at high frequencies of the proposed oscillator stem from the parasitic elements R_v and C_v. Also, the resistor, R_1 should be low to enhance the bandwidth of the proposed circuit.

6. Simulation and Experiment Results

The PSPICE program and experiments are conducted to demonstrate the performance of the proposed three-phase sinusoidal oscillator. The internal construction of VD-DIBA, shown in Fig. 6, is simulated using CMOS transistors with the level-7 TSMC 0.18 μm CMOS parameter. Table 2 displays the channel width (W) and length (L) values for MOS transistors employed in this simulation. The voltages of the power supply are set to ±0.9 V and V_B = 0.28 V. The resistors R_1 = 1.066 kΩ and R_2 = 1 kΩ, the capacitor C = 20 pF, and the bias current I_B = 50 μA (g_m = 91.77 S/V) are selected.

Table 2 The dimensions of the CMOS transistors

CMOS transistors	W (μm)/L (μm)
M_1-M_2, M_7-M_8	2.4/1.8
M_3-M_6	3.6/1.8
M_9-M_{15}	40.5/0.54
M_{16}-M_{18}	13.5/0.54

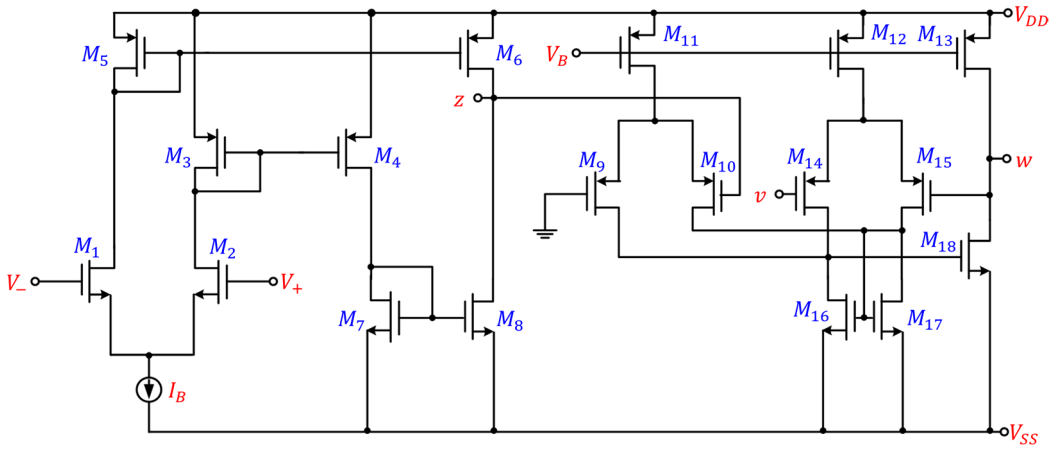


Fig. 6 The internal structure of the CMOS VD-DIBA

Fig. 7 shows the output voltage waveforms in the initial state in case n = 3. The simulated FO of the proposed voltage-mode VD-DIBA LP filter-based multiphase sinusoidal oscillator is 1.2 MHz, while the theoretically calculated frequency in Eq. (14) is 1.26 MHz. Fig. 8 shows the simulated output waveforms in the steady state. It is found that the amplitudes of the output voltages, V_{o1}, V_{o2}, and V_{o3} are 287.56 mVp-p, 287.5 mVp-p, and 287.52 mVp-p, respectively. The phase differences of the output voltages, V_{o1}-V_{o2}, V_{o2}-V_{o3}, and V_{o3}-V_{o1} are around 120°. Fig. 9 shows the simulated output spectrums of V_{o1}, V_{o2}, and V_{o3}. The total harmonic distortion (THD) values for the sinusoidal output voltage waveforms are V_{o1} = 1.08%, V_{o2} = 0.9%, and V_{o3} = 1.34%.

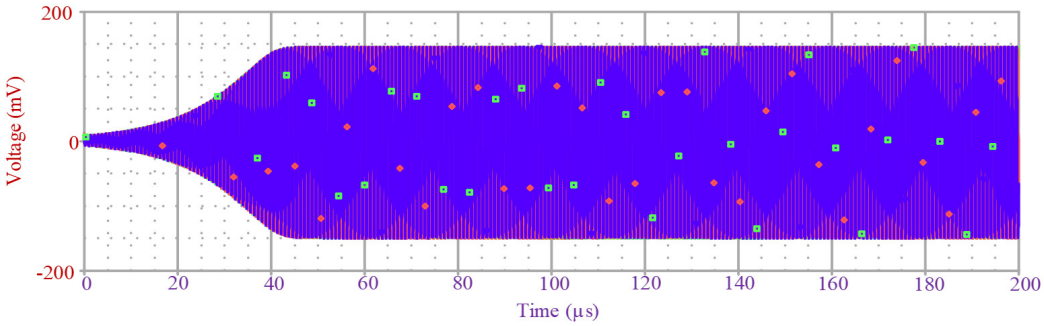


Fig. 7 The simulation of the sinusoidal output voltages at the initial state

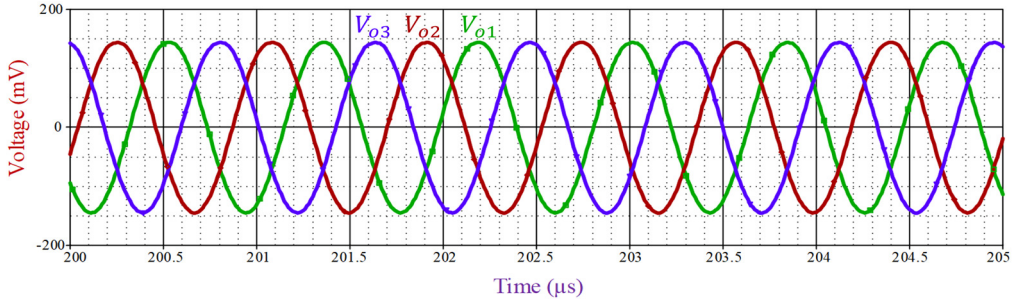


Fig. 8 The simulation of the sinusoidal output voltages at the steady state

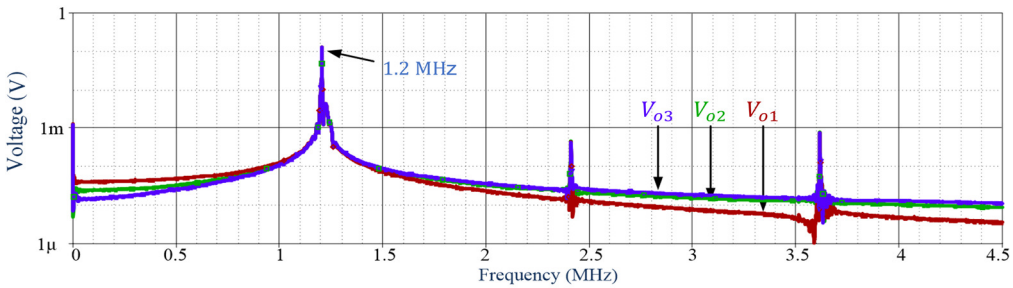
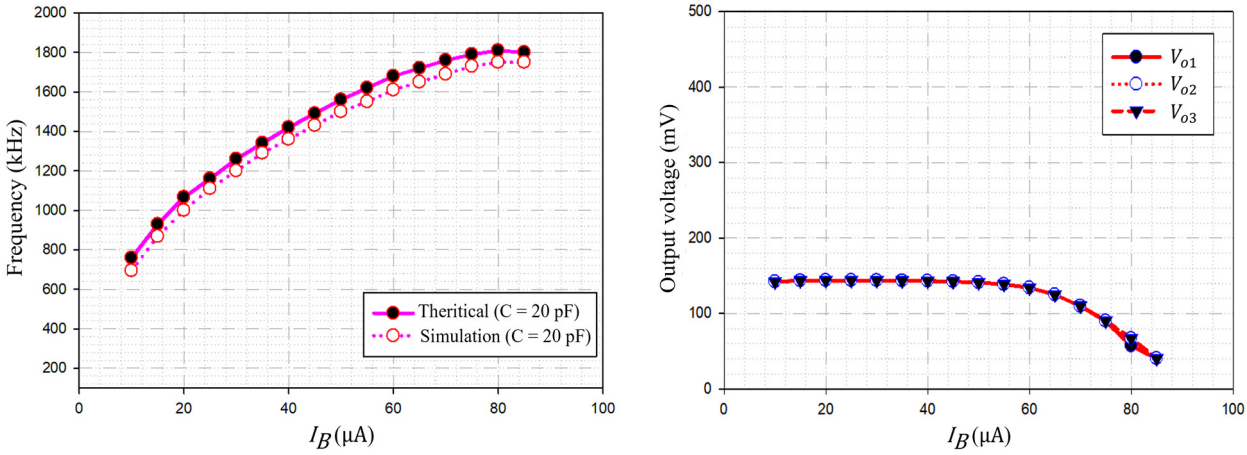


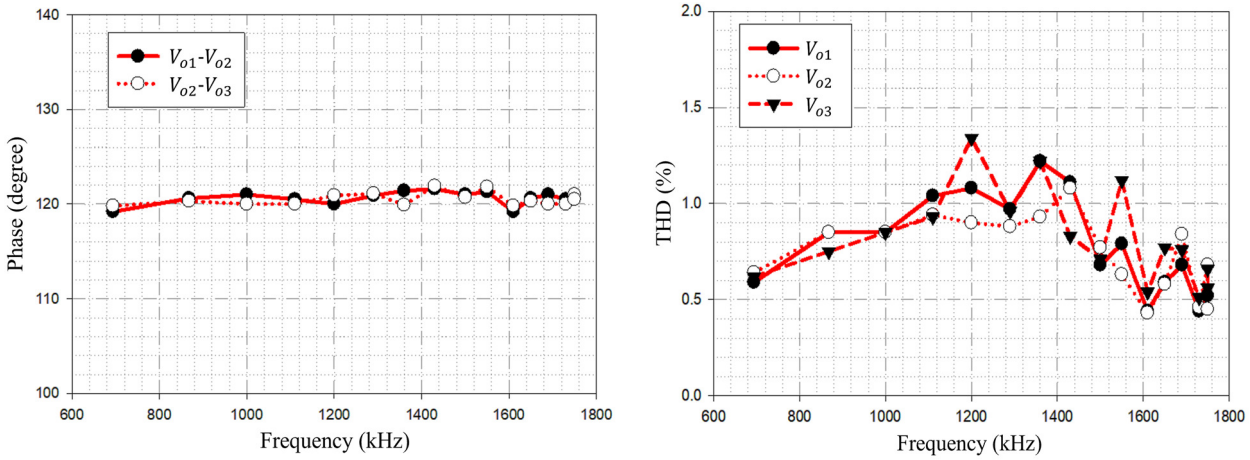
Fig. 9 The simulation of the output frequency spectrum of V_{o1}, V_{o2}, and V_{o3}

The relationship between the theoretical and simulated frequencies and the bias current, I_B, is depicted in Fig. 10(a). As demonstrated by Eq. (14), the frequency is electronically tuned. Fig. 10(b) shows a simulation of the amplitude of the sinusoidal waveforms V_{o1}, V_{o2}, and V_{o3} as the bias current is varied. Over the tuning bias current, the amplitudes of V_{o1}, V_{o2}, and V_{o3} are nearly identical.



(a) Frequency of oscillation (b) Amplitude of output voltage

Fig. 10 The frequency and amplitude of output voltage against the bias current, I_B



(a) Phase response of V_{o1}-V_{o2} and V_{o2}-V_{o3} (b) THD percentage of V_{o1}, V_{o2}, and V_{o3}

Fig. 11 The plot of the simulated phase response of the output voltages and the THD percentage

Fig. 11(a) depicts the phase response of the sinusoidal output voltage waveforms V_{o1}, V_{o2}, and V_{o3} versus the simulated frequency. The simulated phase responses are found to be approximately 120 degrees, as predicted by Eq. (16). Fig. 11(b) depicts the relationship between THD and simulated frequency. Fig. 11(b) shows that the THD percentage is less than 1.5 percent across the entire tuning frequency range. The power consumption of the proposed circuit obtained from the simulation is approximately 1.44 mW.

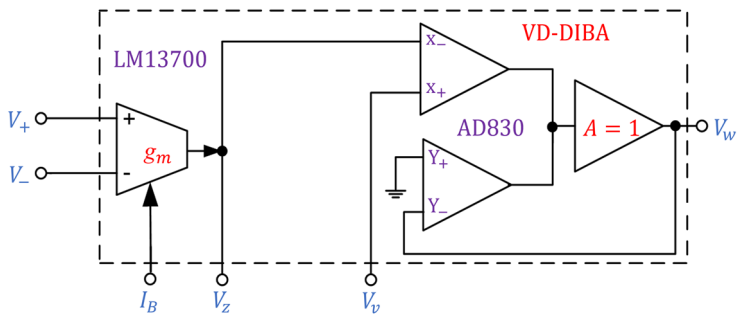


Fig. 12 The internal structure of VD-DIBA based on commercial ICs

For the experiment, two commercial ICs are used to construct the VD-DIBA, as shown in Fig. 12. It is made up of two fundamental blocks: LM13700 (Texas Instruments) for OTA [29] and AD830 (Analog Devices) for differential input voltage buffer [30]. The actual experimental setup of the proposed multiphase sinusoidal oscillator is shown in Fig. 13. The resistors R_1 = 1.01 kΩ and R_2 = 1 kΩ, the capacitor C = 1 nF, the bias current I_B = 95 μA (g_m = 1.9 mS), and the supply voltages are set to ±5 V. The measured frequency from the experiment is 504.40 kHz, which is close to the 524.01 kHz value predicted by theory (3.74% error).

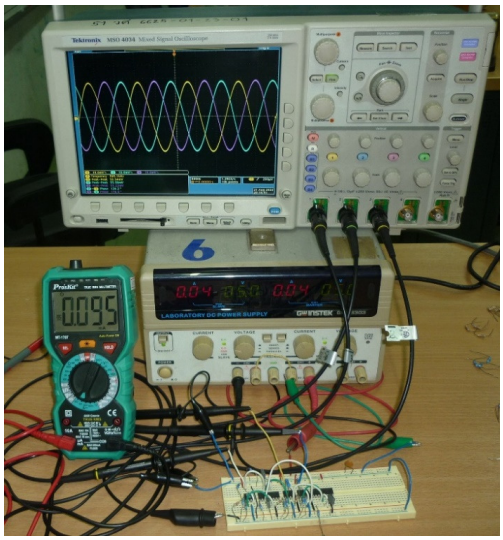
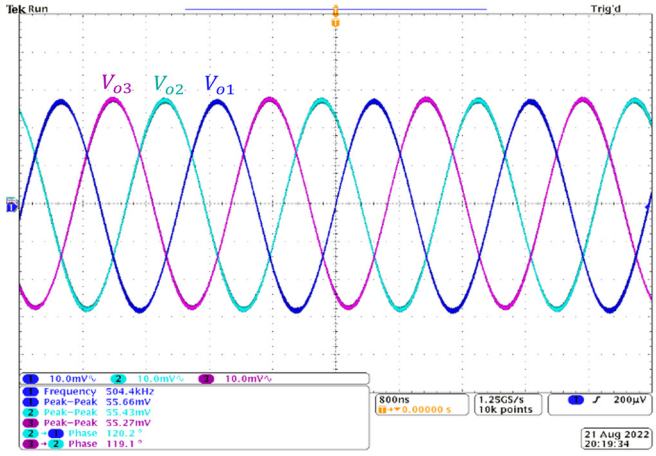
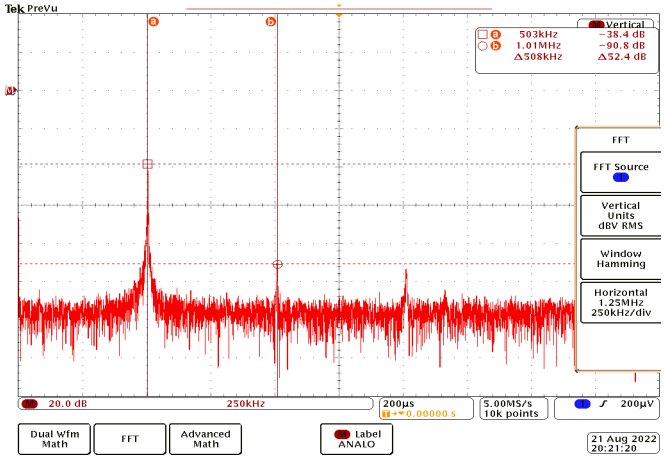


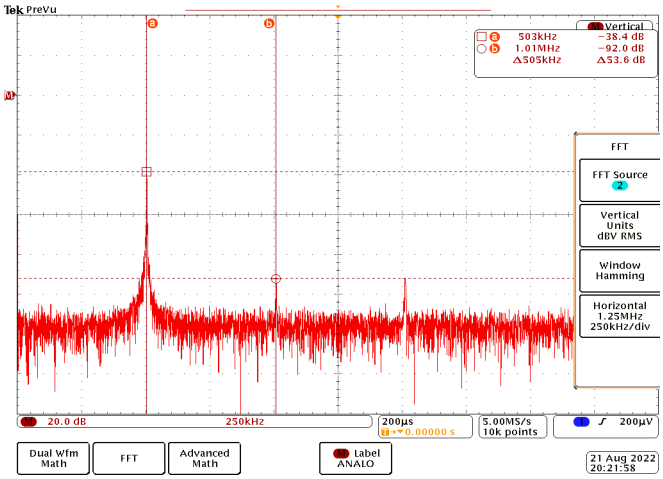
Fig. 13 Experimental setup



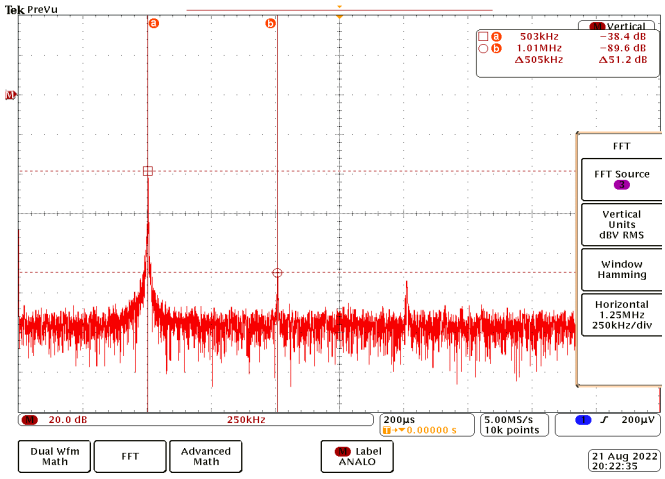
(a) Sinusoidal output waveforms of V_{o1}, V_{o2}, and V_{o3}



(b) Output frequency spectrum V_{o1}



(c) Output frequency spectrum V_{o2}

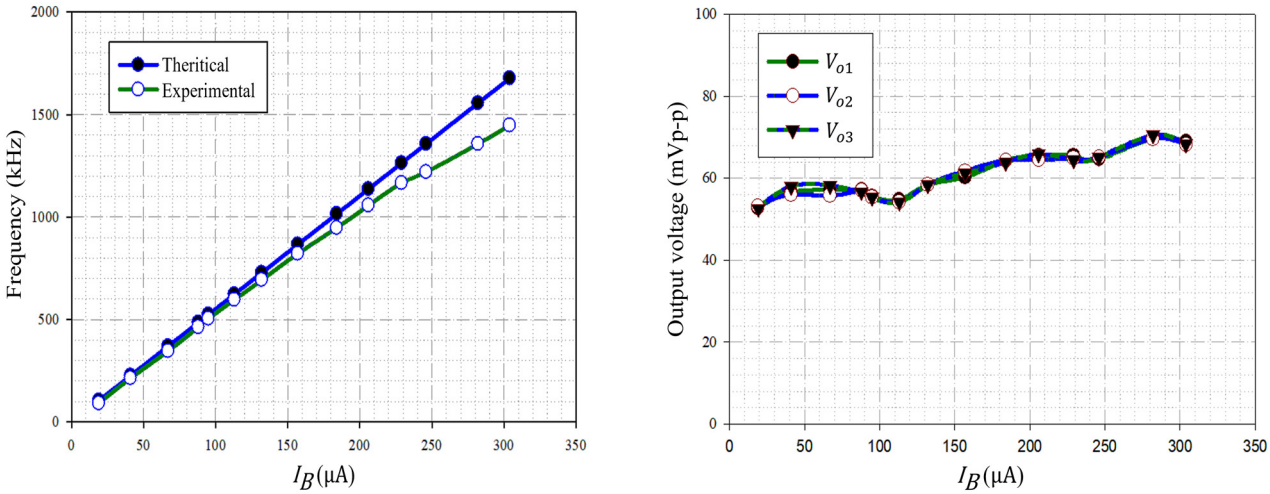


(d) Output frequency spectrum V_{o3}

Fig. 14 The measurement of the sinusoidal output waveforms and their output frequency spectrums

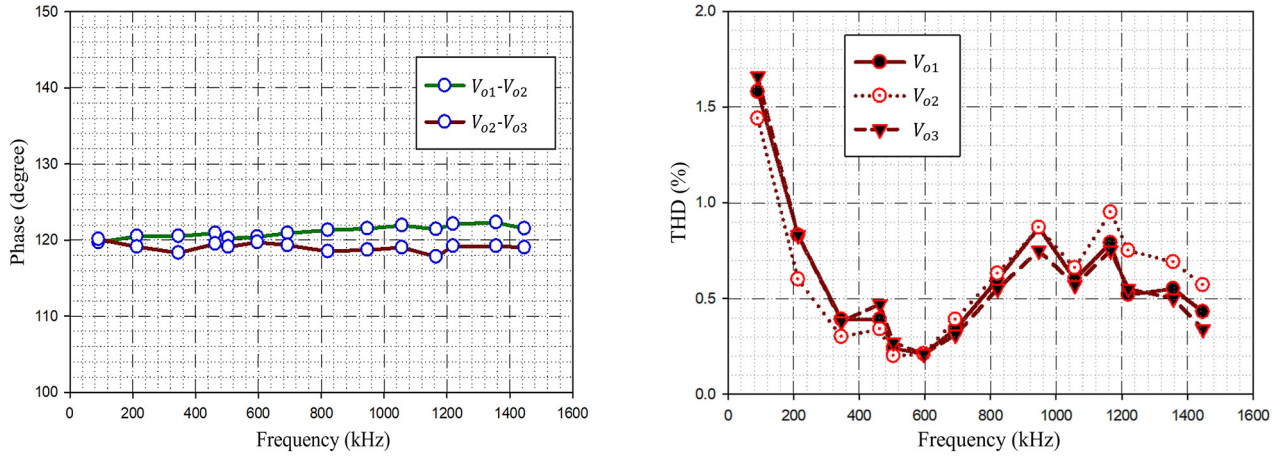
Fig. 14(a) depicts the experimental sinusoidal output voltage waveforms. The amplitudes of the sinusoidal output voltage waveforms V_{o1}, V_{o2}, and V_{o3} are 55.66 mVp-p, 55.43 mVp-p, and 55.27 mVp-p, respectively. The phase differences of the sinusoidal waveforms V_{o2}-V_{o1} and V_{o3}-V_{o2} are 120.2 degrees and 119.1 degrees, respectively, which agree well with theoretical expectations as predicted by Eq. (16). The experimental result of the frequency spectrum of the sinusoidal output waveform V_{o1} with 0.24% THD is shown in Fig. 14(b). Fig. 14(c) depicts the experimental frequency spectrum of the output waveforms V_{o2} with 0.21% THD. Fig. 14(d) shows the frequency spectrum of the output waveform V_{o3} that is experimentally tested with a THD of 0.26%. The power consumption of the proposed circuit obtained from the experiment is approximately 0.4 W.

The relationship between the theoretical and experimental frequency and the bias current, I_B, is depicted in Fig. 15(a). As demonstrated by Eq. (14), the frequency of the proposed oscillator is electronically tuned. Fig. 15(b) depicts the experimental result of varying the bias current and measuring the amplitude of the sinusoidal waveforms V_{o1}, V_{o2}, and V_{o3}. The amplitudes of V_{o1}, V_{o2}, and V_{o3} are nearly identical over the tuning bias current. Fig. 16(a) illustrates the phase response of the sinusoidal output voltage waveforms V_{o1}, V_{o2}, and V_{o3} as a function of the experimental frequency. As predicted by Eq. (16), the testing phase responses are found to be approximately 120 degrees. The relationship between THD and experimental frequency is depicted in Fig. 16(b). This result demonstrates that the THD percentage is less than 2% across the entire tuning frequency range.



(a) Frequency of oscillation (b) Amplitude of output voltage

Fig. 15 The plot of the experimental frequency and amplitude of output voltages V_{o1}, V_{o2}, and V_{o3} against the bias current, I_B



(a) Phase response (b) THD percentage

Fig. 16 The plot of the experimental phase response of the output voltages V_{o1}, V_{o2}, and V_{o3} and the THD percentage

7. Conclusions

This paper proposes a voltage-mode multiphase sinusoidal oscillator with low output impedance nodes using VD-DIBAs as the active elements. The proposed circuit comprises a VD-DIBA, two resistors, and a grounded capacitor per sinusoidal output signal. The VD-DIBA-based gain adjustable first-order LP filter is used to realize the proposed oscillator. The CO and the FO are independently adjusted. The proposed voltage-mode VD-DIBA LP filter-based multiphase sinusoidal oscillator provides odd-phase sinusoidal waveforms without using an additional amplifier. The output voltage nodes have a low impedance. With this feature, it can be built as an MSO without needing voltage buffers. The use of grounded capacitors is particularly advantageous for implementing ICs. The proposed MSO is investigated using PSPICE simulations based on TSMC 0.18 μm CMOS parameters and experiments using commercial ICs (LM13700 and AD830).

Conflicts of Interest

The authors declare no conflict of interest.

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