An analogue building block for signal conditioning instrumentation circuits

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Abstract: The design of analogue signal conditioning circuits for instrumentation applications often requires designing a specific circuit for each case. For board-level design solutions, these circuits are generally implemented by using operational amplifiers (OA) and instrumentation amplifiers (IA). An analogue building block (ABB) is proposed, which can be implemented with three standard OAs. Using different connection schemes and just adding a few resistors, it allows implementing several analogue circuits such as common-mode conditioners, single-ended to differential and differential to single-ended converters, voltage and current amplifiers, current to voltage and voltage to current converters, among others. The proposed ABB is analysed and applied to several typical analogue conditioning problems. The design equations and experimental results for these circuits are presented.

Keywords: analogue building blocks; ABBs; common-mode processing; signal conditioning; differential-mode processing; board level design.

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1 Introduction

Many analogue tasks have moved to the digital domain, but front-ends design and signal conditioning circuits for analogue to digital converter (ADC) inputs remain in the analogue universe. Current ADCs require excellent interfaces and conditioning circuits to be provided with high-quality signals in accordance with their huge dynamic range. So, the tasks to be performed by analogue circuits are few but must be done really well.

Frequent analogue processing functions are common-mode (CM) and differential-mode conditioning (Spinelli et al., 2009, 2012), terminal matching involving single-ended to differential and differential to single-ended conversions (Baert, 1999; Casas et al., 2006; Spinelli et al., 2020), current to voltage and voltage to current converters, voltage, and current amplification (Pallás-Areny and Webster, 1999), among others. They are usually implemented with operational amplifiers and instrumentation amplifiers, designing each circuit as a new one. This process does not have a well-established structure as can be seen in digital hardware design. Sometimes the path through which the designer arrives to a solution is unclear even to him/herself. Perhaps this is why analogue design is sometimes referred to as an 'art', and we analogue engineers love this.

There are many analogue building blocks (ABB) for integrated circuits design, such as differential difference amplifiers (Mahmoud and Soliman, 1998; Sackinger and Guggenbuhl, 1987), current conveyors (Awad and Soliman, 1999; Smith and Sedra, 1968), differential difference current conveyors (Pandey and Paul, 2011) and fully differential difference amplifiers (Matthus et al., 2020; Duque-Carrillo et al., 1995). These circuits are available for integrated circuits designers to implement complex analogue processing function by interconnecting them, thus encapsulating part of the complexity – and problems – inside each building block. This is not the case of board-level design, which is intended to specific problems with production volumes that do not justify manufacturing a custom integrated circuit.

Analogue application circuit designers must work with commercially available integrated circuits such as operational amplifiers, instrumentation amplifiers and fully differential amplifiers that only support the inverting topology (Karki, 2002), but have a very good variety of these devices to select the appropriate ones for each problem to be solved.

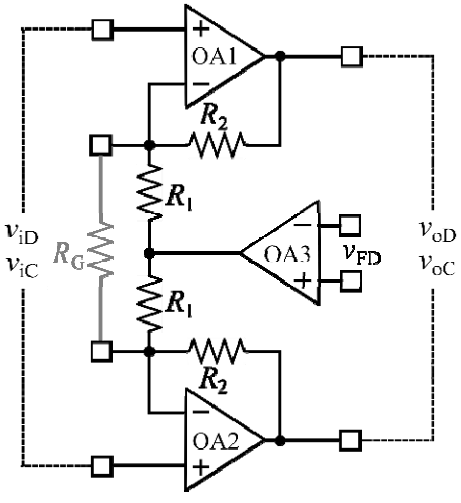
Analogue instrumentation circuits are towards fully differential solutions, because they are suitable for working from a single supply voltage, have a higher dynamic range than their single-ended counterparts, and provide a simple way to interact with current high-resolution ADCs that have differential inputs. There are not many commercial devices to implement this kind of circuits, which must be implemented by general purposes devices and could lead to stability problems (Hurst and Lewis, 1995; Spinelli et al., 2006).

This work proposes an ABB that can be easily implemented with standard operational amplifiers. It allows implementing and ensures the stability of usual instrumentation circuits to process CM and differential-mode signals, and also perform conversions between them. The ABB implementation only requires four operational amplifiers, thus reducing the variety of components in a design and its reliance on the provision of very specific devices.

2 Proposed ABB

The proposed ABB is shown in Figure 1. It has a differential input that can be used as single-ended grounding one input terminal, and a differential output that, as it will be shown later, can also work as single-ended. These features allow implementing fully-differential, single-ended, single-ended to differential and differential to single-ended circuits.

Figure 1 Proposed ABB



Note: It has a differential input, a differential output and an extra differential input that only works on the CM output voltage.

The circuit is composed by a fully differential amplifier (OA1, OA2) with an additional OA (OA3) that works exclusively on the CM output voltage v_{oC}. The gain G_D for differential mode (DM) voltages is given by:

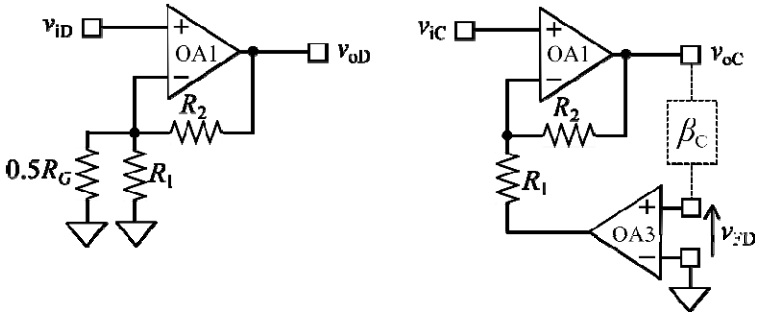
$$G_D = 1 + R_2\left(\frac{2}{R_G} + \frac{1}{R_1}\right) \tag{1}$$

whereas the CM output voltage v_{oC} can be modified by designing the feedback to the differential input voltage v_{FD} of OA3. Then, the DM output voltage v_{oD} is always $v_{oD} = G_D v_{iD}$, but v_{oC} results from the condition $v_{FD} = 0$ and, choosing an appropriate feedback scheme, v_{oD} can be established anywhere like a floating voltage source. This feature allows implementing many of the typical functions used in analogue conditioning stages. Given that the proposed ABB is intended for board-level design, it allows selecting the appropriate OAs for each case, such as low-noise, low-bias current or low-offset voltage requirements.

2.1 Stability issues

Since the circuit works by injecting a feedback voltage to the input of OA3 its stability must be analysed. Even though the ABB can be used for single-ended signals, its structure is fully differential. Therefore, its stability must be analysed for both differential and CM signals (Middlebrook, 1963; Witherspoon and Choma, 1995; Hurst and Lewis, 1995). Figure 2(a) shows the equivalent circuit for differential-mode signals and Figure 2(b) for CM ones.

Figure 2 (a) Differential and (b) CM equivalent circuits



(a) (b)

For differential-mode voltages the circuit works as a standard non-inverter amplifier, its closed-loop gain G_D is given by equation (1) and its open-loop gain $\beta A_{DM}(s)$ by:

$$\beta A_{DM}(s) = A_1(s) / G_D, \tag{2}$$

where $A_1(s)$ is the open-loop gain of OA1. The DM circuit does not present stability problems if unity-gain stable operational amplifiers OA1, OA2 are used, but instability could arise for CM voltages, because the open loop gain $A_3(s)$ of OA3 is increased R_2/R_1 times by the inverter amplifier OA1, which also adds some phase. The open-loop gain for CM signals βA_{CM} also depends on the CM feedback β_C which must be designed for each application, but the worst case corresponds to a unity gain CM feedback $\beta_C = 1$ in the circuit of Figure 2(b). One strategy to ensure stability is to set $R_2/R_1 = 1$ and select an OA with a gain bandwidth product (GBP) much lower than that of OA1 for OA3 ($GBP_1 >> GBP_3$). In this way, the open loop gain 0 dB cross is defined exclusively by $A_3(s)$ thus resulting in a stable circuit. This solution is proposed and analysed in detail in Spinelli et al. (2020) for a single-ended to DM converter. Then, adopting $R_1 = R_2 = R$ results in:

$$G_D = 2\left(1+\frac{R}{R_G}\right), \tag{3}$$

and the open-loop gain for CM voltages βA_{CM} can be approximated as:

$$\beta A_{CM}(s) \approx A_3(s) \text{ for } \mathrm{R}_1 = R_2, GBP_1 >> GBP_3 \text{ and } \beta_C = 1 \tag{4}$$

In this condition, using a stable OA3 with unity gain, a stable circuit is obtained within which two dynamics coexist. For DM voltages its dynamics corresponds to that of a

non-inverting amplifier with a G_D gain implemented with OA1 and, for CM signals, its behaviour looks like that of OA3 when working with unity gain feedback.

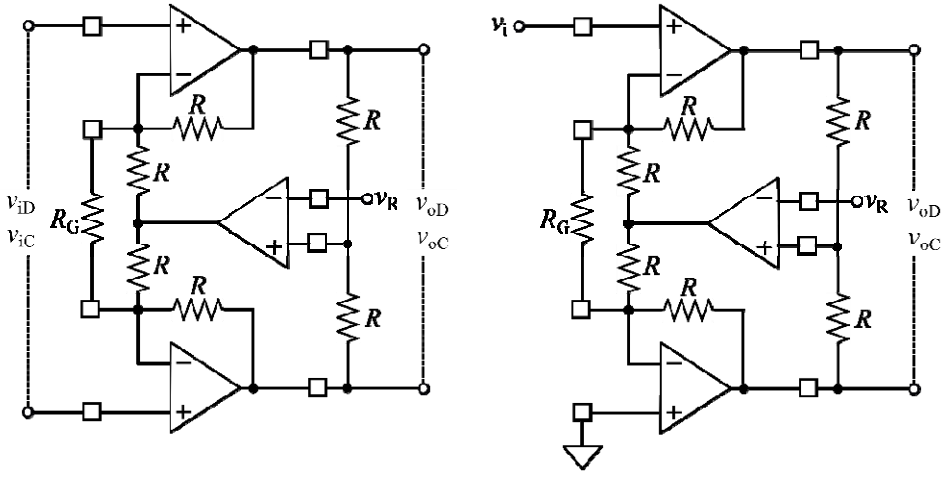
Circuit stability can be affected by the OA3 input capacitance C_{IN} if the output resistance $R_{\beta C}$ of the feedback network β_C is not low enough, because it introduces a pole at $f_P = -(2\pi R_{\beta C} C_{IN})^{-1}$. However, considering C_{IN} values of a few pF and $R_{\beta C}$ of a few kΩ, the pole C_{IN} introduces is of the order of tens of MHz and does not jeopardise stability.

3 Application circuits

3.1 CM conditioner

Today high-resolution ADCs present differential inputs. In order to take advantage of their full input range, an appropriate CM input voltage must be set, typically half of the power supply or reference voltage. The circuits in Figure 3 allow setting the output CM voltage to a desired potential v_R; the circuit of Figure 3(a) for differential input voltages and the circuit of Figure 3(b) for a single-ended input. This latter was published previously in Spinelli et al. (2020). Note that, being a fully differential scheme, accepting single-ended or differential input voltages is easily solved by grounding an input pin.

Figure 3 Both circuits set an output CM voltage $v_{oC} = v_R$, (a) for differential input voltages (b) for single-ended ones



Note: This later also performs a single-ended to differential transformation.

The circuit in Figure 3(a) verifies:

$$v_{oD} = G_D v_{iD}; v_{oC} = v_R, \tag{5}$$

an its single-ended input counterpart of Figure 3(b):

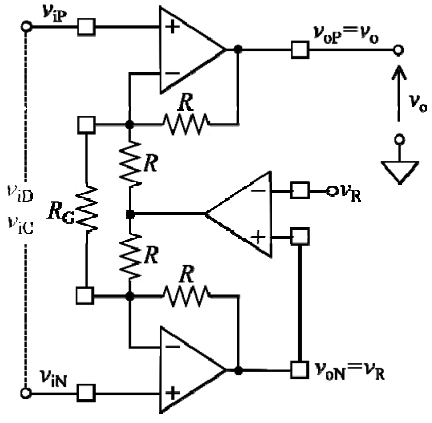
$$v_{oD} = G_D v_i ; v_{oC} = v_R . \tag{6}$$

Both circuits can be also implemented with commercially available fully differential OAs (Karki, 2002; Spinelli et al., 2020). These devices allow amplifying differential signals and establishing a desired CM output voltage $v_{oC} = v_R$, but they only admit the inverter topology that has low input impedance. The proposed circuit provides high input impedance as instrumentation applications usually demand and can be implemented with the proposed ABB by just adding two resistors.

3.2 Differential to single-ended converter

The circuit of Figure 3(b) works as a single-ended to differential converter, but the ABB can also be used for converting differentials voltages to single-ended by using the scheme of Figure 4.

Figure 4 A differential to single-ended converter



The output voltage v_o is given by:

$$v_o = G_D v_{iD} + v_R , \tag{7}$$

which shows that this circuit works like an instrumentation amplifier (Pallás-Areny and Webster, 1999). The input v_R could be set to ground potential or at half of the power-supply voltage for single-supply circuits. Its *CMRR*, in the worst case, is given by (Appendix A):

$$CMRR \approx\sim G_D / 4t, \tag{8}$$

where t is the resistors' tolerance. This *CMRR* is like that of the standard difference amplifier (Pallás-Areny and Webster, 1991), but the circuit of Figure 4 provides high input impedance for its inputs v_{iP}, v_{iN}, v_R, and can be built with the proposed ABB. As occurs in the standard three OA instrumentation amplifier, the input-referenced offset voltage v_{os} of the circuit depends on the imbalance between the offset voltages v_{oS1}, v_{oS2} of OA1 and OA2 as:

$$v_{os} = v_{os1} - v_{os2} \tag{9}$$

3.3 Voltage to current converters

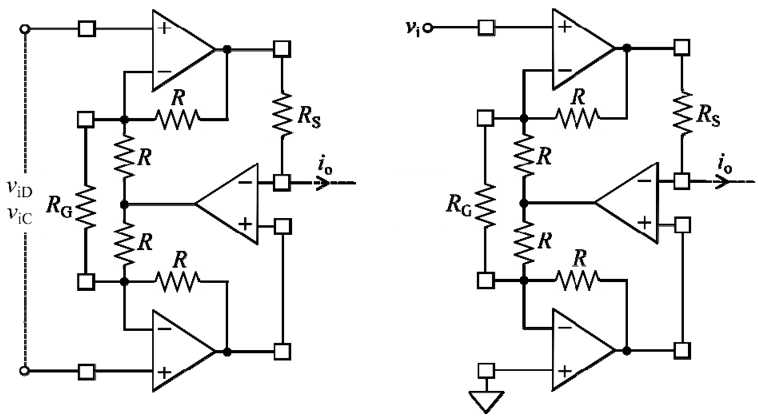
The proposed ABB allows implementing current sources by using the scheme shown in Figure 5. Note that the differential output voltage $v_{oD} = G_D v_{iD}$ appears directly on R_S, thus imposing an output current i_o given by:

$$i_o = G_D v_{iD} / R_S \tag{10}$$

This equation corresponds to a differential input. The circuit also admits a single-ended input by grounding one of its terminals [Figure 5(b)], thus equation (10) becomes:

$$i_o = G_D v_i / R_S \tag{11}$$

Figure 5 Voltage to current converter for a (a) differential or (b) single-ended input



(a) (b)

As shown in Appendix B, the output impedance of this current source depends on the resistors' tolerance t and is given by:

$$R_o \approx\sim R_S / 4t \tag{12}$$

This expression matches that of the well-known Howland current source (Yazdanian et al., 2013; Mahnam et al., 2016) but the circuit in Figure 5 presents high input impedances and can be built with the ABB.

3.4 Current to voltage converter

It is possible to implement current to voltage converters with balanced differential output using the scheme of Figure 6. It can be used for floating [Figure 6(a)] or grounded input current sources [Figure 6(b)]. A single-ended output can be provided by combining this scheme with the output feedback from the circuit in Figure 4.

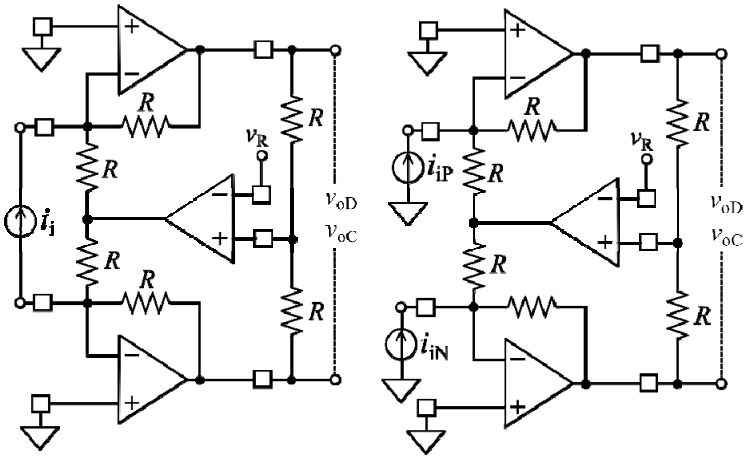
In the case of a floating input current i_i, it flows through the resistors R imposing the differential output $v_{oD} = i_i 2R$ whereas the CM output voltage is set by the feedback at v_R verifying:

$$v_{oD} = i_i 2R; \; v_{oC} = v_R. \tag{13}$$

When grounded i_{iP}, i_{iN} current sources are applied at the inputs the differential and CM voltages v_{oD}, v_{oC} are given by:

$$v_{oD} = (i_{iP} - i_{iN})\,R;\; v_{oC} = v_R \tag{14}$$

Figure 6 Current to voltage converters for (a) floating current sources and (b) for grounded ones



(a) (b)

In this circuit, the bias currents i_{BIAS1}, i_{BIAS2} of OA1, OA2 directly affects the output, because their effects do not differ from those of the input current. Considering this OA parameter, the output voltage results:

$$v_{oD} = (i_{iP} - i_{iN} + i_{BIAS1} - i_{BIAS2})\,R;\; v_{oC} = v_R. \tag{14}$$

Then, to reduce the error produced by the bias currents, low bias current (i.e., CMOS or JFET) operational amplifiers should be used.

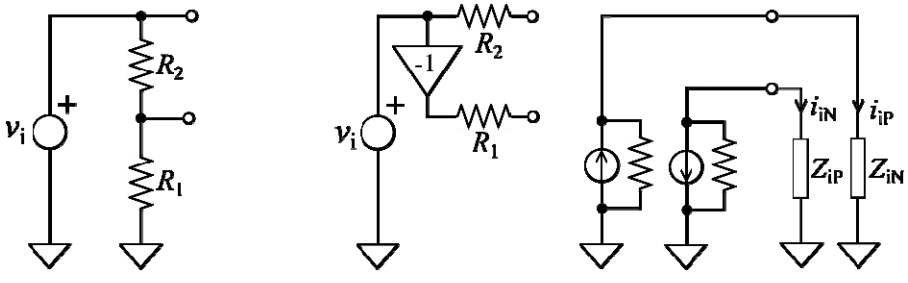
A current amplifier can also be implemented by blending the circuits of Figure 5 and Figure 6, resulting in a circuit that admits grounded or floating input currents as that of Figure 6, and provides a current mode output as the circuit in Figure 5 does.

4 Experimental results

The circuits proposed in the previous sections were built and their design equations experimentally verified. The ABB was implemented with 1% resistors R = 4.7 kΩ and general-purpose operational amplifiers TL072 for OA1, OA2 and OP07 or LF444 for OA3. All these devices from Texas Instruments™ and powered by a symmetrical power supply of ±12 V. Figure 7 shows the voltage and current sources used in the tests to produce both CM and differential-mode signals. The current sources were implemented by using the scheme of Figure 7(b). Their values are $i_{iP} \approx v_i / R_2$ and $i_{iN} \approx -v_i / R_1$ when they flow on low input impedances that verify Z_{iP}, $Z_{iP} << R_1$, R_2. The input signals v_i were generated and the output voltages acquired by a Owon™ VDS6102 digital oscilloscope.

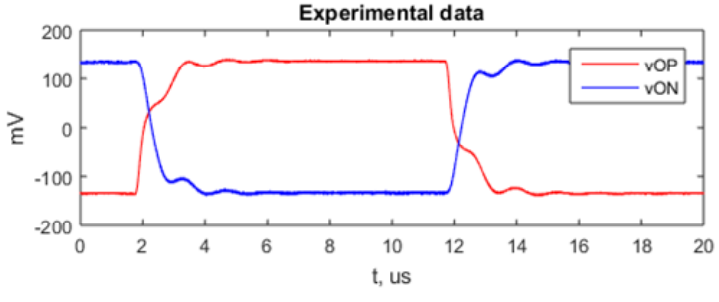
Experimental data, circuits and simulations results are available for the reader as 'supplementary files'.

Figure 7 (a) Voltage and (b) current input sources used in the tests

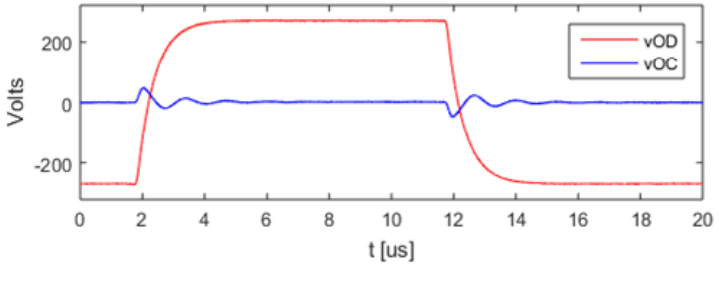


(a) (b)

Figure 8 (a) Experimentally obtained voltages at output nodes v_{oP}, v_{oN} of the circuit of Figure 3 for v_{iD} = 50 mV$_{PP}$, v_{iC} = 25 mV$_{PP}$, G_D = 11.4 (b) Transient responses of CM and DM where the very different dynamics of DM and CM can be clearly appreciated (see online version for colours)



(a)



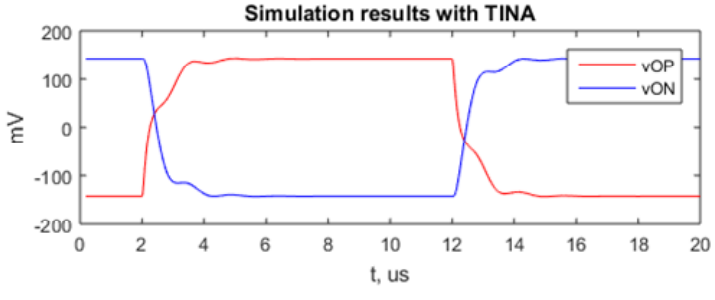
(b)

4.1 CM conditioner

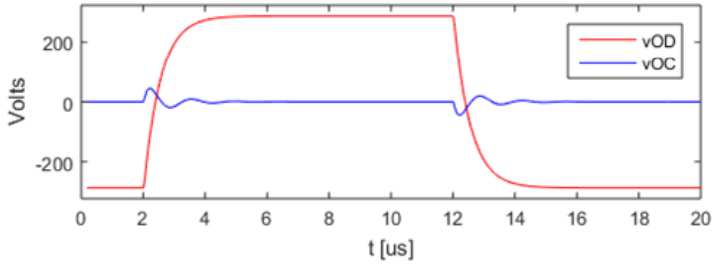
The circuit of Figure 3 was built adopting R = 4.7 kΩ, R_G = 1 kΩ, OA1-2: TL072, OA3:OP07 and v_R = 0, thus setting a gain G_D = 11.4 times. A square wave signal v_i = 50 mV_{PP}, 50 kHz was used with the circuit in Figure 7(a) (R_1 = 0, R_2 = 1 kΩ) to produce an input signal with both common and DM components v_{iD} = 50 mV_{PP}, v_{iC} = 25 mV_{PP} that was applied to the circuit in Figure 3. The upper curves in Figure 8 show the output voltages v_{oP} and v_{oN}, whereas the lower graph corresponds to the CM v_{oC} and differential-mode v_{oD} output voltages. These latter curves show the very different dynamics the circuit presents for CM and differential-mode signals. It also shows a differential-mode gain $G_D \approx 11.4$ times and a good CMRR for low frequencies.

The same test was reproduced by simulation with TINA of Texas Instruments. The results, shown in Figure 9, present a good agreement with the experimental data. In the simulations, the OP07 macro model was slightly modified for a better match with the transient response curves in its datasheet. The model default parameters C1 = 2.9 pF, C2 = 30 pF were changed to C1 = 10 pF and C2 = 20 pF.

Figure 9 Simulation results, (a) voltages at output nodes v_{oP}, v_{oN} of the circuit of Figure 3 for v_{iD} = 50 mV_{PP}, v_{iC} = 25 mV_{PP}, G_D = 11.4 (b) CM and differential-mode transient responses (see online version for colours)



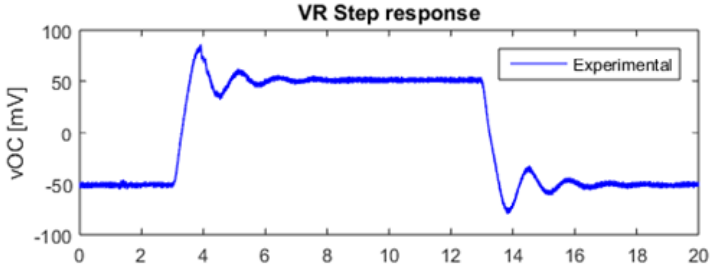
(a)



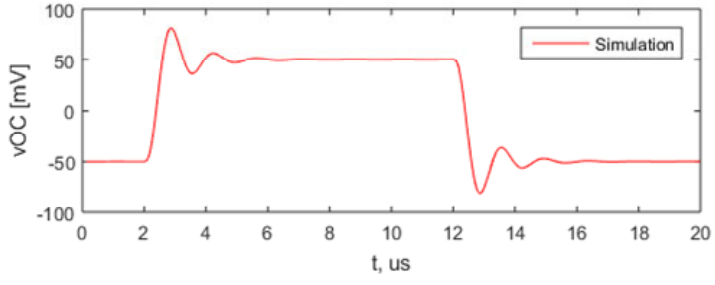
(b)

A second test were carried out with null input v_{iD} = v_{iC} = 0 but applying a 100 mV_{PP}, 50 kHz square wave at the input v_R that exclusively affects the CM output voltage ($v_{oP} \equiv v_{oN}$) which is shown in Figure 10. The upper graph corresponds to the experimentally obtained response and the lower graph to simulation results.

Figure 10 CM output voltage of the circuit in Figure 3 when a square wave 100 mV_{PP}, 50 kHz is applied at v_R, (a) experimental data (b) simulation results (see online version for colours)



(a)



(b)

4.2 Differential to single-ended converter

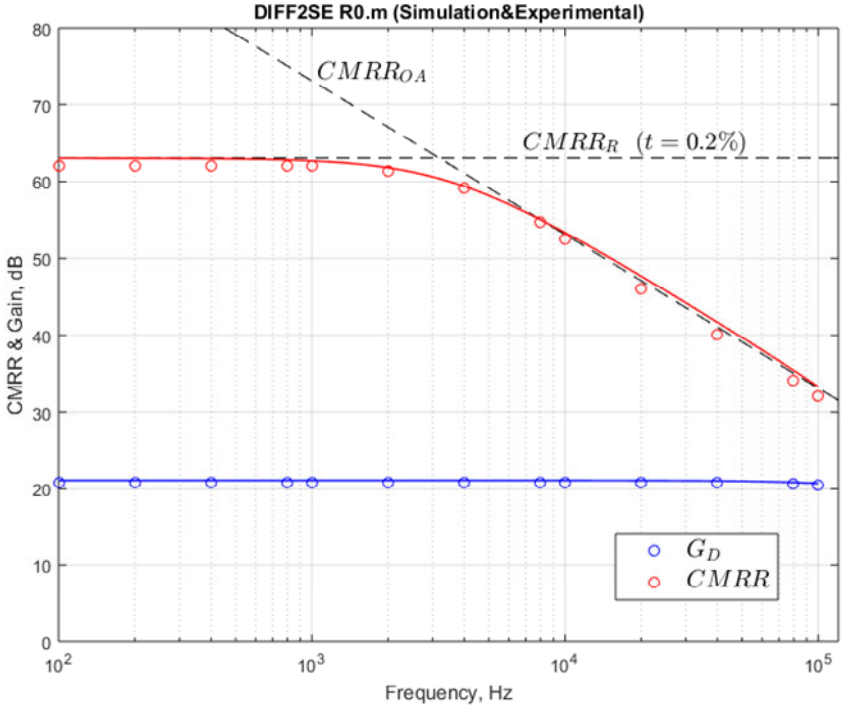
An instrumentation amplifier with a gain G_D = 11.4 times (21 dB) was implemented with the circuit in Figure 4 with R = 4.7 kΩ, R_G = 1 kΩ, OA1-2:TL072, OA3:OP07 and v_R = 2.5 V. Its differential-mode gain and CMRR was measured resulting in the curves shown in Figure 11 where can be seen a gain G_D = 11.4 (21 dB) up to 100 kHz and a CMRR of 62 dB for low frequencies, which corresponds by equation (22) to a resistors' tolerance of 0.2%. Although their nominal tolerance is 1%, fortunately, the matching between them is significantly better. Figure 11 shows in dashed lines the CMRR bounds: $CMRR_R$ corresponding to resistors' mismatching and $CMRR_{OA}$ to the operational amplifier open loop gain. This latter was plotted considering for the OP07 a dc open loop gain of 118 dB and dominant pole at 1 Hz. In the same figure is also indicated the simulation results obtained with TINA.

4.3 Current to voltage converter

The circuit in Figure 6 was built adopting, OA1-2:TL072, OA3:LF444, R = 4.7 kΩ, v_R = 0 and tested using the scheme in Figure 7(b). The OP07 was replaced by a LF444 for a better slew rate (1 V/μs). A sinusoidal signal v_i = 1.9 V_{PP}, f = 200 kHz was applied to the circuit in Figure 7(b) with R_1 = R_2 = 10 kΩ to produce a differential current input i_{iD} = i_{iP} – i_{iN} = 190 μA_{PP} resulting in the output voltages v_{OP}, v_{ON} shown in the upper traces of Figure 12 and a differential-mode output v_{OD} = 1.8 V_{PP}. This value agrees with

that given by equation (12). A second test was made with a single-ended input current i_{iP} = 190 μA$_{PP}$, i_{iN} = 0 obtaining the voltages shown in the lower traces. The amplitude reduces a half as expected by equation (13) and the phase between v_{OP} and v_{ON} are not 180° as when a differential input current was applied. This is because at 200 kHz the OA3 open-loop gain is not enough to provide a balanced output. Note that for the same frequency the circuit works well for a differential input, thus showing the advantages to work with balanced signals and circuits.

Figure 11 Differential-mode gain G_D (in blue) and *CMRR* of the built circuit (in red) (see online version for colours)

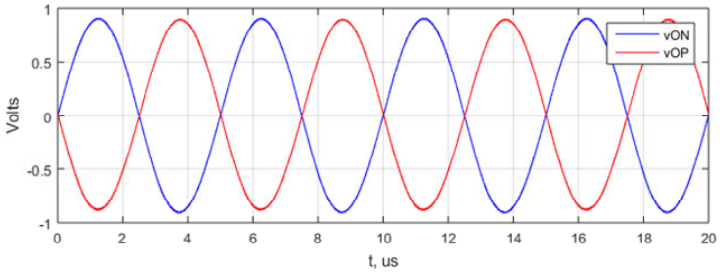


Notes: Experimental data are indicated with markers and simulation results in solid line. The dashed lines show the CMRR bounds corresponding to resistors mismatches and to OA3 (OP07) open-loop gain.

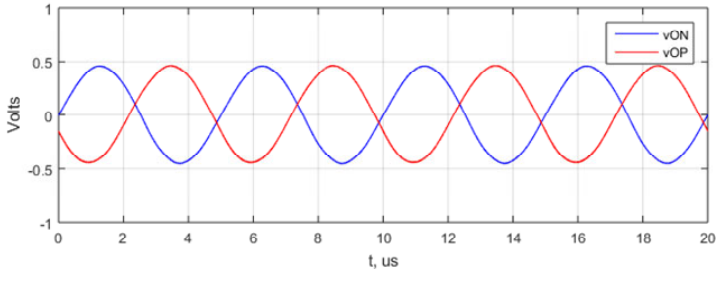
4.4 Current source

A dc current source I_0 was implemented with the circuit in Figure 5(b) using OA1-2:TL072, OA3:LF444 and R = 4.7 kΩ. The resistor R_G was omitted and v_i = 0.38 V, R_S = 2 kΩ was adopted to set I_0 = 380 μA according to equation (10). Figure 13 shows the variation of the output current I_0 as function of the output voltage V_0 obtained using different resistive loads. This curve fits with a line of slope +4.2 μA/V, which corresponds to an output impedance R_0 = 238 kΩ. This value agrees with that predicted by equation (11) for a resistor tolerance of 0.2%.

Figure 12 Current to voltage converter test, (a) traces correspond to a differential input current $i_{iP} = -i_{iN} = 190\ \mu A_{PP}$ (b) to a single-ended input current $i_{iP} = 190\ \mu A_{PP}$, $i_{iN} = 0$ (see online version for colours)

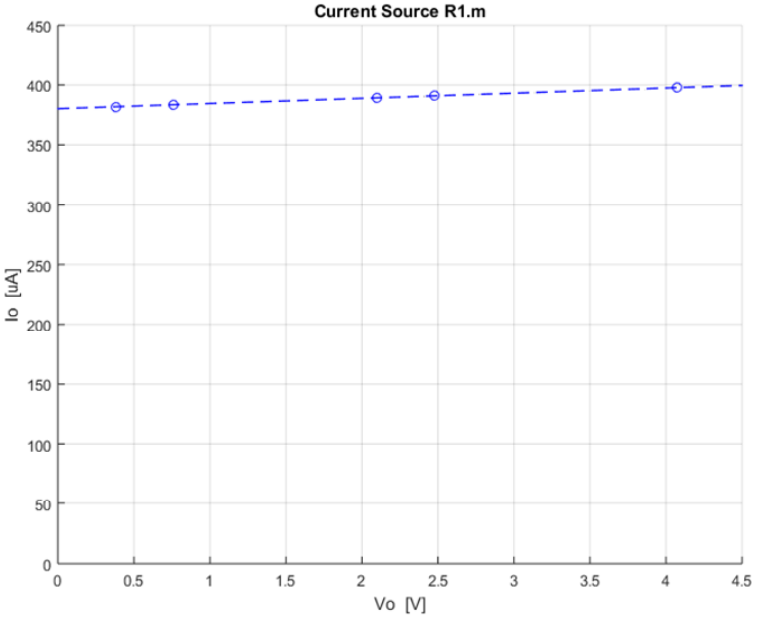


(a)



(b)

Figure 13 Output current I_0 as function of the voltage V_0 on the load (see online version for colours)



5 Conclusions

The proposed ABB allows designing and implementing many types of conditioning circuits within a structured framework. Circuits such as CM conditioner, single-ended to differential and differential to single-ended converters, voltage, current, transconductance and transimpedance amplifiers with both differential or single-ended output and differential or single-ended inputs can be built by just adding 3 or less external resistors. In general, the performance of the solutions it provides is similar to that of typical and well-known custom-made solutions, but they can be built with general purpose devices and inside a framework that ensures stability. It also leads to avoid dependency on very specific integrated circuits and manufacturers. Moreover, thinking in a final product, a reduced variety of components is desirable.

Several application circuits were designed, simulated, built, and experimentally tested. The results obtained show a very good agreement between them, which can be assumed as a validation of the proposed ABB and its design equations.

The AAB is intended for fully differential circuits but can be also used for single-ended topologies and mode transformations. Some circuits exhibit different responses for CM and differential-mode signals, which is useful for teaching analogue signal processing.

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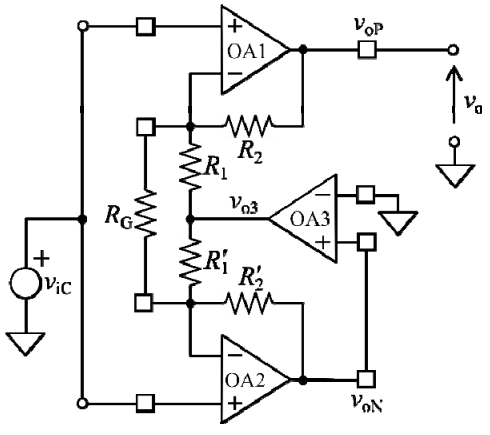
Appendix A

A.1 CMRR of the differential to single-ended converter

To evaluate the *CMRR* of the circuit in Figure 6, a CM voltage v_{iC} must be applied as Figure 14 shows. In this condition, the output voltage is given by $v_o = G_{DC}v_{iC}$, where G_{DC} is the CM to differential cross-gain that allows to calculate the $CMRR = G_D/G_{DC}$ (Pallás-Areny and Webster, 1999).

Figure 14 Differential to single-ended converter considering resistors' imbalances and a CM input voltage v_{iC}



A.1.1 CMRR due to resistors imbalance

The non-inverting inputs of OA1, OA2 are both at the potential v_{iC} and the same occurs with their inverting inputs because of the virtual ground concept. So, there is not potential difference on R_G and the currents $i_{R'_1}$, i_{R_1} flowing on R'_1 and R_1 must verify:

$$i_{R_1} R_1 = -i_{R'_1} R'_1 \tag{16}$$

Since the current on R_1 flows through R_2, and the same occurs with R'_1, R'_2; equation (16) can be written as:

$$\frac{v_{iC} - v_o}{R_2} R_1 = \frac{v_{iC}}{R'_2} R'_1 \tag{17}$$

Solving (17) for v_o results:

$$v_o = v_{iC}\left(1 - \frac{R_2 R'_1}{R'_2 R_1}\right). \tag{18}$$

And the cross-gain $G_{DC} = v_o / v_{iC}$:

$$G_{DC} = 1 - \frac{R_2 R'_1}{R'_2 R_1} \tag{19}$$

Assuming resistors with nominal values R_{10}, R_{20} and tolerances t, the worst case is produced for $R_2 = R_{20}\,(1 - t)$, $R'_1 = R_{10}(1 - t)$, $R'_2 = R_{20}\,(1 + t)$, $R_1 = R_{10}(1 + t)$ and equation (19) becomes:

$$G_{DC} = 1 - \frac{(1-t)(1-t)}{(1+t)(1+t)} \tag{20}$$

Assuming $t << 1$, equation (20) can be approximated by

$$G_{DC} \approx 4t \tag{21}$$

and the CMRR due to resistor mismatches $CMRR_R = G_D / G_{DC}$ results:

$$CMRR_R \approx G_D / 4t \tag{22}$$

A.1.2 CMRR due to operational amplifiers open loop gain

Equation (22) is valid for low frequencies. As frequency increases, even with a perfect matching between resistor, the CMRR degrades because of the limited open loop gain of the operational amplifiers.

The differential input voltage of the circuit in Figure 14 is $v_{iD} = 0$ and no current flows through R_G. Considering that the GBP of OA1, OA2 are greater than that of OA3 and a perfect matching between resistors, the differential output voltage v_{OD} results null: $v_{OD} = v_{oP} - v_{oN} = 0$ and the output voltage v_O given by:

$$v_O = v_{oP} = v_{oN}. \tag{23}$$

The amplifier OA3 works in closed loop to set the node v_{oN} to the ground potential. Assuming a ratio $R_2 / R_1 = 1$ it imposes:

$$v_{ON} = 2v_{iC} - v_{o3} \approx 0, \tag{25}$$

where v_{o3} is the OA3 output voltage that is given approximately by:

$$v_{o3} \approx 2v_{iC}. \tag{26}$$

Finally, the input of OA3, which matches v_{oN} and v_O, results:

$$v_o \approx 2v_{iC} / A_3(s). \tag{27}$$

Then, the cross gain $G_{DC} \approx 2 / A_3(s)$ and the $CMRR_{OA}$ due to the open loop gain of OA3 is:

$$CMRR_{OA} \approx G_D A_3(s) / 2 \tag{28}$$

A.1.3 Overall CMRR

The CMRR of the circuit in Figure 14 depends on both resistors and open loop gain effects. It will be lower than the bounds given by equations (22) and (28) and can be asymptotically expressed by:

$$|CMRR|^{-1} \approx |CMRR_R|^{-1} + |CMRR_{OA}|^{-1} \tag{29}$$

Appendix B

B.1 Current source output impedance

The output current of the circuit in Figure 5 is given by:

$$i_o = G_D v_{iD} / R_S, \tag{30}$$

but this assumes a perfect matching between resistors. Considering that $R_2 / R_1 \neq R'_2 / R'_1$ as Figure 15 suggests, equation (30) becomes:

$$i_o = \frac{v_{iD} G_D}{R_S} + \frac{v_{iC}}{R_S}\left(1 - \frac{R_2 R'_1}{R'_2 R_1}\right) - \frac{v_{oN}}{R_S}\left(1 - \frac{R_2 R'_1}{R'_2 R_1}\right), \tag{31}$$

and i_o does not depends exclusively on v_{iD}, but also on the CM input voltage v_{iC} and the output voltage v_{oN} the circuit imposes on the load R_L. The last effect results in a limited output impedance given by:

$$R_o = R_S / \left(1 - \frac{R_2 R'_1}{R'_2 R_1}\right) \tag{32}$$

Considering that all resistors are of a tolerance t, the output impedance in the worst case is:

$$R_o \approx \pm R_S / 4t \tag{33}$$

Figure 15 Proposed differential input current source considering resistors' imbalances