An Analysis of Modular Multilevel Converter for Full Frequency Range Operations

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***Abstract*— In this paper an analysis of a power converter based on a modular multilevel topology is discussed. A mathematical model of the MMC is developed in order to evaluate its dynamic behavior and to better understand the incidence of the circulating current phenomenon which could compromise converter performance in variable speed drive applications. In fact, if such problem is not properly addressed reliability problems arise.**

Keywords—modular multilevel converter; circulating current; ac-voltage fluctuations.

I. NOMENCLATURE

i_k	*k-th* phase current
i_{kN}	lower side arm current of the *k-th* phase
i_{kP}	upper side arm current of the *k-th* phase
i_{kZ}	circulating current (*k-th* phase)
i_{kZdc}	dc component of the circulating current (*k-th* phase)
i_{kZac}	alternating component of the circulating current (*k-th* phase)
i_{kZn}	*n*-th harmonic component of i_{kZac}
v_g	dc supply voltage of the MMC
$v_{c,k,j}$	capacitor voltage of the *j-th* sub-module of the *k-th* phase
v_{ckU}	total capacitor voltages of the sub-modules of the upper arm of the *k-th* phase
$v_{k,j}$	output voltage of the *j-th* sub-module of the *k-th* phase
v_{kL}	lower side arm voltage (*k-th* phase)
v_{kU}	upper side arm voltage (*k-th* phase)
p_{kU}	upper side arm instantaneous power (*k-th* phase)
W_{kU}	upper side arm stored energy
C	dc-grid capacitance
L	inductance for each arm
N	number of sub-modules per arm

II. INTRODUCTION

Modular Multilevel Converter (MMC) is one of the emerging solutions either for high- or medium- voltage transformerless power conversion [1]. Their basic circuit architecture was proposed for the 15 *kV*/16 ⅔ *Hz* ac/ac conversion of traction drives without the LF (Low-Frequency) transformer [2], [3], [4]. Usually each converter arm includes a freely chosen number *N* of identical sub-modules (SMs), while each converter leg consists of two arms (upper and lower). The main advantages, that make very attractive this circuit topology, are: a modular structure able to be adapted to different voltage and power levels; a redundant operation that performs high availability values and robust failure management (i.e. a sub-module can be short-circuited, while the corresponding arm can still operate with one voltage level less, but without any further restriction [2], [5]); a multilevel waveform expandable to a number of voltage steps depending on the number of sub-modules used for each arm. The increase in the number of voltage levels also allows to reduce the total harmonic distortion (THD), improving the quality of the output voltages and currents with respect to the conventional converters [6], [7]. Moreover, the MMC topology offers an overall high blocking voltage capability with reduced stress on the switching devices of each sub-module. As a consequence, since the requirements for these devices are not critical, conventional power electronic devices can be used.

Besides, the flexibility of the MMC architecture makes it possible to realize different converter topologies (e.g. single or three-phase dc/ac converters as well as multi phase ac/ac converters) by simply rearranging the basic circuit and/or the control strategy [8-10].

The aforementioned advantages also make the MMC topology very attractive for urban mass transit systems as tramways or subway usually operated at 0.75 *kV*, 1.5 *kV* or 3.0 *kV* [11]. In fact, at these voltage levels, the choice of the MMC architecture is justified by the possibility to use commercial power switching devices with smaller blocking voltage, such as power MOS, in order to reduce the conduction losses and also the cost of the circuit. Moreover, a possible choice is represented by the integration of MMC topology with energy storage devices in order to improve the energy efficiency of urban mass transit systems [12-15].

The possibility of using MMC in a variable speed drive application could be a challenge. In fact, the presence of ac-fluctuations of the sub-modules voltages, inversely proportional to the output frequency, limits the needed operating range of the drive [16-18]. The capacitor voltages could be affected by the presence of the so-called circulating current. The circulating currents flow through the six arms of the MMC and could distort the sinusoidal arm currents [19]. As a consequence, if not controlled, the circulating current includes a dominant second-order harmonic component that increases the value of the arm currents and the converter losses [20]. The circulating currents are so defined because they circulate within the converter circuit with no effect on the dc side and/or the three-phase ac side [21]. This phenomenon

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is unique to the MMC circuit topology. Thus, the analysis of the dynamic behavior of the MMC [22], in order to identify the key factors affecting the circulating currents, can play a fundamental role in the design and the control/modulation of the converter. In fact, if such problem is not properly addressed reliability problems arise. As a consequence, a generalized mathematical model of the MMC has been developed in order to evaluate its dynamic behavior and to better understand the incidence of the circulating current phenomenon which could compromise converter performance in variable speed drive applications. Particularly, the amplitudes of the sub-module capacitor voltage fluctuations and their impact on the converter performances are analyzed.

Moreover, a proper PWM control strategy based on the technique proposed in [9] is also performed in order to keep the dc-voltage level of each SM constant to the desired value and to balance the upper and lower arm voltages in each phase. The implemented control technique is able to obtain a $2N+1$ levels output waveform over the full frequency range operation of the converter.

This paper focuses the attention on dc/ac MMC, also addressing the circulating current drawback by providing a proper mathematical model of the converter.

III. MMC MATHEMATICAL MODEL

A. Basic Operating Principles

The circuit in Fig. 1.*a* shows a leg (generic *k-th* phase) of a three-phase converter based on MMC architecture. Each leg consists of a stack of $2N$ sub-modules and two buffer inductors with the inductance L [9]. The leg is divided in two arms (upper and lower). The upper arm includes the SMs from 1 to N, while the lower arm includes the SMs from $N+1$ to $2N$. The architecture of the converter sub-module is depicted in Fig. 1.*b*. It consists of a half-bridge where the switching devices (S_{AH}, S_{AL}) with the dc-grid capacitor (C) can transfer the power in or out the converter sub-module. When the lower switch is closed (S_{AL}=1) and the upper switch is opened (S_{AH}=0), the SM is bypassed. On the other hand, when the lower switch is opened (S_{AL}=0) and the upper switch is closed (S_{AH}=1), the SM is inserted.

B. Voltages and Currents

For sake of simplicity and without loss of generality, we can refer to the single phase system of Fig. 1.*a*. The dc supply voltage v_g is the sum of the voltages across the two arms of a leg, including the voltage drops on the buffer inductors. Thus, the following relationship can be stated:

$$v_g = v_{kU} + v_{kL} + L\frac{d}{dt}(i_{kP} + i_{kN}) \tag{1}$$

where the arm voltages v_{kU} and v_{kL} are defined as:

$$v_{kU} = \sum_{j=1}^{N} v_{k,j} \; ; v_{kL} = \sum_{j=N+1}^{2N} v_{k,j} \tag{2}$$

In eqs. (1-2) $v_{k,j}$ is the output voltage of j-th sub-module, i_{kP} and i_{kN} are the upper side and lower side arm currents, respectively. The arm currents are defined such that a positive

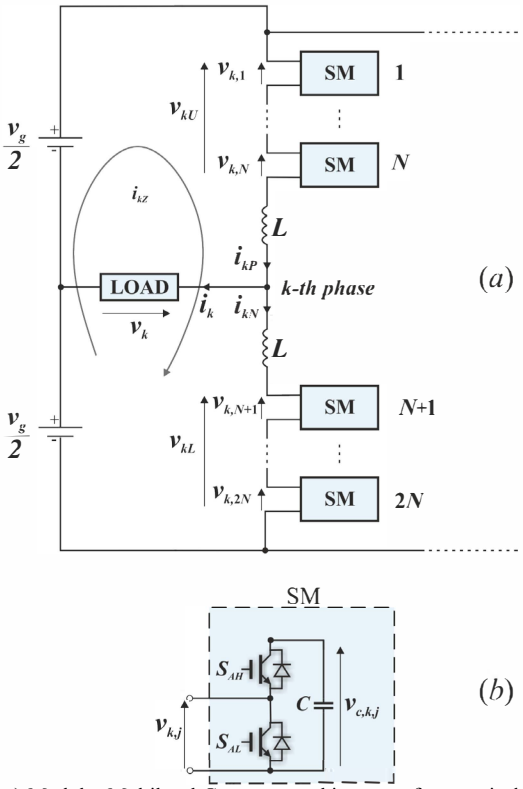

Fig. 1. *a*) Modular Multilevel Converter architecture of a generic *k*-phase for dc/ac conversion; *b*) structure of a sub-module.

current charges the capacitors. Thus, a positive upper arm current flows from the positive dc terminal to the ac terminal, while a positive lower arm current flows from the ac terminal to the negative dc terminal [22], as depicted in Fig. 1.*a*. As a consequence, the ac side current is given by:

$$i_k = i_{kP} - i_{kN} \tag{3}$$

while the corresponding circulating current in the *k*-phase is:

$$i_{kZ} = \frac{i_{kP} + i_{kN}}{2} = i_{kP} - \frac{i_k}{2} = i_{kN} + \frac{i_k}{2} \tag{4}$$

By referring to Fig 1.*a*, it can be easily obtained:

$$\frac{v_g}{2} - v_{kU} - L\frac{di_{kP}}{dt} - v_k = 0 \tag{5}$$

$$\frac{v_g}{2} - v_{kL} - L\frac{di_{kN}}{dt} + v_k = 0 \tag{6}$$

By adding (5) and (6), it gives:

$$\frac{v_g}{2} - \frac{v_{kL} + v_{kU}}{2} = L\frac{di_{kZ}}{dt} \tag{7}$$

Moreover, by subtracting eq. (6) from (5), it follows:

$$v_k = \frac{v_{kL} - v_{kU}}{2} - \frac{L}{2}\frac{di_k}{dt} \tag{8}$$

Eq. (8) can be simplified as:

$$v_{k,eq} = \frac{v_{kL} - v_{kU}}{2} \tag{9}$$

where $v_{k,eq}$ takes into account the equivalent load circuit due to the series of half the arm inductance and the actual load.

Eqs. (7), (8) show the dynamics of the dc and ac side of the converter. Particularly, eq. (7) highlights that the dynamic behavior of the circulating current i_{kZ} depends on the arm inductance value and on the sum of the upper and lower arm voltages. From eq. (8), it can be noted that the output voltage v_k (load voltage) is controlled by the difference between the lower and upper arm voltages.

The circulating current can be defined by the general expression:

$$i_{kZ} = i_{kZdc} + i_{kZac} = i_{kZdc} + \sum_{n=1}^{\infty} i_{kZn} \tag{10}$$

where i_{kZdc} is the dc component of the circulating current, corresponding to the energy exchange between the phase leg and the dc link [22], while i_{kZac} is the alternating component (sum of all the harmonics).

An analysis of the power flow through a converter phase shows that the circulating current impacts on the sub-module capacitor energy and voltage [20]. In order to reduce this phenomenon, the ac component of the circulating current should be reduced. In [23] the control algorithm is devoted to eliminate all high-order harmonics, thus keeping the circulating current equal to its dc value i_{kZdc}. Therefore, by considering i_{kZac}=0, eq. (7) can be rewritten as:

$$v_g = v_{kL} + v_{kU} = (\overline{v}_{kL} + \overline{v}_{kU}) + (\tilde{v}_{kL} + \tilde{v}_{kU}) \tag{11}$$

where $\bar{v}_{kL}$, $\bar{v}_{kU}$ are the mean values of the lower and upper arm voltages, while $\tilde{v}_{kL}$, $\tilde{v}_{kU}$ are the alternating components of the same voltages and v_g is the supply dc voltage. In order to meet (11), it must be as follows:

$$\begin{cases} v_g = \overline{v}_{kL} + \overline{v}_{kU} \\ \tilde{v}_{kL} + \tilde{v}_{kU} = 0 \end{cases} \tag{12}$$

The above relationships reveal that the circulating current is constant when the sum of the mean values of the upper and lower arm voltages equals the dc supply voltage, while their alternating components are 180° out of phase.

IV. Sub-module Capacitor Voltage Fluctuations

In the previous section the basic operating principle and the dynamics of the converter have been described. In order to better understand the converter behavior during transient and steady-state operation, explicit analytical expressions of the arm voltages and currents are presented.

Great attention must be devoted to the dynamics of the sub-modules capacitor voltages. The ac-voltage fluctuation included in each sub-module capacitor voltage is determined by the instantaneous power flowing into the capacitor [22]. In order to highlight the incidence of the circulating current, without emphasis on the harmonic content resulting from a PWM modulation, we can start by considering the ac-side voltage and current as pure sinusoidal waveforms, with a phase shift φ:

$$\begin{aligned} v_k &= \hat{v}_k \sin(\omega t) \\ i_k &= \hat{i}_k \sin(\omega t + \varphi) \end{aligned} \tag{13}$$

where ω is the fundamental frequency in radians per second.

In order to ease the analysis some assumptions are made: the input dc voltage is constant; all sub-modules are identical; the capacitor voltages are instantaneously balanced.

The instantaneous power flowing in the upper arm of the k-phase is given by (see eqs.(4-5)):

$$p_{kU} = v_{kU} i_{kP} = \left(\frac{v_g}{2} - v_k - L \frac{d\left(i_{kZ} + i_k/2\right)}{dt} \right) \left(i_{kZ} + \frac{i_k}{2} \right) \tag{14}$$

where the circulating current (i_{kZ}) at steady state operation can be defined as follows (10):

$$i_{kZ} = i_{kZdc} + \sum_{n=1}^{\infty} \hat{i}_{kZn} \sin(n\omega t + \gamma_n) \tag{15}$$

By referring to eqs. (10), (13), (15) and by neglecting the voltage drop on the buffer inductor (L), the energy stored in the upper arm can be obtained by integrating the instantaneous power (14):

$$\begin{aligned} W_{kU} = \int p_{kU} dt = \int \frac{v_g}{2} i_{kZdc} dt - \int i_{kZdc} \hat{v}_k \sin(\omega t) dt + \\ + \int \frac{v_g}{4} \hat{i}_k \sin(\omega t + \varphi) dt + \int \frac{\hat{v}_k \hat{i}_k}{4} \cos(2\omega t + \varphi) dt + \\ - \int \frac{\hat{v}_k \hat{i}_k}{4} \cos(\varphi) dt + \\ + \int \frac{v_g}{2} \sum_{n=1}^{\infty} i_{kZn} dt - \int \hat{v}_k \sin(\omega t) \sum_{n=1}^{\infty} i_{kZn} dt \end{aligned} \tag{16}$$

and by considering eq. (15), it can be obtained:

$$\begin{aligned} W_{kU} = & \frac{v_g}{2} i_{kZdc} \int dt - \frac{\hat{v}_k \hat{i}_k}{4} \cos(\varphi) \int dt + \\ & - \frac{1}{2} \hat{v}_k \hat{i}_{kZ1} \cos(\gamma_1) \int dt + \\ & + \frac{1}{2} \hat{v}_k \hat{i}_{kZ1} \int \cos(2\omega t + \gamma_1) dt + \\ & + \frac{v_g}{4} \hat{i}_k \int \sin(\omega t + \varphi) dt + \\ & + \frac{\hat{v}_k \hat{i}_k}{4} \int \cos(2\omega t + \varphi) dt - \hat{v}_k \hat{i}_{kZdc} \int \sin(\omega t) dt \\ & + \frac{v_g}{2} \int \sum_{n=1}^{\infty} \hat{i}_{kZn} \sin(n\omega t + \gamma_n) dt + \\ & - \hat{v}_k \int \sin(\omega t) \sum_{n=2}^{\infty} \hat{i}_{kZn} \sin(n\omega t + \gamma_n) dt \end{aligned} \tag{17}$$

In order to guarantee the energy balance at steady state operation or rather that the stored energy in one arm is the same at the beginning and at the end of a fundamental period ($T=1/f=2\pi/\omega$), the sum of the first three terms (dc components) of (17) must be equal to zero. This latter constraint means that:

$$\begin{cases} i_{kZdc} = \dfrac{\hat{v}_k \hat{i}_k}{2v_g}\cos(\varphi) \\ \gamma_1 = \pm\pi/2 \end{cases} \tag{18}$$

Eq. (18) is easily derived from the active power balance, thus highlighting that the dc component of the circulating current must flow through the converter leg at the aim of providing the active power to the ac-side. Moreover, eq. (17) can be written as:

$$W_{kU} = \int p_{kU}\,dt = \overline{W}_{kU} + \tilde{W}_{kU} \tag{19}$$

and the analysis will be focused on the alternating component of the stored energy, because of the direct link to the capacitor voltage oscillations of each sub-module. From eqs. (17), (18), (19), it can be obtained:

$$\begin{aligned} \tilde{W}_{kU} = {} & \frac{\hat{v}_k \hat{i}_{kZ1}}{4\omega}\sin(2\omega t+\gamma_1) - \frac{v_g \hat{i}_k}{4\omega}\cos(\omega t+\varphi) + \\ & + \frac{\hat{v}_k \hat{i}_k}{8\omega}\sin(2\omega t+\varphi) + \frac{\hat{v}_k^2 \hat{i}_k}{2v_g\omega}\cos(\varphi)\cos(\omega t) + \\ & - \frac{v_g}{2}\sum_{n=1}^{\infty}\frac{\hat{i}_{kZn}}{n\omega}\cos(n\omega t+\gamma_n) + \\ & - \frac{\hat{v}_k}{2}\sum_{n=2}^{\infty}\frac{\hat{i}_{kZn}}{(n-1)\omega}\sin((n-1)\omega t+\gamma_n) + \\ & + \frac{\hat{v}_k}{2}\sum_{n=2}^{\infty}\frac{\hat{i}_{kZn}}{(n+1)\omega}\sin((n+1)\omega t+\gamma_n) \end{aligned} \tag{20}$$

The total stored energy in the upper arm of the *k*-th phase can be derived [20], [24]:

$$W_{kU} = \frac{1}{2}C_{eq}v_{ckU}^2 \tag{21}$$

where v_{ckU} is the total capacitor voltages in the upper arm, and C_{eq} is the equivalent capacitance of the series connected capacitors (inserted sub-modules) in the upper arm. By considering the average and the alternating part of the total capacitor voltages, eq. (21) can be expressed as follows:

$$\begin{aligned} W_{kU} = \frac{1}{2}C_{eq}v_{ckU}^2 = \frac{C_{eq}}{2}\left(\overline{v}_{ckU}+\tilde{v}_{ckU}\right)^2 = \\ = \frac{C_{eq}}{2}\overline{v}_{ckU}^2 + \frac{C_{eq}}{2}\tilde{v}_{ckU}^2 + C_{eq}\overline{v}_{ckU}\tilde{v}_{ckU} \end{aligned} \tag{22}$$

The alternating component of the (22), normalized to the input voltage, is:

$$\frac{\tilde{W}_{kU}}{v_g} = \frac{C_{eq}}{2}\frac{\tilde{v}_{ckU}^2}{v_g} + C_{eq}\frac{\overline{v}_{ckU}}{v_g}\tilde{v}_{ckU} \cong C_{eq}\tilde{v}_{ckU} \tag{23}$$

thus, by considering the capacitor voltages equally distributed in each arm (balancing condition), from eqs. (22), (23), the ac-voltage fluctuation included in the *j*-th sub-module capacitor voltage in the upper arm of the *k*-phase is given by:

$$\tilde{v}_{c,k,j} = \frac{\tilde{v}_{ckU}}{N} \qquad j = 1,\ldots,N \quad (upper\ arm) \tag{24}$$

so substituting (23) in (24), it follows:

$$\begin{aligned} \tilde{v}_{c,k,j} = {} & \left(\frac{1}{NCv_g}\right)\cdot\left(\frac{\hat{i}_k}{4\omega}\right)\cdot[\hat{v}_k\hat{i}_{kZ1}\sin(2\omega t+\gamma_1) + \\ & - v_g\cos(\omega t+\varphi) + \frac{\hat{v}_k}{2}\sin(2\omega t+\varphi) + \\ & + \frac{2\hat{v}_k^2}{v_g}\cos(\varphi)\cos(\omega t) + \\ & - \frac{2v_g}{\hat{i}_k}\sum_{n=1}^{\infty}\frac{\hat{i}_{kZn}}{n}\cos(n\omega t+\gamma_n) + \\ & - \frac{2\hat{v}_k}{\hat{i}_k}\sum_{n=2}^{\infty}\frac{\hat{i}_{kZn}}{(n-1)}\sin((n-1)\omega t+\gamma_n) + \\ & + \frac{2\hat{v}_k}{\hat{i}_k}\sum_{n=2}^{\infty}\frac{\hat{i}_{kZn}}{(n+1)}\sin((n+1)\omega t+\gamma_n)] \end{aligned} \tag{25}$$

The above relationship highlights that the ac-voltage fluctuation of a single sub-module is proportional to the amplitude of the load current and inversely proportional to the load frequency and the dc-grid capacitance. Furthermore, this oscillation depends on the load power factor ($cos(\varphi)$), the ratio of the amplitude of the load voltage to the input voltage ($\hat{v}_k/v_g$), and the harmonic content of the circulating current.

Now some considerations can be made in order to simplify the analysis. A symmetrical 3-phase system as load of the MMC (see Fig. 2), and equal circulating currents in each converter leg with a phase shift of 120 degrees can be assumed.

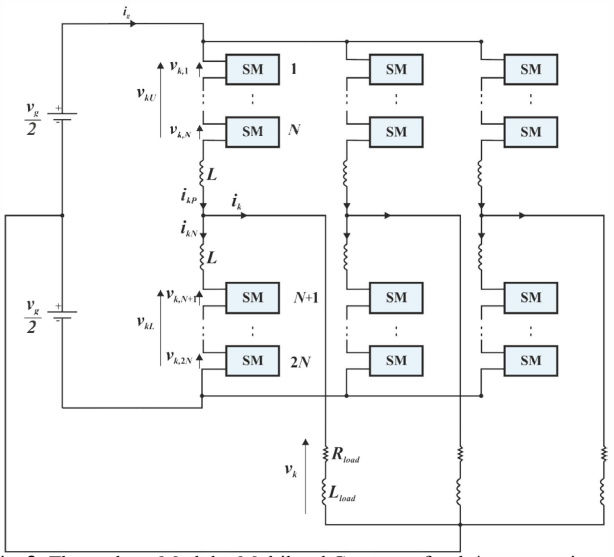

Fig. 2. Three-phase Modular Multilevel Converter for dc/ac conversion.

The input current i_g is the sum of the upper arms currents:

$$i_g = \sum_{k=1}^{3} i_{kP} = \sum_{k=1}^{3} i_{kZ} \tag{26}$$

so the input current is constant if the alternating part of the circulating current does not contain harmonics with an order multiple of 3 (see eq. 15) [25]. Furthermore, a symmetric energy variation in the upper and lower arm is possible if the odd order harmonics of the circulating current are equal to zero. As a consequence, the energy variations in the upper and lower arm of a leg are equal, but shifted of an half the fundamental period.

Accordingly to the above considerations, in a first approximation, eq. (25) can be rewritten as:

$$\begin{aligned}\tilde{v}_{c,k,j} = &\left(\frac{1}{NCv_g}\right)\cdot\left(\frac{\hat{i}_k}{4\omega}\right)\cdot[-v_g\cos(\omega t+\varphi)+\\ &+\frac{\hat{v}_k}{2}\sin(2\omega t+\varphi)+\frac{2\hat{v}_k^2}{v_g}\cos(\varphi)\cos(\omega t)+\\ &-\frac{v_g\hat{i}_{kZ2}}{\hat{i}_k}\cos(2\omega t+\gamma_2)+\\ &-\frac{2\hat{v}_k\hat{i}_{kZ2}}{\hat{i}_k}\sin(\omega t+\gamma_2)+\\ &+\frac{2\hat{v}_k\hat{i}_{kZ2}}{3\hat{i}_k}\sin(3\omega t+\gamma_2)]\end{aligned} \tag{27}$$

where the harmonic content of the circulating current is dominated by the amplitude of the second-order harmonic [26], so neglecting the even high-order harmonics. This choice appears a good approximation as results by comparison with the simulated performance(see Fig. 3). The numerical results have been obtained by performing the control technique proposed in [9], with an ideal modulation strategy, referred to the 3-phase circuit in Fig. 2. Table I summarizes the used circuit parameters.

TABLE I. CIRCUIT PARAMETERS USED FOR SIMULATION

#sub-module per leg	$2N$=4
supply dc voltage	v_g=750 V
dc capacitance	C=30 mF
arm inductance	L=0.5 mH
load inductance and resistance	L_{load}=2 mH; R_{load}=10 Ω
fundamental frequency	f=50 Hz

V. COMPARISON BETWEEN SIMULATED PERFORMANCES AND ANALYTICAL MODEL

A set of simulations have been conducted in order to verify the validity of the proposed analytical model of the converter. Fig. 3 depicts a zoom-view of the steady-state operation of the dc-capacitor voltage ($\tilde{v}_{c,k,j}$). Moreover, it shows the comparison between the simulated waveform (blue solid line) of the ac-voltage fluctuation of a single sub-module and the analytical data (red dashed line) derived from eq. (27), where the amplitude and phase angle of the alternating part of circulating current are estimated by performing a Fourier analysis of the simulation data. Numerical results are in good agreement with the analytical model, and the maximum ac-voltage difference (eq. (28)) exhibits an error of about 2%, showing that the proposed approach is promising for the analytical optimization of the converter design.

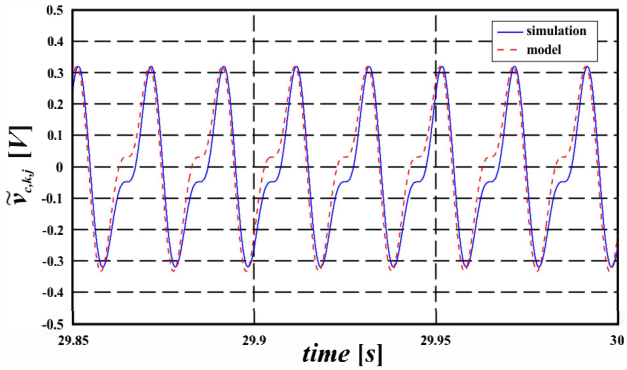

Fig. 3. AC-voltage fluctuation of the j-th sub-module capacitor included in the upper arm of the k-phase (k=1). Numerical simulation (blue solid line) is compared with the result of the analytical model (red dashed line).

The maximum ac-voltage difference on the j-th sub-module capacitor of the k-phase is given by:

$$\Delta v_{c,k,j\max} = \tilde{v}_{c,k,j\max} - \tilde{v}_{c,k,j\min} \tag{28}$$

Fig. 4 reports the maximum ac-voltage differences (upper arm sub-module of k-phase) versus frequency. It can be noted, from the simulation results (blue solid line), that reducing the frequency increases the maximum ac-voltage differences so worsening the start-up performance in variable speed-drive application. Fig. 4 also depicts the behavior derived from the analytical model (red dashed line), thus showing that the numerical simulations are in close agreement with the analytical data.

The following study investigates the analytical maximum ac-voltage differences as a function of the load power factor, $cos\varphi$. Fig. 5 shows the maximum ac-voltage fluctuations on the j-th sub-module capacitor in the upper arm of the k-phase versus the load power factor, by fixing the other circuit

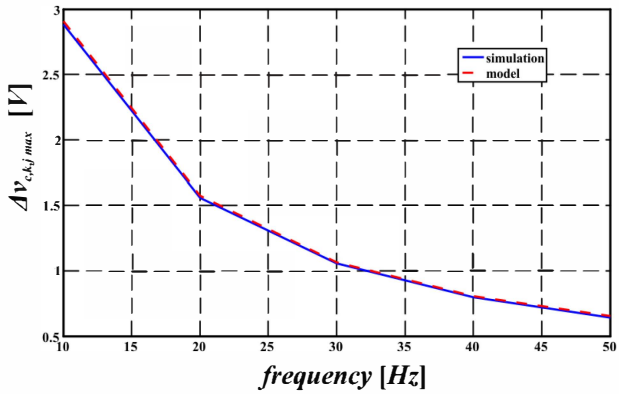

Fig. 4. Maximum ac-voltage differences versus frequency: simulated results (blue solid line); analytical data (red dashed line). First sub-module (j=1) of the upper arm of the first phase (k=1).

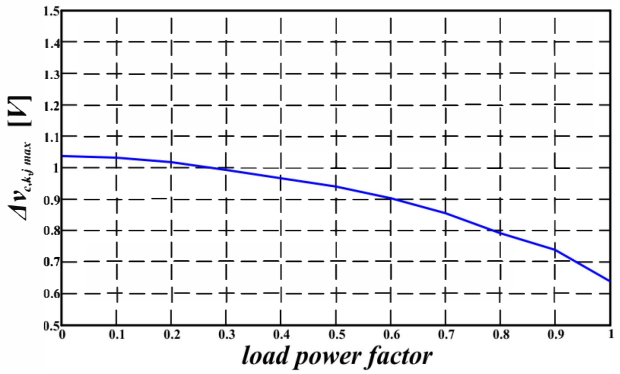

Fig. 5. Maximum ac-voltage differences versus load power factor at frequency f=50 *Hz*.

parameters as reported in Table I. It can be noted that increasing the power factor reduces the maximum ac-voltage difference on the sub-module capacitor.

In Fig. 6 is depicted the analytical maximum ac-voltage differences versus $\hat{i}_{kZ2}$, by fixing the others parameters as in Table I, in order to verify the incidence on the sub-module capacitor voltage fluctuations of the ac components of the circulating current. Fig. 6 shows that increasing the amplitude $\hat{i}_{kZ2}$ increases the magnitude of the maximum capacitor voltage oscillation and also increases the value of the arm currents, thus raising the overall converter losses.

VI. CONCLUSIONS

The paper has focused the attention on the design of a dc/ac Modular Multilevel Converter. Firstly, an adequate description of the circuit is presented, deriving also an analytical model of the converter, in order to evaluate its dynamic behavior and to better understand the incidence of the circulating current phenomenon which could compromise converter performance in variable speed drive applications. The usefulness of the analytical model is clearly shown in deriving the maximum ac-voltage fluctuation of a single sub-module capacitor. Furthermore, some numerical simulation results have permitted to confirm the validity of the proposed analytical approach in order to predict the converter dynamics.

Moreover, the model permits to verify the behavior of the sub-module ac-voltage fluctuations by varying the load conditions (power factor) and/or the amplitude and phase angle of the ac component of the circulating current.

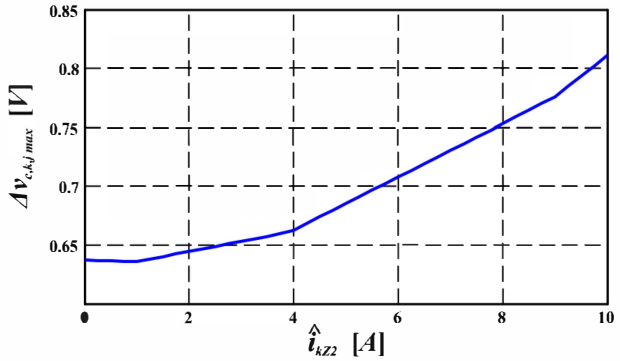

Fig. 6. Maximum ac-voltage differences versus the amplitude of the second-harmonic component of the circulating current.

In particular, it has highlighted that the increase of the ac component of the circulating current can affect the ac-voltage oscillation on the dc-grid capacitors and also the converter efficiency.

Further studies will be performed in order to optimize the converter design on the basis of the proposed modeling.

REFERENCES

[1] Rodriguez, J.; Lai, J. S. ; Peng, F. Z.: *Multilevel inverters: A survey of topologies, controls, and applications*. IEEE Trans. on Industrial Electronics (TIE), vol. 49, no. 4, Aug. 2002, pp. 724-738.

[2] Glinka, M.; Marquardt, R.: *A new AC/AC-Multilevel Converter Family Applied to a Single-Phase Converter*. Proc. Power Electronics and Drive Systems PEDS 2003, 17-20 Nov. 2003,vol.1 , pp. 16-23.

[3] Glinka, M.; Marquardt, R.: *A new AC/AC Multilevel Converter Family*. IEEE TIE, vol. 52, no. 3, June 2005, pp. 662-669.

[4] Lesnicar, A.; Marquardt, R.: *A new modular voltage source inverter topology*. Proc. Eur. Conf. on Power Electron. and Applicat. EPE 2003.

[5] Brando, G.; Dannier, A.; Del Pizzo, A.; Rizzo, R.: *A generalized modulation technique for multilevel converters*, POWERENG2007; International Conference on Power Engineering, Energy and Electrical Drives, Setubal, Portugal, 12-14 April 2007, pp. 624-629.

[6] Franquelo, L. G.; et al.: *The age of multilevel converters arrives*. IEEE Industrial Electronics Magazine, June 2008, pp. 28-39.

[7] Dixon, J.; Pereda, J., et al.: *Asymmetrical Multilevel Inverter for Traction Drives Using Only One DC Supply*. IEEE Trans. on Vehicular Technology, vol. 59, no. 8, Oct. 2010, pp 3736-3743.

[8] Glinka, M.: *Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage*. IEEE Power Electronics Specialists Conference PESC 2004, 20-25 June 2004, pp. 2572-2576.

[9] Hagiwara, M.; Akagi, H.: *PWM control and experiment of modular multilevel converters*. IEEE PESC 2008, pp. 154-161.

[10] Rohner, S.; Bernet, S.; et al.: *Modelling, simulation and analysis of a Modular Multilevel Converter for medium voltage applications*. IEEE International Conf. on Industrial Tech. ICIT 2010, 14-17 March 2010, pp. 775-782.

[11] Coppola, M.; Iannuzzi, D.; Del Pizzo, A.:*A Power Traction Converter based on Modular Multilevel Architecture integrated with Energy Storage Devices*. IEEE Electrical Systems for Aircraft, Railway and Ship Propulsion (ESARS), 2012 , pp.1-7, 16-18 Oct. 2012.

[12] Veneri, O.; Ferraro, L.; Capasso, C.; Iannuzzi, D.: *Charging infrastructures for EV: Overview of technologies and issues*. IEEE Electrical Systems for Aircraft, Railway and Ship Propulsion (ESARS), 2012, pp.1-6, 16-18 Oct. 2012.

[13] Ciccarelli, F.; Iannuzzi, D.: *A Novel energy management control of wayside Li-Ion capacitors-based energy storage for urban mass transit systems*. International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012, pp.773-779, 20-22 June 2012.

[14] Battistelli, L.; Fantauzzi, M.; Iannuzzi, D.; Lauria, D.: *Energy management of electrified mass transit systems with Energy Storage devices*. International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012, pp.1172-1177, 20-22 June 2012.

[15] Iannuzzi, D., Lauria, D., Tricoli, P.: *Optimal Design of Stationary Supercapacitors Storage Devices for Light Electrical Transportation Systems*. Journal of Optimization and Engineering, vol. 13 n. 4, December 2012, pp. 689-704.

[16] Korn, A.J.; et al.: *Low output frequency operation of the Modular Multi-Level Converter*. IEEE Energy Conversion Congress and Exposition (ECCE), 2010, pp.3993-3997, 12-16 Sept. 2010.

[17] Hagiwara, M.; Nishimura, K.; Akagi, H.: *A Medium-Voltage Motor Drive With a Modular Multilevel PWM Inverter*., IEEE Trans. on Power Electronics (TPEL) , vol.25, no.7, pp.1786-1799, July 2010.

[18] Kolb, J.; et al.: *Straight forward vector control of the Modular Multilevel Converter for feeding three-phase machines over their complete frequency range*. IEEE Conference on Industrial Electronics Society IECON 2011, pp.1596-1601, 7-10 Nov. 2011.

[19] Tu; Q.,et al.: Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters. IEEE, Trans. on Power Delivery (TPWRD), vol.26, no.3, pp.2009-2017, July 2011.

[20] Antonopoulos, A.; et al.: On dynamics and voltage control of the Modular Multilevel Converter. European Conference on Power Electronics and Applications, EPE 2009, pp.1-10, 8-10 Sept. 2009.

[21] Rohner, S.; et al.: Analysis and Simulation of a 6 kV, 6 MVA Modular Multilevel Converter. IEEE Annual Conference of Industrial Electronics, IECON 2009, pp.225-230, 3-5 Nov. 2009.

[22] Ilves, K.; et al.: *A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency*. IEEE TPEL, vol.27, no.8, pp.3482-3494, Aug. 2012.

[23] Ängquist, L.; Antonopoulos, A.; Siemaszko, D.; Ilves, K.; Vasiladiotis, M.; Nee, H.-P.: *Inner control of Modular Multilevel Converters - An approach using open-loop estimation of stored energy*. International Power Electronics Conference (IPEC), pp.1579-1585, June 2010.

[24] Spichartz, M.; Staudt, V.; Steimel, A.: *Analysis of the Module-Voltage Fluctuations of the Modular Multilevel Converter at variable Speed Drive Applications*. International Conference on Optimization of Electrical and Electronic Equipment (OPTIM), 2012, pp.751-758, 24-26 May 2012.

[25] Engel, S. P.; De Doncker R. W.: *Control of the Modular Multi-Level Converter for Minimized Cell Capacitance*. EPE'11 ECCE Europe, the 14th European Conference on Power Electronics and Applications, Birmingham, 2011.

[26] Ilves, K.; et al.: *Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters*. IEEE TPEL, vol.27, no.1, pp.57-68, Jan. 2012.