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Performance Comparison of Graphene Nanoribbon Schottky Barrier and MOS FETs

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Abstract

Graphene Nanoribbon (GNR) Schottky barrier (SB) FETs and MOSFETs are studied using self-consistent atomistic simulations. MOSFETs show 30 – 70 % performance improvement in terms of larger on current, larger maximum achievable on-off current ratio, larger cutoff frequency, smaller intrinsic delay and better saturation behavior for ideal structures. Disorders, such as lattice vacancies, edge roughness, and ionized impurities, have a significant impact on device performance and variability, due to strong sensitivity to electrostatic environment and channel atomistic structure.

Introduction

Recent progress in carbon electronics (1-3) has driven much interest to graphene nanoribbon (GNR) field-effect transistors (FETs) for future digital and analog nanoelectronic applications (4-10). GNRFETs demonstrated experimentally to date are realized by connecting the channel to the reservoirs with Schottky contacts (5, 6), whereas ohmic contacts can in principle be obtained by heavily doping the GNR source and drain extensions. Due to the embryonic stage of this new field of research, many issues still remain unsolved. It is, for example, not clear how much performance improvement can be obtained by using a MOSFET device structure, or which role non-idealities like defects, ionized impurities, or edge roughness, will play on device characteristics for both GNR Schottky barrier (SB) FETs and MOSFETs.

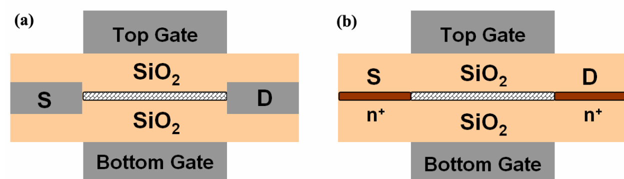

Fig. 1 *Simulated device structure* (a) Schottky barrier (SB) field-effect transistor (FET) and (b) MOSFET. SiO_2 gate insulator is 1.5-nm thick with a relative dielectric constant $\kappa = 3.9$. $N = 12$ armchair-edge graphene nanoribbon (GNR) with a length of 15 nm, a width of 1.35 nm and a band gap of $E_g \approx 0.6$ eV is used as channel material. The SB height in (a) is a half bandgap.

In this study, we focus on optimized GNRFET structures way beyond what is achievable by current technology, in order to investigate the potential and the performance that can be expected if technological challenges are met. However, we consider both defectless devices and more realistic devices in which small amounts of single defects are present, in terms of impurities, vacancies, or rough edges.

Approach

Device characteristics of GNRFETs are calculated by solving the Schrödinger equation using the non-equilibrium Green's function (NEGF) formalism in an atomistic p_Z orbital basis set self-consistently with three-dimensional (3D) Poisson equation. Transport is ballistic and energy relaxation is considered at the GNR edges (11). Simulated SBFET and MOSFET device structures are shown in Fig. 1. For an ideal structure, a perfectly patterned N = 12 (3) armchair-edge GNR is used as channel material, whereas for non-ideal devices, edge roughness, single atomistic vacancy on the GNR, or ionized impurity near the GNR is considered as a defect.

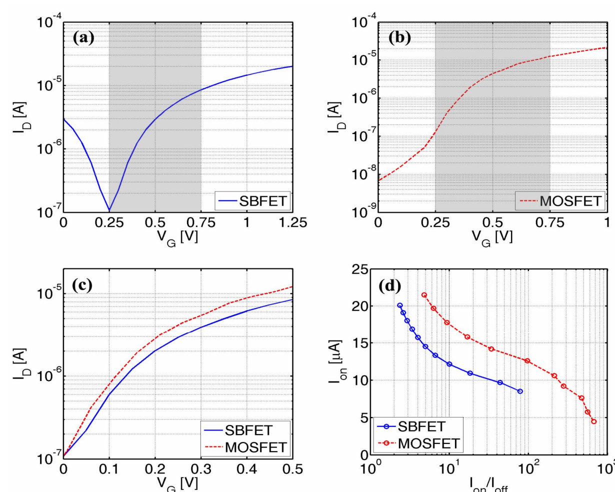

Fig. 2 I_D-V_G characteristics of (a) an ideal SBFET and (b) an ideal MOSFET. For a fair comparison between two different devices, the minimal leakage current I_{min} of SBFET is chosen as a common off current $I_{off} = 10^{-7}$ A, and on state is defined at $V_G = V_{off} + V_{DD}$, where V_{DD} is the power supply voltage of 0.5 V. Gray windows in (a) and (b) show the selected operating voltage range of each device. (c) I_D-V_G comparison of the ideal SBFET and the ideal MOSFET. When $I_{off} = 10^{-7}$ A is assumed, the MOSFET has 50 % larger on current than the SBFET. (d) I_{on} vs. I_{on}/I_{off}. MOSFETs can have a larger on-off ratio than SBFETs.

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Results

A. Ideal structures

First, the device characteristics of defectless SBFET and MOSFET have been compared. Fig. 2a and 2b show I_D-V_G transfer characteristics for each device. For a fair comparison of on current I_{on} (i.e. the current at the on state $V_G = V_D = V_{DD}$), the gate work function has been engineered in order to obtain the same off current $I_{off} = 10^{-7}$ A (i.e. the current at the off state $V_G = 0$ V, $V_D = V_{DD}$) for both devices. The gray windows in Fig. 2a and 2b show the operating voltage range for each device after the work function engineering. In Fig. 2c, the transfer characteristics comparison is shown: The MOSFET has 50 % larger I_{on} and 70 % larger transconductance g_m than the SBFET. MOSFETs can have a significantly larger maximum on-off ratio than SBFETs due to the suppression of ambipolar transport, as shown in Fig. 2d. Fig. 3a shows the output characteristics: MOSFET shows a better saturation behavior, which is also pointed out by the smaller output conductance in Fig. 3b. For an evaluation study of analog and digital performance, cutoff frequency f_T and intrinsic delay τ are compared in Fig. 4, by using a previously developed comparison method that takes the power supply, on and off states into consideration (12): MOSFET has ~ 40 % higher f_T and faster switching speed with smaller delay than a middle-bandgap SBFET. The very high cutoff frequency and the very small delay shown in Fig. 4 are due to the extremely short channel length (15 nm) and the assumption of purely ballistic transport.

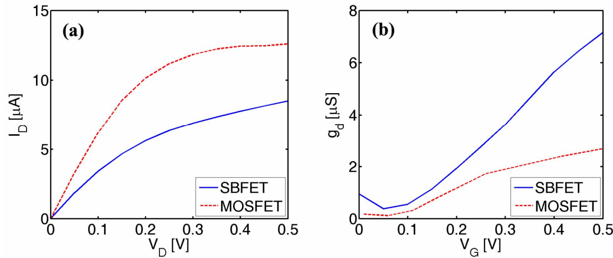

Fig. 3 (a) I_D-V_D characteristics at $V_G = 0.5$ V. (b) Output conductance, g_d vs. V_G for $V_D = V_{DD} = 0.5$ V. MOSFET shows better saturation behavior.

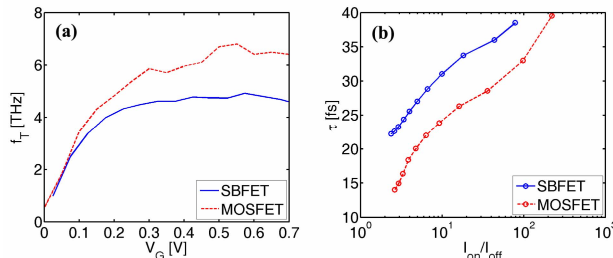

Fig. 4 (a) Cutoff frequency, f_T vs. V_G. (b) Intrinsic delay, τ vs. I_{on}/I_{off}. MOSFET can have higher cutoff frequency and smaller intrinsic delay than SBFET.

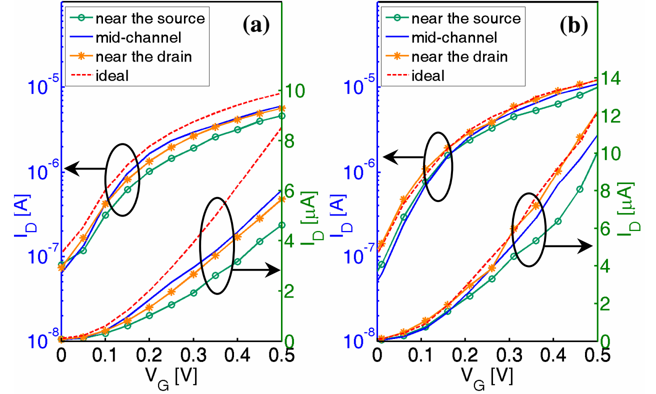

Fig. 5 *The effect of a lattice vacancy* (a) I_D-V_G of an SBFET and (b) I_D-V_G of a MOSFET in the presence of a single atomistic vacancy, in a log scale (left axis) and in a linear scale (right axis). The lattice vacancy is placed in the middle of the channel width direction, and at the different positions along the transport direction: near the source, in the middle of the channel, and near the drain.

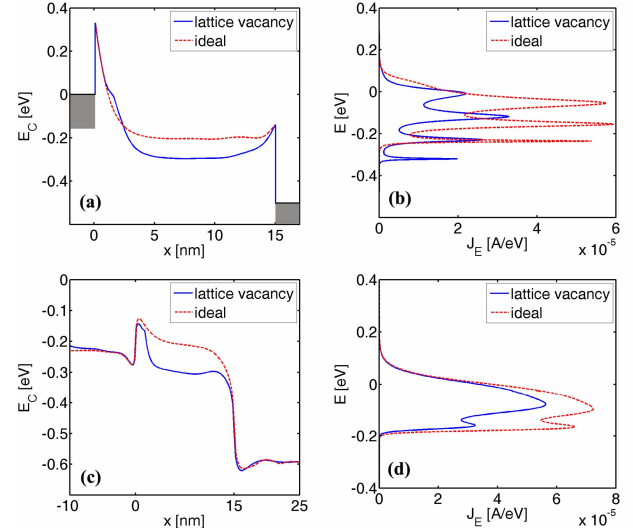

Fig. 6 (a) Conduction band profile along the channel position for an SBFET in the presence of a lattice vacancy near the source at the on state. (b) Energy-resolved current spectrum for (a). (c) Conduction band profile along the channel position for a MOSFET in the presence of a lattice vacancy near the source at the on state. (d) Energy-resolved current spectrum for (c).

B. Atomistic Vacancy

Fig. 5 shows I_D-V_G curves in the presence of a defect, represented by a single atomistic vacancy. Defects have been placed in the middle of the channel width direction, and at the different positions along the transport direction. The defect near the source has the largest effect in both devices, so that the on current is 50 % smaller in SBFET and 17 % smaller in MOSFET compared to the ideal devices. In the presence of a defect, reduced quantum transmission and self-consistent electrostatic effect can result in the reduced

I_{on}. For an SBFET with a defect near the source, thicker SB is induced (Fig. 6a) and quantum transmission is reduced (Fig. 6b) at the on state, which result in a smaller I_{on}. When a defect is located at halfway along the channel or near the drain of a SBFET, electron accumulation between the source and the defect increases potential barrier and reduces the energy window of electron injection from the source to channel, which results in reduced current with a lattice vacancy. In case of a MOSFET with a lattice vacancy near the source, however, potential barrier is not increased, as shown in Fig. 6c. Instead, the reduced number of propagating states due to the lattice vacancy reduced the transmission probability (Fig. 6d), which results in a smaller on current.

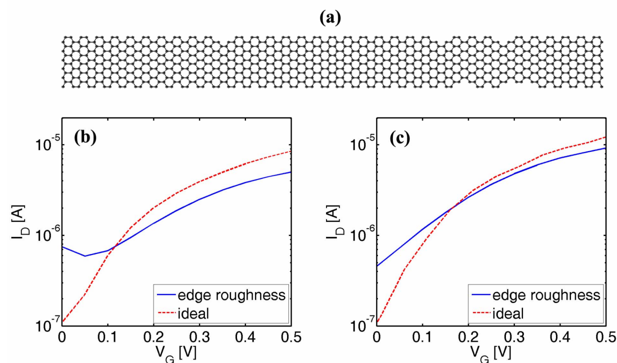

Fig. 7 *The effect of edge roughness* (a) Atomistic configuration of a simulated GNR channel with edge roughness. I_D-V_G characteristics of (b) the SBFET and (c) the MOSFET with the GNR channel shown in (a).

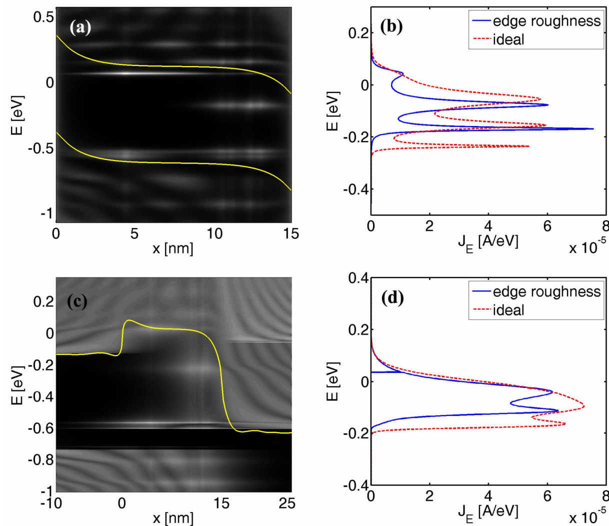

Fig. 8 (a) Local density of states (LDOS) at the off state (V_G = 0 V, V_D = V_{DD}) for the SBFET with the GNR of Fig. 7a as a channel material. (b) Energy-resolved current spectrum at the on state (V_G= V_D = V_{DD}) for the device of (a). (c) LDOS at the off state for the MOSFET with the GNR of Fig. 7a as a channel material. (d) Energy-resolved current spectrum at the on state for the device of (c). The solid bright lines in (a) show the band gap of an ideal SBFET, and the solid bright line in (c) is the conduction band of an ideal MOSFET.

C. Edge Roughness

The state of the art in patterning is far from atomic scale precision, and even optimistically one can assume a degree of edge roughness present in GNRs, as exemplified in Fig. 7a. In general, the off currents are increased due to the gap states induced in the bandgap region, which can enhance the leakage current at the off state. Fig. 8a and 8c clearly show the energy states in the band gap region for an SBFET and a MOSFET, respectively, at off states. On the other hand, the on currents are decreased due to the compensation of self-consistent electrostatic effect and quantum transport effect (13). For an SBFET, even though the gap states near the beginning of the channel may facilitate quantum transport, the self-consistent electrostatic effect can reduce the energy window for electron to inject from the source to the channel (Fig. 8b). For a MOSFET, quantum transmission is reduced due to the carrier transport through the imperfect channel as shown in Fig. 8d. With the simulated structure, I_{off} is increased by a factor of 7 and 4 for an SBFET and a MOSFET, respectively, and I_{on} is reduced by 40 % and 10 % for an SBFET and a MOSFET, respectively.

D. Ionized Impurity

A single ionized impurity can be modeled as a positive fixed charge equal to +0.4q placed 1.84-Å far from the GNR surface, according to *ab-initio* calculations (14). We investigate its effect when it is in the middle of the channel width direction, and at the different positions along the transport direction. For an SBFET, the effect of a charge near the source is the most severe because it has a dramatic effect on the Schottky barrier and the tunneling probability. Fig. 9a shows thin SB (the solid line) at the beginning of the channel position, which results in an increased source-drain current. When the charge impurity is located in the middle of the channel of a SBFET, the electrons are trapped by the positive charge and the source-drain current is reduced. If the charge is located near the drain, the electrons are accumulated near the drain and low charge density near the source lowers the potential barrier at the beginning of the channel, which opens up the energy window more for electron flow from the source to the channel. For MOSFETs, however, the self-consistent potential effects have only a limited effect on source-drain currents. Even in the case of an impurity near the source, the barrier height is hardly changed and the barrier thickness is still thick enough (Fig. 10c) at the on state. When the impurity is located halfway along the channel or near the drain, electrons are trapped by a charged impurity, which degrades the on current. However, the variation of I_{on} for different positions of charged impurities is always smaller than 10 % for MOSFETs, since the potential barrier in the above threshold regime is always below the source Fermi level.

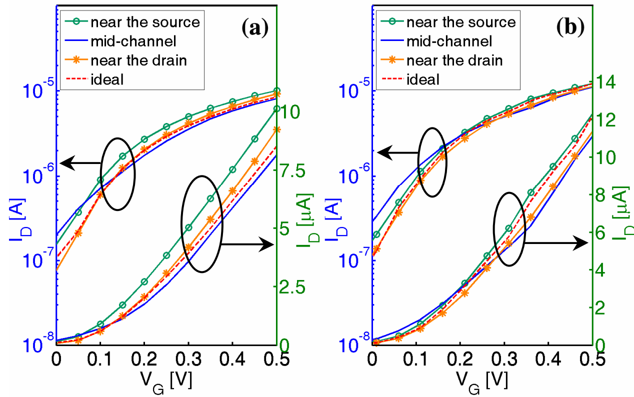

Fig. 9 *The effect of an ionized impurity* (a) I_D-V_G of an SBFET and (b) I_D-V_G of a MOSFET with an ionized impurity in a log scale (left axis) and in a linear scale (right axis). The impurity is located in the middle of the GNR width direction, and at the different positions along the transport direction.

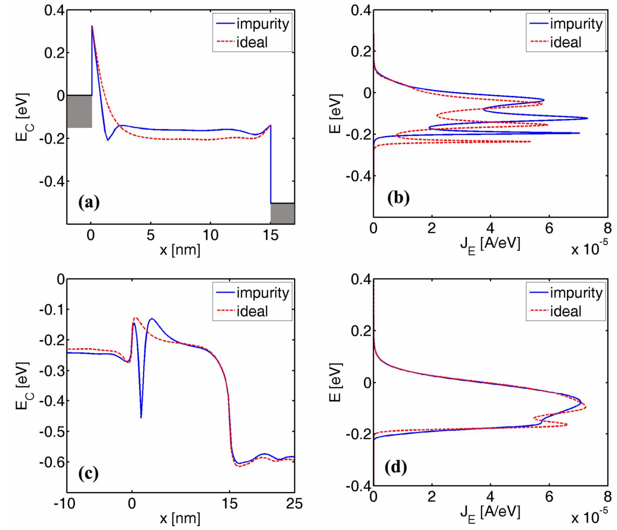

Fig. 10 (a) Conduction band profile along the channel position for an SBFET in the presence of an ionized impurity near the source at the on state. (b) Energy-resolved current spectrum for (a). (c) Conduction band profile along the channel position for a MOSFET in the presence of an ionized impurity near the source at the on state. (d) Energy-resolved current spectrum for (c).

Conclusion

We have presented performance comparisons between GNR SBFETs and MOSFETs. As also discussed in the case of carbon nanotube (CNT) FETs (15), MOSFETs show better device characteristics as larger maximum achievable on-off ratio, higher f_T, and smaller τ in the ideal structure without any defects or impurities. In the presence of atomistic vacancy in the channel GNR, the on current of an SBFET is more severely affected by the defect than that of a MOSFET. The edge roughness of GNR results in a larger I_{off} and a smaller I_{on} in general due to the induced gap states, quantum-mechanical transport, and electrostatic effects. An ionized impurity has a much smaller effect on a MOSFET than on an SBFET, where it can considerably alter the Schottky barrier and the electrostatics.

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