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RESEARCH ARTICLE

Design and Control of Novel Grid Tied Multilevel Filter-Less Inverter Using Current Based Sliding Mode Control

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ABSTRACT The role of control techniques is increasing due to the high penetration of renewable energy sources at grid level. The importance of inverters also rises as it balances the supply between the renewable source and grid power system. The issues related to penetration of renewable energy like power quality maintenance, protection against the detection of islanding and maintaining the integrity of grid; control techniques play a vital role to solve these problems. This paper proposed an internal control technique known as current based sliding mode control (SMC) for a filter less multilevel inverter (MLI). The aim of proposed research work is to achieve 27 level output voltage by using an inverter, which approaches sinusoidal wave without using any filters. To control the output of MLI, a current based SMC is implemented in order to achieve the robustness, a good dynamic response, a smaller number of voltage ripples and a smaller current THD. Moreover, a comparative analysis of SMC is done with the conventional PI controller. The response of the controller has been investigated for different cases e.g., introducing sag, swell, faults and harmonics in grid level has been implemented on MATLAB/Simulink. To validate the results of SMC for MLI, an experimental setup was also established which consists of National Instruments (NI) based hardware in loop (HIL) system and dSPACE 1202. The HIL system results show consistency with simulation results.

INDEX TERMS Filter less, hardware in loop (HIL), multilevel inverter (MLI), sliding mode control (SMC), total harmonic distortion (THD).

I. INTRODUCTION

DC to AC power converters are used for integration of renewable energy resources. Traditional two-level inverters have certain drawbacks like high switching losses, high voltage stress, low power quality and high electromagnetic interference, etc. [1], [2]. On other hand, MLIs have better performance comparatively, and are considered more significant in high voltage and power conversion applications. Despite of its advantages, the main challenges in the design of MLI were complexity, increase in number of switches, and more than one DC sources [3].

In literature, various topologies of MLI were proposed considering different issues. Most of the topologies were derived from three basic topologies i.e. Diode clamped MLI (DCMLI), Flying capacitor MLI (FCMLI) and cascaded H

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Bridge MLI (CHBMLI) [4]. Out of these basic topologies, CHBMLI is considered as most simple and advanced, while FCMLI and DCMLI topologies have issues regarding capacitor voltage balance when output levels are increased [5]. Based on the value of DC sources, the CHBMLI is classified into two topologies i.e., symmetrical with same value of each DC source and asymmetrical with different DC magnitudes. Kumar et al. [6] discussed hybrid topologies to reduce the number of input DC sources by combining floating capacitors with H bridge, which required a complex modulation scheme to balance capacitor voltage. Chattopadhyay and Chakraborty [7] proposed the level doubling network used with DC sources in the ratio of 1:7 to increase the output levels with a complex capacitor charging technique. Krishnachaitanya and Chitra [8] designed 15-level asymmetric MLI topology using nine switches and three DC sources but the voltage stress on the switches was high. So, it is inferred that the inverter topology with comparatively low voltage on high frequency switches has efficient performance. The switching losses of inverter were reduced by operating high voltage switches with low frequency as compared to low voltage switches [9]. Ziaeinejad and Mehrizi-Sani [10] proposed CHBMLI based on trinary sequence (1:3:9) DC sources were presented which operated at low frequency [11] and had higher level output with a smaller number of switches. In a trinary inverter for nine level output, the conducting switches per level were four as compared to five active switches in other asymmetric topologies [12]. Therefore, CHBMLI have gained considerable attention due to its modular design, simple control, reliability and there are no capacitor imbalance problems. Further trinary asymmetric CHB generates high quality voltage with minimum harmonics. Also, it requires least number of switches and DC sources [13], [14], [15]. Moreover, the complex mathematical process was previously required for finding switching angles for trinary CHB inverter [16]. Vargas et al. [17] introduced a sinusoidal pulse width modulation (SPWM) technique developed for 9 level trinary inverter by applying logical operations on carrier waves. Among different techniques of SPWM, carrier distribution or level shifting offered a superior output voltage with less THD and it is compatible with CHB topology.

According to IEEE 1545 standards [18], total harmonic distortion (THD) should be less than 5% at the point of common coupling (PCC). Inverters are interfaced with the grid using filters made up of passive components like capacitors and inductors for THD reduction. Addition of filter results into increment in cost, weight, and power loss of the inverter. Park et al. [19] proposed higher order filter with reduced filter size. However, the higher order filter produces extra resonant peaks which requires a proper damping scheme [20], [21]. THD and filter size can be reduced by increasing the switching frequency but it is inefficient due to rise in switching losses. The wide band gap (WBG) technology-based switches have the ability to operate at much higher frequencies with minimum switching losses. Rockhill et al. [22] proposed that WBG Silicon Carbide (SiC) based inverter could operate at 50 kHz switching frequency in comparison to 16 kHz Silicon (Si) based converter,which reduced the filter size. However, the SiC based inverter is costly and only suitable for high power applications [23]. Therefore, in order to address all these limitations, systems without filters are being proposed.

Inverters are mostly integrated with feedback control to stabilize system in accordance with the set parameters. The feedback control uses the difference of actual and the reference value to verify that the reference value is being followed by the system. In literature, many control techniques were used with inverters considering different objectives. Shi et al. [24] proposed feedforward control strategy was implemented with traditional PI control for half bridge three phase inverter, however it required high settling time and high overshoot which adversely affect the performance. In order to obtain low THD, the model predictive control (MPC) was implemented for LC filter based three phase inverter which requires load information and complex calculation for accurate performance [25]. Mohamed et al. [26] discussed a comparison between hysteresis control and space vector PWM (SVPWM) current control was made for grid-connected inverter. The system parameters did not affect the performance of the hysteresis controller and its implementation was also simple. However, variable switching frequency and high ripple current were the shortcomings in this type of controller. Various other controllers have also been used with three phase grid tied inverters such as partial feedback linearization control, H-infinity control and deadbeat control etc, as elaborated by Jena et al. [27]. Yang et al. [28] proposed a novel SMC design for PV based grid-tie inverters, which offered compensation in the fluctuations and external disturbances as well as had an improved error tracking ability. Further, this controller had a relatively easier implementation as compared to other non-linear controllers. Ozdemir et al. [29] proposed a super twisting algorithm of SMC for three-phase grid-tied three-level neutral point clamped inverters. This controller had less THD and also operated at deteriorated/imbalanced voltages and offered considerable suppression in chattering along with efficient tracking performance. Sebaaly et al. [30] implemented the current based SMC on 3L-NPC. It was observed that there is low THD with respect to grid. Furthermore, in case of DC link voltages, SMC delivered a better response at high switching frequency. Sebaaly et al. [31] proposed space vector modulation-based SMC which was implemented on the 3L-NPC. The SMC controlled the amplitude and phase of the current signal with reduced harmonics. Due to the aforementioned characteristics and nonlinear properties of SMC, the SMC can be utilized for voltage and current regulation. The SMC demonstrated robustness against disturbances in the system and offered quick-dynamic response [32].

The conventional PI controller has many applications but it has some limitations e.g., it has high starting overshoot. It is very sensitive to controller gains and also, its response is very slow towards the external disturbances [33]. On the other hand, SMC shows very quick response towards external disturbances. SMC is very useful for higher order systems

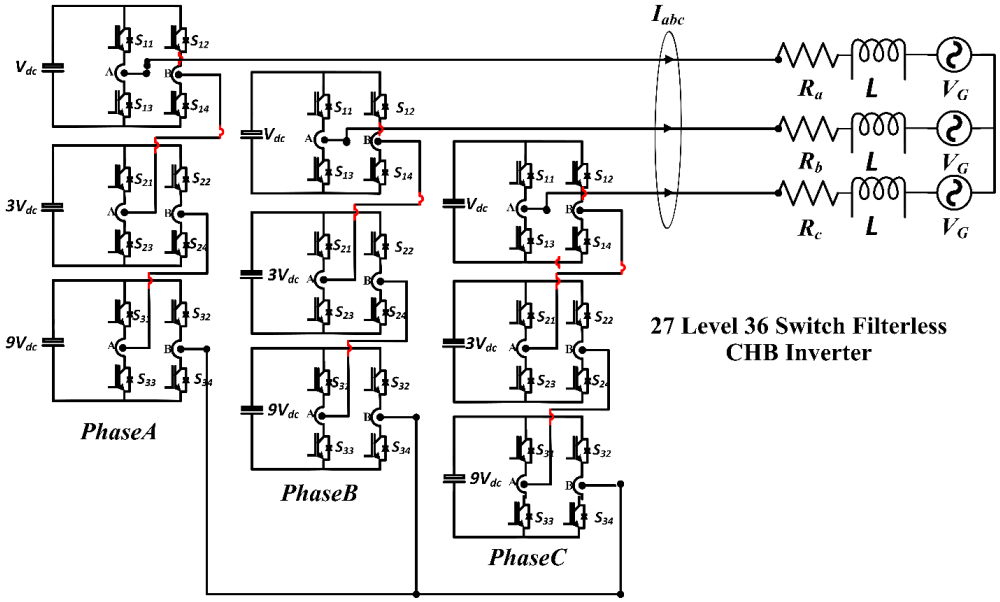

FIGURE 1. Circuit configuration of grid connected 27 level CHBMLI.

because it replaces the original system with new one with lower order. Moreover, SMC produce the desirable and smooth output power because it is designed by using direct power control. Also, it helps to remove inaccuracy. Due to these features of SMC, it is preferable to implement it on Inverter to control its output Current [34], [35].

The main contributions of this article are as follows:

- Trinary based cascaded H-bridge MLI is proposed for filter-less grid tied operations. Logic sum based PWM Technique is designed for Trinary based MLI to achieve 27 level output voltage.
- SMC controller was designed for the trinary based CHBMLI, a mathematical model of SMC was derived and simulated for the system, which was not found in literature. Beside this, the SMC is compared with PI controller to demonstrate its effectiveness.
- To further validate the simulation results, the topology of CHBMLI in HIL based OPAL RT system and the SMC was tested for CHBMLI by using dSPACE 1202 MicroLabBox.

The rest of the study is discussed Section wise. The Mathematical model of CHBMLI topology is discussed in Section 2. The Section 3 focused on the modulation scheme and conduction states of CHBMLI. The discussion on derivation of equations for SMC and their feasibility is mentioned in Section 4. Section 5 explains the simulation results and hardware implementation of HIL system. The conclusion is given in Section 6.

II. MATHEMATICAL MODEL OF CHBMLI

Figure 1 shows the detailed structure of the proposed three phase grid tied inverter. The trinary asymmetric cascaded H-bridge MLI topology can generate 27 levels. Each bridge is connected with deparated DC source. The line connecting the inverter with the grid has resistance R and some Inductance L. The system equation can be written as:

$$\begin{bmatrix} i'_a \\ i'_b \\ i'_c \end{bmatrix} = A \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + B \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} + C \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \tag{1}$$

where

$$A = \begin{bmatrix} \frac{-R}{L} & 0 & 0 \\ 0 & \frac{-R}{L} & 0 \\ 0 & 0 & \frac{-R}{L} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix},$$

$$C = -B$$

The dq model and their equations can be obtained by applying transformation from stationary (abc) to rotatory (dq) frame of reference using the following transfer matrix:

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \tag{2}$$

After applying Park's transformation, the system's equation in matrix form can be written as:

$$\begin{bmatrix} i'_d \\ i'_q \end{bmatrix} = X \begin{bmatrix} i_d \\ i_q \end{bmatrix} + Y \begin{bmatrix} U_d \\ U_q \end{bmatrix} + Z \begin{bmatrix} V_g d \\ V_g q \end{bmatrix} \tag{3}$$

where

$$X = \begin{bmatrix} \frac{-R}{L} & w \\ -w & \frac{-R}{L} \end{bmatrix}, \quad Y = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}, \quad Z = -Y$$

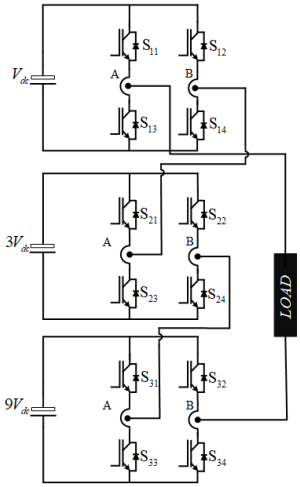

FIGURE 2. Trinary cascaded H-bridge topology.

In Eq (1), u_abc shows the inverter output voltage, $v_{grid,abc}$ shows the grid voltages and R is the resistance and L is the inductance through which inverter is connected to the grid.

A. CHB TOPOLOGY

Figure 2 displays the CHB topology for single phase. The asymmetric configuration possesses DC sources with different magnitudes. This topology utilizes a smaller number of components with ability to produce higher number of the voltage levels. The trinary sequence uses three DC sources in the ratio 1:3:9. The DC voltages are set in accordance with desired output voltage levels. For example, $V_{dc1} = 1V_{dc}$, $V_{dc2} = 3V_{dc}$ and $V_{dc3} = 9V_{dc}$. The specific voltage levels e.g., $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 4V_{dc}$ etc, can be achieved by selecting DC sources along with appropriate switching sequence. The output voltage levels can be increased by addition of DC voltage sources along with the switches. For achieving 27 levels, 12 switches and 3 voltage DC sources are used. For n DC sources, the output voltage level is given by Eq (4)

$$VoltageLevels = 3^n \tag{4}$$

where n shows the number of DC sources.

The sequence of DC source across each cell of inverter is indicated by Eq (5).

$$V_{dck} = 3^{k-1}V_{dc} \tag{5}$$

where $k = 1, 2, 3 \ldots, L$ which represents the sequence of DC source across the bridge and V_{dc} is the DC voltage across CHBMLI topology.

The formula to achieve maximum magnitude of output voltage levels is represented by Eq (6).

$$V_o = (3^n - 1)V_{dc}/2 \tag{6}$$

III. MODULATION SCHEME

In this research, a multi carrier phase disposition (PD) technique was used in which all the carrier waves are in phase.

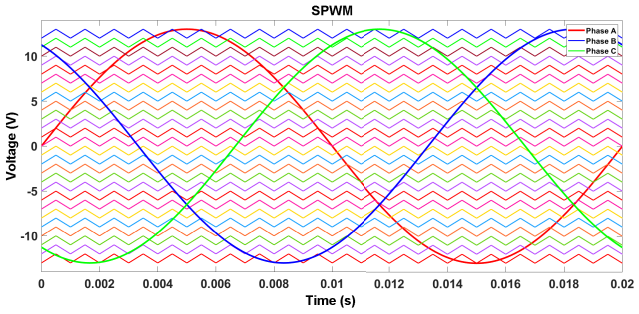

FIGURE 3. Scheme for multi carrier phase disposition to achieve 27 levels.

To achieve the required PWM signals for switches, a low frequency sinusoidal reference signal was compared with triangular carrier signals having high switching frequency as revealed in Figure 3.

Since for N level MLI, N-1 carrier waves are required to generate PWM waves. To achieve 27 levels, 26 carrier signals are compared with reference signal to produce 26 command signals. In single phase, there are 12 switches. Therefore, some digital logic-based operations are required to convert the 26 command signals into the 12 driving gate signals for the single-phase inverter design. It will guarantee a voltage output signal with 27 levels. The remaining two phases will be switched using a similar method, making a total of 36 switches in a three-phase system [17]. The Eq (7-18) indicates the gate signals for switches in which C_1,C_2,C_3,...,C_{26} are the command signals.

$$\begin{aligned} S_{11} &= C_1 \otimes C_7 \otimes C_4 \otimes C_3 \otimes C_6 \otimes C_{10} \otimes C_{16} \\ &\quad \otimes C_{13} \otimes C_{12} \otimes C_{15} \otimes C_{19} \otimes C_{25} \otimes C_{22} \otimes C_{21} \\ &\quad \otimes C_{24} \otimes C_9 \otimes C_{18} \end{aligned} \tag{7}$$

$$\begin{aligned} S_{12} &= C_2 \otimes C_8 \otimes C_5 \otimes C_3 \otimes C_6 \otimes C_{11} \otimes C_{17} \\ &\quad \otimes C_{14} \otimes C_{12} \otimes C15 \otimes C20 \otimes C_{26} \otimes C_{23} \otimes C_{21} \\ &\quad \otimes C_{24} \otimes C_9 \otimes C_{18} \end{aligned} \tag{8}$$

$$S_{13} = \sim S_{11} \tag{9}$$

$$S_{14} = \sim S_{12} \tag{10}$$

$$S_{21} = C_3 \otimes C_{21} \otimes C_9 \otimes C_{12} \otimes C_{18} \tag{11}$$

$$S_{22} = C_6 \otimes C_{24} \otimes C_{15} \otimes C_9 \otimes C_{18} \tag{12}$$

$$S_{23} = \sim S_{21} \tag{13}$$

$$S_{24} = \sim S_{22} \tag{14}$$

$$S_{31} = C_9 \tag{15}$$

$$S_{32} = C_{18} \tag{16}$$

$$S_{33} = \sim S_{31} \tag{17}$$

$$S_{34} = \sim S_{32} \tag{18}$$

In Eq (7-18), it can be seen that XOR operation is applied on 26 command signals. In Upper bridge with low DC source, the switches have more command signals as compared to switches in other bridges with higher DC sources. These specific command signals decide the state of specific switch with goal to achieve 27 level output signals.

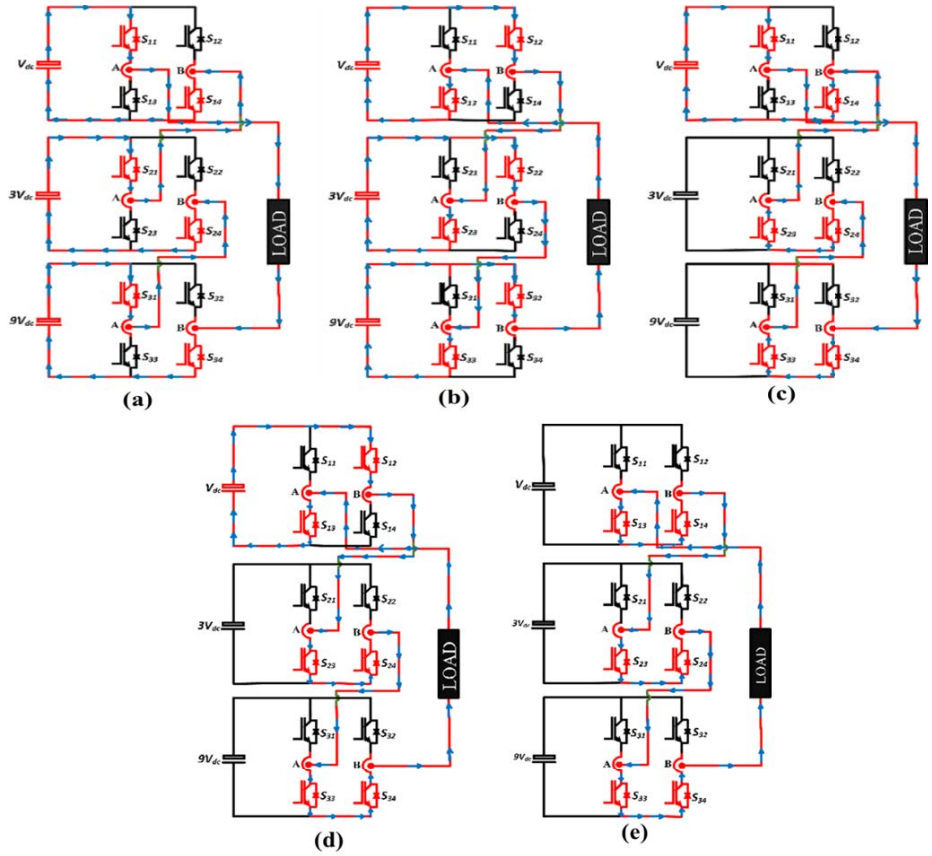

FIGURE 4. Conduction path followed by switching signals (a) output voltage levels = 13 (b) output voltage levels = −13 (c) output voltage levels = +1 (d) output voltage levels = −1 (e) output voltage levels = 0.

TABLE 1. Conduction states of MLI.

S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	H_1	H_2	H_3	Vo
1	0	1	0	1	0	1	1	1	+13
1	1	1	0	1	0	0	1	1	+12
0	1	1	0	1	0	-1	1	1	+11
1	0	1	1	1	0	1	0	1	+10
0	0	0	0	1	0	0	0	1	+9
0	1	0	0	1	0	-1	0	1	+8
1	0	0	1	1	0	1	-1	1	+7
0	0	0	1	1	0	0	-1	1	+6
0	1	0	1	1	0	-1	-1	1	+5
1	0	1	0	0	0	1	1	0	+4
0	0	1	0	0	0	0	1	0	+3
0	1	1	0	0	0	-1	1	0	+2
1	0	0	0	0	0	1	0	0	+1
0	0	0	0	0	0	0	0	0	0

Table 1 shows the conduction states for the MLI. H_1, H_2 and H_3 shows the H-bridges across which DC sources are connected. The states of these H-bridges decide the levels of output voltage waveform. Only two switches of each bridge are shown in table, rest of the switches states are complementary e.g., S_{13} and S_{14} are complementary to S_{11} and S_{12}. To attain 27 levels, 12 switches were used. It means $2^{12} = 4096$ combinations can be made in which 64 conduction states are possible for this CHBMLI topology. Rest of 4032 combinations will cause either short circuit or open circuit and no output levels can be produced.

Figure 4 shows the conduction paths for $+13$, -13, $+1$, -1 and $0V$. The rest of conduction paths can be drawn in similar way. The highlighted path with arrow shows the direction of current flow through the load. The positive flow of current through load shows positive voltage level and the reverse flow of current through load shows negative voltage level

IV. SLIDING MODE CONTROL

Sliding mode Control causes the system's state trajectories to move in the direction of a sliding surface. In the direction of the equilibrium point, the states start to slide once they reach the sliding surface. The sliding surface must be selected in accordance with the system. Then a control law is constructed that compels states to move in the direction of the sliding surface. In this research, a SMC is designed to track output current of the inverter. The derivative current i'_d, i'_q can be written as:

$$i'_d = \frac{1}{L}[U_d - V_{gd} - Ri_d + \omega L i_q] \tag{19}$$

$$i'_q = \frac{1}{L}[U_q - V_{gq} - Ri_q - \omega L i_d] \tag{20}$$

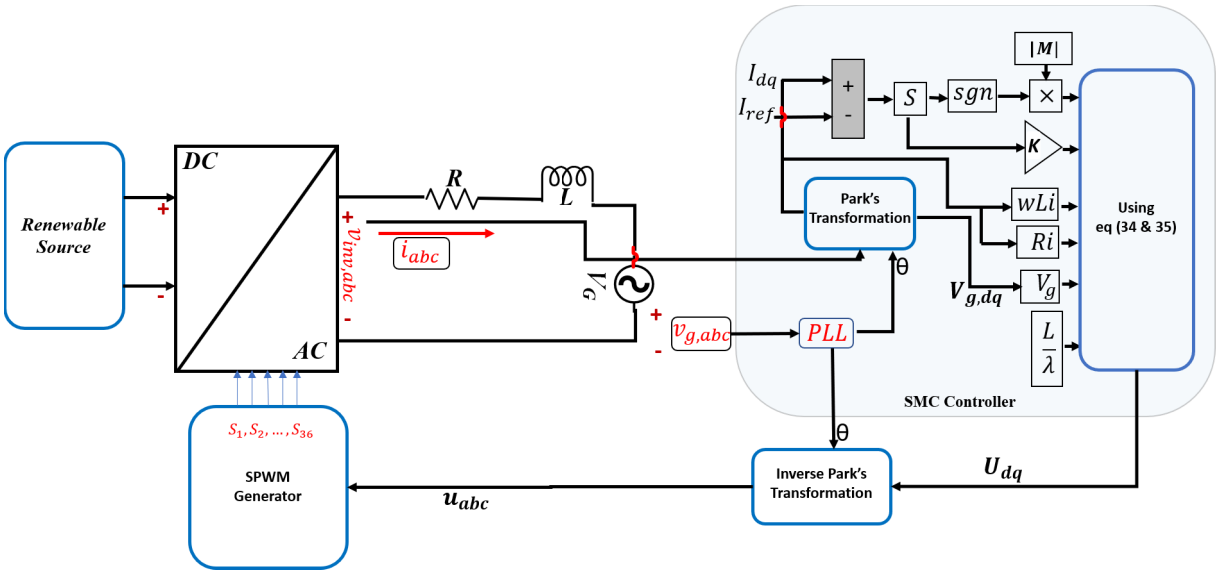

FIGURE 5. Control schematic diagram.

In dq frame of reference, two sliding surfaces are required. S_d represents the sliding surface in d-axis, which controls the direct current and S_q is the sliding surface in q-axis, which controls the current in the q-axis. Similarly, $i_{(d,ref)}$ and $i_{(q,ref)}$ are the reference currents in d and q-axis. The sliding surface is indicated by Eq (21).

$$S = \lambda e \tag{21}$$

where λ is the sliding coefficient and e is the error, which is the difference between reference current and actual current.

$$S_d = \lambda(i_d - i_{d,ref}) \tag{22}$$
$$S_q = \lambda(i_q - i_{q,ref}) \tag{23}$$

The control law should satisfy the condition where S'_d and S'_q should be equal to zero.

$$S'_d = \lambda i'_d = 0 \tag{24}$$
$$S'_q = \lambda i'_q = 0 \tag{25}$$

By putting values of Eq (19,20) in Eq (24,25), S'_d and S'_q becomes

$$S'_d = \frac{\lambda}{L}[U_d - V_{gd} - Ri_d + \omega Li_q] \tag{26}$$
$$S'_q = \frac{\lambda}{L}[U_q - V_{gq} - Ri_q - \omega Li_d] \tag{27}$$

The stability and reachability criteria can be achieved by following conditions:

$$S_d S'_d < 0 \tag{28}$$
$$S_q S'_q < 0 \tag{29}$$

It can be written in term of function as

$$S_d S'_d = S_d(-K_d S_d - M_d sgn(S_d)) < 0 \tag{30}$$
$$S_q S'_q = S_q(-K_q S_q - M_q sgn(S_q)) < 0 \tag{31}$$

$-KS - Msgn(S)$ is the reaching law equation proposed by Sreekumar and Jiji [33]. This law presume that operations will occur in three modes i.e., reaching, sliding and steady state mode, beginning at any moment within a finite period of time. To reduce chattering effect, K should be greater than M. Furthermore, M_d, M_q, K_d and K_q are the control variables and the following conditions can be applied on these variables to prove stability and reachability criteria.

$$-K_{dq}|S_{dq}| - M_{dq} < 0 \tag{32}$$
$$K_{dq}|S_{dq}| + M_{dq} < 0 \tag{33}$$

$M_d > 0, M_q > 0, K_d > 0, K_q > 0$

The selection of the values for control parameters is one of the important tasks because higher values cause the chattering problem as well as it reduces the dynamic response. On the other hand, smaller values cause the problems related to the convergence of the controller. So, tradeoff between the values has to be made By rearranging Eq (26,27), the equations for control law will be derived as:

$$U_d = \frac{L}{\lambda} \times (-K_d S_d - M_d sgn(S_d)) + V_{gd} + Ri_d - \omega Li_q \tag{34}$$

$$U_q = \frac{L}{\lambda} \times (-K_q S_q - M_q sgn(S_q)) + V_{gq} + Ri_q + \omega Li_d \tag{35}$$

U_d represents the control law for d-axis and U_q represents the control law for q-axis as shown in Figure 5.

V. RESULTS AND DISCUSSION

The output of each individual H-bridge is shown in Figure 6. The Bridge 1 has lower voltage of 23 V and high switching rate. The bridge 2 has higher DC voltage of 69 V and comparatively low switching rate. Finally, the bridge 3 has higher

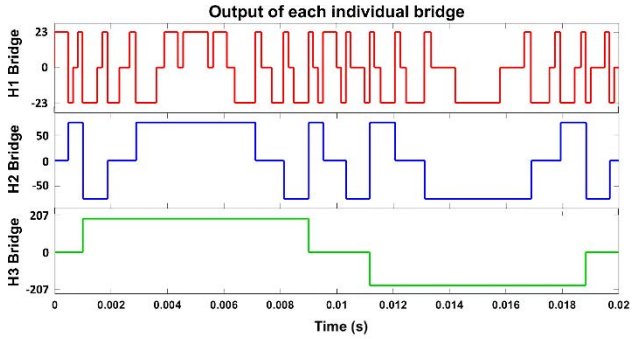

FIGURE 6. Output of each individual bridge.

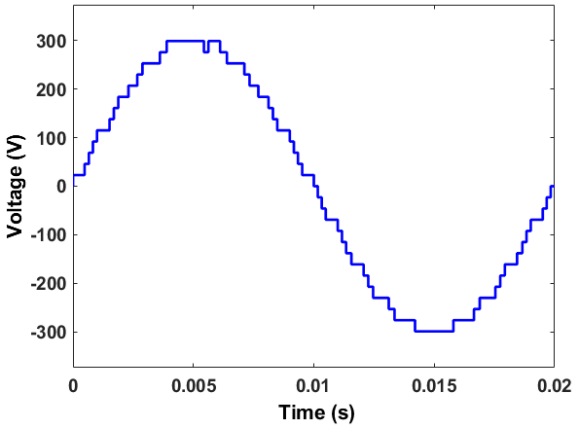

FIGURE 7. 27 level inverter output waveform.

DC voltage of 207 V and lowest switching rate among all the bridges. At higher voltages, higher switching rate causes more losses. So, in this topology the switching rate of higher voltage bridge is low and vice versa.

There is tradeoff between switching rate and voltage of the bridge. This is the advantage of this topology and also the digital logic design (DLD) logics plays a vital role in order to reduce the number of switching gate signal as well as the losses of overall the inverter topology.

Figure 7 shows the output voltage of trinary inverter for phase A, which is the summation of three individual H-bridges. It can be seen that total output levels are 27 and output voltage is 300 V which is the sum of individual DC voltages.

In order to check the performance of proposed SMC, the comparison was made between conventional PI controller and SMC.The PI controller was designed in Matlab/Simulink and it is used to control the output current of CHB MLI. The transfer function of the grid connected system was derived based on the values of the line resistance and line inductance as shown in Eq (36). By using this transfer function, the tuning of PI controller was done in Matlab/Simulink. In our research work, the value of K_p and K_i are 0.208 and 104.28 respectively.

$$H(s) = \frac{1}{0.0012s + 0.2} \tag{36}$$

TABLE 2. System parameters.

Symbol	Description	Value
S_f	Switching Frequency	1 kHz
V_{grid}	Rms Value	176V
K_d	d-axis 1st Parameter	2500
K_q	q-axis 1st Parameter	6500
M_d, M_q	d-axis & q-axis 2nd Parameter	0.0001
λ	d-axis & q-axis 3rd Parameter	0.1
K_p	Proportional gain	0.208
K_q	Integral gain	104.28

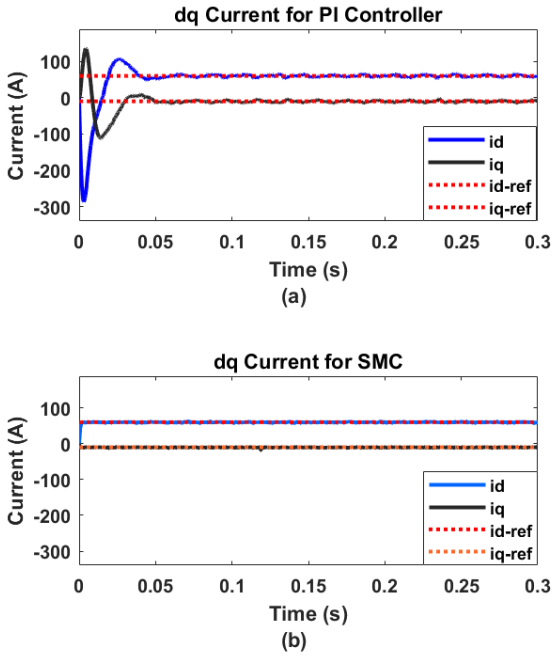

FIGURE 8. Output current under NGO (a) dq Current for PI controller (b) dq current for SMC.

Table 2 represents the design variables for PI controller and SMC. Simulation results are based on it. For SMC, it was observed that steady state error and chattering effect decreases for large values of K_d and K_q. The percentage overshoot is small for large values of λ. On the other hand, large value of M_d and M_q gives small percentage overshoot but high-rise time. So, trade-off has to be made between different control design parameters to achieve best results.

The controller results were obtained for different operating conditions by using the design control parameters as shown in Table 2. Different operating conditions include normal grid operations (NGO) in which grid voltage contains no harmonics. Also, step response is added for variations in currents under NGO. At abnormal grid operations (AGO), 5% of 3rd,5th and 7th order harmonics are injected at grid voltage. Further, 20 % of sag and swell are also introduce at grid level in order to investigate the behavior of controllers.

Figure 8 shows inverter current response under NGO. Figure 8(a) shows the dq current for PI and 8(b) shows the response of current for SMC controller. By analyzing the

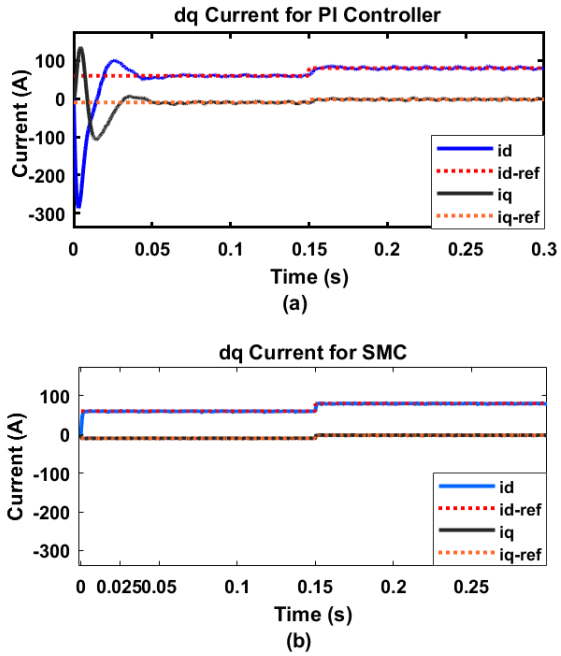

FIGURE 9. Variation in output reference current under NGO (a) dq current for PI controller (b) dq current for SMC.

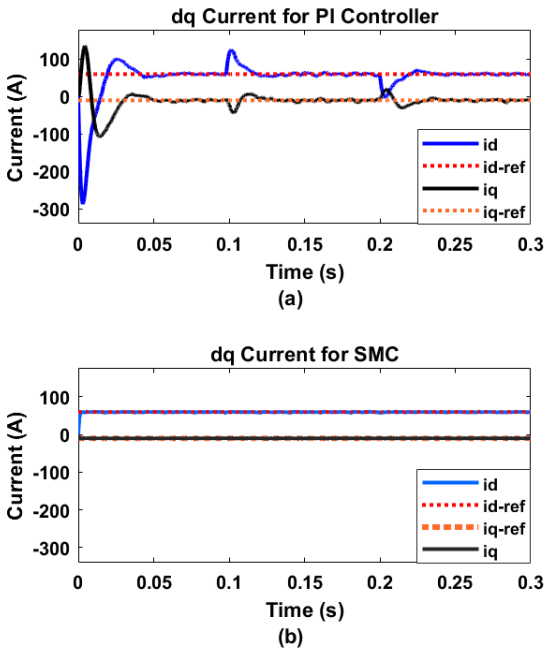

FIGURE 11. Output current under sag condition (a) dq current for PI controller (b) dq current for SMC.

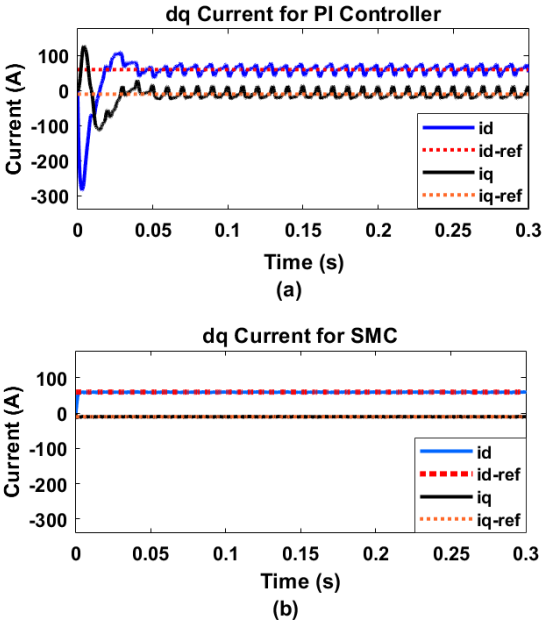

FIGURE 10. Output current under AGO (a) dq current for PI controller (b) dq current for SMC.

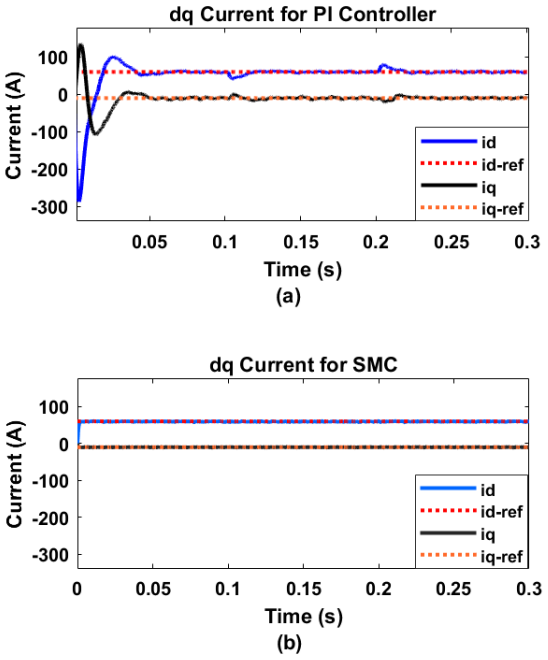

FIGURE 12. Output current under swell condition (a) dq current for PI controller (b) dq current for SMC.

simulation results for PI under NGO, the rise time and percentage overshoot for current I_d are observed to be 12.02ms and 13.06% respectively, whereas the fall time and percentage undershoot for current I_q is 2.72ms and 75.45%. The settling time of 60ms has been recorded. For SMC controller, It is observed that the rise time and percentage overshoot for current I_d is 1.16ms and 3.62% whereas the fall time and percentage undershoot for current I_q is 0.3ms and 24.37% respectively. The settling time of 5ms has been recorded.

Figure 9 shows the result for variation in output currents at NGO condition. The variation in reference current is made by applying step input at 0.15s. It can be observed in figure 9(a) that the rise and fall time of the I_d and I_q is 12.1ms and 2.75ms. An overshoot of 13.06% and undershoot of 74% is

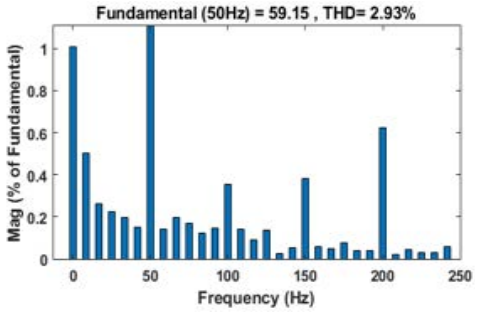

FIGURE 13. THD of inverter current using SMC under NGO.

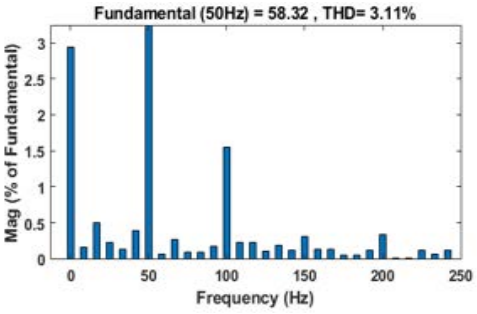

FIGURE 14. THD of inverter current using SMC Under AGO.

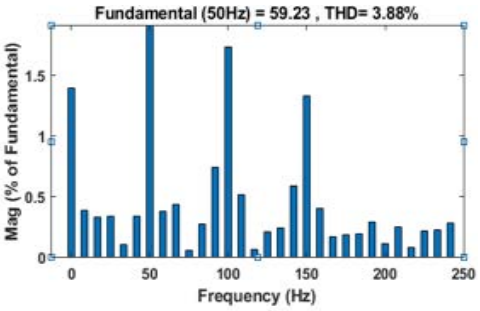

FIGURE 15. THD of inverter current using PI controller under NGO.

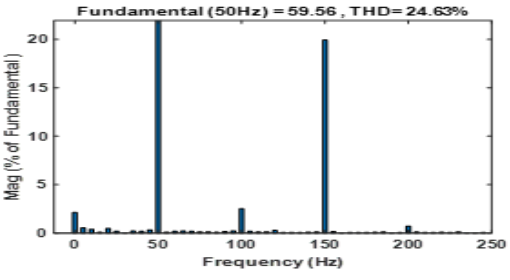

FIGURE 16. THD of inverter current using PI controller under AGO.

observed for I_d and I_q for PI controller. Figure 9(b) shows the current response for SMC controller where rise and fall time of current I_d and I_q is 1.15ms and 0.3ms.An overshoot of 3.6% and undershoot of 24.4% is observed.

Figure 10 shows the results for output currents at AGO condition. Figure 10(a) indicates the effect of current

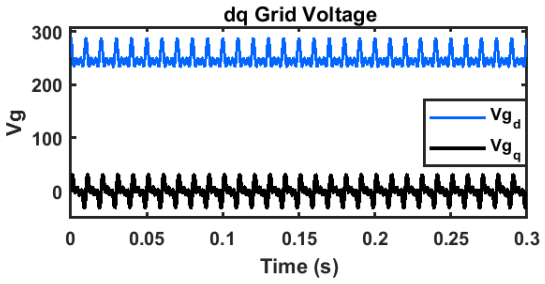

FIGURE 17. Grid voltages under AGO.

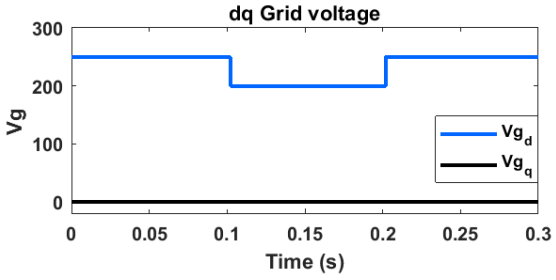

FIGURE 18. Grid voltages during sag.

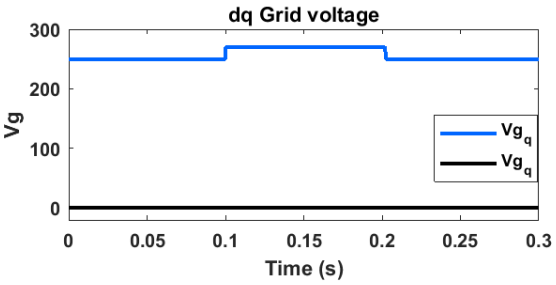

FIGURE 19. Grid voltages during swell.

during PI controller and 10(b) indicates the output current for SMC controller. For PI controller, It is observed that the rise time and percentage overshoot for current I_d is 11.89ms and 14.36% whereas the fall time and percentage undershoot for current I_q is 1.14ms and 24.74% respectively. The settling time of 19.154ms has been recorded. For SMC, the rise time and percentage overshoot for current I_d is 1.126ms and 1.91% whereas the fall time and percentage undershoot for current I_q is 0.290ms and 40.14% respectively.

Figure 11 shows the results for sag condition at grid level. Figure 11(a) indicates the effects on output current during sag for PI controller. Figure 11(b) shows the effects during SMC controller. It is observed that the rise time and fall time of the currents I_d and I_q is 11.66ms and 1.99ms under PI controller. An overshoot of 13.11% and undershoot of 134.79% is observed for I_d and I_q. On the other hand, for SMC controller the rise and fall time of the I_d and I_q is 1.044ms and 0.56ms. An overshoot of 0.115% and undershoot of 45.84% is observed for I_d and I_q. The transients can be observed at the time when sag is introduced at grid for PI controller. But

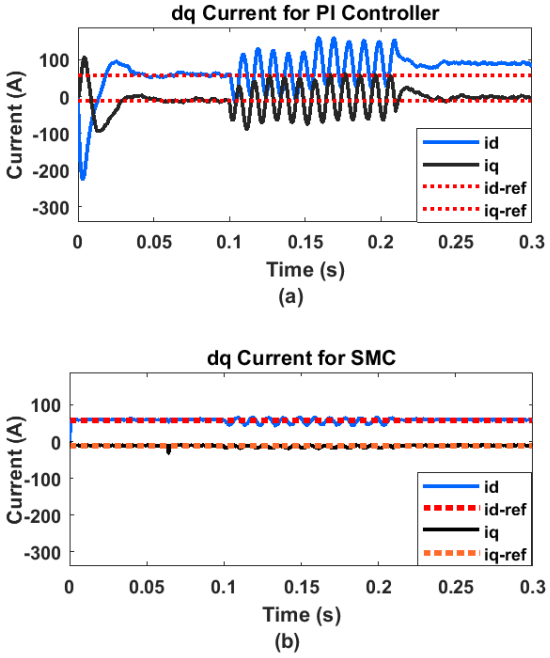

FIGURE 20. Single phase to ground fault with 1Ω short circuit resistance, (a) dq current for PI controller (b) dq current for SMC.

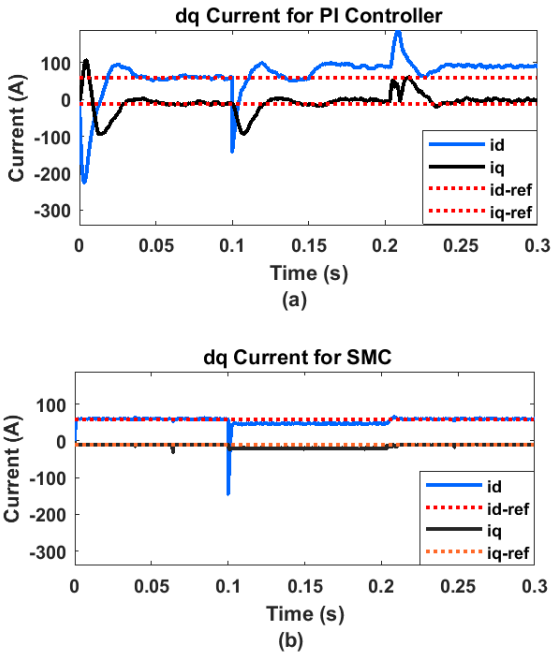

FIGURE 22. Three phase to ground fault with 1Ω short circuit resistance, (a) dq current for PI controller (b) dq current for SMC.

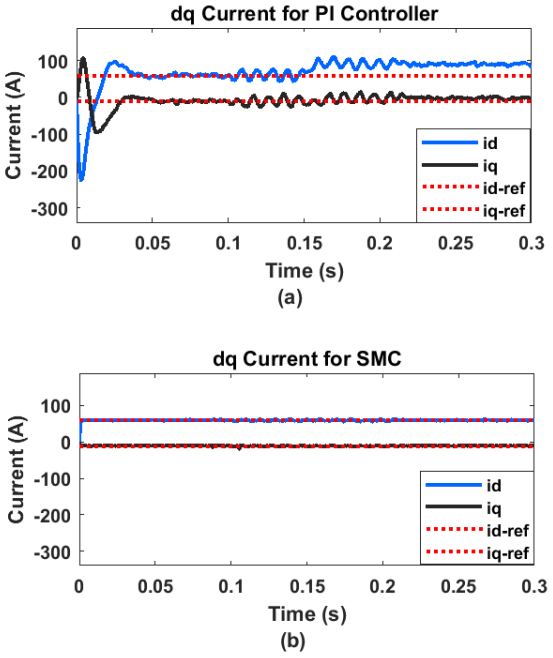

FIGURE 21. Single phase to ground fault with 5Ω short circuit resistance, (a) dq current for PI controller (b) dq current for SMC.

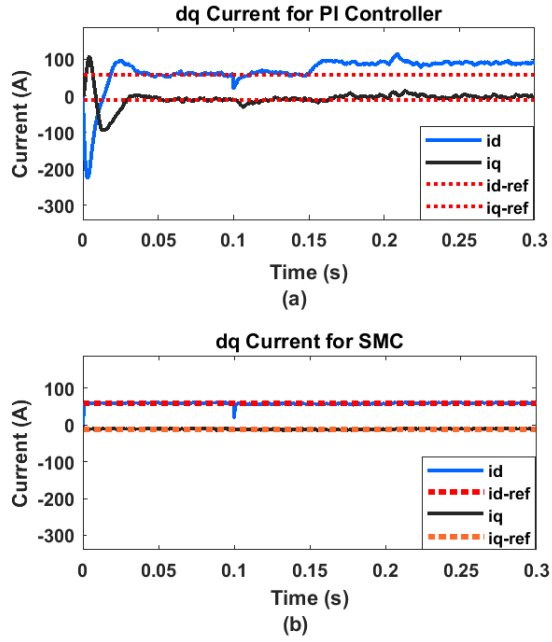

FIGURE 23. Three phase to ground fault with 5Ω short circuit resistance, (a) dq current for PI controller (b) dq current for SMC.

in case of SMC there are no transients and it is more robust as compared to PI controller.

Figure 12 shows the results for sag condition at grid level. Figure 12(a) indicates the effects on output current during sag for PI controller. Figure 12(b) shows the effects during SMC controller. It is observed that the rise time and fall time of the currents I_d and I_q is 12.02ms and 2.72ms under PI controller. An overshoot of 13.66% and undershoot of 7.089% is observed for I_d and I_q. On the other hand, for SMC controller, the rise and fall time of the I_d and I_q is 1.088ms and 0.183ms. An overshoot of 0.780% and undershoot of 4.93% is observed for I_d and I_q.

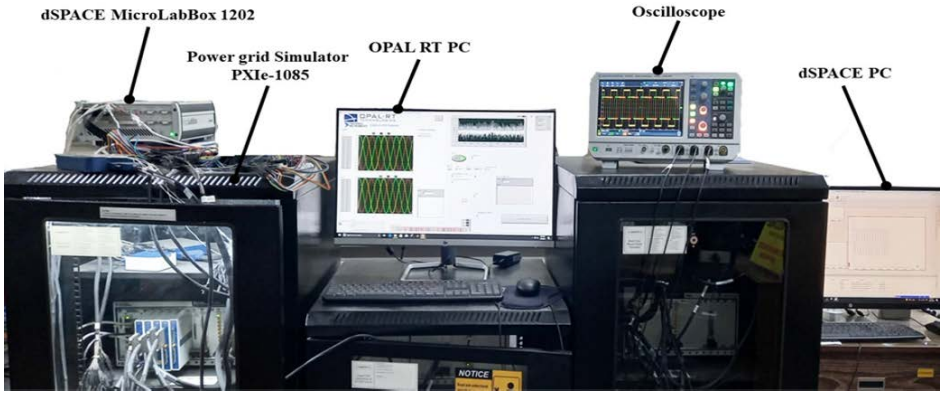

FIGURE 24. HIL setup consisting OPALRT, power grid simulator PXIe-1085 and dSPACE 1202 MicroLabBox.

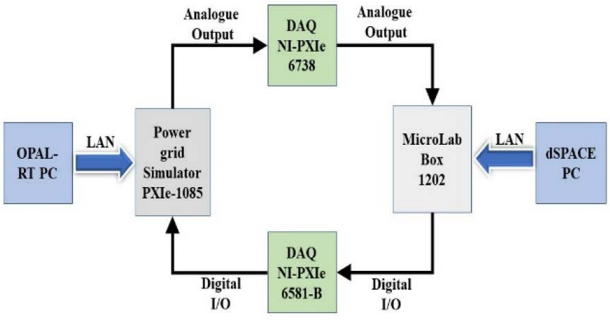

FIGURE 25. Block diagram of HIL based system.

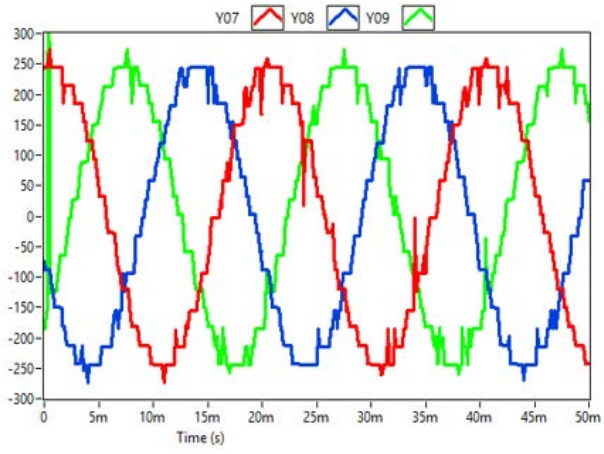

FIGURE 26. Open loop three phase inverter output voltage on OPALRT front panel.

Figure 13 shows THD under NGO for SMC controller, which is 2.93%. Figure 14 shows THD under AGO for SMC controller, which is 3.11%. It is observed that THD is less than 5%, which is acceptable according to IEEE-63547 standard.

Figure 15 shows THD under NGO for PI controller, which is 3.88%. Figure 16 shows THD under AGO for PI controller, which is 24.63%. it is observed that during AGO, the THD is quite high and it is not acceptable according to IEEE standards.

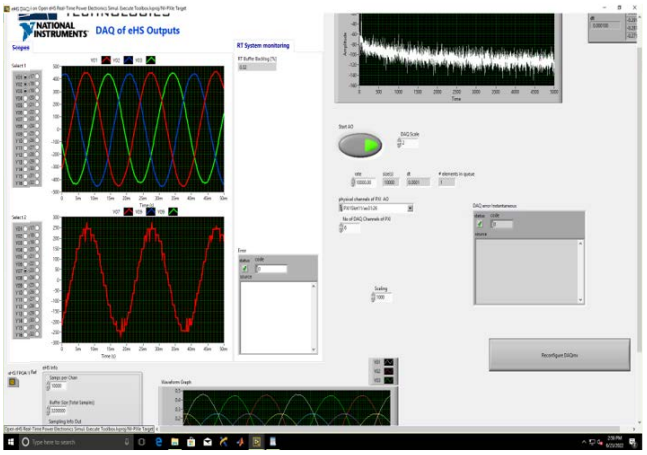

FIGURE 27. Closed loop three phase inverter output current for SMC with three phase inverter output voltage on OPALRT front panel.

Figure 17 shows the grid voltages under AGO. Figure 18 and 19 shows the grid voltages during sag and swell in the grid. It can be clearly seen that the abnormalities are introduced in grid for 0.1s i.e., from 0.1s to 0.2s.

The behavior of both the controllers were also investigated under grid faults conditions. The single-phase and three-phase short circuit faults were introduced between 0.1 and 0.2s. Both single and three phase short circuit faults were analyzed for two different resistance values i.e., 1Ω and 5Ω. Figure 20 shows the single phase short circuit fault for 1Ω resistance.The rise time and fall time of current I_d and I_q is 12ms and 2.5ms for PI controller. An overshoot of 25% and undershoot of 1.21% is observed. In case of SMC controller, the rise time and fall time for current I_d and I_q is 0.84ms and 1.77ms. The overshoot is 1.90% and undershoot is 16.39 %.Figure 21 indicates the single phase short circuit fault with 5Ω resistance. It is observed that the rise time and fall time of the currents I_d and I_q is 9.1ms and 1.21ms under PI controller.An overshoot of 24% is observed and undershoot is almost negligible. On the other hand, for SMC controller, the rise and fall time of the I_d and I_q is 0.94ms and 42.39ms. There is negligible overshoot and undershoot.

TABLE 3. Comparison of parameters for PI and SMC during NGO & AGO.

Parameters	NGO (PI)		NGO (SMC)		AGO (PI)		AGO (SMC)		% Change (NGO)		% Change (AGO)	
	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q
Rise Time/Fall Time	12.02ms	2.72ms	1.16ms	0.3ms	11.89ms	1.14ms	1.126ms	0.290ms	-90.34%	-88.97%	-90.52%	-74.96%
Overshoot/Undershoot	13.06%	75.45%	3.62%	24.37%	14.36%	24.75%	1.91%	40.14%	-72.28%	-67.70%	-86.71%	+38.34%
Settling Time	60ms	72ms	5ms	2ms	71ms	45ms	19.15ms	19.15ms	-91.66%	-97.22%	-73.02%	-57.44%

TABLE 4. Comparison of parameters for PI and SMC during SAG & SWELL.

Parameters	SAG (PI)		SAG (SMC)		SWELL (PI)		SWELL (SMC)		% Change (SAG)		% Change (SWELL)	
	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q
Rise Time/Fall Time	11.66ms	1.99ms	1.04ms	0.56ms	12.02ms	2.72ms	1.08ms	0.18ms	-91.04%	-71.85%	-90.94%	-93.27%
Overshoot/Undershoot	13.11%	134.79%	0.11%	45.84%	13.66%	7.08%	0.78%	4.93%	-99.12%	-65.99%	-94.29%	+30.45%
Settling Time(SAG or SWELL APPLIED)	25ms	35ms	6ms	7ms	16ms	38ms	2ms	8ms	-76%	-80%	-87.5%	-78.94%
Settling Time(SAG or SWELL REMOVED)	40ms	37ms	5ms	4ms	14ms	30ms	5ms	4ms	-87.50%	-89.18%	-64.28%	-86.66%

TABLE 5. Comparison of parameters for PI and SMC during single phase fault.

Parameters	R=1Ω (PI)		R=1Ω (SMC)		R=5Ω (PI)		R=5Ω (SMC)		% Change (R=1Ω)		% Change (R=5Ω)	
	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q
Rise Time/Fall Time	12ms	2.5ms	0.84ms	1.77ms	9.1ms	1.21ms	0.94ms	42.39ms	-93%	-29.2%	-89.59%	+97.13%
Overshoot/Undershoot	25%	1.21%	1.90%	16.39%	24%	0.73%	0.87%	9.03%	-92.37%	+92.62%	-96.37%	+91.92%
Settling Time(FAULT APPLIED)	16.20ms	33.49ms	13.70ms	15.90ms	15.41ms	41.82ms	14.98ms	11.66ms	-15.43%	-52.52%	-2.72%	-72.24%
Settling Time(FAULT REMOVED)	54.60ms	39.90ms	23.85ms	21.83ms	60.59ms	28.35ms	41.50ms	35.61ms	-56.41%	-45.28%	-31.50%	+20.30%

TABLE 6. Comparison of parameters for PI and SMC during three phase fault.

Parameters	R=1Ω (PI)		R=1Ω (SMC)		R=5Ω (PI)		R=5Ω (SMC)		% Change (R=1Ω)		% Change (R=5Ω)	
	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q	I_d	I_q
Rise Time/Fall Time	8.21ms	2.84ms	2.06ms	0.38ms	9.36ms	2.94ms	0.95ms	0.28ms	-74.09%	-86.54%	-89.82%	-90.34%
Overshoot/Undershoot	22.96%	0.32%	3.20%	21.05%	23%	77.23%	0.82%	-42.95%	-86.03%	+98.48%	-96.42%	+91.92%
Settling Time(FAULT APPLIED)	55.05ms	45.44ms	13.52ms	4.52ms	55.47ms	33.64ms	14.14ms	8.19ms	-75.45%	-90.04%	-74.50%	-75.62%
Settling Time(FAULT REMOVED)	57.6ms	53.77ms	21.47ms	27.39ms	31.15ms	35.42ms	20.6ms	17.80ms	-62.84%	-49.16%	-33.86%	-49.74%

Figure 22 and 23 shows the behavior of currents for three phase fault. Figure 22 shows the three phase short circuit fault with 1Ω short circuit resistance. The rise time and fall time of current I_d and I_q is 8.21ms and 2.84ms for PI controller. An overshoot of 22.6% and undershoot of 0.32% is observed for PI controller. For SMC controller, the rise time and fall time for current I_d and I_q is 2.06ms and 0.38ms. The overshoot and undershoot is 3.205% and 40.05%. Figure 23 indicates the three phase short circuit fault for 5Ω resistance. It is observed that the rise time and fall time of the currents I_d and I_q is 9.36ms and 2.94ms during PI controller.An overshoot of 23% and undershoot of 77.23% is observed. On the other hand, for SMC controller, the rise and fall time of the I_d and I_q is 0.952ms and 0.284ms. There is negligible overshoot and undershoot.

It is noted that when fault is introduced, the actual current path is started to deviate from the reference point. The single-phase fault is more severe as compared to three phase but in both cases the SMC shows better disturbance rejection as compared to PI controller. In addition to this, the output current quickly approached the reference current by using SMC. On the other hand, the output current became unstable by using PI controller after the introduction of fault.

Table 3 to 6 shows the quantitative analysis of PI and SMC during NGO, AGO, SAG, SWELL and short circuit fault conditions. The rise time, overshoot, settling time, THD etc. performance of SMC is better than PI which shows the robustness of controller. The percentage decrease in parameters of SMC as compare to PI were also mentioned in tables.

The experimental hardware in loop (HIL) based setup was established for three phase 27 level in order to validate the results of the proposed SMC as shown in Figure 24. The OPAL RT HIL system based on LABVIEW FPGA was used in which topology of inverter was implemented. The NI based real time power grid simulator PXIe-1085 was integrated with OPAL RT. On the other side, the dSPACE 1202 was used as a controller in which SMC was implemented in dSPACE control Desk application. The data from dSPACE was fed into OPAL RT through NI PXIe- 6581B. The output data from inverter was fed into dSPACE through NI PXIe-6738 forming closed loop. The CHB topology is simulated at a time step of 395ns using the PXIe-1085 real-time power grid simulator. The DC voltages across H-bridge were same as used for

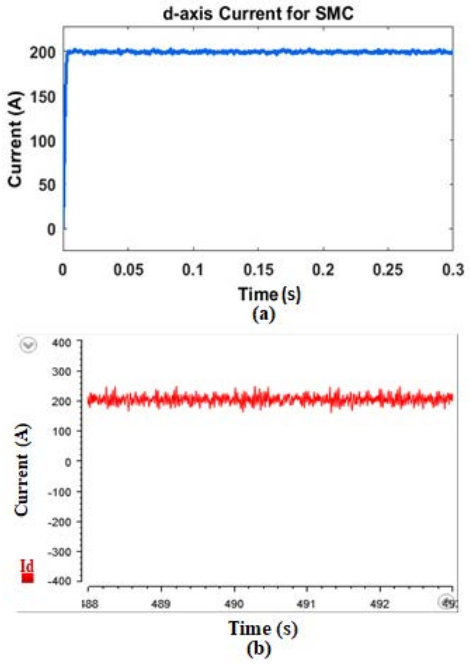

FIGURE 28. dSPACE output current for SMC (a) Simulated d-axis current, $I_d = 200$A (b) Experimental result, $I_d = 200$A.

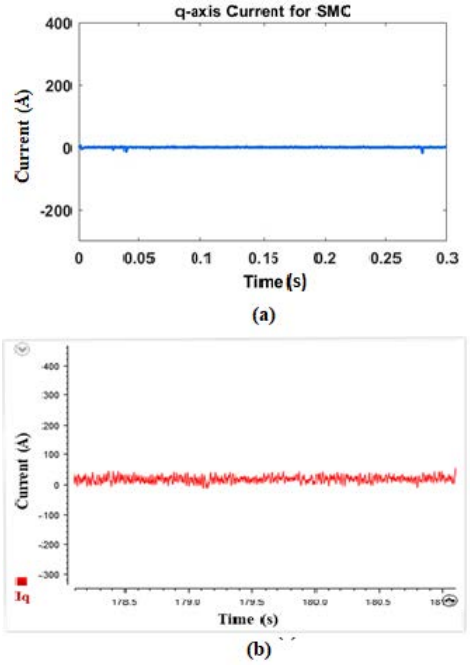

FIGURE 29. dSPACE output current for SMC (a) Simulated d-axis current, $I_q = 0$A (b) Experimental result, $I_q = 0$A.

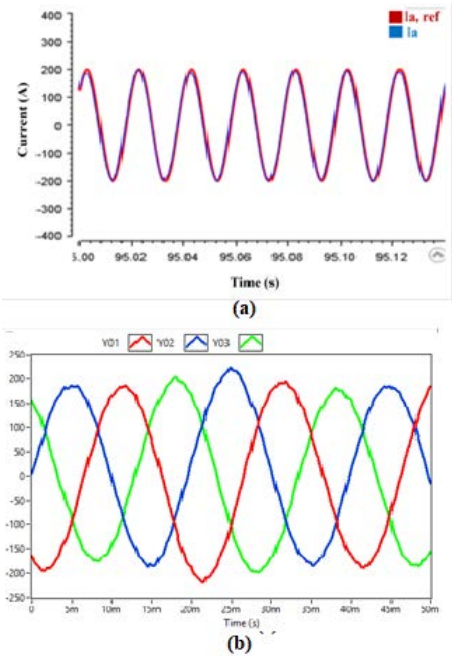

FIGURE 30. HIL based current result for 200A under SMC (a) Phase A inverter output current (dSPACE Result), (b) Three phase inverter output current (OPAL RT result).

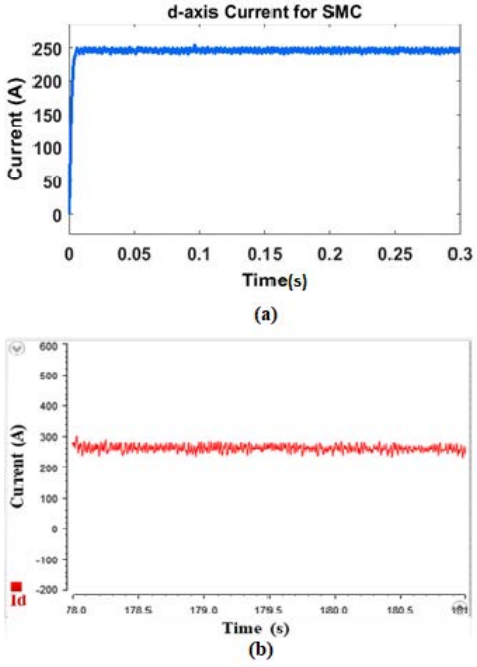

FIGURE 31. dSPACE output current for SMC (a) Simulated d-axis current, $I_d = 250$A (b) Experimental result, $I_d = 250$A.

simulations i.e, $V_{DC1} = 23$V, $V_{DC2} = 69$V and $V_{DC3} = 207$V and the switching frequency used was 1 kHz.

Figure 26 displays the OPAL-RT front panel showing the open loop three phase inverter voltage obtained by using the SPWM technique on dspace-1202. Similarly, Figure 27 shows the closed loop three-phase output current. The current response of the inverter when SMC- based closed loop controller is used on dspace-1202 with a 0.0001s time-step is shown in Figures 32 and 33.

Figure 28 and 29 display the results for direct and indirect currents with reference of 200A and 0A. Figure 28(a) shows the simulated result of Matlab and Figure 28(b) displays the result generated by dSPACE control desk.

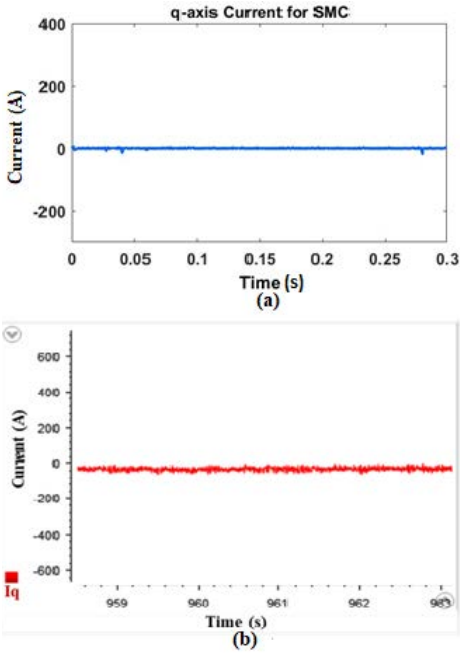

FIGURE 32. dSPACE output current for SMC (a) Simulated d-axis current, $I_q = 0$A (b) Experimental result, $I_q = 0$A.

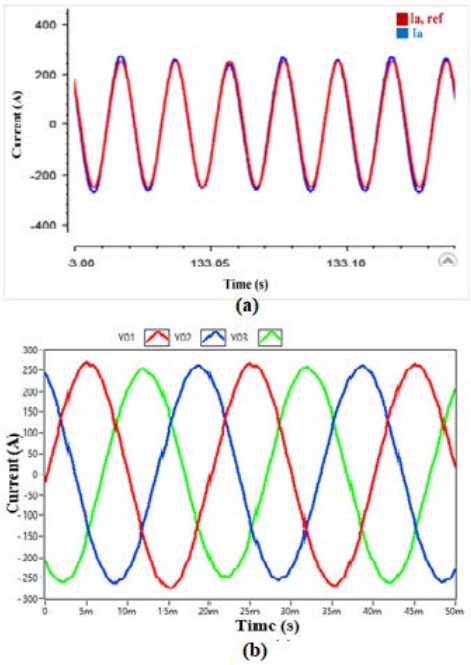

FIGURE 33. HIL based current result for 250A under SMC (a) Phase A inverter output current (dSPACE result), (b) Three phase inverter output current (OPAL RT result).

Similarly, Figure 29 shows the result for I_q which is zero. Figure 30 explains the HIL based result for 200A under NGO of SMC. Figure 30(a) shows the experimental result for phase A Inverter output Current. Figure 30(b) displays the OPAL-RT result. This result was obtained from OPAL

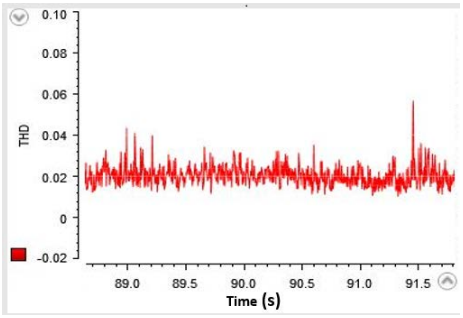

FIGURE 34. HIL current THD waveform for SMC under NGO.

RT in which measurement blocks are used. In similar way, Figure 31,32 and 33 shows the result for 250A direct current with 0A indirect current. Figure 34 shows the THD of current waveform. The Y-axis represents the percentage THD in fraction which is less than 5 percent. Both OPAL RT and dSPACE shows the same current, which validates the control feasibility and effectiveness.

VI. CONCLUSION

In this paper, trinary cascaded H-bridge topology is used to design a filter less inverter. The benefit of this topology is that it can generate maximum level of outputs with using a smaller number of switches and less switching losses occurs. The PWM technique is designed by using logic sum operations. This topology also ensures less THD approximately less than 5%, which is acceptable according to IEEE standards. This article has also discussed the Sliding mode control (SMC) implemented on the 27 level Multilevel Inverter. Moreover, the SMC implemented on MLI is compared with PI controller. The current based SMC is implemented in order to control the current of grid connected 27 level cascaded MLI as renewable energy interfaced to grid. Different operating conditions have been implemented in which Sag, Swell, short circuit faults and Harmonics are introduced at grid level. The controller shows different behavior under different operating conditions. The results shows that SMC injects very low THD currents to the grid as compared to conventional PI control technique. By using SMC, the output current response has less settling time, overshoot and it follows the reference current with negligible steady state error. The SMC shows better disturbance rejection under AGO as compared to PI controller. Moreover, its dynamic response is faster than PI controller. The experimental results verify the better dynamic performance of SMC technique, which shows better response against any external perturbations.

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