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Low Power Multi-Channel Interface for Charge Based Tactile Sensors

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LOW POWER MULTI-CHANNEL INTERFACE FOR CHARGE BASED TACTILE SENSORS

by

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Analog front end electronics are designed in 65 nm CMOS technology to process charge pulses arriving from a tactile sensor array. This is accomplished through the use of charge sensitive amplifiers and discrete time filters with tunable clock signals located in each of the analog front ends. Sensors were emulated using Gaussian pulses during simulation. The digital side of the system uses SAR (successive approximation register) ADCs for sampling of the processed sensor signals.

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Chapter 1

Introduction

This thesis encompasses the design and verification of a analog mixed signal chip designed in a 65 nm CMOS technology that is able to process signals from an E-skin (electronic skin) sensor array. To better understand the design decisions made for this SoC (system on a chip) background will be provided on the applications, typical sensor materials, and state of research. The subsequent sections detailing the design are divided up into the system overview, analog and digital design process, verification and layout, and conclusion.

1.1 Motivation

The motivation for this thesis is to design a low power, low noise, analog front end to process the charge pulses arriving from a piezoelectric taxel array. By integrating as much of the analog and digital circuits onto a single chip, die power and area can be reduced by several orders of magnitude compared to existing solutions. This would make the electronics low power enough and small enough to be used in robotic prostheses without requiring significant resources to power. The reduction in size and power would mean less weight for the user to carry on their person without compromising functionality of the prosthesis. E-skin research has yielded advances

in the material design and sensing capabilities of the device itself, but the electronics necessary to interface with these sensors is still a developing area.

Long term impacts of E-skin development could enable applications of robotic prostheses in the medical field. It would make it easier for patients to learn how to use their prosthetic limbs as they would have a sense of touch again. Robotic limbs could be controlled without line of sight or invasive surgery to sense the biological signals and done through sensing of the surface of the skin. In order to realize these advances small and low power interfaces are needed.

1.2 Electronic Skin

The sensor array can be described as a flexible material containing sensors/transducers which provide tactile information. Because of these qualities the arrays are treated as an electronic equivalent to skin, or E-skin. Each sensor in a E-skin sensor array is commonly referred to as a taxel (tactile pixel). The output of each taxel corresponds to the force applied to it and generates a signal across two leads as an output. In addition, taxels operate independent of their neighbors which can be leveraged to gain localized information from the array. E-skin arrays can be wired such that one lead on a taxel is a row and the other is a column (see Figure 2.2). Other wiring methods for E-skin use a interface per taxel rather than per row or column. By measuring the output of each row and column location and intensity can be determined. By increasing the resolution of sensors on the E-skin array more information can be taken from the area such as the geometry of contact area, force distribution, and temperature.

To maintain a high spatial resolution taxels are kept small and packed tightly together. Researchers want to keep taxel resolution high as it provides more information to the system while keeping the physical size of the sensor small. High taxel

resolution creates a design bottleneck as more channels and subsequently more electronics are needed to process the signals. Standard approaches would require multiple discrete chips to accomodate the high channel counts, but an integrated approach enables a more compact solution. The project proposed in this thesis and other similar integrated circuits have the advantage over discrete solutions as more channels can be added to increase taxel resolution without significant cost to area and power.

1.3 Applications

E-skin has clear applications anywhere tactile information is useful or needed. The first application is in biomedical sensing. Researchers have developed novel ways to acquire biological data from E-skin sensors such as ECG (electrocardiogram), EEG, and electromyogram to name a few [1]. E-skin is currently being investigated for use on prosthetic limbs to provide patients with a form of haptic feedback for their artificial limb(s) [2]. In this application accuracy and speed can be sacrificed in favor of data throughput and minimized power consumption. This is done to maintain a lighter weight and longer operating time for the patient using the E-skin system. This is the primary target application area for the SoC design in this thesis as it benefits the greatest from the high level of integration in this work.

Another potential application area for E-skin is for use in manufacturing and industrial settings. Manufacturing facilities may use E-skin on their robotics to prevent injury to workers by detecting collisions or for handling products on an assembly line without damaging them. This area diverges from the biomedical applications as it favors high speed and accuracy without much consideration for power consumption or physical size of the device.

1.4 Literature Review

The current state of research surrounding electronic skin systems is focused on many different areas. A prominent focus area is the development of high performance sensors that increase resolution and linearity of the array. Research in this area is often done by developing novel methods to fabricate the sensor array, or through the characterization of new materials that yield greater taxel performance. A consequence of increased spatial resolution is the increase in information and need to process it efficiently. This problem space is another area of research that focuses on gesture recognition on E-skin arrays. Researchers look to use compression algorithms, classification algorithms, and digital signal processing to bypass the information bottleneck that exists between the user and the electronics. An emerging focus area in E-skin research to solve the problem of taxel resolution and signal processing is the design ASICs that interface directly with the E-skin array. Researchers seek to accomplish this by offloading much of the signal processing to analog interface circuitry to extract information from the sensors.

Research on the construction of E-skin sensors looks at increasing resolution by simply shrinking the size of the sensor. A typical taxel size for an E-skin array can be anywhere from $1 - 5$mm in diameter like those presented in [3] while new research seeks to reduce the size to tens of micrometers or even nanometers. Other papers like Yang et al. utilize liquid metals like gallium or indium to create novel tactile sensors for signal generation [4]. By using gallium Yang et al. can also fabricate inductors, resistors, capacitors, transistors, diodes, and memristors in the sensor array [4].

Gesture recognition allows the prosthetic to internally compress the large quantity of raw sensor data into a reduced set of corresponding gestures. This is critical since there exists a information bottleneck between the electronics and the user. In practice,

myoelectric interfaces can convey information back to the user but only in a coarse fashion. Processing the data can become a computationally complex task when array resolution is increased and complex gestures need to be classified. To solve this problem researchers have turned to machine learning and classification algorithms. Ibrahim et al. [5] use a fixed point SVD (singular value decomposition) to process and classify the tactile information [5]. Other researchers such as [2, 6, 7, 8] use machine learning techniques to perform gesture recognition. Taube et al. [6] do this with Si-NWs (silicon nano wires) [6] to create a self learning neural network for gesture recognition. Other researchers used more conventional methods to implement and train their neural networks. In the case of Abbass et al. and Franceschi et al. patients were given electric stimulation based on the tactile gesture performed on the E-skin. The correctness of their guesses on the felt gesture were used in a reinforcement learning algorithm to optimize the system [7, 8].

A third area of active research is the development of ASICs for processing the signals coming off sensors and extracting as much information from the signal as possible. This is an emerging area of research, so few dedicated analog front ends are published. Papers like Lee et al. designed and tested a chopper stabilized analog front end in 180nm CMOS technology for use in ECG, PTT, PPG, BP, and FT using a custom in house sensors along with PVDF based sensors [1]. A similar approach to this problem was taken by Schmitz et al. where the analog processing, gesture recognition and digital readout were done on a single SoC fabricated in 130nm CMOS technology [2]. Both implementations remove the need for complex digital signal processing by offloading the task to analog circuitry prior to sampling. Papers such as [5, 7, 8, 9] use FPGAs and discrete components such as the Texas instruments DDC232 [10] for signal processing and gesture recognition which consume large amounts of power. The large power consumption of these systems make them difficult to implement on

robotic prostheses without large batteries. The E-skin solutions such as [6] and [11] are novel and solve many of the design problems facing E-skin systems. However the difficulty of fabricating devices like Si-NWs or gallium integrated circuits on flexible substrates is high and the electronics industry could only make small batches as much of the infrastructure isn't present. This work focuses on more conventional E-skin sensors that can be fabricated in bulk, as the primary focus is the reduction in power consumption and size while maintaining high channel density.

Chapter 2

System Overview

2.1 Sensor Materials and construction

The primary material used in the development of taxel sensors is polyvinylidene fluoride (PVDF) as it exhibits multiple useful sensing applications, including both pressure and heat, making it an appealing sensor. This work will be exclusively on the pressure sensing modality and will not measure the temperature of the E-skin array. In addition to these properties PVDF is also inherently event driven, meaning that no stimulating circuit is needed to measure the applied pressure, reducing power consumption. PVDF sensors are also very easy to fabricate in bulk. These qualities are why PVDF sensors are targeted for use as taxels in this thesis.

Piezoelectricity is a phenomenon where a material generates an electric charge when a force is applied to it. This is caused by a change in the electric dipole moment of the material when stressed. When this occurs a spare electron is emitted from the molecule which generates a charge on the material. If the force is maintained the material's dipole moment will conform to the new geometry and only release charge when returning to its original shape. The pyroelectric property is similar to the piezoelectric property, only the energy needed to change the dipole moment comes from changes in temperature instead of kinetic energy.

PVDF Films can be polled along a target axis to maximize the charge generated per force applied, allowing the sensor's sensitivity to be tuned along a specific axis based on the application's needs. To poll the film, the PVDF is exposed to a large potential difference 3 kV [3] which aligns the domains of the molecules and improves their response to the force along the polling axis. After polling of the PVDF material is complete, practical PVDF sensors are constructed by placing a wafer of PVDF between two conductive plates or conductive paint [3] Figure 2.1. Electrical contact is needed so the charge can be sent to electronics for processing.

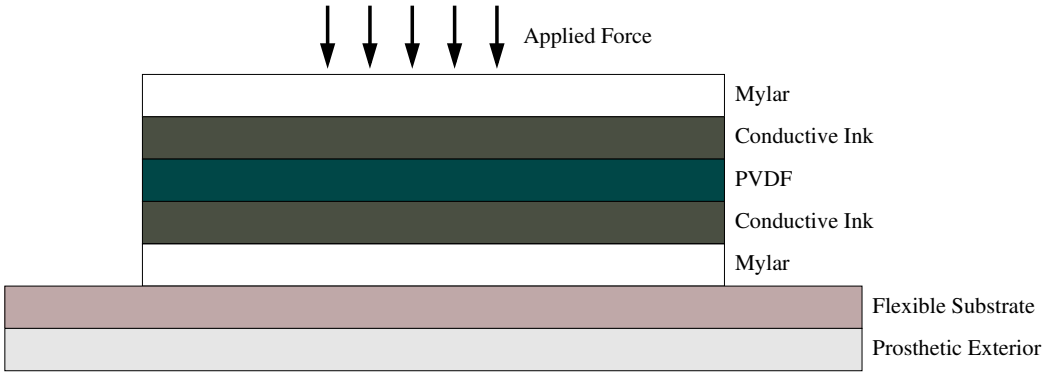


Figure 2.1: Cross section of a PVDF sensor/taxel layers not drawn to scale

2.2 Array Construction

The requirements for E-skin is to be flexible and maintain high spatial resolution. The E-skin array must be flexible to conform to the irregular surfaces of a prosthetic limb. The flexible substrate must also be compressible to allow for taxel deformation as the taxel favors pressure perpendicular to its surface. The high resolution of the E-skin array also requires routing schemes that do not require large quantities of wires or reduce the information that can be gathered. To prevent information loss the analog interface circuitry must handle the positive and negative pulses arriving from the PVDF taxel. On a press one terminal will have an absence of charge and the

nother will have an excess of charge. Once the pressure is removed from the taxel the charge polarity on the terminal is reversed. These signals are needed by the circuitry to determine duration of press.

The construction of the PVDF E-skin sensor arrays is done first by laying PVDF taxels over a flexible substrate. The sensor array constructed for this thesis uses Ecoflex 00-30, which is a common visoelastic silicone material. Common uses for it include orthotics, prostheses, and simulating human tissue for training medical professionals. This makes it a perfect fit for the flexible substrate under the taxel array. The wiring of the taxel array is done by wiring the top part of the taxel to the row and the bottom side to the column. A 4×4 wiring diagram can be seen in Figure 2.2 The advantage of this wiring configuration is that each row and column is

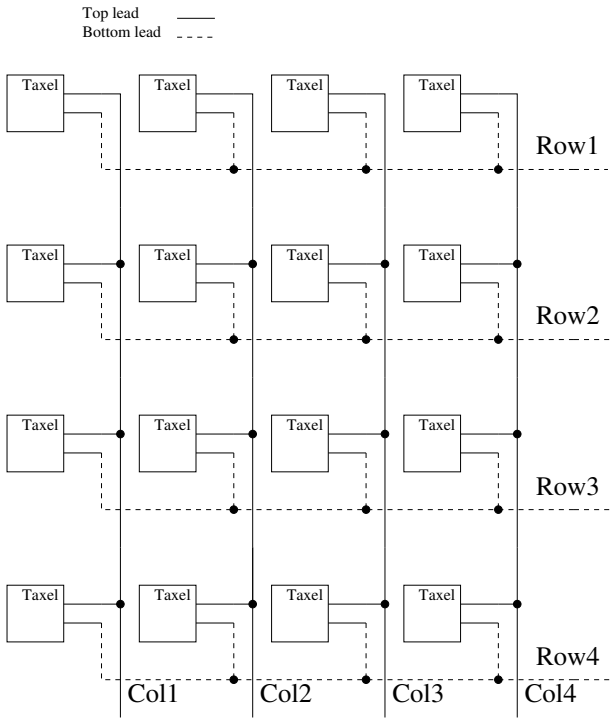


Figure 2.2: 4×4 example of a row/column wiring configuration

connected to a AFE (analog front end) and will process both charge pulse polarities. This makes determining the exact taxel that was stimulated and the duration of

Figure 2.3: Experimental 4×4 row column wired E-skin array

pressure applied straightfoward. Other ways of wiring the array can be done however they do not provide a good balance between wiring overhead and taxel count an example of this can be seen in Figure 2.4. Here two wires are used per taxel instead of a row column scheme. It can be seen from Figure 2.2 and Figure 2.4 that row column wiring scales much better than two wires per taxel.

2.3 Sensor Characterization

Piezoelectric sensors are typically used as vibration sensors or thermal sensors which provide a continuous signal and make constant contact with a surface. Literature on the use of PVDF sensors as charge pulse based sensors is sparse. We made use of a commercially availible sensor sold by TE connectivity and characterized it for

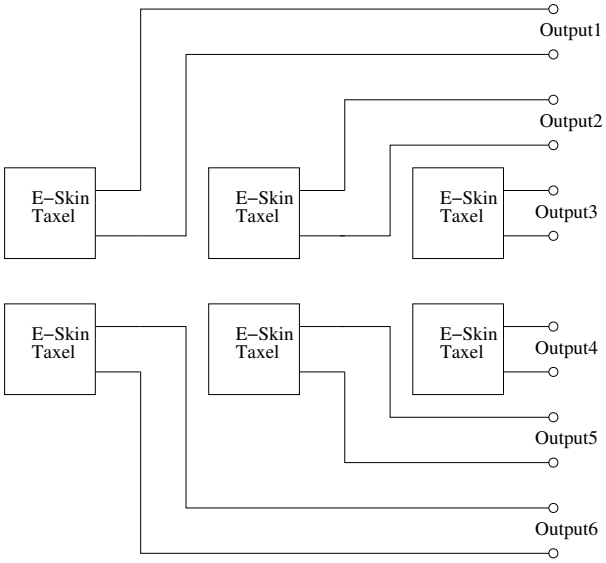


Figure 2.4: 2×3 E-skin routing using 2 terminals per taxel

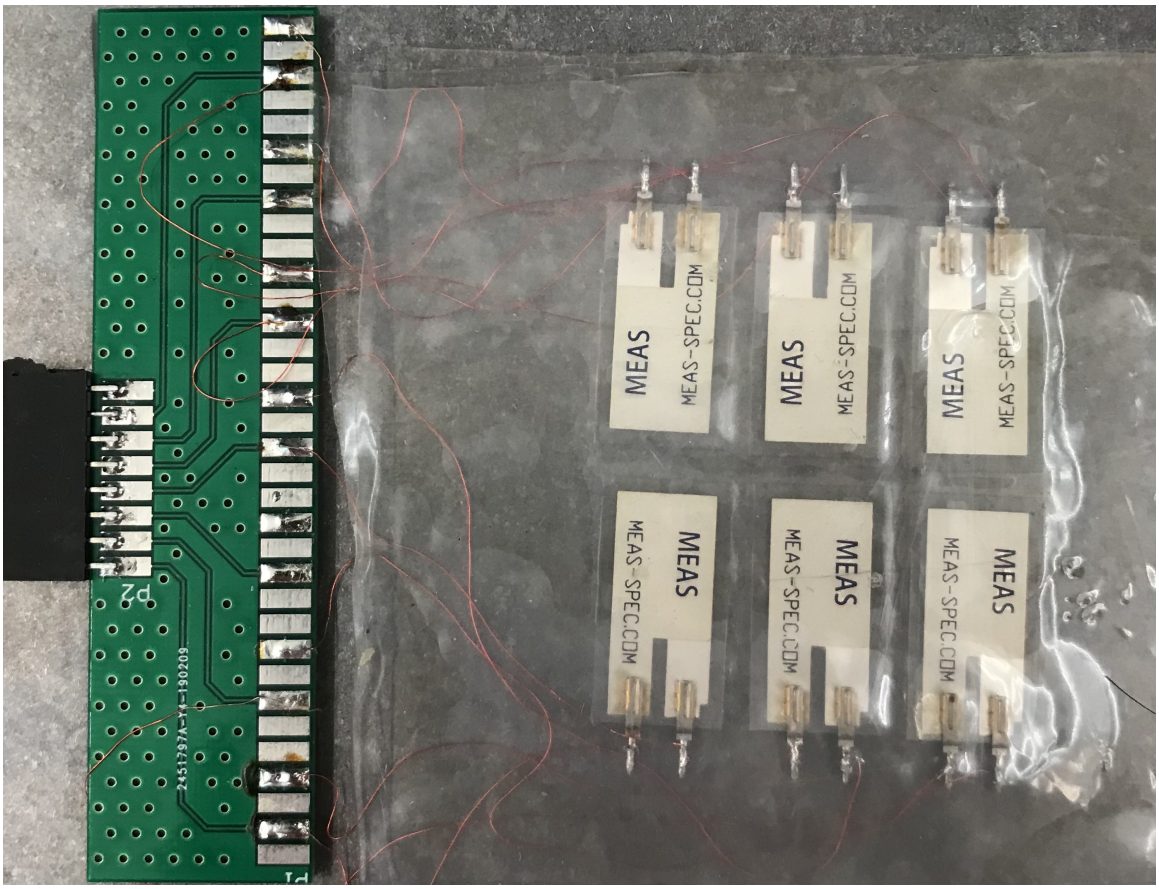


Figure 2.5: Experimental 2×3 independent E-skin array

pulse generation. To characterize the charge pulse coming off the PVDF sensor, a test rig was made with discrete components comprised of a simple op amp CSA (see appendix), a 4x4 taxel array, and a MSP430 Texas instruments microcontroller. The test board can be seen in Figure 2.6. Much of the characterization was done by applying varying amounts of force, using different materials, and changing contact duration to the piezo sensor over time . The results of the testing indicate that contact area, impulse, applied force, elasticity of substrate, elasticity of contacting material, and device polling all have an effect on the output charge of the PVDF sensor. Variables such as impulse will change the duration of the charge while the elasticity of the materials may add high frequency components to the charge pulse, and polling along multiple axis will introduce nonlinear distortion in the charge pulse. A CSA interfacing with the taxel would need to integrate across multiple low frequency time constants much larger than what a discrete CSA could provide without a significant increase in size and component count. Due to the complexity of the sensor exact

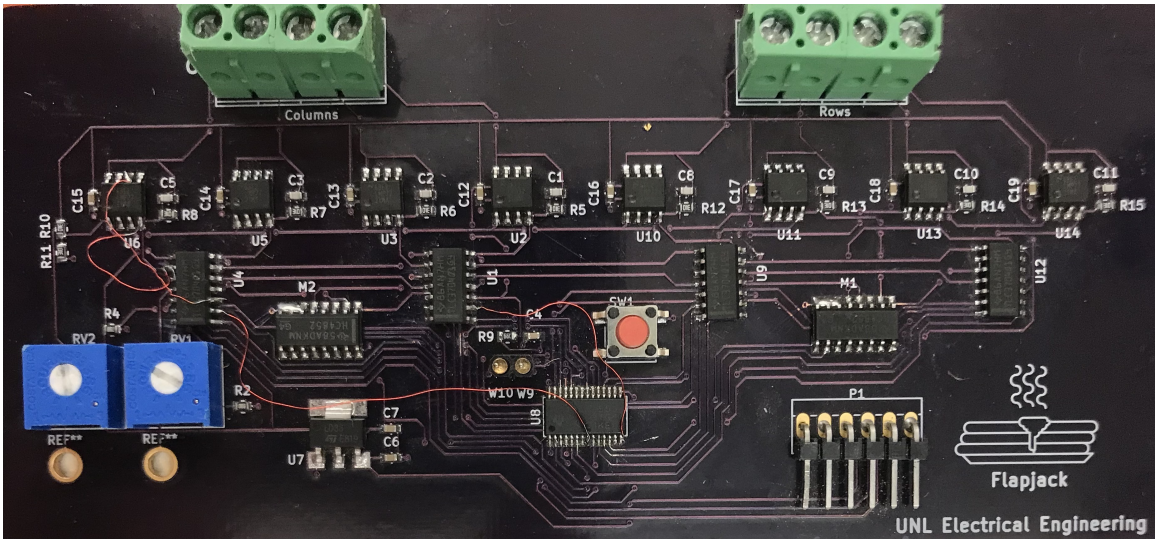


Figure 2.6: Test board for PVDF sensor characterization

output characterization was difficult. Some examples of the output characterization results are shown in Figure 2.7.

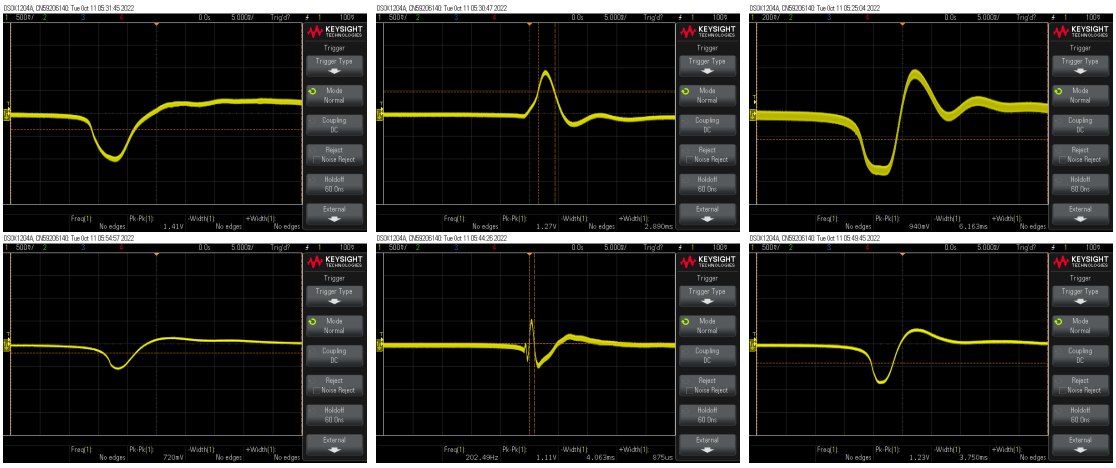


Figure 2.7: Output of CSAs on test board. Top row is press, release, and both. Bottom row is a light touch press and release,V/div=500 mV,T/div=5 m sec

2.4 System Specifications

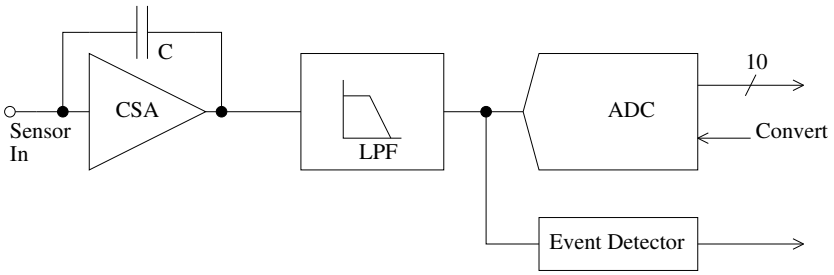


Figure 2.8: Diagram of the analog channel processing chain

The target implementation for this project is an integrated circuit in a 65 nm CMOS technology. Designing an integrated circuit for processing E-skin signals allows for greater functionality of the interface electronics with minimal cost to overall area and packing density. The core system specifications of the analog channel derived from the sensor characterization are to integrate incoming charge pulses from -1 to 1 pC. The analog channel must reliably detect small charge movements to identify when the taxel has experienced a change in pressure applied.

The analog circuits used must keep noise in the circuit to a minimum. Due to the low frequency nature of the signals filtering is used to remove high frequency noise.

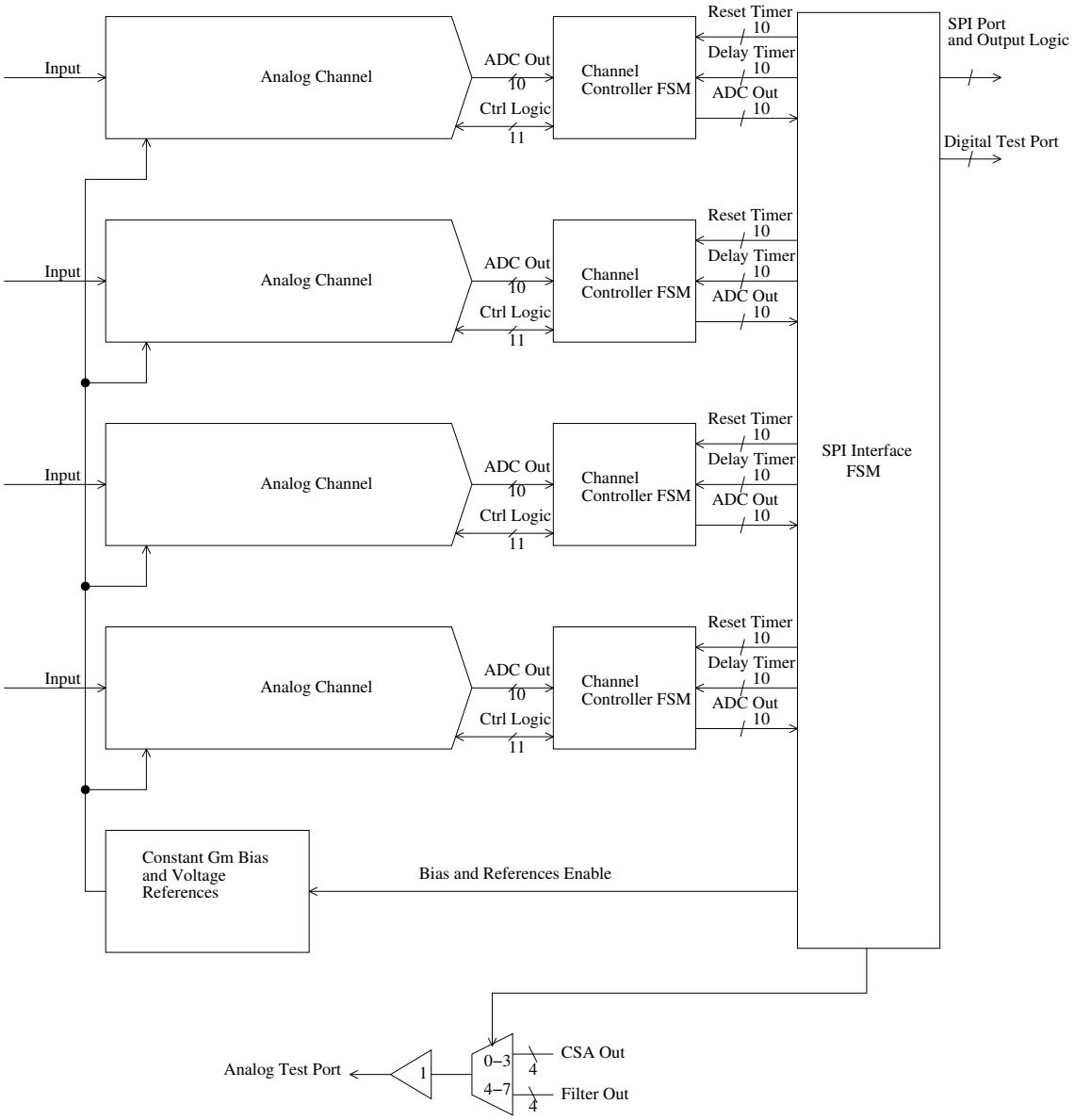


Figure 2.9: Diagram of the mixed signal system for processing E-skin signals

If the noise is too large and approaches the bit resolution of the ADC in magnitude, accuracy will be lost. Similarly, if the magnitude of noise is too large, false tactile events could be detected.

The power consumption of each analog channel must remain as low as possible. The purpose of this project is to place the E-skin system on a prosthetic limb. Any increase in power consumption will reduce operating time or increase battery size and weight. Keeping the power consumption small for each analog channel will allow for scalable spatial resolution.

Each analog channel contains a charge sensitive amplifier, low pass filter, a circuit for detecting charge pulse events, and an ADC for digitizing the signal. A block diagram of the analog channel signal processing chain can be seen in Figure 2.8. The purpose of the CSA is for converting incoming charge to a proportional voltage and driving the input to the low pass filter. The low pass filter is present to remove high frequency noise before digitization. The event detector is used to signal the digital circuitry to begin digitization. The ADC is an event driven circuit controlled by digital circuitry and will convert the voltage to a corresponding digital value.

The overall system design can be seen in Figure 2.9. The core specifications of the system is that it must provide tuning and control for each analog channel. The SoC must have a host of debugging options both analog and digital. The chip must have a form of digital readout to acquire data from. To ensure that debugging can be done multiplexers and buffer circuits have been added to select which analog portion of the circuit will be buffered and output on a test pin. The wiring is not shown in Figure 2.9 due to its complexity. The advantage of using the analog test port is in the event of an internal failure with the ADCs the analog signal could still be sampled by an external system such as a microcontroller. The remainder of the system specifications will be addressed in the subsequent sections.

Chapter 3

Design Process

3.1 Analog Front End Design

The analog front end consists of four major components, a charge sensitive amplifier, switched capacitor low pass filter, and two comparators for event detection. The difficulty in the design was to first have viable time constants in the extremely low frequency range (< 100 Hz) for waveform shaping and filtering. The second goal was to have as little noise contribution as possible in the AFE while also keeping power consumption to a minimum keeping in line with the system goals.

3.1.1 Op Amp

The core of the analog front end design is an op amp and is used in both the CSA and the lowpass filter and can be seen in Figure 3.1. The topology is based on an earlier design by Abdel Moneim et al. [12]. The key design parameters were to obtain a rail to rail input and output range to prevent information loss by maximizing dynamic range. Keep the root mean square (RMS) noise of the output under 2.5 mV while under unity gain feedback to avoid instability in the least significant bits of the ADC during conversion. The slew rate must also be high enough to drive the CDAC (capacitive digital to analog converter) and inputs to downstream circuitry .

The unity gain frequency must also be large enough to allow for a max value clock frequency of 32 kHz for use in low frequency switching circuits. The operation of the

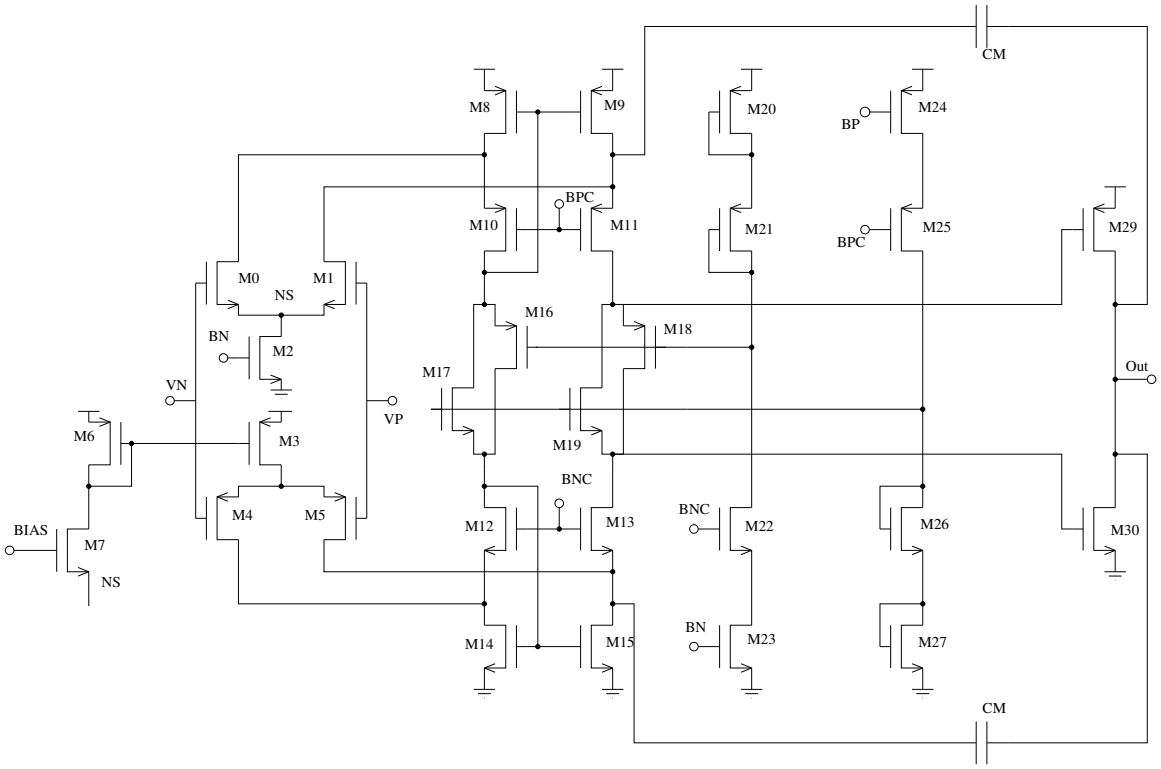


Figure 3.1: Rail to rail op amp

op amp is similar to a two stage op amp. A key difference is the two differential pairs at the input of the amplifier and the biasing of the output stage. The differential pairs that make up the input are M0-M2 and M3-M5. The common mode range of each differential pair can be approximated as

$$V_{BN} < V_N \leq V_{DD} + V_t - V_{ov8} \tag{3.1}$$

$$V_{BP} > V_N \geq V_{SS} - V_t + V_{ov14} \tag{3.2}$$

assuming no changes in threshold voltages across transistors where V_N is the inverting input voltage, V_t is the threshold voltage, V_{BN} and V_{BP} are bias voltages, and V_{ov14}

is the overdrive of the FET. This is a general approximation however as second order effects will change this. From the equations it can be seen that the input pair will be in saturation across the entire supply rail. This is because one input pair will be in cutoff while the other is in saturation based on the common mode input voltage.

A disadvantage of using complementary input pairs is there exists a input voltage range where both of the pairs are on. Having both input pairs on doubles the effective transconductance of the input stage, G_m, which reduces the phase margin of the amplifier and leads to instability of the op amp. To compensate for this, FETs M6 and M7 are used to shut off the P input pair if the input voltage gets large enough to bias the N input pair in saturation. To accomplish this, the source of M7 is connected to the source of the N input pair. This is because the source of the N input pair tracks the gate voltage, so if the gate voltage gets larger than $BIAS$, it shuts off the P input pair. Due to the low power nature of the op amp, the input pairs are operating in weak to moderate inversion so the performance of the current switch circuit is maximized and the transconductance only 4µS across the operating range. The change in input transconductance, with and without the correction circuitry can be seen in Figure 3.3 and Figure 3.2

The remaining components of the op amp is a cascode stack and a class AB output stage. The cascode stack is made up of M8−M11 and M12−M15 and its main purpose is to simply act as a current summing junction to sum the currents from the input pairs. The remaining transistors M16−M30 make up the class AB output stage of the op amp. Transistors M16−M19 and M20−M27 bias the cascode stack and AB output stage FETS M29 and M30. This bias is established with two translinear loops. For accuracy, translinear loops should be operated in weak inversion to prevent the square law operation of strong inversion from altering the operation. The two capacitors shown in Figure 3.1 are the Miller compensation capacitors each are 1 pF.

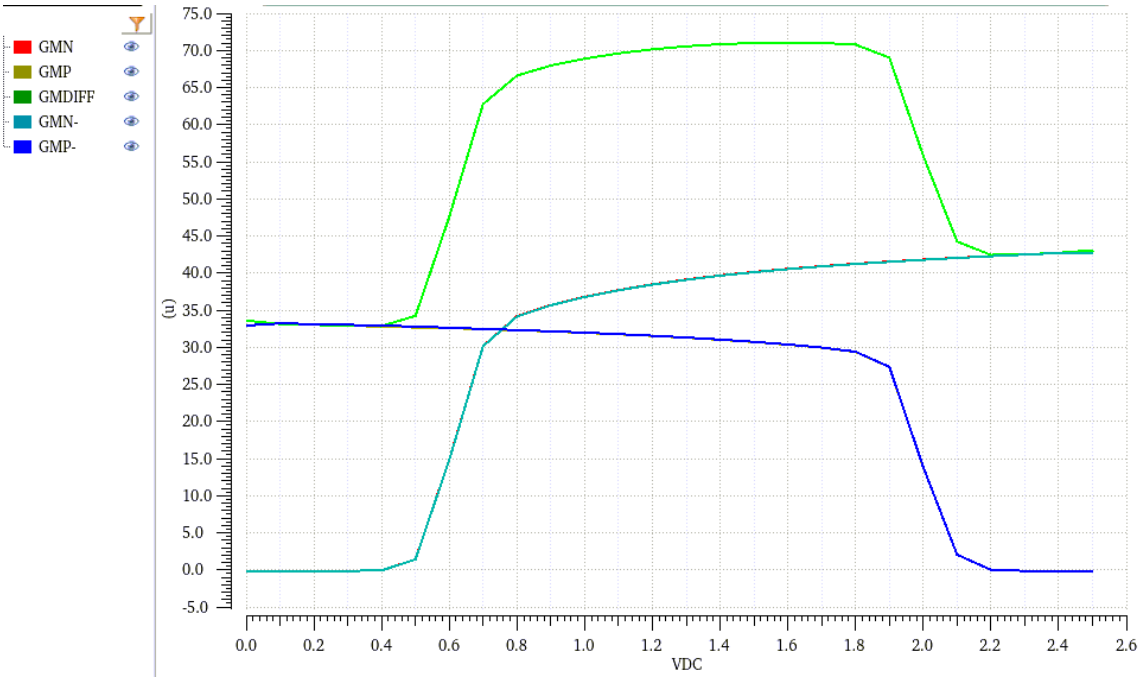


Figure 3.2: input pair transconductance without correction circuitry

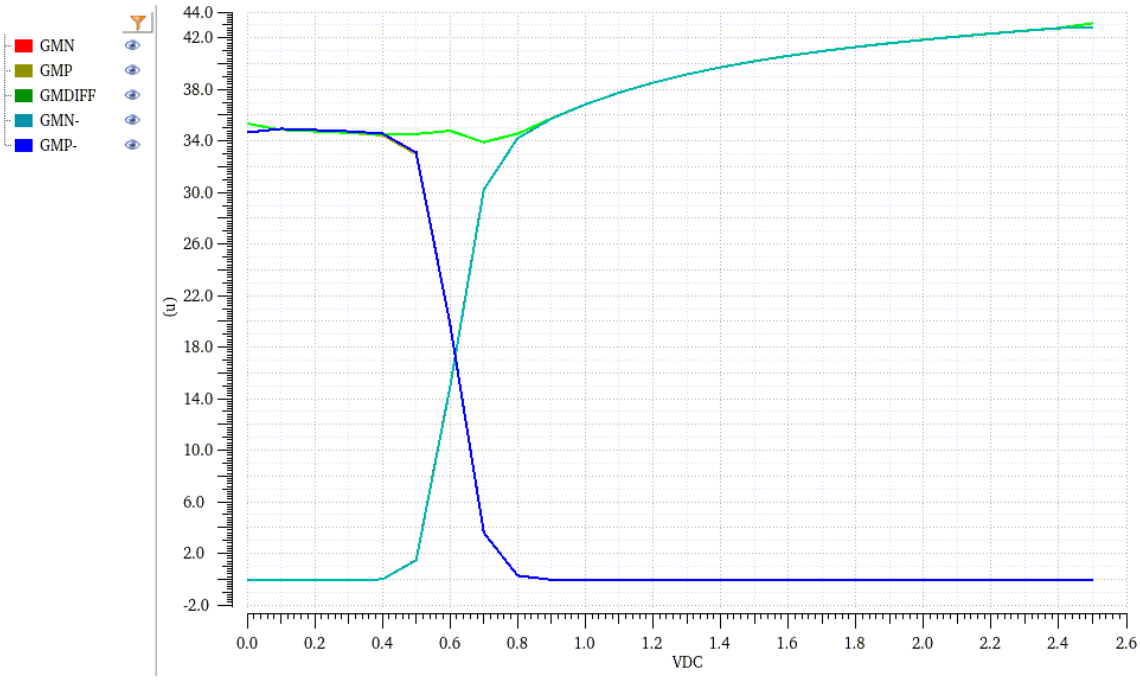


Figure 3.3: Input pair transconductance with correction circuitry

This value was chosen to give the amplifier a large phase margin across all operating voltages and PVT variations to keep yield high.

The biasing of the op amp was done with a simple constant g_m circuit which can be seen in Figure 3.4.

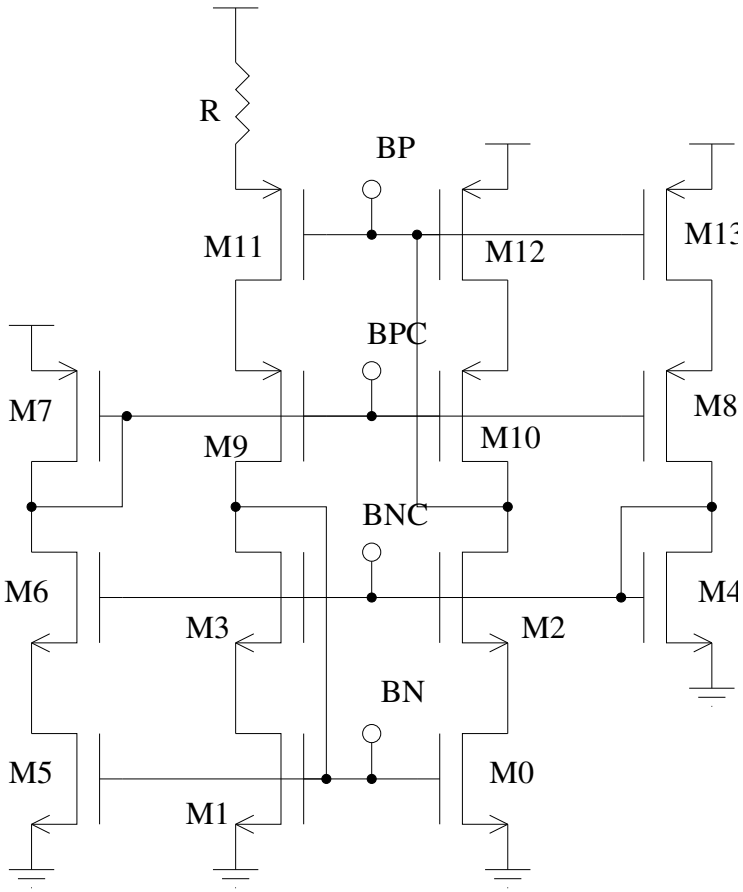


Figure 3.4: bias circuit for op amp

To limit the noise contribution power consumption of the op amp was cut as much as possible. Methods such as chopper stabilization and autozeroing [13] are perfect for this application as they have very small noise contributions at low frequencies. These methods were investigated but were ultimately deemed too power hungry to implement. This is because chopper stabilization requires a large 3 dB frequency for the op amp as well as a low pass filter to remove the modulated noise. Autozeroing

is similar in its power consumption but instead requires peripheral circuitry such as an offset/null circuit or separate op amp all together [13]. To reduce the $1/f$ noise of the op amp FETs were given large areas. Larger area FETs have less noise flicker noise but more thermal noise. The overall increase in thermal noise is acceptable for this application as flicker noise dominates the signal band of interest.

3.1.2 Charge Sensitive Amplifier

The CSA used in the interface circuitry must be able to process charge pulses arriving from a sensor rather than a continuous charge flow. A common form of CSA that processes charge pulses finds applications in radiation spectroscopy [2] and can be seen in Figure 3.5. This topology however is application specific and can only integrate properly in one direction where E-skin requires integration in both direction. In addition to this the time constant created by the C0 and M4 is much too small and fixed for the time constants needed for E-Skin. The charge sensitive amplifier design for the analog front end takes inspiration from analog integrators used in differential analyzers and a Texas instruments IC design of an analog array for integrating pulses arriving from photodiodes [10]. To remedy these problems, an op amp topology is used and can be seen in Figure 3.6 with a feedback capacitor of 1 pF. By using transmission gates connected in the configuration shown, the capacitor can be pre-charged to a arbitrary voltage level then placed in the feedback path of the op amp to establish a DC level and still allow for charge integration in positive and negative directions. By removing the feedback resistor and only using a capacitor for biasing, the CSA can integrate many different frequencies. The use of an op amp also provides a high accuracy of integration due to the large gain reducing charge loss. The drawback is that the CSA will need to be reset periodically as the op amp will repeatedly store its own error causing the DC level to drift with time. This is because of the removal of a

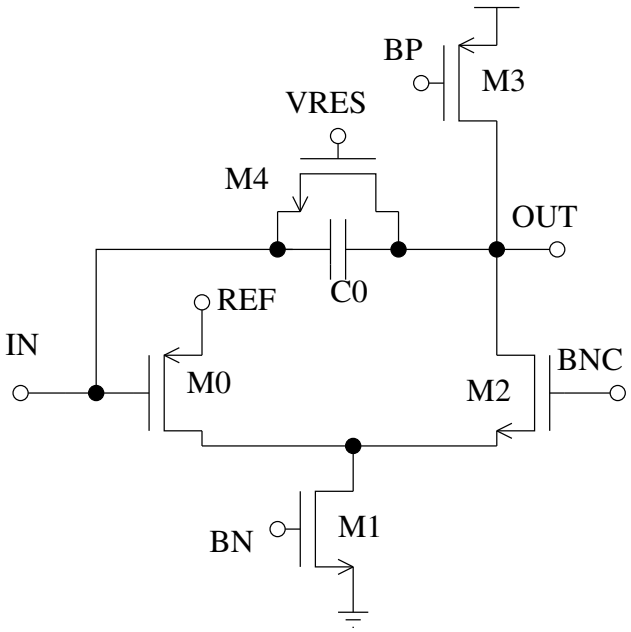


Figure 3.5: Original concept for CSA design

feedback resistor to obtain high time constants. It was found via simulation that the rate of error accumulation was about 20 mV/sec but this error rate will most likely be different than the simulated results after fabrication. Resetting the CSA every second or so is sufficient to maintain a bias level on the op amp without introducing significant downtime, which could otherwise lead to missed events. The time to

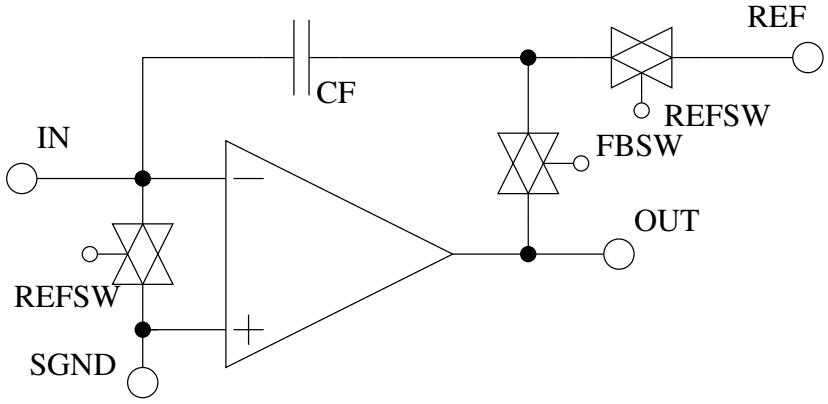


Figure 3.6: Op amp CSA with resettable capacitor biasing

reset is near instant relative to the clock speed of the analog FSM controller because

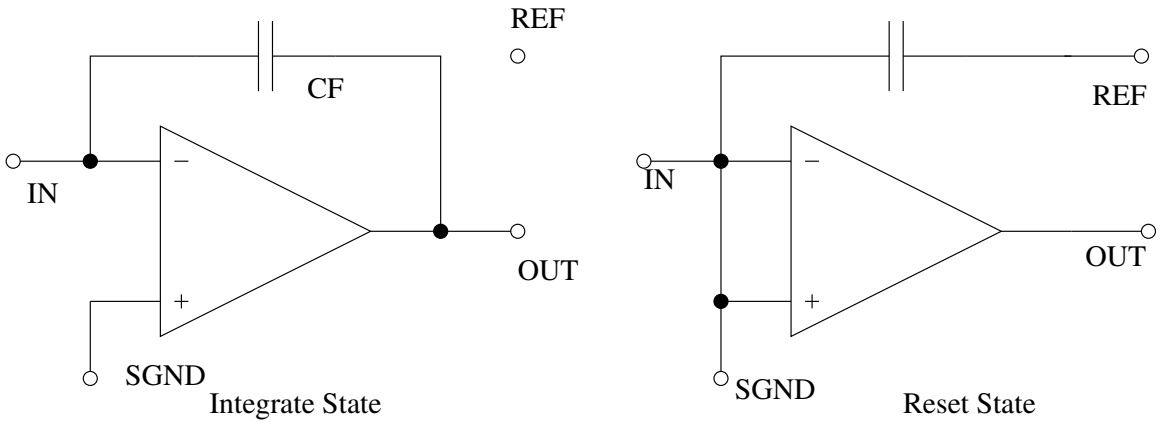


Figure 3.7: CSA operating states for bias reset and charge integration

the buffers for the reference voltages are capable of driving the 1 pF CSA feedback capacitor easily. So the primary limiter in the up time of the CSA is the channel controller clock cycle which operates at a low frequency 1 kHz to conserve power.

When connecting a sensor to the input of the CSA, large amounts of noise is generated at the output due to high sensor capacitance. The equivalent capacitance of the taxel and the feedback capacitor create a high gain path for low frequency noise ($100\ \text{Hz} - 200\text{Hz}$) and is proportional to the equivalent capacitance of the taxel. There are many ways to filter the noise, for example the DDC232 Texas Instruments chip [10] uses sigma delta ADCs to shape the noise and move it out of the band of interest. This is far too power hungry to implement per channel for this application. Our solution is a combination of limiting taxel capacitance and a low frequency filter. The tradeoff is that some precision is lost in favor of a much lower power consumption, making it more suitable for portable applications like prostheses. The loss in precision is because of the use of a SAR (successive approximation register) ADC instead of a sigma delta modulator to remove noise. The precision requirement is much more relaxed for this application making the tradeoff acceptable.

3.1.3 Switched Capacitor Filter

To filter the noise at the output of the CSA, a switched capacitor low pass filter is used. Switched capacitor was chosen over other methods such as G_m-C and RC filters because of its ability to filter low frequencies, ease of tuning, and small die area [14]. Switched capacitor elements work on the principle that two non-overlapping clocks control how charge is distributed in the circuit. This method allows large valued equivalent resistances to be implemented in a compact manner. A diagram of a basic switched capacitor resistor element is shown in Figure 3.8. By keeping the clock much

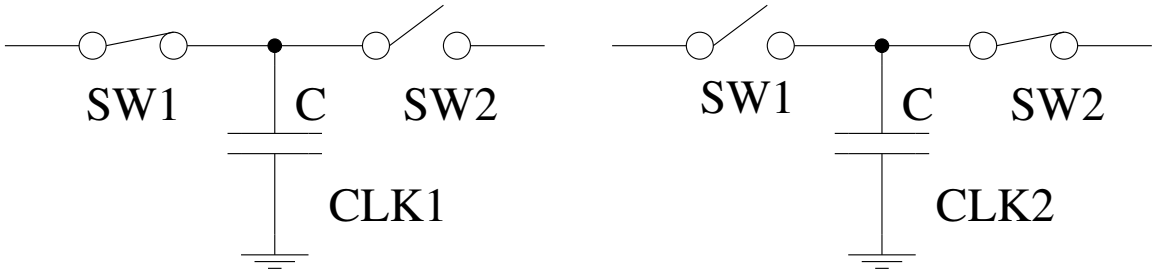


Figure 3.8: Idealized diagram of a switched capacitor resistor

faster than the maximum frequency of the signal ($f_{clk} >> f_{max,sig}$) switched capacitor elements can be approximated as resistors and follow the equation Equation 3.3.

$$R_{eq} \approx \frac{1}{C f_{clk}} \tag{3.3}$$

If the signal starts to approach the clock frequency, the Z transform must be used and the switched capacitor system should be treated as a sampled data system. Due to the nature of the signal we are trying to filter being sub 10 Hz and a minimum of 1 kHz being available for the clock frequency, the approximation holds and the switched resistor elements can be treated as linear resistors.

The switched capacitor filter topology can be seen in Figure 3.9 and is designed with a 100 Hz cutoff frequency.

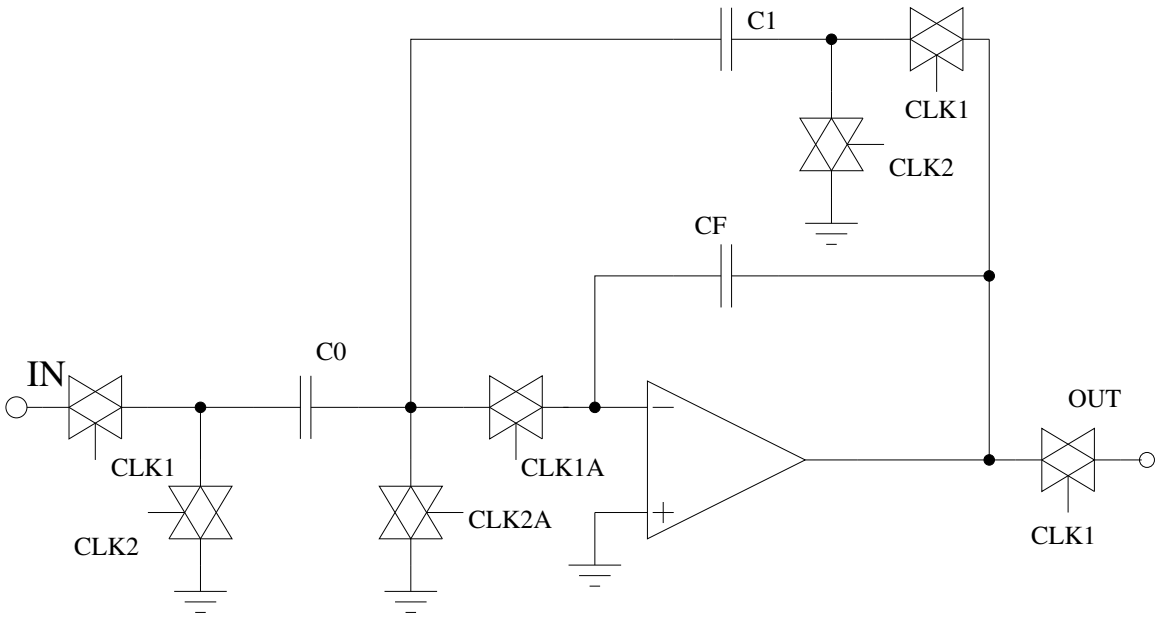


Figure 3.9: First order low pass filter used in the analog front end

The cut off frequency of the filter cannot be made much lower than 100 Hz without the use of a very large time constant integrators [14]. The primary benefit of having lower cut off frequencies for E-skin is removing more noise from the output of the CSA. These components cannot exist as a single stage due to their inability to hold a DC level without external feedback elements. Using a 2^{nd} or 3^{rd} order filter system would be too expensive for area as some topologies may require up to three op amps and tuning circuitry to maintain a certain bandwidth or Q value [14].

When designing a integrated filter of any variety, dynamic range is always a concern. To ensure that dynamic range in the switched capacitor remains high, transmission gate switches were selected in lieu of bootsrapped switches. This is because some bootstrapped switch topologies have the capability to put stress on the CMOS transistors due to voltages going above the power supply voltage. Using transmission gates allow for a high dynamic range or rail-to rail operation. By carefully designing the transmission gates, charge injection can be minimized without the need to include

a dummy switch in circuit. This is because the switching of the transmission gate creates equal and opposite amounts of charge in the FET channels which partially mitigate charge injection. The only signal dependent charge injection in the circuit exists at the input node and the feedback path. All other charge injection manifests as a DC offset in the output. To further reduce error caused by charge injection, advanced clocking and switch sharing is done. Turning switches on that are connected to ground nodes slightly before the actual clock edge reduces the charge injection and keeps it constant across state transitions. The transmission gates that close slightly faster are denoted with an "A" suffix in Figure 3.9. The second method used to reduce charge injection is switch sharing is a simple method to remove redundant switches in the circuit, fewer switches means fewer sources for charge injection errors. The redundant switches that were removed in Figure 3.9 were for connecting capacitor C1 to C0 and CF.

A phenomenon occurs with switched capacitor circuits during a clock edge where all capacitors are connected together and charge flow occurs. During charge redistribution the op amp experiences a brief, but significant jump in input voltage, causing its output to quickly slew, generating a "spike" at the output of the output of the amplifier. This is due to the op amp bandwidth and slew rate limiting how quickly it can compensate for the redistributed charge. This can be problematic for switched capacitor circuits that must interface with downstream continuous time circuits such as a comparator. The spikes at the output of the filter would cause the comparator to output glitches to the digital circuitry. This is not an issue for our analog front end as the filter will interface with a ADC and sampling can be timed to avoid the spikes that occur on the clock edges using clocked comparators.

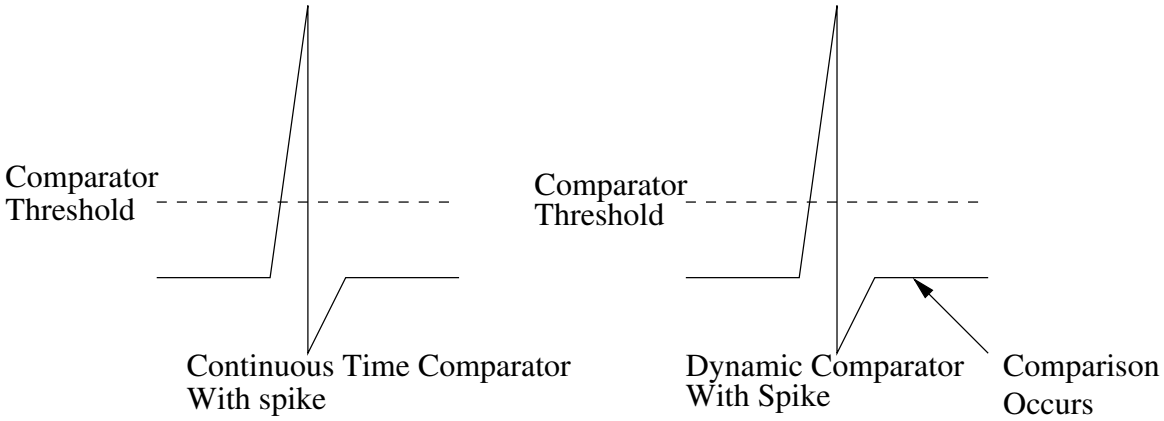


Figure 3.10: Spike effectson event thresholds for continuous and discrete time comparators

3.1.4 Comparator

The comparator design had three goals, 1) which as to determine if an event had occurred, 2) whether the pulse was positive or negative, 3) do it without the need for an external reference. The first two needs address the core functionality of the comparator in the circuit, namely to detect when an event has occured, i.e. when a taxel has had a significant change in applied pressure. This pressure change creates a charge pulse that can be detected as a voltage change at the output of the CSA and LPF. This circuit allows the downstream ADC to be disabled the majority of the time, saving significant power. The last requirement (reference-free) allows multiple channels to be integrated on chip without needing additional per-channel tuning circuitry for each AFE. For example, with a shared global reference, each channel would need additional calibration DACs to compensate for PVT, increasing power consumption. Due to complications with creating a reference free comparator. Many comparator designs were tested from squaring circuits, window detectors, and multi threshold comparators. A modification was made to the channel design as an external reference could be used. This is because of the high gain of the op amp in the LPF

compensated for large PVT variation. The remaining error would come from the input offset voltage which was not the limiting factor in setting the event thresholds.

To better accommodate for the sampled data system, dynamic comparators were used. Without the ability to clock the comparators, the spikes generated at the output of the switched capacitor filter would be continuously compared against the event threshold levels. This would greatly decrease the sensitivity of each channel as the event thresholds would need to be moved further away from the signal ground to prevent the detector from reporting a false event. By using a dynamic comparator, the comparison timing can be moved away from the voltage spikes and allowing the detection thresholds to be placed near the baseline. Another cause for error is the input offset voltage of the comparator which can decrease the sensitivity of the analog channel to small input charges. The comparator input offset is mitigated by increasing the current flow through the differantial input pair. The cut off for the sensor accuracy is 20 mV which is set by the DC level of the CSA because the CSA will integrate its own error, causing the DC level to move until reset. This provides a lower limit of what can be detectable as an event.

The dynamic comparator design can be seen in Figure 3.12 and is designed by [15]. The comparator design is the same one designed in [16], as its low power consumption and small footprint make it ideal for this application. The comparator, despite being a continuously clocked, only consumes 6 µW rms due to the low frequency system clock used. To detect positive and negative going pulses, the event detector simply makes use of two dynamic comparators which are both connected to the output of the switched capacitor low pass filter. The schematic of the event detector circuit can be seen in Figure 3.11. The lvl_h and lvl_l are set within 20 mV of the CSA output to account for the accumulated error. The two transmission gates at the input to the event detector are for preventing glitches when the FSM transitions

states. Once an event is detected the COMPSW transmission gate opens and the VCMSW transmission gate closes to hold the input at a fixed a value while the CSA was reset.

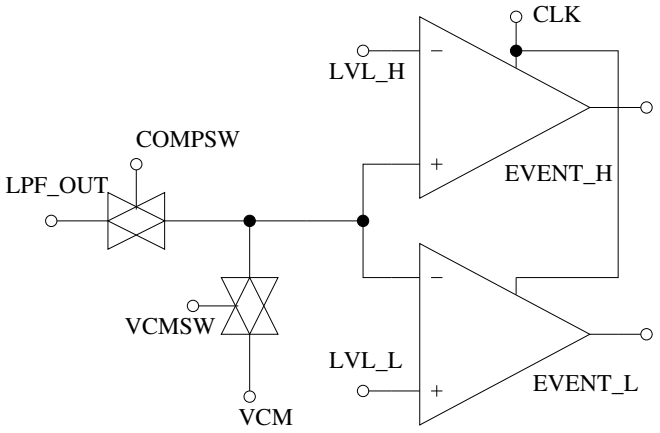


Figure 3.11: Schematic of event detection circuit

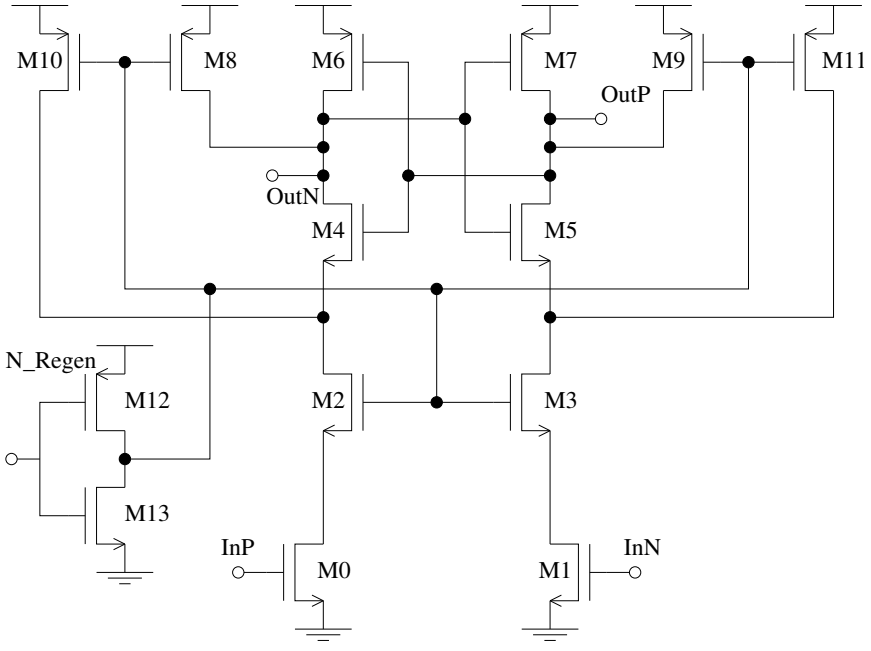


Figure 3.12: Schematic of dynamic comparator

3.2 Digital Back End Design

3.2.1 Analog to Digital Converter

The analog to digital controller selected for this design is a 10−bit SAR (successive approximation register) ADC and is the same design as [16] which is based off of the design of [17]. The benefit of this SAR topology is that the CDAC used in the ADC creates voltages based off capacitance size differences rather than purely capacitor size. This technique reduces the size of the CDAC and ADC subtantially. The size reduction makes this ADC ideal for E-skin applications as each analog channel can have a dedicated ADC while keeping the per channel area low. this enables integration of many channels onto a single chip.

The ADC, unlike the other components in the analog front end does not have a rail to rail dynamic range. This makes it a limiting factor in the representation of data. The reason is because the ADC interpolates codes at the low and high end of the dynamic range, due to the noise floor at the low end and non-linear FET behavior at the high end.

3.2.2 Digital FSM Channel Controller

The analog channel controller is the primary driver of all switches, clocks, and control signals for the analog portion of the design. It is largely event driven and autonomous excluding two external registers for tuning delays for reset and integration. A diagram of the finite state machine can be seen inFigure 3.13. The two external registers are used to change a 10-bit counter initial value. This allows the integration time of the CSA to be adjusted programmatically, compensating for potential PVT variations across the channels.

Another advantage of the variable delay is that the integrator can be set to in-

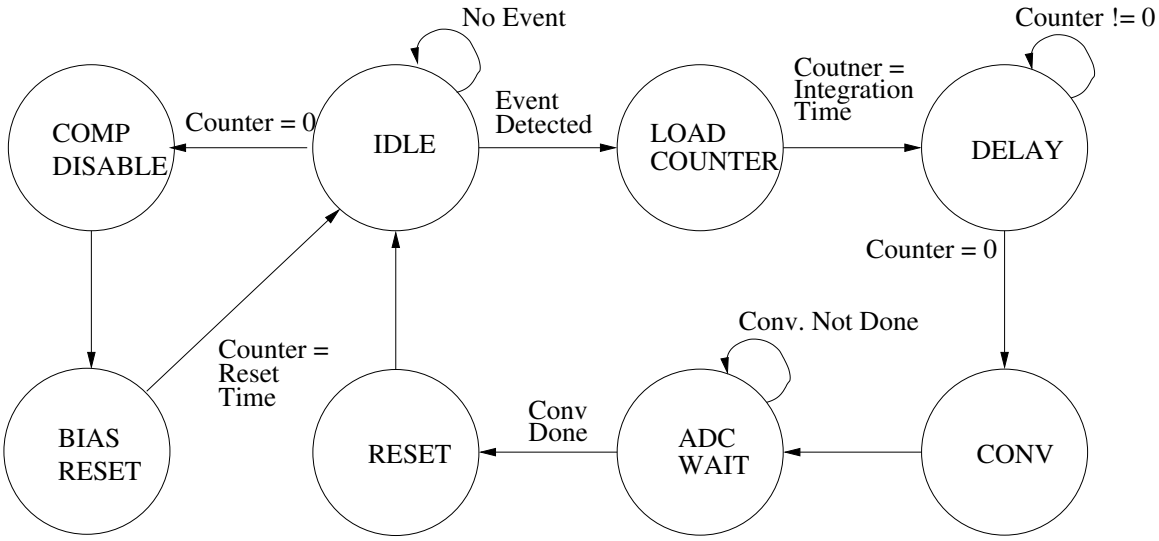


Figure 3.13: FSM of Analog channel Controller (extra states omitted)

tegrate over smaller time periods. Timing can be adjusted to integrate relatively long e-skin signal charge pulses over several integrate-measure-reset cycles, allowing the total charge transfer to be summed in the digital domain. This allows the integrator to effectively integrate charge pulses that would otherwise exceed the limits of the power rails, but at the cost of multiple ADC conversions and the associated power consumption. The technique is similar to what is done in other E-skin related work [2].

Along with controlling the reset time, the channel controller also controls the clocking for the switched capacitor circuit. Due to the very low frequency nature of the system, the maximum clock frequency is 32kHz. A clock divider is implemented in digital alongside the FSM for tuning the switched capacitor filter cutoff frequency and comparators. The clock divider is a simple 5-bit counter with clock gating cells implemented to prevent glitches should a switch in clock frequency occur mid cycle.

Figure 3.14 and Figure 3.15 show the changing of the channel FSM control signals under event detection and bias reset respectively. The event detection scenario is initiated by a comparator outputting 2.5 V or a logic one during a rising clock edge.

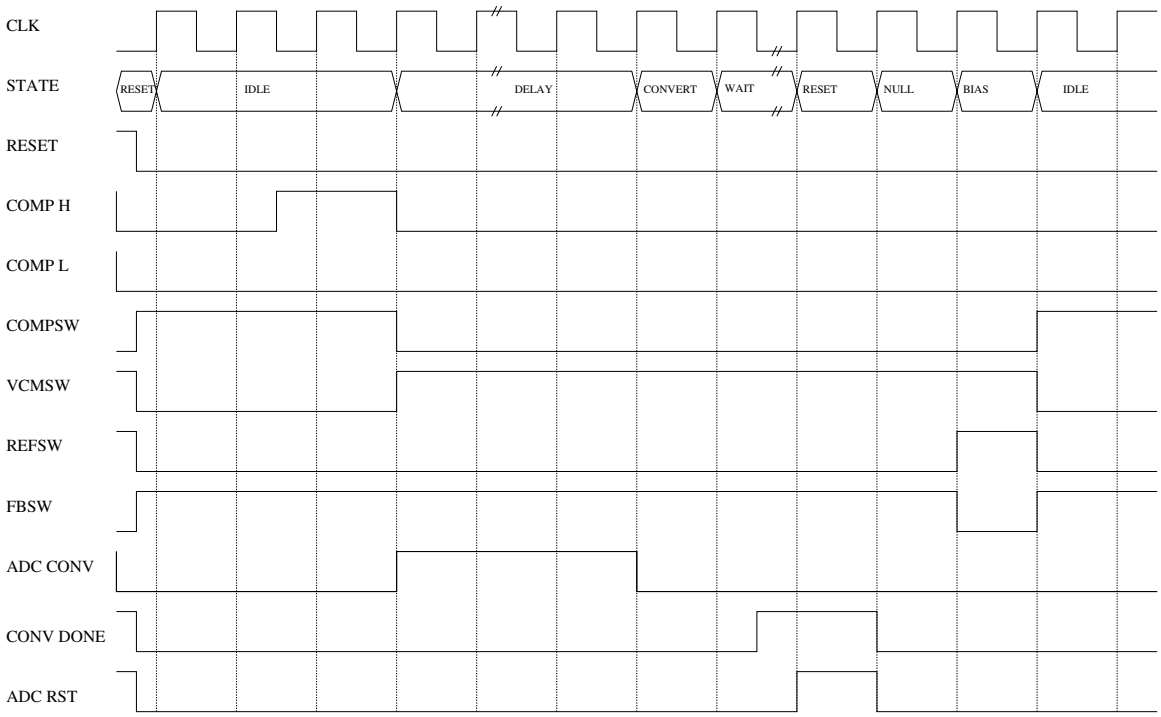


Figure 3.14: Timing diagram for interface between analog and FSM controller for event detection. Delay shortened for clarity

Once then, the FSM will delay a tunable number of clock cycles before disabling the comparator network to prevent any glitches. The ADC is then pulsed for conversion and the FSM waits for the conversion to finish. After the conversion, the CSA bias and bias reset counter are reset upon returning to the idle state.

The bias reset scenario is triggered when the FSM internal counter reaches zero. Upon reaching zero the FSM disables the comparator network and resets the bias of the CSA. The bias reset is done by turning off the feedback switch and turning on the reference switch to store charge on the capacitor. After the bias reset the FSM returns to the idle state to await a taxel event.

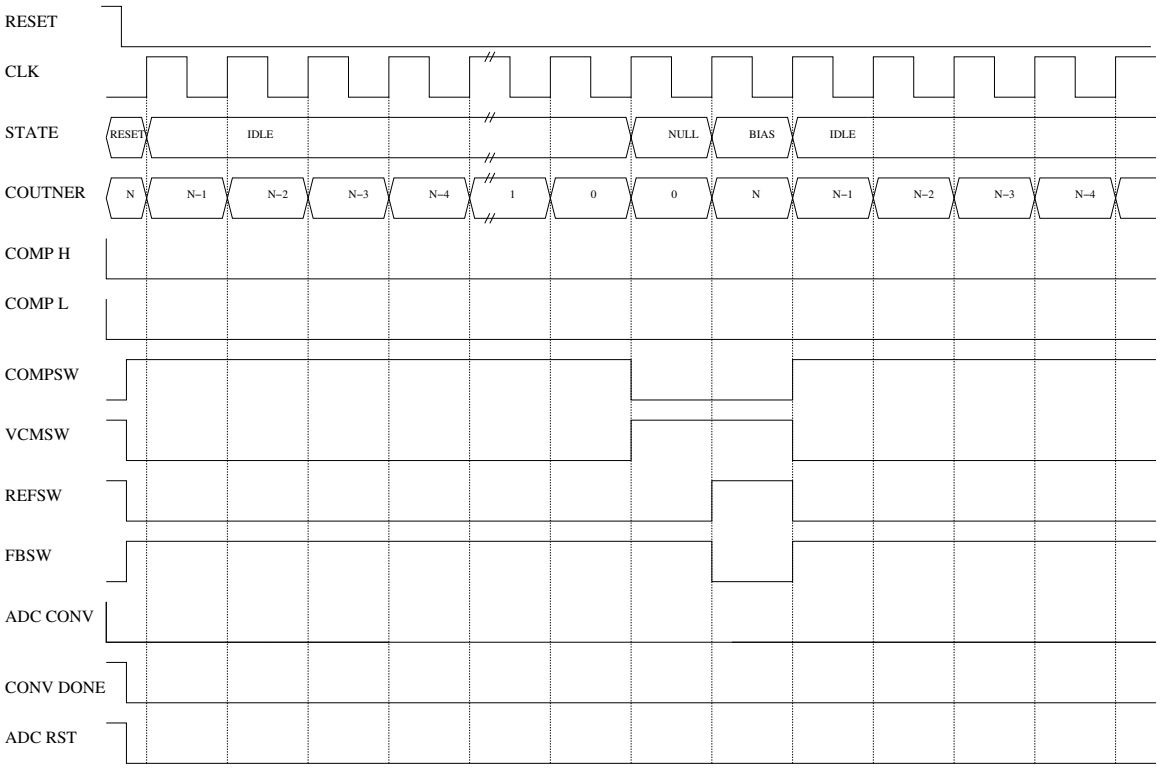


Figure 3.15: Timing diagram for interface between analog and FSM controller for bias reset. Delay shortened for clarity

3.2.3 Data Readout

To get data off the chip as well as set delay times and tune the filter, an SPI interface is used. Instead of using an internally supplied clock for the read/write logic, the SPI module would use the clock provided by the SPI master to avoid placing synchronizer circuits at the input of each SPI pin. The SPI controller supports mode 0 operation. This means that data is shifted in and out of the master on the falling edge and sampled on the rising edge of the clock. The bit transfer length is 24 bits to send and receive information. The orientation of the bit transfer can be seen in Figure 3.16.

The most significant bit of the transfer is the read/write flag where a 0 is read and 1 is a write. The bits following the read/write are for the 5-bit register address. The active memory locations only go up to 21 register leaving the remaining 10 memory

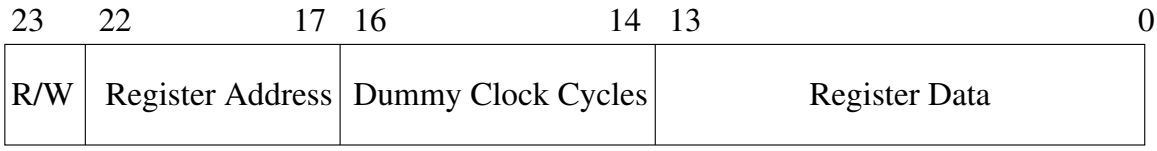


Figure 3.16: SPI data transfer bits stream example

locations inactive. Reading or writing to a memory location that is not active will return zeros. A list of the available memory locations can be seen in Table 3.1. The spare clock cycles used in bits 16 to 14 are there to aid in latching the data into the memory locations and give additional clock cycles during a transmit to load the data into the MISO shift register. The remaining bits 13-0 are used to store the data that will be written to or read from a memory location. Most registers are 10 bit values and ignore the upper 4 bits in the data block. The registers that control the event threshold levels require all 14 bits to increase the tuning capability.

To prevent timing issues with the asynchronous ADC output, the ADC controls the latching of the data to the memory location rather than having it done with the rising edge of the FSM clock. At the same time the data is latched to the memory location, a status bit is set high in the CHIP_CTRL_0 register. To get the data from the SPI controller, a two step read must be done, where the first read is to determine which analog channel has generated a new sample, then a second read to acquire the sample data. When communicating with the SPI controller, the CS pin must be deasserted and reasserted on each 24 bit transfer in the two step read.

The maximum SPI clock that can be used is 10 MHz but should not be run at this frequency to ensure timing violations do not occur. Due to the clock domain crossing that occurs between the channel FSM and the SPI writing to the reset timer and delay register should be minimized to prevent glitching at the output of the FSMs. This is because of the lack of synchronizers circuits at the clock domain crossing between the SPI and channel controller. A known bug of the FSM is that the SPI shift registers

Address	Name	function
0x00	CHIP_CTRL_0	ADC status and bias enable
0x01	TRIM_A	integration delay register channel A
0x02	TRIM_B	integration delay register channel B
0x03	TRIM_C	integration delay register channel C
0x04	TRIM_D	integration delay register channel D
0x05	ADC_A	ADC data register A read only
0x06	ADC_B	ADC data register B read only
0x07	ADC_C	ADC data register C read only
0x08	ADC_D	ADC data register D read only
0x09	CHNL_A	Channel A enable and tuning
0x0A	CHNL_B	Channel B enable and tuning
0x0B	CHNL_C	Channel C enable and tuning
0x0C	CHNL_D	Channel D enable and tuning
0x0D	SIG_DEBUG_CTRL	Analog debug enable and select
0x0E	EVENT_L_LVL	DAC voltage reference low
0x0F	EVENT_H_LVL	DAC voltage reference high
0x10	BIAS_TIMER_A	bias reset timer channel A
0x11	BIAS_TIMER_B	bias reset timer channel B
0x12	BIAS_TIMER_C	bias reset timer channel C
0x13	BIAS_TIMER_D	bias reset timer channel D
0x14	CHIP_CTRL_1	enable bits for ADC VCM and SGND

Table 3.1: List of memory locations in SPI controller

initialize to unknown values and must be flushed prior to data transmissions. This can be accomplished by simply writing zeros to any available register upon power up, afterwards any SPI transmission will happen normally.

Chapter 4

AFE Layout and Simulation

4.1 CSA

4.1.1 Layout

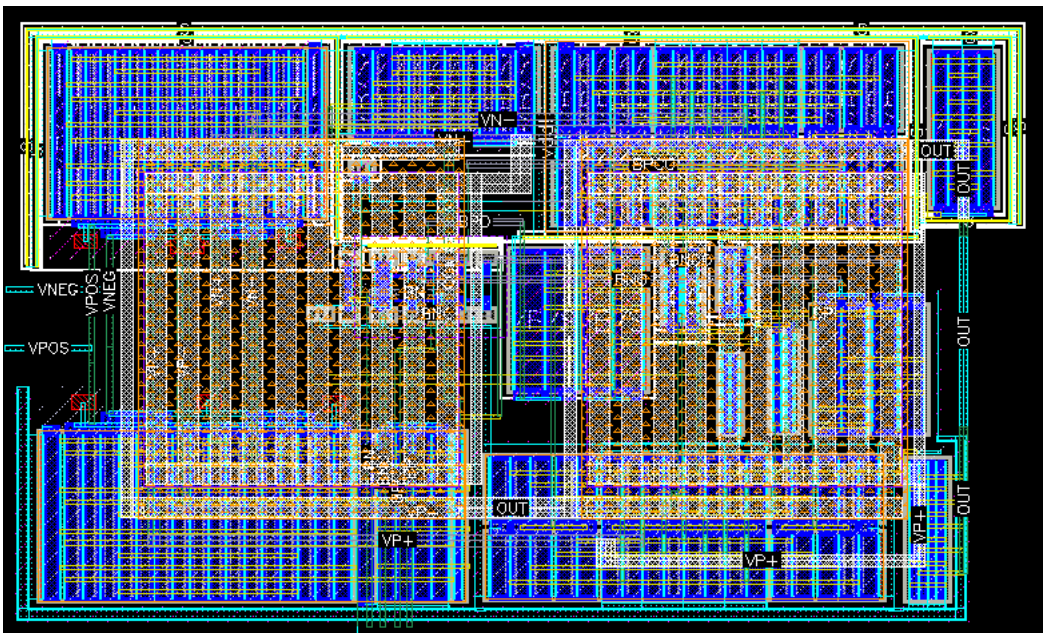


Figure 4.1: Op amp layout with MiM miller capacitors shown

The physical layout of the op amp was designed with the idea that the it would need to match the height of the ADC and be narrow and rectangular to have a high packing density on the chip wafer. This lead to the design seen in Figure 4.1. Opti-

mizations were made to reduce the area occupied by the op amp. The Miller compensation caps were implemented using MiM capacitors that sit on metal 8 (M8). The dimensions of the layout is 73×43 µm. The translinear loop and biasing transistors were placed in the center of the op amp located underneath the MiM capacitor on the right in Figure 4.1. This was done so that the area wasted by trying to match the height of the op amp to the rest of the analog channel was minimized.

To ensure that the layout behaved as accurately as possible to the schematic while also providing high yield, antenna diodes were placed on the input pairs. This is done to bleed excess charge built up on the gates of CMOS transistors during the fabrication process and improve matching for differential pairs by equalizing V_t. Each of the input pairs are placed using the common centroid layout technique to maintain matching and limit any input offset errors created by them. Common centroid layouts are arranged carefully in patterns that mirror symmetry across multiple axes. Examples of these patterns can be seen inFigure 4.2. Each cell also included dummy FETs at the edge of each centroid layout to prevent the etching process from adding to any mismatch error. To ease the burden on routing the wires to each of the FETs, a one dimensional common centroid layout is used. It is believed to be an acceptable trade off between ease of routing and matching as the op amp will be under feedback which will reduce any offset errors due to its high gain. The same approach is taken with the current mirrors in the layout as well. The loss of matching quality is acceptable as the error will be greatly diminished by feedback.

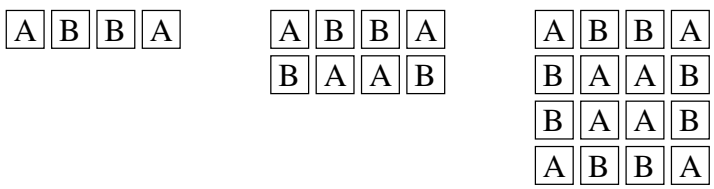


Figure 4.2: Common centroid layout examples excluding Dummy FETs, A and B represent MOSFETs

Each cell is wired following the wiring conventions used in digital designs where M1(metal 1) may go any direction while M2 is horizontal and M3 is vertical to better interface with mixed signal and digital components of the layout. The vias used to wire the analog components are minimum double cut vias to ensure that the route makes contact. Multiple small routes are placed across each cell to reduce resistivity, prevent unwanted voltage drops, and increase yield. Careful consideration was taken when sizing the width of each route by assessing how long it is and how much current it carries. Routes such as the VSS connection for transistor 2 in Figure 3.1 can be thin and short while the route for the output should be wide > 0.5 µm because of its length.

4.1.2 Input Range and Power

In total, the average power over the rail to rail common mode range is 30.43 µW. With the op amp making the core of the design it can be said that the average power dissipated per channel will be 60 µW.

4.1.3 AC Performance

The post layout simulation AC results can be seen in Figure 4.3. To acquire the phase margin and noise at the output, a transient noise and stability simulation were done. The DC gain of the op amp is approximately 80 dB with a bandwidth of 1 MHz across the entire operating range with the exclusion of being within 50 mV of each rail. This is because the op amp bias collapses at these extreme values and forces the output FETs to shut off crippling the gain. The open loop 3 dB frequency of op amp is very small and varies across the input range by about 30 to 120 Hz. This is an acceptable margin for error as the op amp will be under feedback during normal operation and has an approximate GBW (gain bandwidth product) of 3 MHz. The

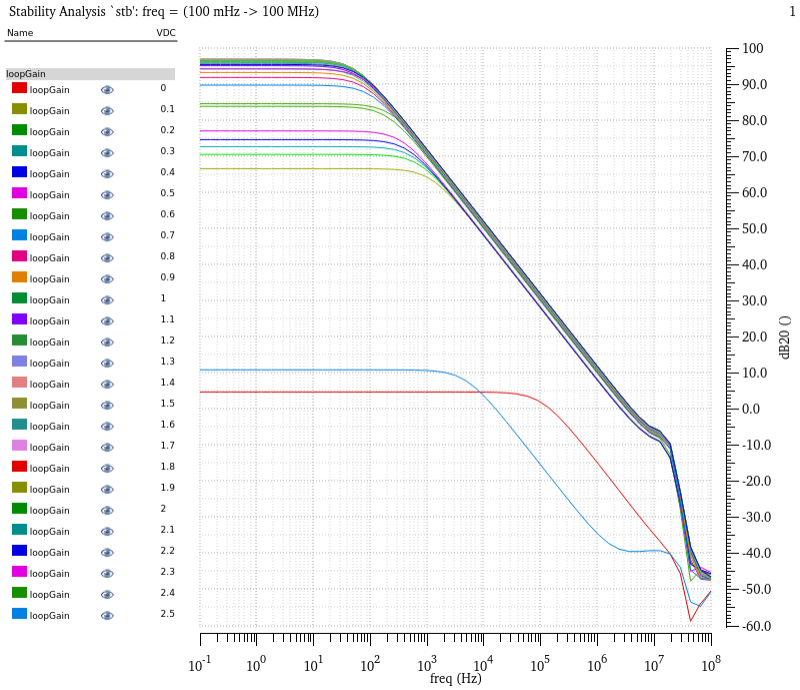


Figure 4.3: Frequency response of op amp with 4 pF load capacitance tested from 0 V-2.5 V

phase margin across the operating range can be seen in Figure 4.4. The phase margin of the op amp only has a 13 ° phase shift across the entire operating range excluding the extreme cases where the op amp output section is shut off.

4.1.4 Transient Performance

The output of the CSA layout simulation is shown in Figure 4.5a. Simulations where charge pulses of different magnitudes were input into the a charge integration circuit implemented with the op amp. The schematic of the test circuit is shown in Figure A.1. The resulting integrated output of the CSA is shown in Figure 4.5a, where the op amp's output voltage initially starts at a reference voltage, then rises or falls depending on the magnitude and direction of the charge flow during the integration. Ideally the net change in voltage is proportional to the total integrated charge. The

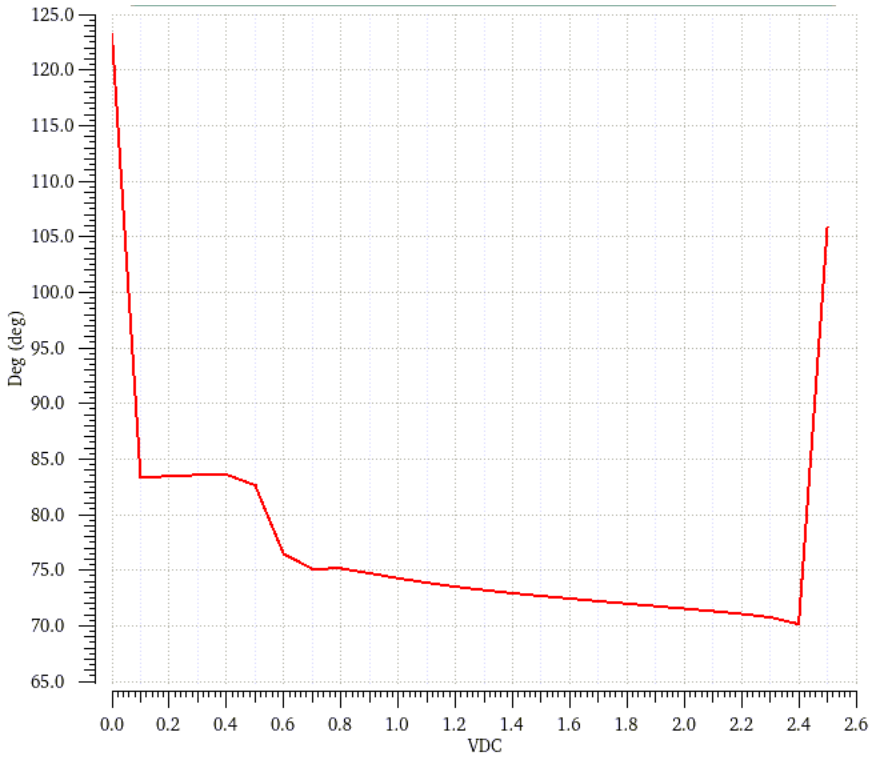
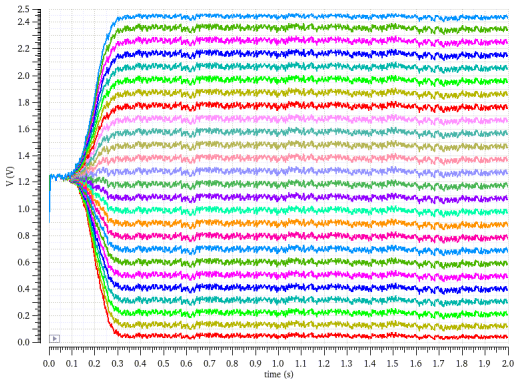
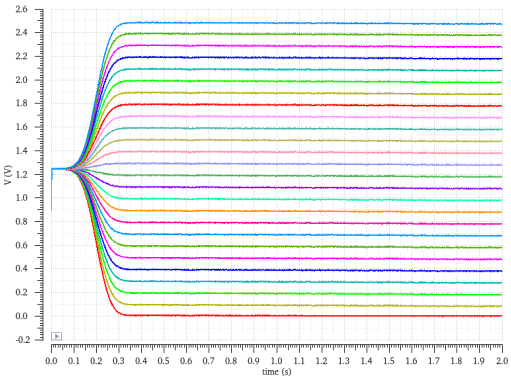


Figure 4.4: Phase margin vs. input voltage for the op amp with a 4 pF load capacitance, post layout load capacitance

noise seen at the output of CSA is a direct result of the high gain path created by the taxel capacitance and feedback capacitance. The test taxel used a capacitance of 1.36 nF which was a value provided by [3] for a conventional piezoelectric sensor tab. The commercially availible sensor generates an RMS noise of 392.6 mVrms at the output of the CSA. Using a smaller custom made taxel with a capacitance of 136 pF greatly attenuates the noise at the output down to 39.26 mVrms. The output with custom taxel can be seen in Figure 4.5b. Through careful sizing of the taxel the analog front would no longer need a low pass filter prior to sampling. To achieve this, a minimum taxel capacitance of 5 pF would be needed. In this case, the removal of the low pass filter would further reduce the area of the analog front end, further increasing packing density of the design.



(a) Output of CSA with a sensor capacitance of 1.346 nF



(b) Output of CSA with a sensor capacitance of 136 pF

Figure 4.5: Output of CSA with a commercially available sensor (Figure 4.5a) left and a custom made taxel with lower capacitance (Figure 4.5b) right

4.2 Switched Capacitor Filter

4.2.1 Layout

The layout of the switched capacitor circuit follows the same scheme as the CSA. The rail to rail op amp is used as the core of the filter with transmission gates placed along the border of the amplifier. The smaller capacitors in the design were done with MOM capacitors. These types of capacitors were used because the capacitance used in the switched capacitor resistor elements is substantially smaller than the feedback capacitance, allowing for easier wire routing to the transmission gates. The feedback capacitance of the filter was implemented as a MiM capacitor (denoted by the light tan and orange geometries)and placed adjacent to the miller capacitors of the op amp as shown in Figure 4.6.

4.2.2 AC Performance

To obtain the frequency response of the switched cap filter, PAC (periodic AC) analysis and PSS (periodic steady state) analysis were used to verify filter operation. PSS

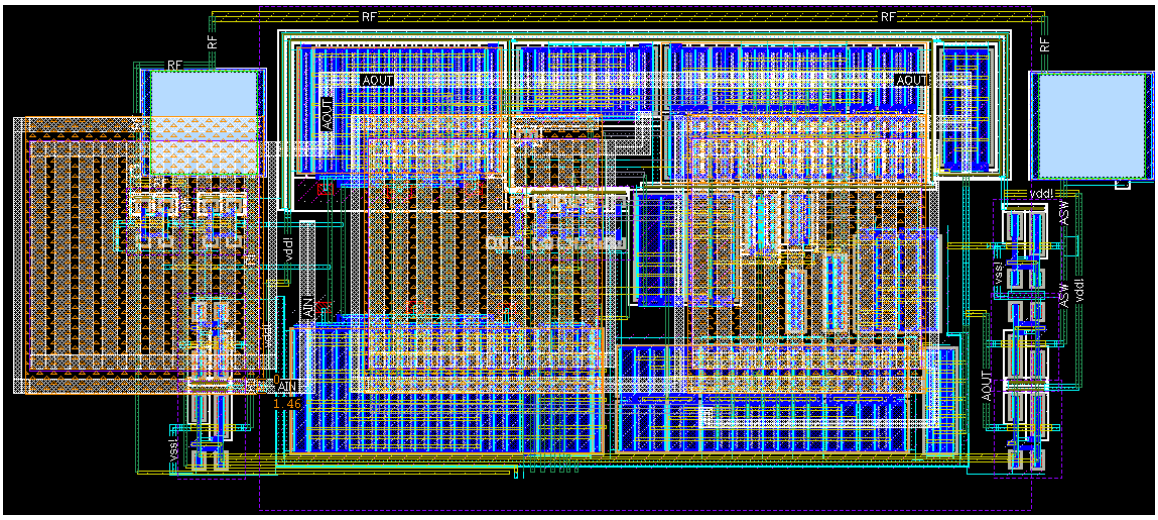


Figure 4.6: Layout of switched capacitor filter

determines the stability of a clocked system and establishes a small signal model for the circuit. PAC uses this small signal model to extract the frequency response of the switched capacitor filter, which can be seen in Figure 4.7. The target cut off frequency is 100 Hz but can go lower to further filter noise. The smaller cut off frequency comes at the cost of increasing error in the DC level. The change in the DC level is caused by the lack of sampling in the output in the switched cap filter. Due to the slower switching frequency the filter accumulates more offset across the feedback capacitor than what is removed by the switched feedback capacitor. In future designs the DC offset can be corrected for by changing the voltage at the non-inverting input to alter the DC level at the output. The harmonics created at the output of the circuit have been omitted for clarity in Figure 4.7. The most notable for this circuit are the first and third harmonics which are multiples of the switching frequency.

4.2.3 Power Consumption

The power consumption of the switched capacitor low pass filter is dominated by the power consumption of the op amp used, which is approximately 30.43 µW. Even at

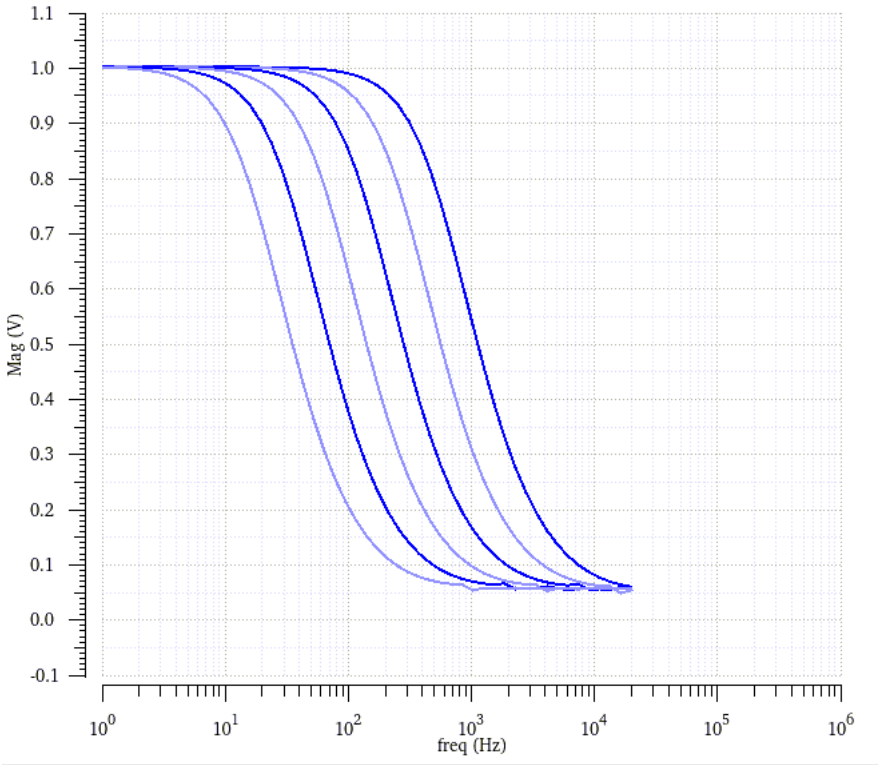


Figure 4.7: Frequency response of switched capacitor low pass filter with different clock frequencies 1-32 kHz from left to right

the highest clock frequency of 32 kHz , the filter only dissipates 33.43 µW. As the filter's clock frequency approaches 1 kHz the power consumption approaches that of the CSA or 30.43 µW.

4.3 Bias

4.3.1 Layout

The layout for the bias circuit follows the same conventions as the op amp. Common centroid layout patterns were used to maintain matching between FETs. Any mismatch in FET parameters could cause a change in voltage and bias level, altering the performance of circuitry. The difficulty with the layout of a constant G_m bias circuit is the odd number of transistors located at the BP and BN nodes that require

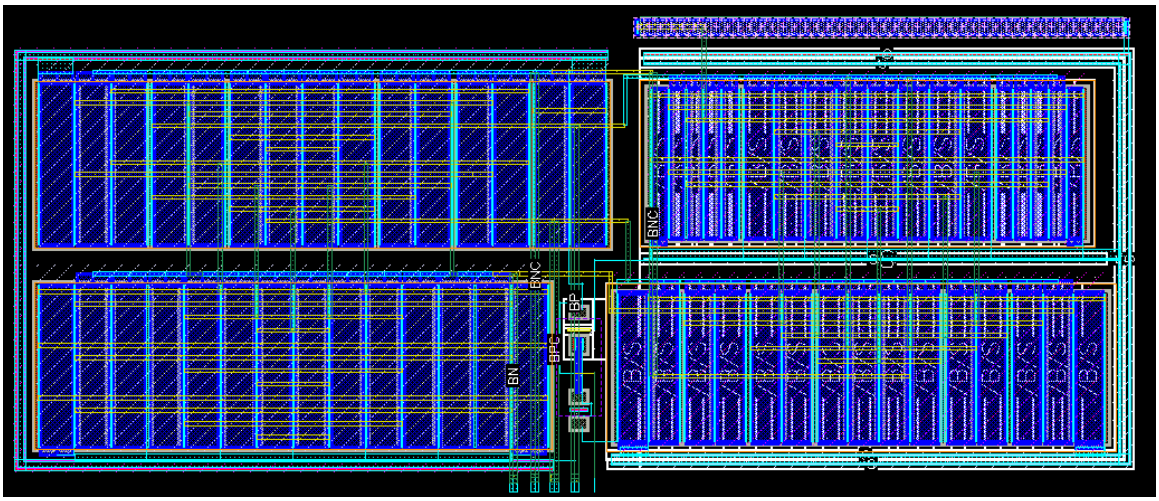


Figure 4.8: Layout of bias op amp bias circuit

matching. To ensure matching quality matching a 3 pattern common centroid scheme was used CABBA, where A, B, and C are FETs.

4.3.2 Power Consumption and Noise

The power consumption of the constant Gm bias circuit is 15.08 µW. Keeping the current low in the constant G_m bias circuit and increasing the transconductance in the biased circuit conserves power and area. As a result of the low power consumption and large area, the noise of the bias circuit at its highest is 155.7 µVrms. It is very important to keep the noise RMS noise low as the bias will be connected to high gain signal paths and could be amplified.

4.4 Full Analog Channel

The analog channel layout goal was to minimize the area while making it easy to array the AFEs in a multi-channel chip. To accomplish this the components of the design were placed in line with one another to keep them narrow and rectangular. Smaller cells such as transmission gates and comparators are placed such that they

do not go past the height of the op amp and alter the geometry of the channel, which can be seen in Figure 4.9. To better interface with the rest of the circuitry, the SAR ADC is rotated and placed on its side to prevent any routes from having to wrap around the layout and increase the height unnecessarily. A simple clock generator cell is placed in each analog channel for the switched capacitor filter. This cell simply creates the non-overlapping clocks needed for filter operation from a source clock provided by the digital back end. All op amp biasing voltages and reference voltages are wired together in the channel and connected by large metal routes to ease top level integration.

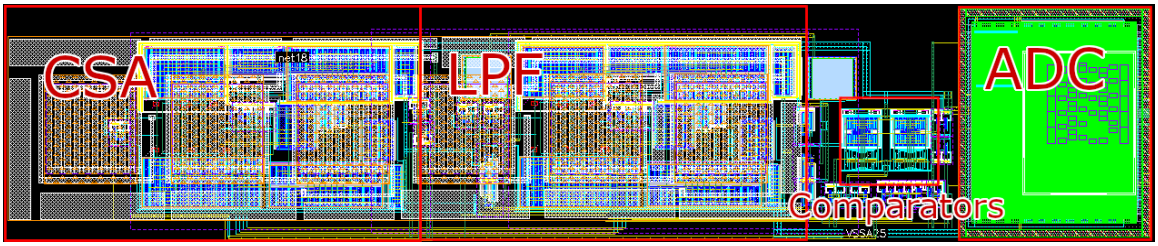


Figure 4.9: Layout of analog channel showing components

4.5 Digital Back End

The digital back end was layed out using 65 nm standard cells and laid out using innovus software. The total area of the layout of the digital back end is 8000 µm^2 and the density of standard cells within the allotted area is 98%, or only 2% of cells are fill cells. The digital layout can be seen in Figure 4.10. Rather than do separate layouts for each analog controller and SPI interface the digital blocks were placed in one layout to reduce overall area and make it easier to route the clock tree.

To verify the operation of the digital layout, the verilog and static timing characteristics generated by Innovus were loaded into a VHDL testbench via Xcelium. To test the digital controller, two different processes were used. The analog channel

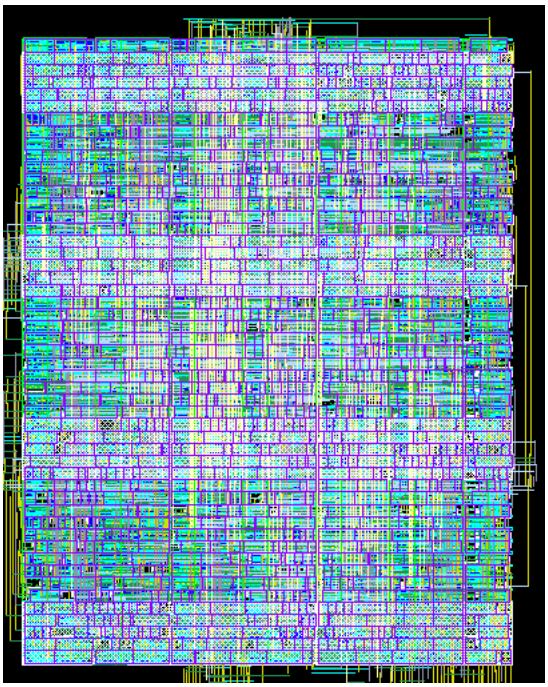


Figure 4.10: Layout of digital core

controller's operation was verified using an AMS (analog mixed signal) simulation, while the rest of the interface was tested in a VHDL testbench. The test consisted of writing typical values to each register in a random order then reading the values back. The reason for this was to ensure that the SPI interface could read and write in an arbitrary order rather than sequentially. Once the SPI initialization was complete, the ADC data ready latches were tested by pulsing the ADC conversion done pin for each channel and reading out the values through SPI. Some timing violations occurred in the simulation however these were in the bias reset register and the integration delay register. This is because the registers cross into the clock domain of the analog channel controller without synchronization. This is acceptable as these registers will not be repeatedly read or written to under normal operation, nor will the read write occur during an event.

4.6 System Layout

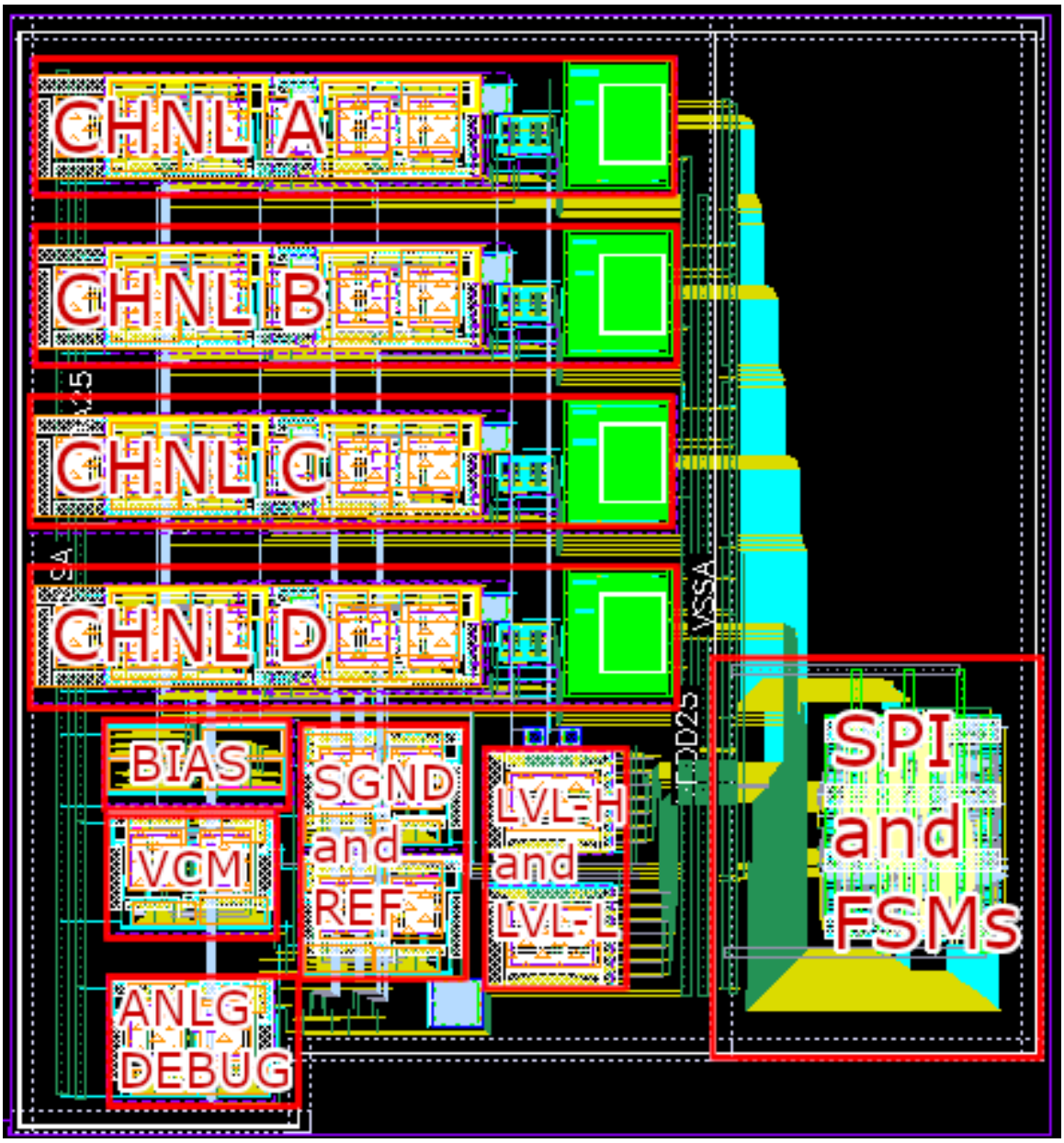


Figure 4.11: Layout of E-skin system with components highlightec

The complete layout for the E-skin system prototype can be seen in Figure 4.11. and the whole chip dye in Figure 4.12. The prototype supports a 2×2 taxel array due to area limitations. The layout can be divided into three separate sections, analog

channels, supporting circuitry, and digital section. The analog channels can be seen in the top left of Figure 4.11. The wide pitch between them AFEs is because each AFE has a bus between it for the analog control circuitry. The width of the bus was set to better match level converters along the NT_N boundary and to not provide adequate space for the ADCs in the analog channel.. The wiring bus connecting each AFE to the digital back end while wide was done to provide space for ease of routing. In the future multiple metal layers will be better utilized to reduce the width of the bus. The supporting circuitry is in the bottom left of Figure 4.11. This section consists of DACs for event levels, buffer circuits for driving chip pins and voltage references, and the op amp G_m bias circuit. The digital section is on the right of the chip and makes connections to the analog side via a large wire bus. Due to the use of various metal layers in the analog channel layout the digital connections must be placed around it which increases the overall area of each channel. In order to prevent dummy fill density errors in the layout the various cells used as voltage references or buffers needed to be spaced out further increasing the area. The total area of the system is 507 µm × 407 µm. With an estimated worst case static power consumption of 729 µW. This includes peripheral circuitry and continuous operation of the digital back end at 10 MHz.

The power supplies used for the design are analog 2.5 V, digital 2.5 V, digital 1 V. Both analog and digital circuitry are shielded by double substrate guard rings and a NT_N moat for substrate and power level isolation. Due to the slow switching nature of the digital signals the level shifters stretch over the NT_N moat use the analog ground instead of a digital one. This is because the digital signals going into the analog domain don't switch fast enough to create substantial noise in the circuit.

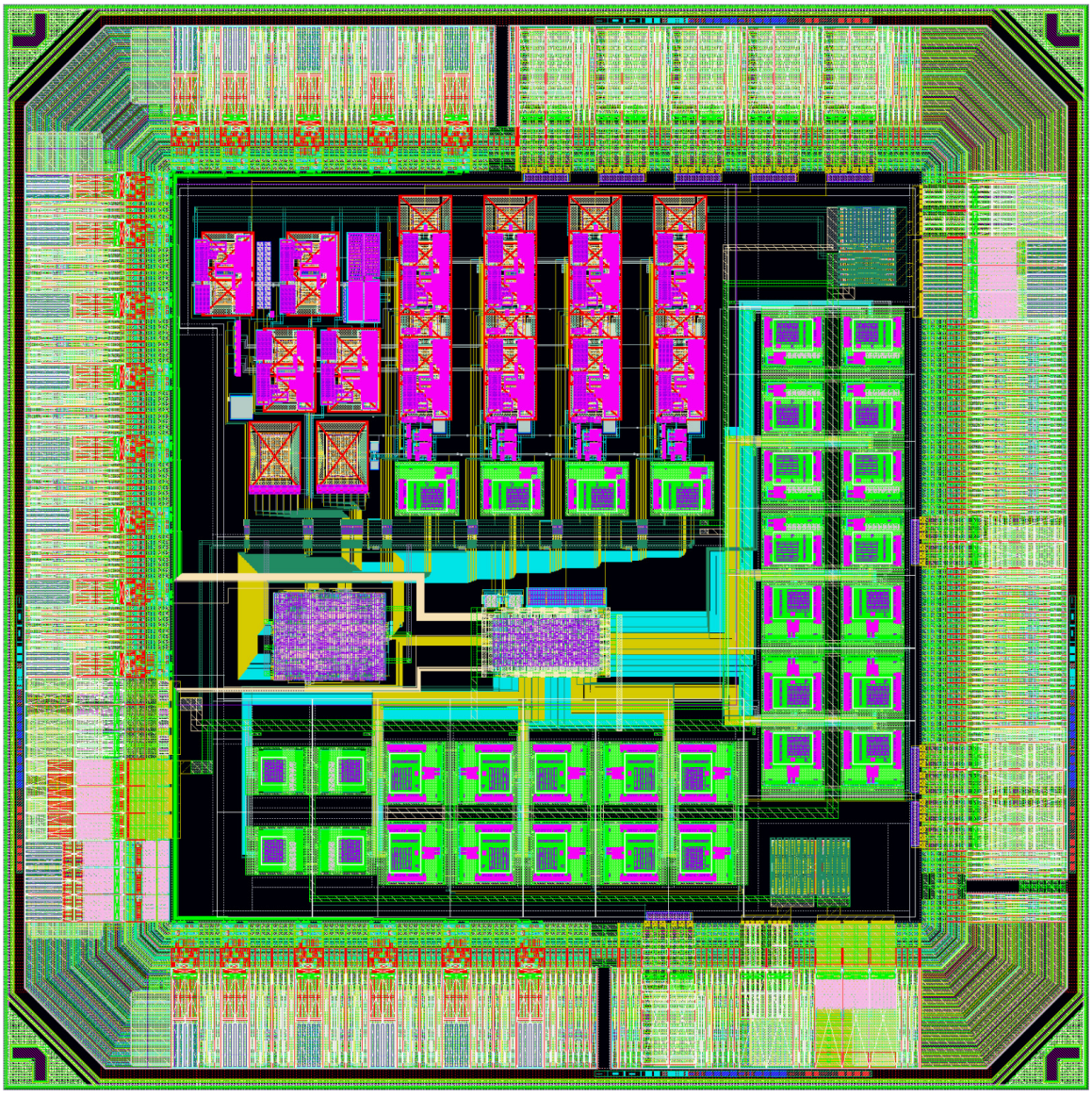


Figure 4.12: Full layout of Chip die with ADC characterization array

Chapter 5

Testing and Future Work

5.1 Testing

To test the IC, a test board was designed with a port for a ESP32 microcontroller to connect to select pins. The ESP32 will interface with a DATA_RDY pin, SPI pins CS, MISO, MOSI, SCLK, and a 32 kHz clock pin for the FSMs. The chip power will be provided by low dropout regulators for the digital and analog supplies The schematic can be seen in Figure 5.1. To begin testing the IC, Power must be applied before connecting the sensor array. This is done to prevent an charge buildup on high impedance nodes and damage the chip. Once this is done, initialization can be done via SPI to set bias reset timers, delay timers, and event levels. At this point the chip will be ready to process taxel events. The ESP32 microcontroller will monitor the DATA_RDY pin and perform a two step read to acquire a data from the taxels. During testing, proper operation of critical analog and digital signals can be observed through the ANLG_DBG pin and the DGTL_DBG_VECTOR pins. The ANLG_DBG pin muxes internal CSA and filter signals to a buffered output while the DGTL_DBG_VECTOR is a set of ten pins that monitor all channel FSM signals for autonomous switching. If any autonomous signal changes such as the FBSW and REFSW in any channel the output of the corresponding DGTL_DBG_VECTOR will

go high.

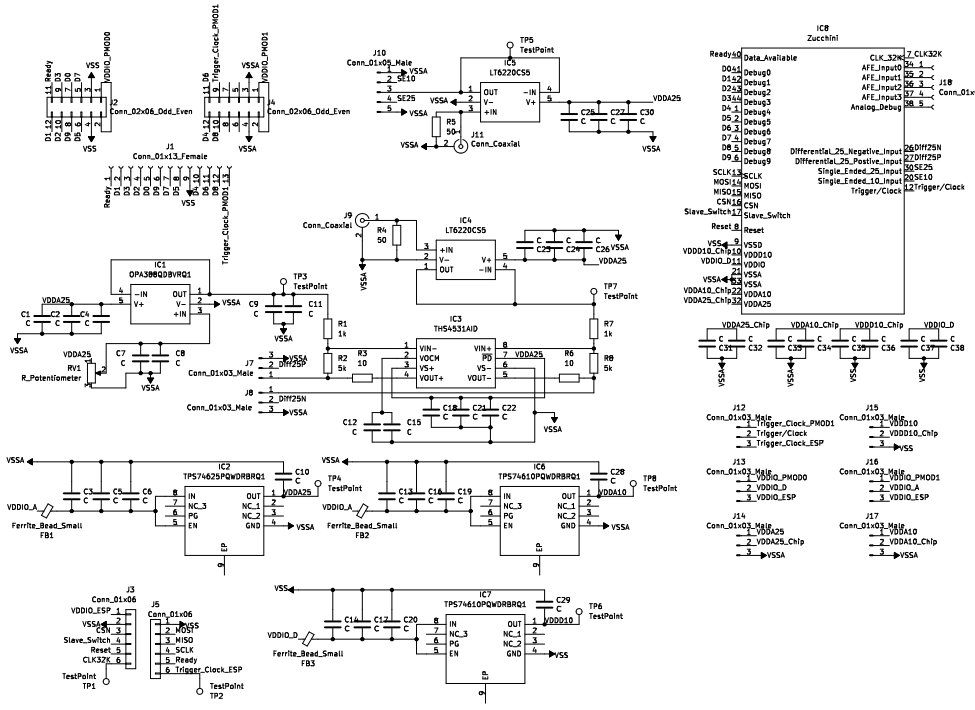


Figure 5.1: Schematic of test board with Zucchini IC shown

A potential point of failure is the PVDF sensors operating in voltage mode rather than charge mode. If substantial force was applied to the taxel array charge could flow into a high impedance node, causing damage to the chip. In future versions of the chip this could be mitigated with smaller taxels and robust ESD protection. Another potential point of failure in the system is the clock domain crossing from the output of the ADC to the latches in the SPI interface, preventing data read out. In the event of a failure to read out ADC data over SPI the IC can be configured to output analog signals through the analog debug pin. This was done to ensure that data can be partially gathered from the CSAs and low pass filters. This can only be done on one AFE at a time. Similarly the control signals from each analog channel

FSM can be probed using the digital debug pins on the IC.

5.2 Future Work

5.2.1 Sensor Array

Future work on the sensor array should be put into two different goals, finding or fabricating a smaller sensor that is tuned to forces applied perpendicular to its surface and developing a more complete sensor model for simulation. Reducing the size of the sensor will 1) reduce the noise at the output of the CSA, 2) reduce the potential for ESD damage to the chip by dumping charge into a high impedance node, and 3) increase sensor spatial resolution. Reducing the size of the sensor would reduce the noise at the output of the CSA by reducing the capacitance. In addition to the removal of noise at the output of the CSA, a smaller sensor would increase spatial resolution of the array. A better model of the PVDF sensor for charge pulse output would improve the accuracy of the circuits. This could be accomplished by adding some stochastic models to vary the width of the charge pulse emitted from the sensor model.

5.2.2 Circuits

Future work on the circuits is focused on a few key areas, 1) further reducing the power consumption of the CSA, 2) removing the low pass filter, 3) investigating circuits for converting charge directly to a digital value such as an integrating ADC. Reducing the power consumption of the CSA would require changing the topology of the amplifier. The CSA does not require a open loop gain of 96 dB to integrate charge and hold a DC level, lower open loop gains are viable and can function without issues. Finding

a circuit topology that reduces power consumption while keeping rail to rail output is the next step.

Finding a way to remove the low pass filter would halve the power consumption of the AFE. By removing the low pass filter from the analog front end, the op amp could have its power consumption reduced as it would not need to slew rapidly to prevent kickback. From Section 3.1.3 it can be seen that the purpose of the low pass filter is to remove the noise created by the sensor input capacitance. If the noise is mitigated by a smaller sized taxel, the filter would serve no purpose as the CSA would double as a low pass filter. Removing the low pass filter would also improve the amount of events per second that could be handled by the analog front end.

Improvements to channel packing on the chip is another focus of future work on E-skin systems. Ensuring that the size and routing overhead of the analog channels is manageable would allow for more channels to be placed on a single chip. To accomplish this, the optimization of cell layouts should be done to reduce routing overhead and area. In the current layout, there is a 20 µm region between channels for routing. Since the channels are 55 µm wide, reducing this spacing would significantly increase the channel density on chip.

Investigation into methods to convert charge directly to a digital value is another focus area. There would be no need to have a CSA and SAR ADC to perform charge integration then conversion; a single circuit would be able to do both. A design that directly converts the taxel input could potentially reduce the size and power consumption even further than an improved AFE of the same design. With careful design, dynamic range wouldn't be in issue for the CSA as the digital values could be sampled, summed, and read out as one value. This would make the limiting factor of dynamic range just the ADC rather than the ADC and CSA.

Chapter 6

Conclusion

To conclude, electronic skin as a biomedical sensor array is presented and discussed. The state of the art of E-skin research is presented. The thesis presents a low power event driven analog front end to process charge pulses arriving from a E-skin taxel array. The chip supports a 2×2 taxel array complete with a SPI readout of data. An single AFE channel dissipates only 72 µW of power while maintaining rail to rail operation and filtering low frequency noise. Including periperals the estimated power dissipation of the entire analog front end is 450 µW The digital circuits are capable of operating the AFE in single sample mode or a continuous sample and sum mode while reading data out over SPI. The estimated chip returns from fabrication in December of 2022 and testing is ready to begin as soon as it returns. Future work on the chip will focus on further 1) cutting power consumption, 2) reducing sensor size and optimizing for charge pulse generation, 3) increasing AFE packing density through area reduction, 4) reducing pitch between AFE channels, and 5) investigating methods of directly converting charge to a digital value.

Appendix A

Appendix

A.1 Register bit fields and information

bias reset control registers and delay control registers such as trim_x and bias_timer_x follow the formula

$$T = \frac{f_{clk}}{1023} \cdot reg \tag{A.1}$$

similarly the global event threshold register event_l_lvl and event_h_lvl can be described by the formula

$$V = \frac{V_{DD}}{16384} \cdot reg \tag{A.2}$$

All bit fields in Table A.1 are enabled with a logic 1 and disabled with a logic 0. LPF

9	8-6	5-3	2	1	0
N/A	LPF CLK SEL	FSM CLK SEL	FSM EN	LPF EN	CSA EN

Table A.1: register bit map for channel_x registers

CLK SEL and FSM CLK SEL are both six to one multiplexers that select clock values based on the values shown in Table A.2. The FSM EN, LPF EN, and CSA EN are all enable values used to enable or disable parts of the AFE for power characterization.

To enable the register bit fields a 1 should be written to the bit field. the ADC FLAGS bit field is a status bit field that is cleared only through a register read. The

binary	clock frequency
000	32 kHz
001	16 kHz
010	8 kHz
011	4 kHz
100	2 kHz
101	1 kHz

Table A.2: selectable frequencies for FSM and low pass filter

9-6	5	4	3	2	1	0
ADC FLAGS	BIASEN	VCMEN	REFEN	SGNDEN	DIVEN	N/A

Table A.3: register bit map for AFE control register 0

BIASEN, VCMEN, REFEN, SGNDEN, and DIVEN are all bit fields for enabling peripheral circuitry. BIASEN enables and disables the constant g_m bias on a 1 and 0 write respectively. VCMEN, REFEN, SGNDEN, and DIVEN are all for enabling the common mode voltage buffer, reference buffer, and signal ground buffer, while DIVEN is to enable the voltage divider circuit. The digital debug register is a set of

9-6	5	4	3	2	1	0
CHNLEVNT	REFSW	FBSW	VCMSW	CMPSW	ADCCNV	ADCRST

Table A.4: register bit map for digital debug output

external pins that represent the autonomous signals of the AFE front end controllers. Each pin is the output of an logic OR gate so channel debugging could be done should there be any glitches in the FSM.

9-3	2-0
N/A	ANLG DBG MUX SEL

Table A.5: Analog debug register bit map

The ANLG DBG MUX SEL is three bit field for selecting a analog signal from the any AFE signal chain and buffering it to output on the external analog debug pin. the selection follows the values shown in Table A.6

Binary	Signal
000	CSA_A
001	CSA_B
010	CSA_C
011	CSA_D
100	LPF_A
101	LPF_B
110	LPF_C
111	LPF_D

Table A.6: Selectable analog debug outputs of the analog front end

9-3	2	1	0
Not Used	DBG BUF EN	DAC_H EN	DAC_L EN

Table A.7: register bit map for control register 1

The chip control register 1 only uses three of its bits to enable or disable peripheral circuitry for power consumption. The DBG BUF EN is a bit flag that enables or disables the buffer for the analog debug pin. DAC_H EN and DAC_L EN are for enabling or disabling the DACs used for setting the global thresholds for event detection.

A.2 Reference circuits

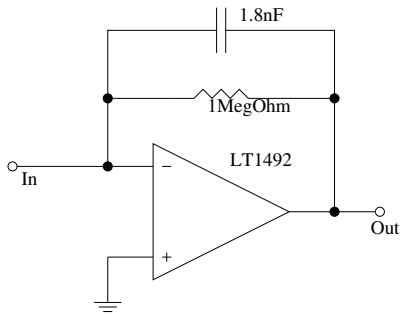


Figure A.1: CSA used for sensor characterization

The circuit shown in Figure A.1 is the discrete CSA used to test and characterize the PVDF sensor.

Bibliography

[1] K. Lee, H. Y. Chae, K. Park, Y. Lee, S. Cho, H. Ko, and J. J. Kim, "A multi-functional physiological hybrid-sensing e-skin integrated interface for wearable IoT applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 6, pp. 1535–1544, 2019.

[2] J. A. Schmitz, J. M. Sherman, S. Hansen, S. J. Murray, S. Balkır, and M. W. Hoffman, "A low-power, single-chip electronic skin interface for prosthetic applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 6, pp. 1186–1200, 2019.

[3] S. P. Division, *Piezo Film Sensors Technical Manual*. Measurement Specialties, Norristown, Pennsylvania, 1999.

[4] J. Yang, W. Cheng, and K. Kalantar-zadeh, "Electronic skins based on liquid metals," *Proceedings of the IEEE*, vol. 107, no. 10, pp. 2168–2184, 2019.

[5] A. Ibrahim, M. Valle, L. Noli, and H. Chible, "FPGA implementation of fixed point CORDIC-SVD for E-skin systems," in *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 318–321, 2015.

[6] W. Taube, F. Liu, A. Vilouras, D. Shaktivel, C. G. Nunez, H. Heidari, F. Labeau, D. Gregory, and R. Dahiya, "Modelling of nanowire FETs based neural network

for tactile pattern recognition in e-skin," in *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pp. 572–575, 2016.

[7] Y. Abbass, M. Saleh, S. Dosen, and M. Valle, "Embedded electrotactile feedback system for hand prostheses using matrix electrode and electronic skin," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 5, pp. 912–925, 2021.

[8] M. Franceschi, L. Seminara, L. Pinna, M. Valle, A. Ibrahim, and S. Dosen, "Towards the integration of e-skin into prosthetic devices," in *2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 1–4, 2016.

[9] M. Franceschi, L. Seminara, S. Dosen, M. Strbac, M. Valle, and D. Farina, "A system for electrotactile feedback using electronic skin and flexible matrix electrodes: Experimental evaluation," *IEEE Transactions on Haptics*, vol. 10, no. 2, pp. 162–172, 2017.

[10] T. Instruments, *32-Channel, Current-Input Analog-to-Digital Converter*. Texas Instruments, Dallas, Texas, 2004.

[11] W. Gao, H. Liu, D. Gao, B. Gan, T. Wei, and Y. Hu, "Sensroc4: An multichannel low-noise front-end readout ASIC dedicated to CZT detectors for PET imaging," in *2013 3rd International Conference on Advancements in Nuclear Instrumentation, Measurement Methods and their Applications (ANIMMA)*, pp. 1–6, 2013.

[12] K. M. AbdelMoneim and S. A. Mahmoud, "3V CMOS rail to rail op-amp," in *2007 Internatonal Conference on Microelectronics*, pp. 373–376, 2007.

[13] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[14] S. Tumati, "Design of large time-constant switched-capacitor filters for biomedical applications," Master's thesis, Texas A&M University, College Station, TX, December 2004.

[15] J. Mei, X. Shen, H. Zhou, F. Ye, and J. Ren, "A low kickback noise and offset calibrated dynamic comparator for 2b/c SAR ADC," in *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1–3, 2014.

[16] Z. Pan, "A low-power, low-area 10-bit SAR ADC with length-based capacitive DAC," Master's thesis, University of Nebraska Lincoln, Lincoln, NE, December 2022.

[17] P. Harpe, "A compact 10-b sar adc with unit-length capacitors and a passive FIR filter," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 636–645, 2019.