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A Low-Power, Low-Area 10-Bit SAR ADC with Length-Based Capacitive DAC

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A LOW-POWER, LOW-AREA 10-BIT SAR ADC WITH LENGTH-BASED CAPACITIVE DAC

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A 2.5 V single-ended 10-bit successive-approximation-register analog-to-digital converter (SAR ADC) based on the TSMC 65 nm CMOS process is designed with the goal of achieving low power consumption (33.63 pJ/sample) and small area (2874 μm^2). It utilizes a novel length-based capacitive digital-to-analog converter (CDAC) layout to achieve low total capacitance for power efficiency, and a custom static asynchronous logic to free the dependence on a high-frequency external clock source. Two test chips have been designed and the problems found through testing the first chip are analyzed. Multiple improved versions of the ADC with minor variations are implemented on the second test chip for performance evaluation, and the test method is explained.

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Chapter 1

Introduction

1.1 Background

In a mixed-signal system-on-chip (SoC), it is essential to have analog-to-digital converters (ADCs) to bridge the gap between the real-world analog signal and the digital signal, in which form the signal is usually stored and processed.

Nowadays, ultra-low-power SoCs are becoming more extensively needed, as battery-powered applications that involve massive amounts of sensing, such as mobile and Internet of Things (IoT) devices, emerge rapidly over the time. Low-power, low-area ADCs with moderate resolution (8-16 bit) and speed (10-100 MSPS) are well suited for these applications, and advances in this type of ADC not only allows for longer battery life, but also reduces cost due to its smaller chip area.

1.2 ADC Architectures

Among all ADC architectures, successive approximation register (SAR) ADCs meet all the criteria for ultra-low-power, medium resolution, and medium speed applications the best.

While sigma-delta ADCs provide extended resolution with low noise, they usually

have lower signal bandwidth and higher power consumption due to oversampling. A good example is presented in [8]. The paper introduces a sigma-delta ADC design with 22.3 bits of equivalent dynamic range but only 1 kHz of signal bandwidth. As for power, the ADC consumes 12.7 mW at 640 kSPS output rate.

At the other end, flash ADCs can sample as fast as 10 GSPS, but they require a huge number of resistors and comparators, as well as the succeeding error correction logic, indicating large area and higher power. This makes the flash architecture only suitable for low resolution ADC designs. According to a long-term ADC performance survey [4], all the included flash ADC designs use 6 bits or lower.

Between the two extremes, SAR ADCs physically implement the efficient binary search algorithm to search for the input voltage within its input range, and have a very low power consumption naturally.

1.3 SAR ADC Fundamentals

A single-ended SAR ADC consists of a sample-and-hold circuit to store the input analog voltage at a certain moment, a digital-to-analog converter (DAC) to generate voltages to be compared against the sampled analog voltage, a comparator, and a logic block to control the process. In practice, the most common implementation combines the sample-and-hold circuit and the DAC into a capacitive DAC (CDAC) to save area and power. Binary-weighted capacitors inside the CDAC enable both temporarily holding the analog voltage and shifting it based on digital input through charge-redistribution. In SAR ADCs with a CDAC, comparisons are carried out between a common-mode voltage and the CDAC's output. The block diagrams in Figure 1.1 show how the components are connected in both typologies.

Generally, a SAR ADC finds the corresponding digital code through comparing

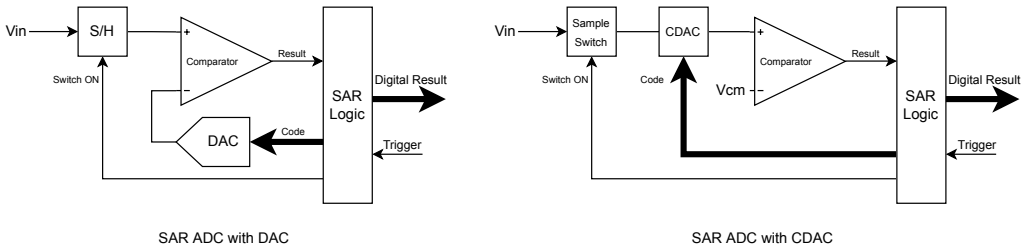


Figure 1.1: SAR ADC Block Diagrams

and trying to match the DAC output with the analog input voltage. The code sent to the DAC that generates the closest voltage is the final digital result. The whole process is based on the binary search algorithm, and for an N-bit ADC, N comparisons are needed for a conversion. Example waveforms of 4-bit ADCs are given in Figure 1.2. Illustrated in the left plot (conversion waveform of a DAC based SAR ADC), starting by comparing half the V_{ref} (V_{dd} in this case) against the stored input voltage, the ADC can determine whether the input is within the range $(0, \frac{V_{ref}}{2})$ or $(\frac{V_{ref}}{2}, V_{ref})$, hence deriving the most significant bit (MSB). Knowing the first comparison result, the ADC changes the internal DAC voltage by $\frac{V_{ref}}{4}$ towards the input voltage, and then perform the next comparison to find if the new DAC voltage is higher than the input or not. Based on the result, DAC voltage is shifted towards the input voltage again, but this time, with half the step size, $\frac{V_{ref}}{8}$. Following that is another comparison. This cycle continues with the step size cut in half every bit until the least significant bit (LSB) of the DAC code is determined. Through the four approximation steps, the DAC output voltage is now as close to the analog input as possible, and the analog voltage can be represented using $V_{analog} = \frac{DAC\_Code}{2^4-1} \times V_{ref}$.

When CDAC is used in place of separate DAC and sample-and-hold circuit, the analog input signal is directly loaded onto the CDAC. With the CDAC digital code set to the middle initially during sampling, its voltage can swing within the approximate range of $(V_{analog} - \frac{V_{ref}}{2}, V_{analog} + \frac{V_{ref}}{2})$. While the conversion process and the output

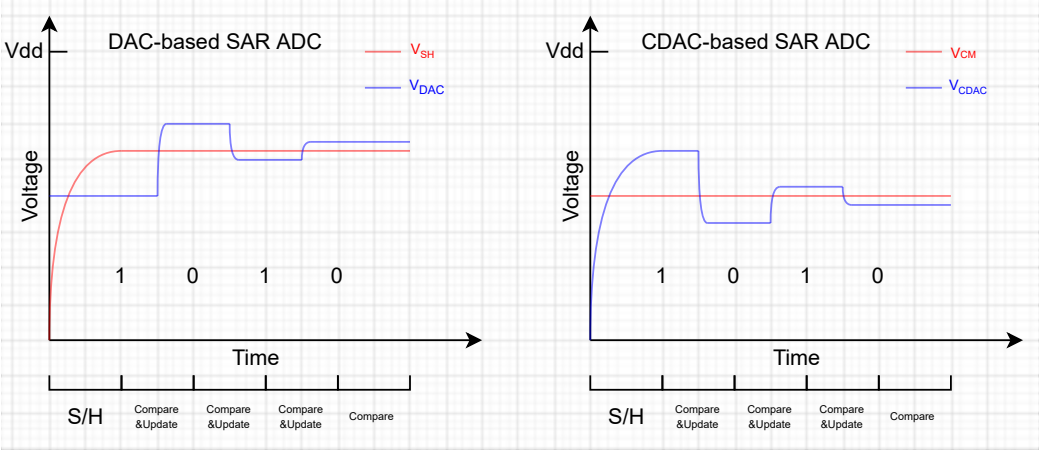


Figure 1.2: SAR ADC Conversion Waveforms

result stay the same, the CDAC voltage successively approaches a common mode voltage instead of the input voltage.

In Figure 1.2, the input voltage for both ADC types is set to 21/32 of V_{dd}. Though the output code is the same in both cases, the comparison result to digital output mapping is different. When the DAC voltage is lower than the input, the digital result for the bit is a "1". By contrast, when the CDAC voltage is lower than the common mode voltage, the output is a "0". Both, however, try to adjust the DAC/CDAC voltage closer towards the input voltage/common mode voltage.

1.4 Motivation

Industry and academic mixed-signal applications need ultra-low-power and area-efficient SAR ADCs that can be easily driven without substantial buffering. One popular method to reduce SAR ADC power consumption and area is using optimized switching schemes, such as the "set and down" monotonic scheme [2], the V_{cm}-based scheme [10], and the tri-level scheme [9]. These particular schemes respectively cut down the CDAC switching power by 81.26%, 87.52%, and 96.89%, and the CDAC

area by 50%, 50%, 75%, compared to the conventional method. However, almost all advanced switching schemes require a differential topology, and some also need a third buffered voltage besides the V_{ss} and V_{dd} for switching the CDAC, which introduces extra area, power, and complexity.

Unlike advanced switching schemes, lowering total CDAC capacitance is a universal and more efficient approach to reduce power and area. CDAC size in the past designs is mainly limited by component matching, and the conventional method of connecting exponentially increasing numbers of large unit capacitors to achieve good matching makes the total capacitance and area scale even faster in high resolution ADCs. Fortunately, a new length-based capacitor matching technique [1] offers a way to reduce the number of unit capacitors required while maintaining high linearity by leveraging the increased precision of lithography in modern CMOS technologies. This is a promising method for research requiring low-power and low-area ADCs.

1.5 ADC Performance Metrics

1.5.1 Sampling Rate

Sampling rate describes how fast an ADC is able to perform conversions, measured in samples per second (SPS). A faster sampling rate reduces the aliasing caused by an unfiltered signal that has higher frequency than the Nyquist limit. It also leads to finer time resolution in a data acquisition system. A SAR ADC's highest sampling rate is usually below 100 MSPS, and is highly dependent on the CDAC and the comparator design because the former has large RC delay, slowing down both sample-and-hold and voltage settling between comparisons. The latter, given the number of comparisons performed in one conversion, has an accumulated impact on the speed.

1.5.2 Power

The power of a SAR ADC is usually rated in milliwatts at the highest sampling rate, or it can also be described by the energy needed for one conversion (joule per sample). The power consumption can be divided into quiescent power, such as leakage and bias power, and dynamic power from digital logic and CDAC switching. In a single-ended SAR ADC, the power of the voltage divider for generating common mode voltage and the leakage of the CDAC make up a significant part of the quiescent power. On the other hand, the comparisons, the logic, and the CDAC voltage shifting are the three major sources of dynamic power.

1.5.3 Linearity

The linearity of an ADC significantly affects the accuracy of the digital output code. Nonlinearities can be presented in two forms: differential nonlinearity (DNL) and integral nonlinearity (INL).

DNL describes the difference in analog voltage range between two consecutive digital codes. Ideally, each digital code represents a small segment of the analog voltage, and all the segments have the same width. When one segment is wider or narrower than its neighbor segments, DNL is present. In an extreme case, the segment becomes wide enough (> 1 LSB) that it completely truncates the neighbor segments. Then, there will be missing codes, meaning no unique digital code will be mapped to truncated segment of the analog voltage. In DNL plots, a value of -1 indicates a missing code. A SAR ADC's DNL is mainly affected by capacitor mismatch in the CDAC, and it is the most significant around the middle code where every capacitor switches, accumulating the errors from each.

INL is an integral of DNL, and it describes the how much the analog-to-digital

mapping deviates from the ideal linear one. A perfect analog-to-digital domain transfer characteristic is a straight line (before quantization), but with added INL, the transfer function becomes a curve.

1.5.4 Signal-to-Noise-and-Distortion Ratio (SINAD/SNDR)

SINAD, or SNDR, is a combination of the more commonly used signal-to-noise ratio (SNR) and total harmonic distortion (THD). The difference between the two is their relationship to the signal. While noise is uncorrelated to the signal, distortion only shows up when signal is present. Both are valuable criteria when it comes to ADC performance evaluation. This is because the distortion caused by harmonic/nonlinearity and the thermal/flicker/jitter/quantization noise all can significantly degrade ADC's accuracy. SINAD is a unified metric for quantifying how well an ADC preserves signal fidelity.

The following equation shows how SINAD is defined.

$$SINAD = 10\log_{10}\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right) = -10\log_{10}(10^{-SNR/10} + 10^{-THD/10}) \quad (1.1)$$

From the equation, it is obvious that SINAD varies with the input signal magnitude. Thus, it usually assumes full-scale input swing, and the calculated value represents the highest achievable SINAD.

The ideal SINAD considering only quantization noise for an N-bit ADC is given by the standard equation:

$$SINAD_{ideal} = N \times 20\log_{10} 2 + 20\log_{10}\sqrt{\frac{3}{2}} \quad (1.2)$$

In case of a 10 bit ADC, this number is at around 61.97 dB.

1.5.5 Effective Number of Bits (ENOB)

ENOB is a more intuitive way of representing SINAD. An N-bit ADC with M bits of ENOB has a SINAD level equal to the SNR level of an ideal M-bit ADC that only has quantization noise. Practically, M is always smaller than N because of the added noise from other sources and distortion. ENOB can be derived from measured SINAD through the following equation:

$$ENOB = \frac{SINAD_{max} - 20\log_{10}\sqrt{\frac{3}{2}}}{20\log_{10}2} \tag{1.3}$$

1.5.6 Analog Input Range

The analog input range is the range of the input voltage that can be reliably converted into digital code without clipping to zero or maximum. A SAR ADC is not a rail-to-rail device due to the unswitchable parasitic capacitance narrowing the CDAC output swing. A wider analog input range benefits maximum SINAD and ENOB because higher signal power is allowed.

1.6 Thesis Outline

In Chapter 2, details are given on the ADC design at both component level and assembly level. In particular, a single-ended implementation of a 10-bit SAR ADC using a length-based CDAC design, which is adapted from a fully-differential version [1], is presented. Discussions on the components' design challenges and the consideration behind the design choices are included. Further, design schematic and layout will be given as well as the simulation result on the analog extracted circuit.

Chapter 3 talks about ADC testing. The chapter includes the integration of the two fabricated test chips as well as the testbench setups and test methods. Further,

the test result of the first chip is analyzed and the improvements made to the ADCs in the new test chip are listed.

Chapter 4 is a summary of the thesis work.

Chapter 2

Design and Simulation

2.1 Capacitive DAC (CDAC)

2.1.1 Overview

In a SAR ADC, a CDAC that also works as the sample-and-hold capacitor is commonly used. It provides an easy way to modify the sampled voltage through charge redistribution. For instance, a conventional top-plate sampling 5-bit CDAC is shown in Figure 2.1.

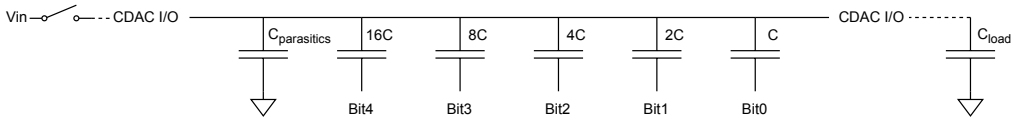


Figure 2.1: CDAC Example Schematic

There are five capacitors with binary-weighted capacitance. Their top plate is merged together into the CDAC input/output that can drive a small capacitive load, which, in this ADC, is the comparator's input. The bottom plates are, instead, driven by the digital codes, switching to either V_{dd} or V_{ss}. After the input voltage is sampled onto the top plate and the sample switch is open, a single bit change in the digital

code will shift the output to a new voltage calculated in the following equation:

$$V_{DAC} = V_{sampled} \pm \frac{C_{bit}}{16C + 8C + 4C + 2C + C + C_{load} + C_{parasitics}} * V_{dd} \qquad (2.1)$$

where C_{bit} represents the corresponding capacitance of the changed bit. A switch from 0 to 1 in a bit will have a plus sign in the equation and vice versa. The term, $C_{load} + C_{parasitics}$, is fixed and it attenuates the voltage swing of the CDAC.

Conventional CDAC designs usually dominate both power consumption and area in a SAR ADC. To achieve the precisely binary-weighted capacitance, the CDAC bits are made by connecting exponentially increasing numbers of unit capacitors in parallel. This method offers the needed matching and linearity that using exponentially larger monolithic capacitors lacks. However, it requires the unit capacitors to be large in size to minimize the capacitance error introduced by both process variation and interconnect parasitics. Obviously, this requirement leads to larger area, higher and fast-scaling total capacitance due to the large number of units (1023 for 10-bit ADCs), thus higher power because more charge is needed to change the voltage.

It is common to see conventional CDACs' total capacitance in the picofarad range just to meet the matching requirement. However, regardless of the need for matching, a CDAC can be designed with a much more relaxed noise constraint. Calculated using $V^2_{noise,rms} = kT/C = (1.38 \times 10^{-23}) * 300/C_{cdac}$, the CDAC noise decreases with the increasing total capacitance, and this noise needs to be low to ensure the CDAC's resolution. Fortunately, the targeted 10-bit 2.5 V (around 2 V swing range) ADC requires merely 4.341 fF total capacitance (over 200 times less than the conventional matching-restricted design) to keep CDAC noise below half the LSB voltage.

Thus, to make a power-efficient and area-efficient CDAC, it is crucial to reduce the total capacitance and improve matching among small capacitors. Overall, an in-

terdigitated MOM (metal-oxide-metal) capacitor is preferred over parallel-plate MIM (metal-insulator-metal) capacitor because of its inherently higher capacitance density, better matching, and lower parasitics in the used 65 nm technology. The former with its less strict design rules also allows for highly customized and compact layout. Futher, by increasing the spacing between fingers, the MOM capacitor can be made lower capacitance at the expense of larger area, and according to [5], it would maintain similar matching performance. On the contrary, MIM capacitors' plate distance is fixed by the CMOS technology and their matching is tightly coupled to their area and capacitance, making them less flexible.

2.1.2 Topology

A novel CDAC topology used in the ADC has a mix of length-based and number-based bits to cut down the area and capacitance by reducing the number of units. It also introduces a capacitance "subtraction" approach to realize equivalent ultra low LSB capacitance while taking advantage of the good matching from the long finger length. This topology was originally proposed by Harpe et al. in [1].

An illustration of this topology is shown in Figure 2.2. In this CDAC, the outermost metal frame works as the common top-plate while the metal stripes inside form the bottom plates of the bit capacitors. Each row consists of two capacitors with different length. It is well-established that a fringe MOM capacitor's capacitance is proportional to the finger length. Thus, when driving the two capacitor strips in a row with inverted digital signals, the CDAC output voltage will change in a way as if a small capacitor defined by the stripe length difference was used. The following text will refer the longer finger as the positive capacitor (C_{pos}) and the shorter one as negative capacitor (C_{neg}). For example, when driving the positive capacitor from V_{ss} to V_{dd} and the negative capacitor from V_{dd} to V_{ss}, the change in CDAC output

voltage can be written in the following equation:

$$\Delta V_{CDAC} = \frac{C_{pos} - C_{neg}}{C_{pos} + C_{neg} + C_{other\_bits} + C_{load} + C_{parasitics}} * V_{dd} \tag{2.2}$$

where C_{other_bits} is the sum of capacitance of all other positive and negative capacitors in the CDAC. This capacitance "subtraction" technique brings the good matching performance of the long finger length to the small equivalent capacitors, making matching between effective attofarad capacitors possible. Furthermore, the symmetrical layout cancels out the edge effect at the ends of the strips in a pair of positive and negative capacitors.

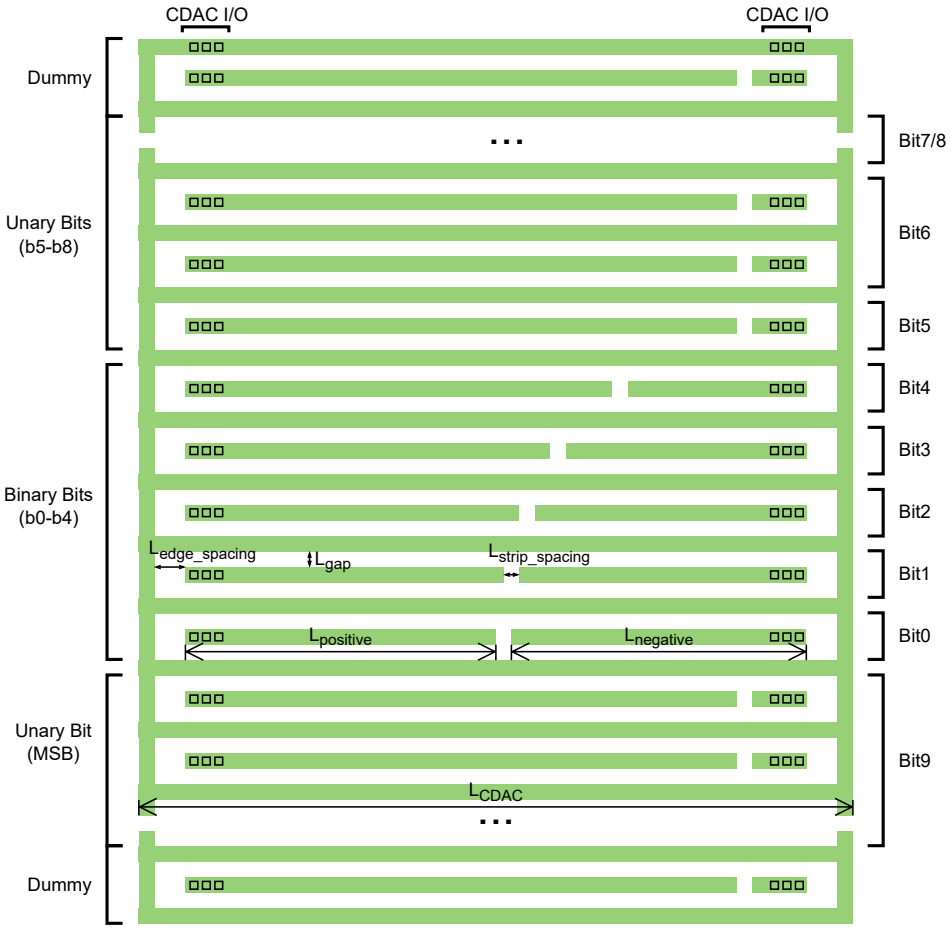


Figure 2.2: CDAC Layout Topology and Dimensions

Being able to make this type of matched tiny effective capacitors is not beneficial on its own. In fact, it has some disadvantages. To begin with, it introduces good matching among the small equivalent capacitors at the cost of a higher total capacitance (higher power) and area. Also, seen from the equation, another downside of this technique is the reduced swing range because the equivalent capacitance ($C_{pos} - C_{neg}$) in the numerator is always lower than the total finger capacitance ($C_{pos} + C_{neg}$) in the denominator. In other words, the lower the ratio of the equivalent capacitance to the total capacitance, the narrower the swing range. Consequently, the lowered signal swing range and signal power also hurt the CDAC's SNR. In addition, according to the test result in the original paper [1], the matching performance will suffer from lower equivalent capacitance ratio as well.

The real advantage of this topology is the large saving in the CDAC area and total capacitance when used in the lower bits of a CDAC. By properly varying the finger length difference in these bits, a binary scaled equivalent capacitance can be easily achieved without doubling the total capacitance and area every higher bit. In Figure 2.2, these length-based bits are labeled as binary bits. These bits prevent the unit capacitor number from scaling exponentially, and the CDAC area and total capacitance saved from this number reduction would far outweigh the performance loss due to the binary bits.

While a small number of binary bits will significantly reduce the CDAC area and total capacitance, it is not optimal to use only binary bits in a 10-bit SAR ADC. There are mainly two reasons. Firstly, the exponentially increasing length difference means the CDAC will have to be really long, which not only defeats the goal of small area and low capacitance, but also makes the CDAC prone to global process variations. Second, the lower equivalent capacitance ratio in the binary bits accentuates all the downsides mentioned previously.

Practically, for the higher bits, connecting multiple unit capacitors to achieving the binary scale is preferable to avoid the long layout length. Unlike the conventional layout where each unit is a single capacitor, the unit in this case is, similar to the binary bits, a pair of positive and negative capacitors. It needs the minimally-sized negative capacitor just to keep the symmetry of the structure. These number-based bits are referred to as unary bits in Figure 2.2.

Mixing binary and unary bits, the total number of units needed for the entire CDAC can be calculated using the following equation:

$$N_{unit} = N_{binary\_bits} + 2^{N_{unary\_bits}} - 1 \tag{2.3}$$

and the total CDAC capacitance is roughly the number of units times the capacitance of each unit.

Among binary bits, the matching is mainly based on structural similarity. Although this length-based capacitance scaling method has not been widely adopted and verified, it was practically proven capable of meeting the matching requirement for the 10-bit differential ADC with 9.18 bit ENOB in the original paper [1]. On the other hand, unary bits follow the conventional method of connecting identical units to improve matching. Interestingly, the first unary bit with a single unit bridges the matching between binary and unary bits because it not only has the same layout as all other units in unary bits, but also is, in a sense, length-based with double the equivalent capacitance of the last binary bit.

2.1.3 Layout Dimensions And Analog Extraction

The 10-bit CDAC used in this single-ended ADC has 36 unit capacitors, and it consists of 5 binary bits and 5 unary bits to target a reasonable balance between the equivalent

capacitance ratio and the total capacitance. The layout is shown in Figure 2.2.

In this layout, the MSB capacitor is put on the other side compared to the rest of the bits, and one unary dummy unit is inserted on each end of the CDAC. The small black rectangles in the figure are vias. The ones at the end of the capacitor fingers connect the metal strips down to the CDAC driver, whereas the ones at the top work as the CDAC input and output port.

Concretely on the dimensions, the CDAC has a total length (L_{CDAC}) of 51.44 μm. The green wires are metal on layer 6 and 7, and all of them have a width of 0.12 μm. L_{gap} and $L_{strip\_spacing}$ are both 0.13 μm, and $L_{edge\_spacing}$ is 1.15 μm. As for the capacitor fingers, since the figure is not to scale, detailed specifications are listed in Table 2.1. $C_{equivalent}$ represents the extracted effective capacitance.

Table 2.1: CDAC Layout Dimension and Extracted Capacitance

Bit	Type	$L_{positive}$ (μm)	$L_{negative}$ (μm)	ΔL (μm)	$C_{positive}$ (fF)	$C_{negative}$ (fF)	$C_{equivalent}$ (fF)	C Ratio
0	Binary	24.985	23.785	1.2	8.29403	7.89795	0.39608	1.000
1	Binary	25.585	23.185	2.4	8.49207	7.69991	0.79216	2.000
2	Binary	26.785	21.985	4.8	8.88815	7.30383	1.58432	4.000
3	Binary	29.185	19.585	9.6	9.68031	6.51167	3.16864	8.000
4	Binary	33.985	14.785	19.2	11.2646	4.92734	6.33726	16.000
5	Unary	43.585	5.185	38.4	14.4333	1.75870	12.6746	32.000
6	Unary	43.585×2	5.185×2	76.8	28.8752	3.52604	25.34916	64.000
7	Unary	43.585×4	5.185×4	153.6	57.7591	7.06074	50.69836	128.000
8	Unary	43.585×8	5.185×8	307.2	115.534	14.1377	101.3963	256.000
9	Unary	43.585×16	5.185×16	614.4	231.062	28.2689	202.7931	512.000

Seen from the extraction result, the total CDAC capacitance is 583.37554 fF, which is much higher than the previously calculated minimal required capacitance. Also, having a total of 405.18998 fF of effective capacitance, the estimated swing range of this CDAC is around 1.739 V. The actual number will be slightly lower due to the added parasitic capacitors.

Though the extraction result shows perfect binary scaling when it comes to the effective capacitance, the actual performance is yet to be silicon verified because there is no statistical performance data of this custom layout for linearity simulation.

2.2 CDAC Driver

Simple as it is, the CDAC driver is a series of inverters designed to drive the CDAC fast enough to meet the clock timing, while maintaining balanced parasitic capacitance on the positive and negative halves of the CDAC. Every single inverter is kept at minimal length, 280 nm, and a width of 2 μm for PMOS and 1 μm for NMOS. The transistor multiplier is used to increase the total width of the inverter. This method makes it easier to put all the inverters inside a rectangular area. In bit 0 to 5, only one inverter is used in each bit. For higher bits, a binary scaled number of the inverters are connected in parallel to achieve a higher drive strength. From bit 6 to 9, the numbers of inverters in each bit are 2, 4, 8, and 16. The final layout is shown in Figure 2.3.

Figure 2.3: CDAC Driver Layout

In the layout, there are two horizontally mirrored blocks of inverters placed beneath the two ends of the CDAC for easier routing. The space between the two blocks is left empty for the logic blocks and the level shifters that are discussed later.

The simulation result of the analog extracted ADC shows that, with this driver, the CDAC can settle within 450 ps (the worst case) after the bit data input is updated. Given the simulated total logic delay before the comparison is over 1 ns, there is over 550 ps of timing slack.

2.3 Sample Switch

2.3.1 Overview

A switch is placed between the CDAC and the analog voltage input, and it is only closed during the sampling phase to allow the CDAC to be charged or discharged to the input voltage. Intuitively, a switch can simply be a transmission gate, but the downside is its signal-dependent effective on-resistance ($R_{DS(ON)}$) because of the varying $V_{gs} = V_g - V_{in}$. This problem, on a SAR ADC with a relatively large CDAC capacitance, would cause varying RC delay and transient-voltage-based phase shift distortion on AC signal, lowering the ADC's SINAD. A bootstrapped sample switch solves this problem by using a single pass transistor, whose V_{gs} is independent of the input voltage, and is fixed at a constant voltage equal to V_{dd}. Other than a stable and low on-resistance from the constant and high V_{gs}, a bootstrapped switch also helps preserve the ADC's linearity by having low and linear charge injection from the small pass transistor, which is even more critical when using a small CDAC.

The principle behind bootstrapping is straightforward. When the switch is open, V_{dd} is held across a capacitor. Then, when the switch closes, this charged capacitor is tied between the gate and source of the switch transistor, boosting the gate voltage to $(V_{dd} + V_s) = (V_{dd} + V_{in})$ to get a fixed V_{gs}.

2.3.2 Topology

Shown in Figure 2.4 is the schematic of the sample switch. In the schematic, all transistors are kept at the minimal size (280 nm long, 400 nm wide) except for M0, which has double the width at 800 nm. According to the analog extraction result, C0's capacitance is 204.988 fF.

This design is a slightly modified version of the traditional designs described in [6] and [7]. Here, M0 is the switch transistor and C0 is the bootstrapping capacitor. M0, M1, M3 utilize deep N-well, and the bulk switching on them not only prevents excessive V_{gb} damaging the gate oxide, but also minimizes drain to source leakage caused by body effect while the switch is off.

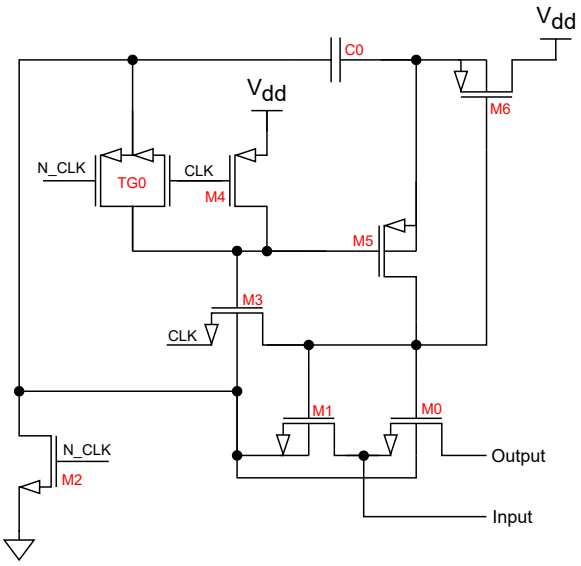


Figure 2.4: Sample Switch Diagram

In "off" state, CLK is low and the complimentary N_CLK is high. Firstly, the transmission gate TG0 is off, but M4 and M2 stay on. While M2 pulls one side of the capacitor down to ground, M4 turns on M3 and disables M5. The low CLK signal present on the source of M3 would sink all the charge stored on the gate of M0, M1, and M6. Thus, M0 and M1 are turned off, isolating the input. M6, on the contrary,

is activated to charge C0 to V_{dd}.

When turning on the switch, TG0 is turned on while M2 and M4 are turned off. At the same time, the source and drain on M3 swap their roles and the current starts to flow from the positive CLK into the gate of M0/1/6. This "precharging" phase does not last long as M3 is turning off. Following it, M5 begins to conduct, and the gate voltage of M0/1/6 is further boosted by the charge from C0. As a result, M6 disconnects the right side of the capacitor from V_{dd}, and the input voltage is exposed to the left side of the capacitor through M1, lifting the right side by the same amount. M0's gate, connected to the capacitor's right side through M5, is now bootstrapped.

In this topology, an important difference from the original design in [6] is the use of TG0 and M4 in place of N_CLK to drive M5's gate. The reason is that, when driven by a clock that is at 0 V when the switch is closed, M5 can experience a maximum of 5 V V_{sg} when the switch input voltage is at 2.5 V. Since the used technology does not have transistors that tolerate 5 V (1 V, 2.5 V, 3.3 V available), TG0 and M4 are introduced to clamp M5's V_{sg} down to 2.5 V.

2.3.3 Design Considerations

2.3.3.1 On-resistance

To get a consistently low on-resistance across the input voltage range, V_{gs} on the switch transistor needs to be high and stable. This usually means the increasing size of C0 because the charge stored on it is shared across multiple FETs when the switch turns on, and the gate voltage can be approximated using:

$$V_g = V_{in} + \frac{C_0}{C_0 + C_{tot}} * V_{dd} \tag{2.4}$$

where C_{tot} represents the sum of all the gate capacitance and parasitics attached to the right side of the capacitor. Seen from Equation 2.5, one way to boost gate voltage is to increase C_0 and reduce the number of FETs that share the charge. This design uses a transmission gate TG0 in place of a bootstrapped NMOS seen in the conventional design in [7], reducing the number of FETs sharing the charge by one. Without bootstrapping, TG0 introduces variable on-resistance. Fortunately, thanks to the small gate capacitance of M3 and M5, the negative effect on the switch transistor gate voltage is negligible when the input signal is under 100 MHz.

Other than reducing the charge sharing, this design also introduces a precharging mechanism though M3. The clock that is connected to M3 can discharge the gates of M0/1/6 when the switch is turning off, but it can also precharge them (drain and source nodes flip on M3) before they source charge from C0 when turning on. This effectively turns the gate voltage equation into the following:

$$V_g = V_{in} + V_{pre} + \frac{C_0}{C_0 + C_{tot}} * (V_{dd} - V_{pre}) \tag{2.5}$$

The reduced dependency on $C0$ allows smaller capacitor to be used to achieve the same gate voltage.

2.3.3.2 Charge Injection

Besides low on-resistance, charge injection also affects the ADC's linearity. When the switch is turned off, the negative channel charge in M0 escapes through the source and the drain terminals, resulting in a voltage drop on CDAC. Simulation has proven that the charge injection amount is signal dependent, and it is impossible to keep the voltage drop within half the LSB even with the smallest transistor size given the small CDAC. The goal now becomes making the injection amount as linear

as possible, turning this error into a gain/offset error that can be easily calibrated digitally. Through trial and error, TG0 turns out to be the key component. One possible explanation is that using a bootstrapped NMOS (referred to as MB in the following text) here as in the conventional design [7] instead of a transmission gate significantly slows down the turn-off process, especially when the input voltage is low (can be as long as several nano seconds). This is because this bootstrapped NMOS can only be turned off by discharging its gate, which is the same node as the pass (switch) transistor's gate. However, C0 will not be disconnected from this gate until M5 is disabled, which, interestingly, requires MB to be off first. This interdependency ends up discharging C0 and slowing down the turning off when the input is low because M5 is held on. With the slow turning off speed, the channel charge on M0 is less likely to evenly bleed out through its drain and source but rather take the path with lower impedance, thus the non-linear charge injection.

2.3.4 Layout

Figure 2.5 is the layout of the sample switch. Sitting at the top left corner are all the deep-N-well transistors. The vertical strips made of metal 1 to 3 layers form the bootstrap MOM capacitor.

2.3.5 Simulation

The circuit setup for testing the sample switch is shown in Figure 2.6.

The 200 Ohm resistor is an overestimation of the total resistance on the ADC signal input line in the actual chip including the 100 Ohm resistor used in the ESD protection structure. The 600 fF capacitor represents the CDAC and the parasitic capacitors. In the test, the capacitor is first discharged by setting Vin to 0 V and closing the switch for a long enough time. Then, the switch is opened and Vin is set

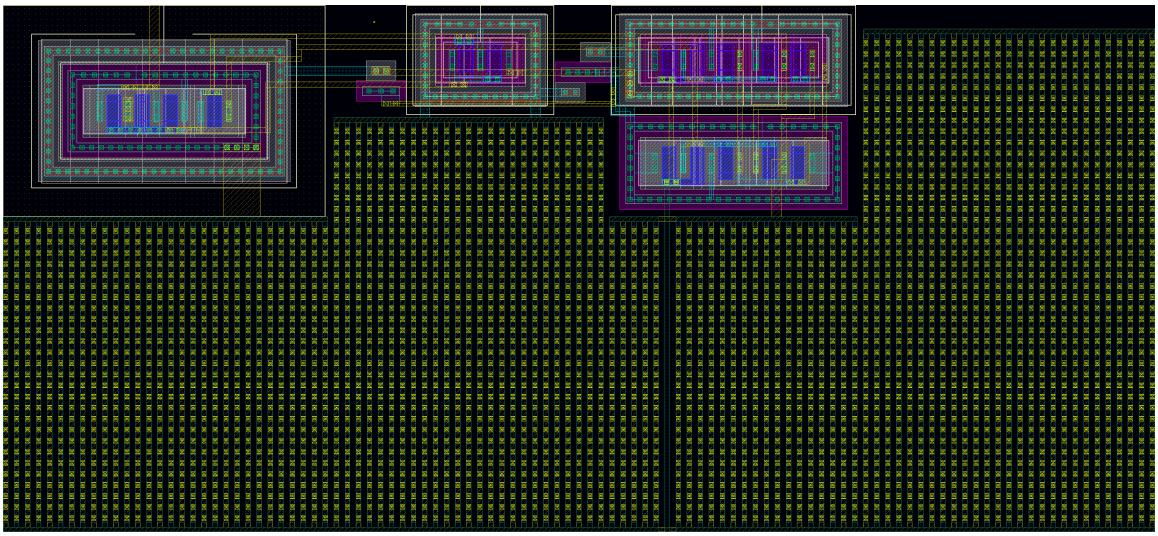


Figure 2.5: Sample Switch Layout

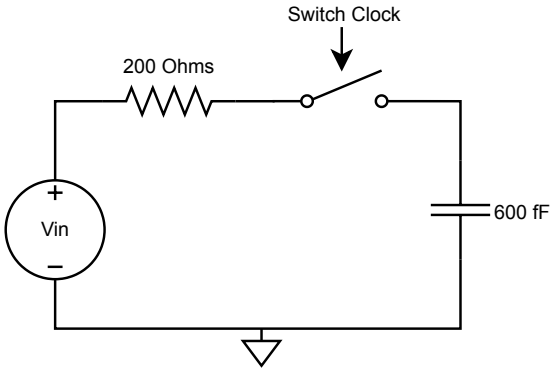


Figure 2.6: Sample Switch Simulation Circuit

to 2.5 V before the switch is closed again. Then, the time that it takes to charge the capacitor can be measured and it indicates the longest sample and hold time that the ADC needs. A similar method can be used to test the discharging time with Vin set to the opposite voltages. For testing the charge injection effect, the capacitor is first reset to 0 V. Next, different Vin from 0 V to 2.5 V will be supplied for charging the capacitor. After the charging is done and sample switch is disabled, a voltage drop from charge injection is measured and plotted in a graph of input voltage versus charge injection amount. In addition, V_{gs} of the bootstrapped pass (switch) transistor

can be monitored to see the turn-on/turn-off speed, and power consumption of the switch can also be measured.

Table 2.2: Sample Switch Simulation Result Summary

Metric	Performance
Charging Speed (0 V-2.499 V)	7.5 ns
Discharging Speed (2.5 V-0.001 V)	8.2 ns
Turn-on Speed	370 ps
Turn-off Speed	300 ps
Charge Injection	2.99-8.65 mV
Power	162 fJ/switch

The test result is summarized in Table 2.2. Given the charging and discharging speed, a conservative and safe sample and hold duration is around 10 ns. This takes possible process, voltage, temperature (PVT) variations into account, and can make sure the CDAC is brought to the input voltage within the error margin.

Specifically for charge injection, Figure 2.7 shows the injection amount versus the input voltage. Given that the LSB voltage is around 1.7 mV, the slight non-linearity in the curve has marginal effect on the overall ADC linearity.

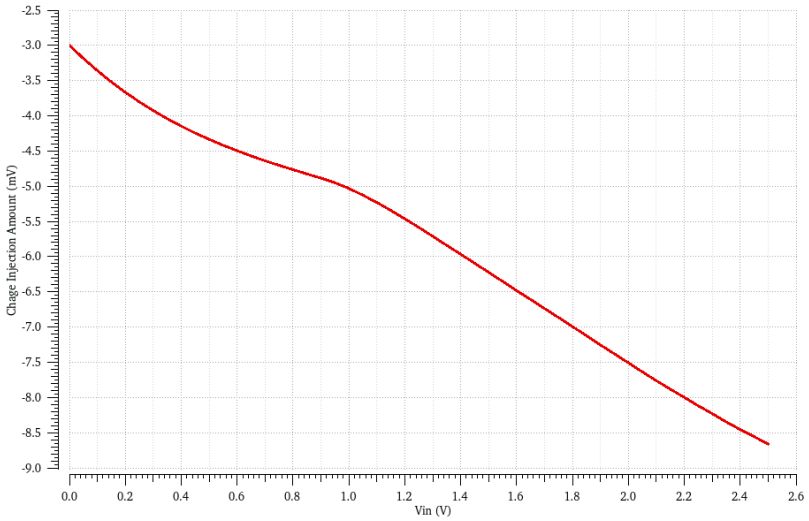


Figure 2.7: Sample Switch Charge Injection Versus Input Voltage

2.4 Comparator

2.4.1 Overview

A SAR-ADC, at its core, relies on a comparator to convert analog voltages into digital bits. Despite its simple function, outputting a "1" when the positive input voltage is higher than the negative input and a "0" vice versa, the comparator can heavily affect the ADC's performance in terms of SNR (signal-to-noise ratio), speed, offset error, power consumption, and so on.

The comparator used in this ADC was designed with the following focuses. To begin with, the transient noise during comparison has to be low enough to support the 10-bit resolution. At the same time, the design also requires low kickback noise because it is more prominent on a CDAC with lower total capacitance. Attention was also paid to some other design goals including low offset, fast speed, low power, no memory effect (hysteresis), and small layout area.

2.4.2 Topology

The comparator design is shown in Figure 2.8, and it was originally proposed in [3]. It consists of ten 2.5 V MOSFETs. M1 through M4 form a pair of cross-coupled inverters that amplifies the voltage difference on the two outputs, and eventually latches onto the result during comparisons. M5/6 and M9-12 are responsible for isolating the input FETs and resetting the cross-coupled inverters during idle, respectively. M7 and M8 are the two input MOSFETs. The transistors use the minimal length 280 nm, and a width of 2 μm for PMOS's and 1 μm for NMOS's.

To perform a comparison, the comparator first starts with the idle state when CLK is low. At this time, cross-coupled inverters are pulled to V_{dd} by the four reset FETs M9-12, and M5/6 are in cut-off state, isolating the two input FETs (M7/8). When

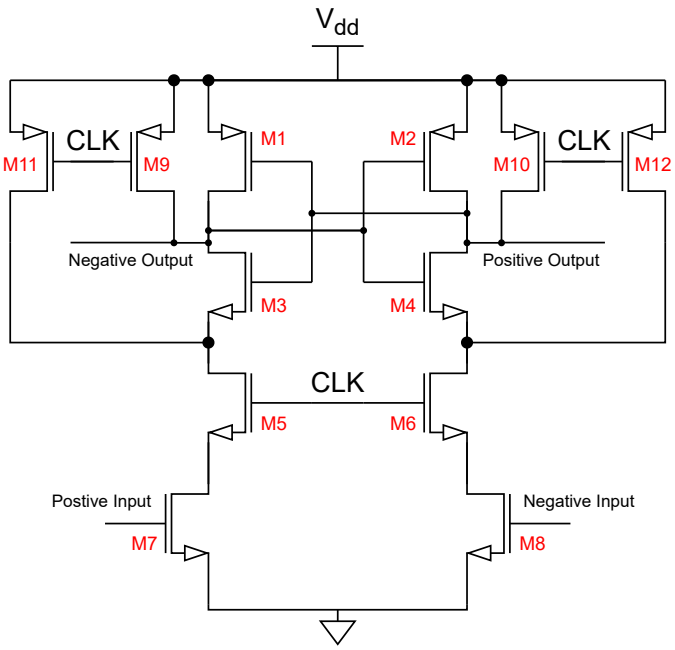


Figure 2.8: Comparator Schematic Diagram

the CLK rises up, the comparison starts. M9-12 no longer pull up the output nodes, and M5/6 starts to allow current to flow through the input FETs. Then, the left and right branches formed by M3/5/7 and M4/6/8 start to discharge at certain rates according to the input voltages, and a small voltage difference starts to appear on the two outputs. Next, the falling voltage on the outputs, as a result, activate M1/2 to enable the regeneration process inside the cross-coupled inverters to further amplify the output voltage difference. Eventually, the output node with a lower voltage will fall to ground, whereas the other output goes up to V_{dd}.

2.4.3 Design Considerations

2.4.3.1 Kickback Minimization

One of the design goals is low kickback. Generally, kickback noise is caused by the capacitive coupling between the drain and the gate of the input FETs (C_{gd}). When a

voltage swing happens on the drain node, charge moves in or out the gate node. This charge, when flowing through resistors or into capacitors (including parasitics) that are connected to the gate, causes a change in the voltage. In case of a SAR ADC, the kickback charge flows into the CDAC and alters its voltage, and this error is even more significant when a single-ended small CDAC is used.

In this design, low kickback noise is achieved by placing the input FETs closest to the ground rail to reduce the swing on the drain nodes and properly sizing them to minimize the charge stored on C_{gd}. The first method largely reduces the voltage swing present on the drain node of the input FETs during a comparison. Assuming the input voltages are always higher than the input FETs' threshold voltage, the drain nodes are always pulled to ground. However, small voltage spikes do exhibit on the drains at the beginning of a comparison when M5/6 are suddenly turned on and the charge rushes into the drain nodes of M7/8. The good thing is that, as the drain nodes get discharged by the input FETs, they will quickly settle back to ground. Overall, the charge is pushed out, and soon, pulled back in to the input gates even before the outputs fully resolve, resulting in minimal impact on the comparator input voltages.

2.4.3.2 Transistor Sizing

When it comes to transistor sizing, a balance among noise, kickback, matching and speed is explored. Larger transistor size improves performance in terms of flicker noise and matching, but it also increases the coupling between gate and drain (larger C_{gd}), leading to worse kickback. Further, transistors with big W/L ratio have the benefit in lower thermal noise and higher transconductance (g_m), which can make the circuit faster. When the input FETs have higher g_m, they pull their drain down to ground more strong, and will have a smaller voltage spike on their drain that causes kickback.

Combining the two factors mentioned above, it is obvious that using minimal length has the advantage in low thermal noise, high g_m, and fast speed while keeping the overall C_{gd} small. Thus, all the transistors use the minimal length 280 nm.

For width, it is examined and chosen to get acceptable flicker noise/matching, drain-gate coupling, and speed. The flicker noise goes down but the other two go up with increasing width, thus a trade-off. All the PMOS's share the same width for layout purposes, and so do the NMOS's. One more consideration behind the chosen widths is related to the meta-stable state voltage, which will be talked about in the next subsection.

2.4.3.3 Meta-stable Voltage

There is always a meta-stable state between the start of the comparison and the full result resolution. In this state, the current difference of the two branches in the comparator is being amplified and turning into the output voltage difference. The voltage from which the outputs deviate from is referred to as the "meta-stable voltage" (shown in Figure 2.9). This voltage, manifesting at the comparator outputs, is related to the drive strength difference of the PMOS versus NMOS, and it is sometimes problematic because the logic circuit that interfaces with the comparator can recognize a low meta-stable voltage as the comparison result (logic low in this case).

To avoid the problem, one method is using extra logic gates to filter the outputs and only shows the result when one output is logic high and the other is at logic low. However, this adds noticeable propagation delay and will slow down the ADC operation, given that 10 comparisons are needed for this ADC. Fortunately, the comparator uses 2.5 V but the logic block works on 1 V, and this comparator topology has logic high at its output when idle. With properly tuned PMOS/NMOS width ratio, the

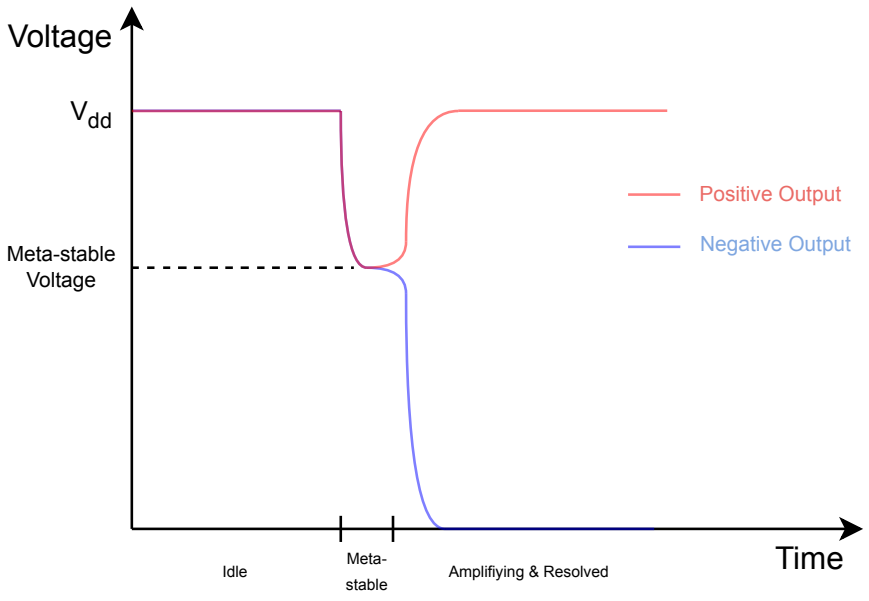


Figure 2.9: Comparison Stages

meta-stable voltage does not fall below 1.3 V across all input voltages and corners. At the output, a single 1 V inverter that also works as the level shifter is enough to eliminate all meta-stable voltage problems. This is because the 1 V inverter's trip-point voltage is around 0.5 V, and both the idle 2.5 V and the meta-stable 1.3 V are recognized as logic high.

2.4.4 Layout

The comparator layout is shown in Figure 2.10. This layout follows the common-centroid method to achieve both horizontal and vertical symmetry among PMOS's and NMOS's as well as all the wires. When process variation happens, each pair of the transistors will be affected similarly, keeping the balance of the two branches in the circuit. At the top of the layout, there is an inverter to buffer the clock signal. Also the two inputs and the big N-well are connected to the substrate through reverse-biased antenna diodes.

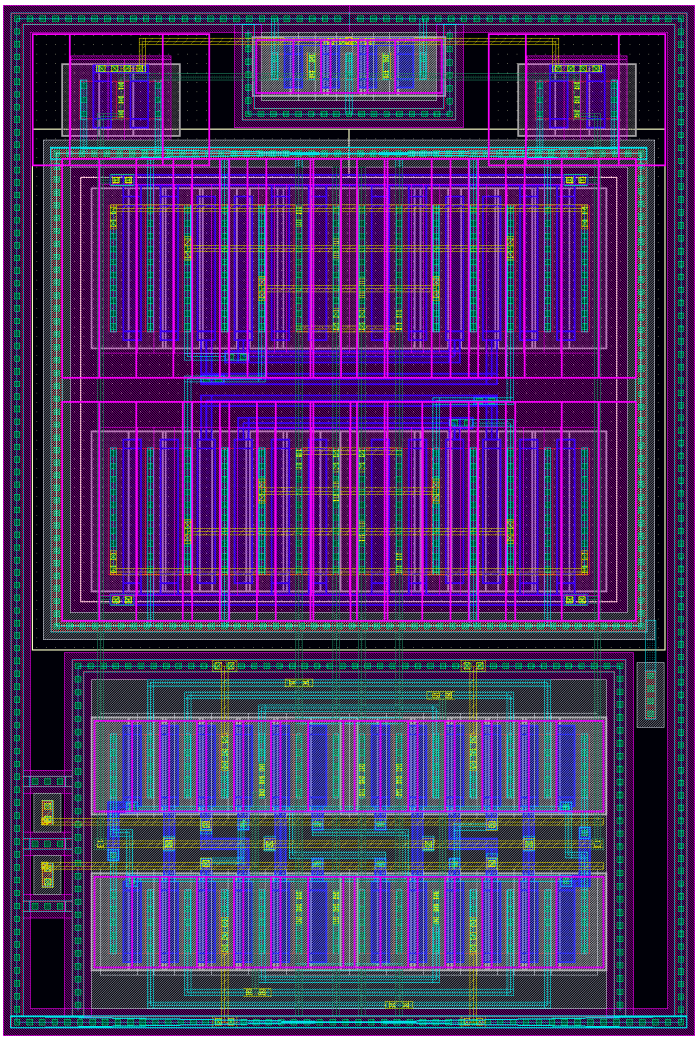


Figure 2.10: Comparator Layout

2.4.5 Simulation

The simulation circuit is shown in Figure 2.11. The idea of this testbench is to resemble the actual circuit inside the ADC. All resistors represent the wire resistance and the capacitors are the CDAC and the common mode voltage bypass capacitor. In the simulation, with Vcm set to 1.25 V initially, the sample switches are closed for 20 ns to charge the capacitors. Following that, the comparator clock starts a comparison and then reset it after 5 ns. During this process, probing the two comparator input

voltages reveals the kickback noise. Energy per conversion is calculated by integrating current flowing into the comparator and multiplying by the 2.5 V supply voltage. Also, looking at the output signals, the propagation delay can be found. For the comparison delay, the duration between the comparison clock reaching 50% and one of the outputs falling below 0.5 V is measured. For the reset delay, it is the time between the 50% clock point and the same previous output reaching 2.499 V. Further, periodic noise analysis is used to simulate the input referred noise of the comparator.

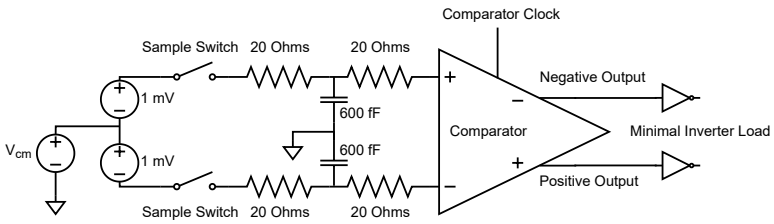


Figure 2.11: Comparator Simulation Circuit

A separate circuit is used for testing the input offset voltage. In the circuit, the comparator is connected to a verilogA model. This model supplies the analog inputs to the comparator, clocks the comparator, and monitors the comparator outputs. One input is always at 1.25 V, while the other one starting from 1.251 V changes based on the comparison result. When the comparison result shows the second input is lower than 1.25 V, the model increases it by a step value, and vice versa. The step value starts at 0.5 V and is multiplied by 0.9 every time the second input voltage is changed. The goal of the model is to find the voltage to the second input that flips the comparison result, or the input offset voltage. With this circuit ready, a Monte Carlo simulation is performed to find the offset voltage distribution.

Using the methods discussed above, the simulation result is listed in Table 2.3.

Table 2.3: Simulated Performance of the Comparator

Parameter	Min	Typical	Max	Unit
Input Offset Voltage	0	±14	±33	mV
Kickback Noise	2.9 (V_{cm} at 2.5 V)	3.8 (V_{cm} at 1.25 V)	5.0 (V_{cm} at 0.5 V)	mV
Input Referred Noise @ Vcm=1.25 V		620		μV
Propagation Delay (Comparison)	300 (Best Corner)	406	544 (Worst Corner)	ps
Propagation Delay (Reset)	200 (Best Corner)	270	350 (Worst Corner)	ps
Energy per Comparison+Reset	1.59 (Best Corner)	1.82	2.09 (Worst Corner)	pJ

2.5 Logic

2.5.1 Overview

A logic block is designed to control the sampling procedure. This procedure can be divided into three consecutive parts: sample and hold, conversion, and reset. To be specific, the sample and hold is when the sample switch is closed and the CDAC is charged to the voltage of the external source. After the sample switch opens again, the conversion phase is when the ADC manipulates the CDAC's voltage and compares it to a fixed common mode voltage to perform the SAR algorithm. Finally, the reset phase logs the conversion result for data output as well as reverting all the changes made to the CDAC code, getting it ready for the next sample. In the following sections, the same terminologies will be used to distinguish the three parts.

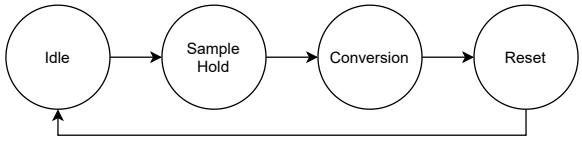


Figure 2.12: Logic State Diagram

The designed logic block is fully-asynchronous. An external pulse triggers the sampling procedure as well as determining the sample and hold duration by its pulse width. At the falling edge of the pulse, the conversion process starts automatically. Then, the resulting code will be latched by D Flip-flops (DFF) after the conversion.

Quickly after that, an ADC ready flag is generated as the ADC becomes ready for a new sample. During the process mentioned above, no external clock is needed as the flow is controlled by different events. Since almost everything happens spontaneously and the speed is limited mostly by the FETs' drive strength and parasitics, ADCs with asynchronous logic do not need a high speed external clock to achieve a fast sampling rate.

In addition, the designed logic block uses static logic, and it consists of S-R latches and other standalone logic gates. Comparing this to a dynamic setup, where certain gate capacitance and manually added capacitors are responsible for controlling the timing, a static one would be more stable and power-efficient. Further, less coupled capacitance in the static logic circuit also means smaller chance of overshoot from clock feed-through. This prevents hazardous voltages from forming on gates during switching. However, one downside of the static logic is the increased area.

With the single-ended ADC configuration, the conventional switching scheme is implemented because of its simplicity. There are four main blocks making up this logic, namely: the sample logic, the bits logics (MSB and non-MSB), the comparator logic, and the data latch. Figure 2.13 is a diagram of how these blocks are connected:

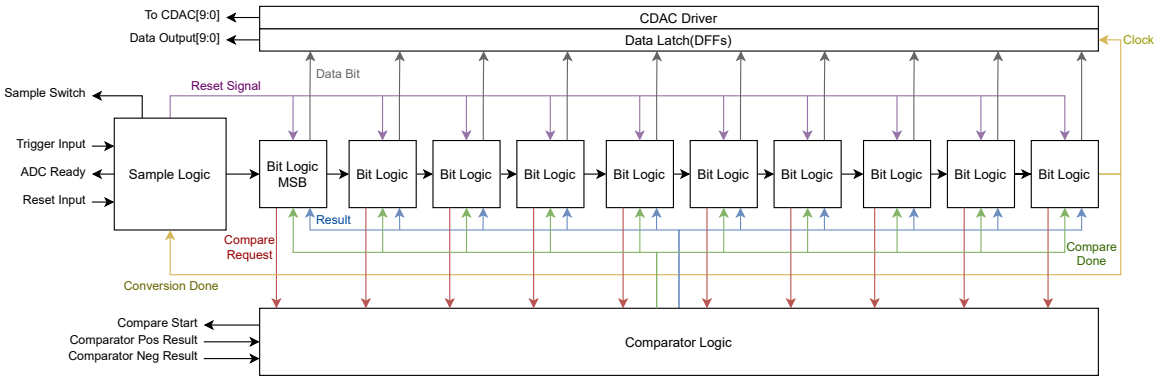


Figure 2.13: ADC Logic Block Diagram

Details of each block are given in the following sections.

2.5.2 Sample Logic

The sample logic keeps the ADC status information, controls the sample switch, and starts the conversion. Here is the circuit diagram of the this block:

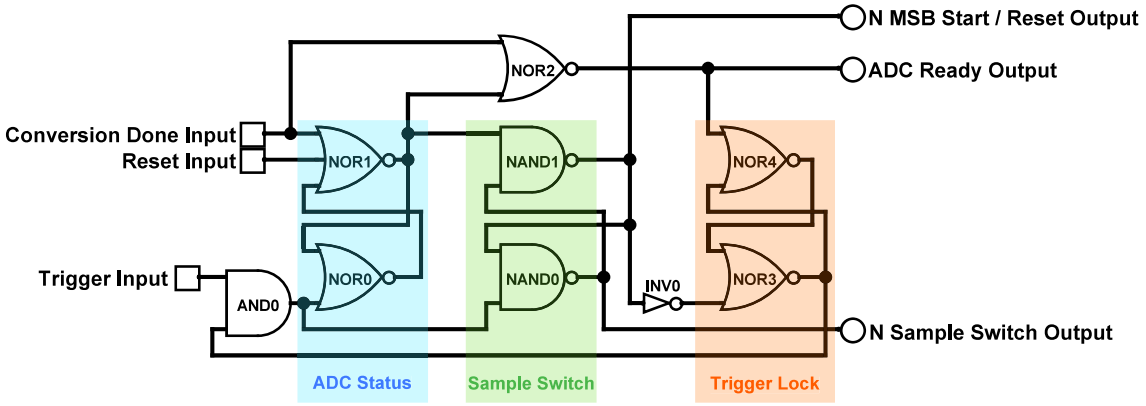


Figure 2.14: Sample Logic Circuit Diagram

In the diagram above, each square is an input and each circle represents an output. If an input or output has an initial "N" in its name, it means that input/output is active low.

The three S-R latches inside the sample logic store the overall ADC status, the sample switch status, and the trigger lock status respectively. The ADC status latch is set (NOR0 outputs 0, NOR1 outputs 1) at the rising edge of the trigger and remains set until the conversion is done. The trigger lock latch disables the input trigger (NOR3 outputs "0", NOR4 outputs "1") when the conversion process starts, and enables it when the ADC is ready after reset phase. The sample switch latch makes use of all four states of a NAND S-R latch. When idle, both NAND gates (NAND0, NAND1) output "1", disabling both the sample switch and the proceeding conversion phase logic. Since the trigger signal will arrive earlier at NAND0 then NAND1 because of the delay of NOR0 and NOR1, once triggered, the output of NAND0 always goes to "1" first, enabling the sample switch, while NAND1 still

outputs “0”. After the delay, the input to NAND1 also becomes the “1”, making the NAND S-R latch hold the state. When the trigger signal input goes low, the sample switch latch flips its outputs and starts the conversion.

Following is the description of each input and output pin of this logic block:

- *Trigger Input*: ADC trigger pulse input. A rising edge on this pin closes the sample switch and starts the sample and hold process, and the following falling edge opens the sample switch and starts the conversion phase. This input is only effective when the ADC is ready, meaning extra switching during the conversion and reset phases is ignored. If this pin is held high at the end of the reset, another sample and hold phase will start as soon as the ADC becomes ready.

- *Reset Input*: Holding this reset input high will force the whole logic into the idle state. Normally, the logic can reset itself after every conversion, so this reset input is here just in case of an unwanted state possibly caused by glitch or startup.

- *Conversion Done Input*: This input is set by the LSB’s bit logic (next bit start signal). A transition of low to high indicates the end of the conversion phase, whereas a high to low edge means the end of reset phase.

- *N MSB Start / Reset Output*: Active-low conversion phase start signal and active-high reset signal that resets all bit logic blocks.

- *ADC Ready Output*: ADC ready flag to be read by the external controller. “1” when idle and “0” when ADC is busy in any sampling phase.

- *N Sample Switch Output*: Active-low sample switch control signal. When at “0”, the sample switch is closed.

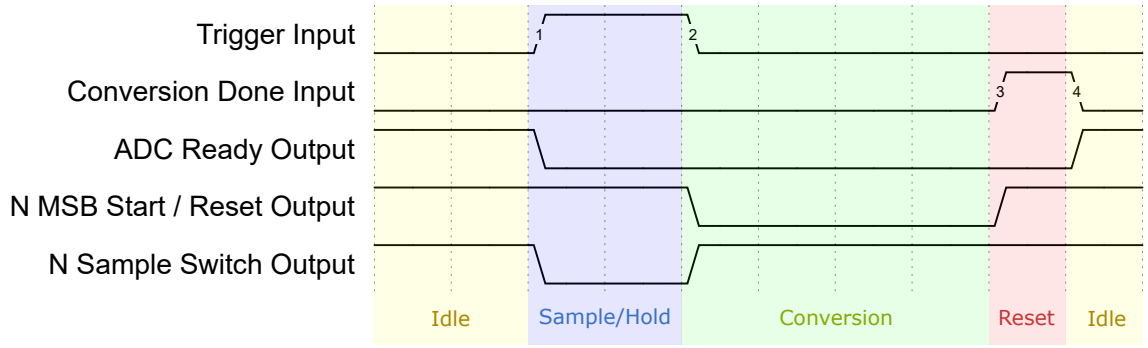


Figure 2.15: Waveform of Sample Logic in a Sampling Cycle

To be straightforward, Figure 2.15 shows the waveform of this block in a sampling cycle. There are four states labeled and colored differently. Also, numbers from 1 to 4 on the waveform denotes the events that push the process forward.

2.5.3 Bits Logic

The conversion of each bit can be broken into the steps shown in Figure 2.16.

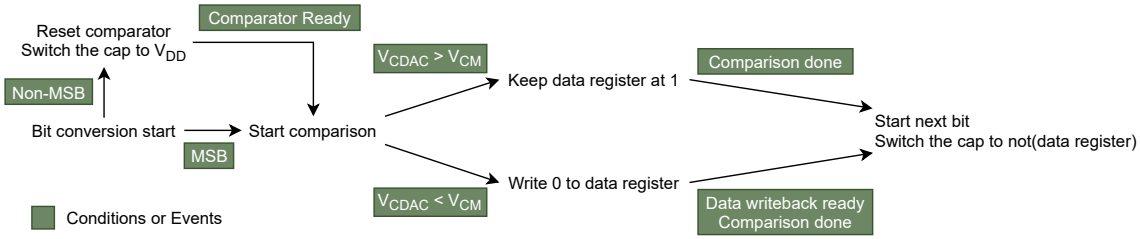
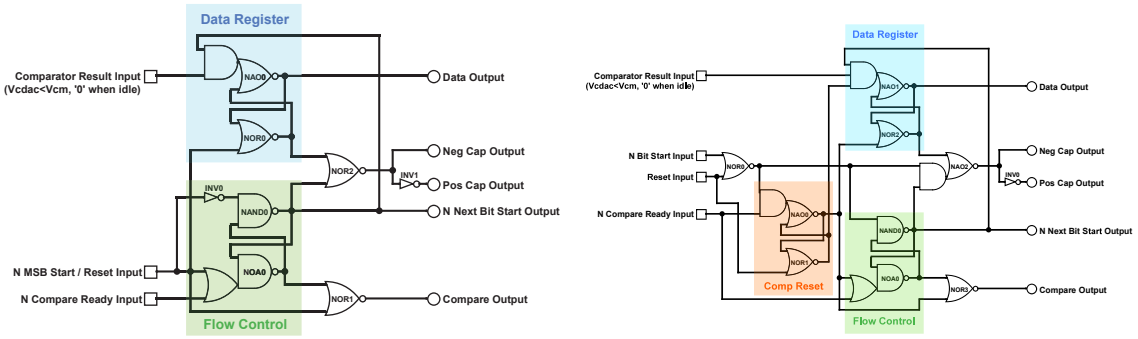


Figure 2.16: Bits Logic State Diagram

Every bit conversion starts from "Bit conversion start". For a non-MSB bit, the logic first needs to switch the corresponding bit capacitor to V_{dd} and reset the comparator. Then, it requests a new comparison once the comparator is ready. The MSB, however, requests comparison at the beginning because the MSB cap has been connected to V_{dd} and the comparator has been reset during the reset phase. After the comparison result is resolved, a temporary data register for the bit, which is default to "1", is set to "0" if the CDAC voltage is higher than the common mode

voltage (V_{cm}). Finally, once the comparison done signal is asserted, the bit capacitor is switched to the inverse of the data just stored and the next bit conversion starts. For example, when V_{cdac} is lower than V_{cm}, the temporary data register is kept default at "1". Then, when the comparison done signal comes in, the next bit conversion starts and the current bit capacitor is switched from "1" to "0".

To achieve the logic operation, circuits are designed for MSB and non-MSB bits. These circuits are modular and can be chained together for SAR ADCs of different bit depths. For example, a chain of bit_logic_MSB—bit_logic—bit_logic can be used for a 3-bit SAR ADC. Figure 2.17a and 2.17b are the diagrams of the two circuits.



(a) Bit Logic MSB Circuit Diagram (b) Bit Logic Non-MSB Circuit Diagram

Figure 2.17: Bit Logic Blocks Circuit Diagram

Both of these circuits have a data register, which temporarily stores the converted bit, and a flow control register, which keeps track of when the bit conversion finishes. Additionally, the non-MSB bit logic block also has a comp reset register that implements the function of waiting for the comparator to be ready (reset) before requesting a comparison.

The input/output pins are defined as follows:

- *N MSB Start / Reset Input (MSB only)*: Active low MSB conversion start that also resets the bit logic MSB when pulled high.

- *N Bit Start Input & Reset Input (non-MSB only)*: Conversion of the bit starts only when both inputs are low, and the bit logic always resets as long as the reset input is high. N bit start input is connected to the previous bit logic's N next bit start output, while the reset input is controlled by the sample logic's N MSB start/reset output. Separate reset and bit start inputs allow all the bit logic blocks to reset at the same time, achieving a faster reset speed.

- *N Compare Ready Input*: Active low compare ready input. This is the signal that indicates the comparator status. A "0" means the comparator has resolved to a result, whereas an "1" means it has been reset and ready for a new comparison. This signal is crucial in pushing the conversion process forward.

- *Comparator Result Input*: This is the input that sets the data register. If the comparison shows that V_{cdac} is lower then V_{cm}, this pin will be driven high, and the data register, which is reset to "1" during idle will be overwritten by "0". Also, the result input is only valid during the conversion of the current bit. This ensures that the comparison result is only written to a single bit every time. Further, the result signal has to be received before the compare ready input, which will disable the result input.

- *Data Output*: Temporary digital code bit. This bit is reset to "1" during idle, and can be changed during the conversion according to the input voltage. Once all the bits have been converted, the data on this output is the final result. Then, all the bits of this data output will be latched into DFFs to preserve the data before it is reset.

- *Neg Cap Output / Pos Cap Output*: Outputs that drive the CDAC bit capacitors through the CDAC driver.

- *N Next Bit Start Output*: Active low signal that indicates the end of the bit's conversion.

- *Compare Output*: Compare request output. This output sends out a pulse during conversion of a bit. The rising edge of this pulse represents a request for comparison, and the falling edge is a request for resetting the comparator.

To give an intuition of how these blocks work, an example waveform is given in Figure 2.18. This example shows how a 2-bit ADC converts each bit and then resets. Inside the example ADC, the two bits are controlled by a bit logic MSB block (MSB in the figure) and a bit logic block (LSB in the figure) respectively. These two blocks' inputs and outputs are plotted, and the ones with the label in the same color are connected together. Also, the waveform is divided into steps shown in different colors, and the conversion process (green) is now shown in much more detail.

2.5.4 Comparator Logic

The comparator logic block is responsible for turning the comparison request signal from all bit logic blocks into a single clock signal that is sent to the comparator. The block also includes the circuit needed to buffer the "comparison result" signal and generate the active-low "comparison ready" signal, which indicates the completion of a comparison when at "0" and shows that the comparator has been reset when at "1".

Generating the comparator clock is straightforward. The bit logic block asserts the "comparison request" signal only after the comparator is reset and ready, then quickly deserts it on the arrival of the "comparison ready" signal before the next bit starts. Because of this, each request signal is a pulse that is only active during its own bit period, and there is no overlap between any of the two pulses. This way,

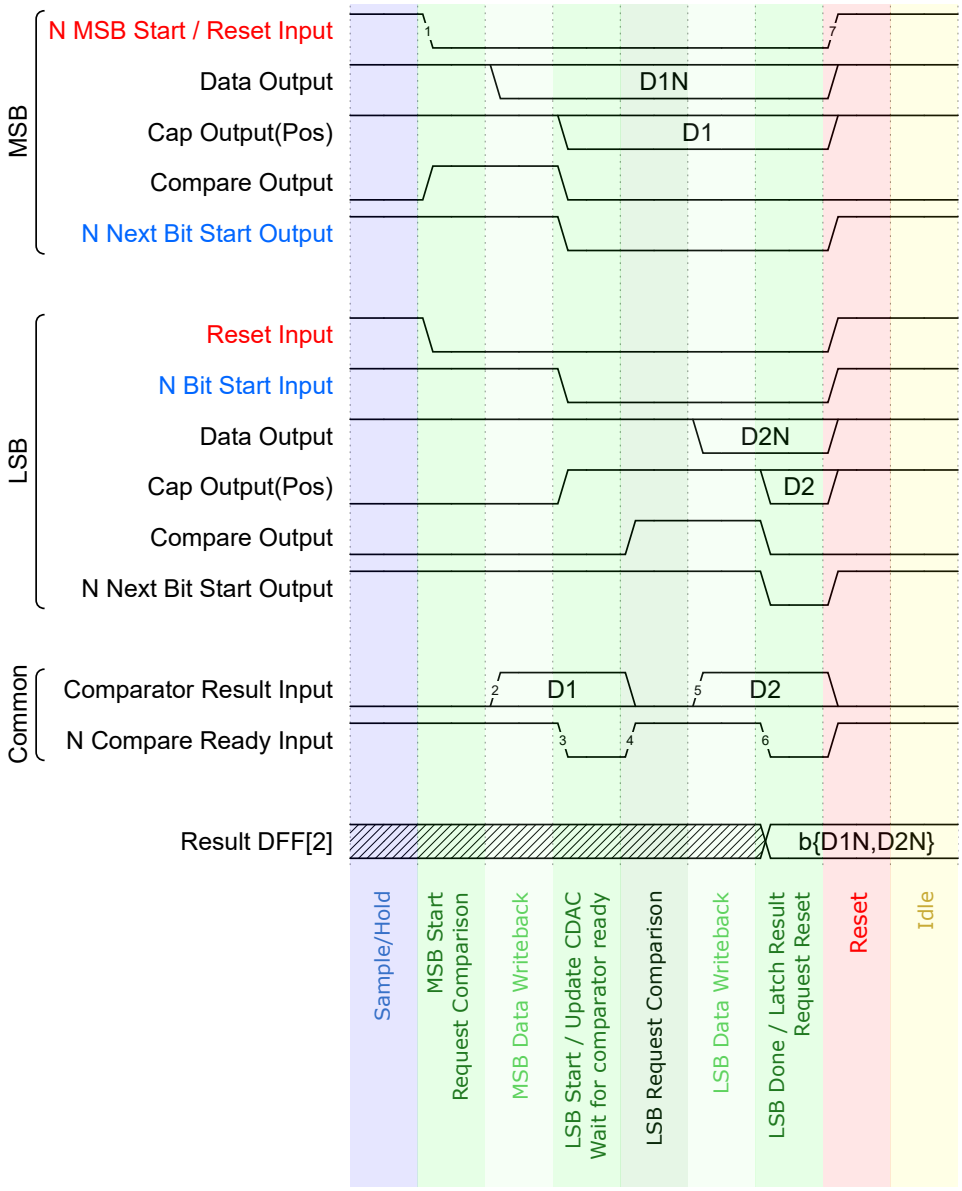


Figure 2.18: Waveform of a 2-bit Bit Logic Chain in a Sampling Cycle

the circuit needed is simply a 10-input OR gate. Practically, this many inputs in a single gate result in a high stack of transistors, which is not desirable for keeping the propagation delay consistent across all inputs. Thus, the actual circuit uses two 5-input NOR gates and a 2-input NAND gate, as shown in Figure 2.19.

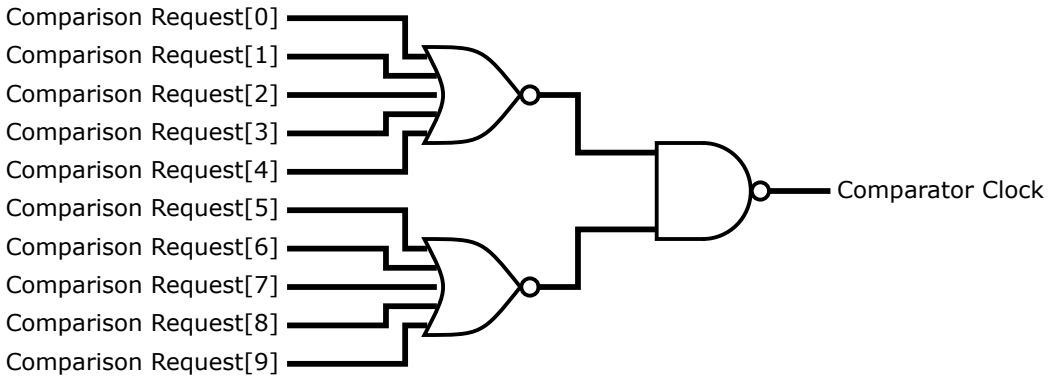


Figure 2.19: Comparator Clock Generation Circuit

To buffer the comparison result for data write-back and to generate the comparison ready signal that drives the conversion flow, the circuit shown in Figure 2.20 is used. In the schematic, the delay cell is an inverter with two PMOS's and two NMOS's in series to slow down the signal propagation. Together with the high threshold cells, the resulting longer delay between the comparison result and the comparison ready can make sure the data is reliably written back before moving on to the next bit.

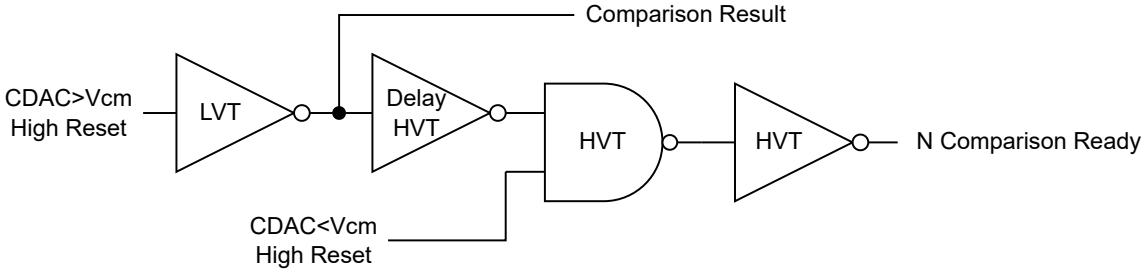


Figure 2.20: Comparison Result/Ready Generation Circuit

The "comparison result" idles at "0" and is set to "1" whenever a comparison

shows that CDAC voltage is higher than the common mode voltage. This "1" will be caught by the currently active bit logic block to update its data register. Simultaneously, it will also propagate through the delay cell shown in the diagram and trigger the "comparison ready" signal to activate the next bit logic block. On the contrary, when the CDAC voltage is lower than the common mode voltage, the "comparison result" stays at "0" while the "comparison ready" is asserted to skip the write-back process and proceed to the next bit directly.

2.6 ADC Assembly

2.6.1 System Diagram

Putting all the components discussed above together with the level-shifters to bridge the 2.5 V analog with the 1 V digital and a voltage divider with a bypass capacitor to generate the common-mode voltage, the top-level ADC system diagram is shown in Figure 2.21.

2.6.2 Layout

In the layout, all the components are fitted into a rectangular space that measures 58.34 μm by 49.27 μm. In Figure 2.22, the placement of each component and the usage of the metal layers is displayed.

Metal layer 1 to 3 are used for routing between transistors and components. Metal 4 and 5 form the shield that isolates the lower routing from the CDAC and the common mode voltage bypass capacitor that sits on metal 6 and 7. Because the maximum metal width allowed is 12 μm, the shield is made by stitching pieces of metal 4 and 5 together. To reduce the parasitic capacitance between CDAC and analog

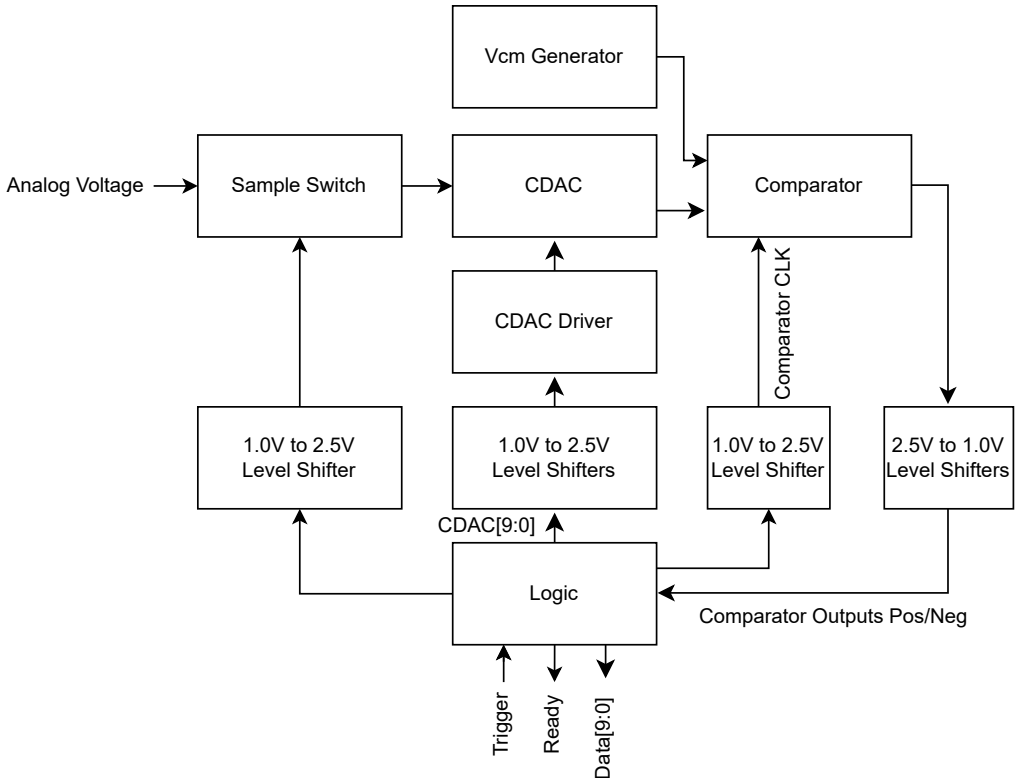
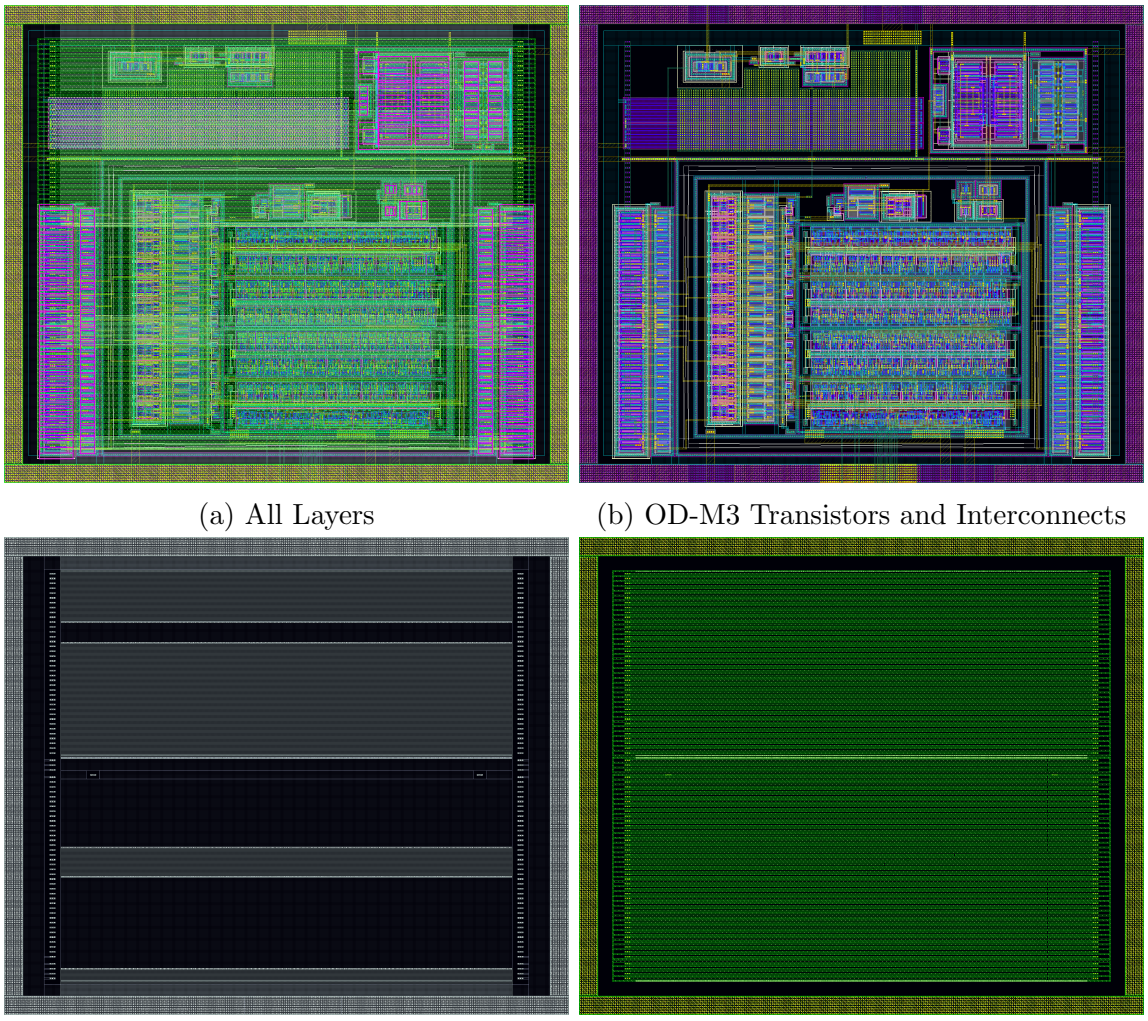


Figure 2.21: ADC Top-level System Diagram

ground, metal 4 is mostly used under the active area of the CDAC. On the contrary, M5 is mostly used under the bypass capacitor area to increase its capacitance.

To achieve better noise performance, there is a 1.5 μm-wide NT_N shape surrounding the digital block dividing the substrate into the analog and the digital domains. Along the two sides of this shape, there are substrate ties providing a low-impedance path to the ground in its own domain, lowering the chance of the noise getting across the domains. Further, a 1.95 μm-wide "metal and via wall" surrounding the whole ADC and extending from substrate to metal 7 is connected to the analog ground to provide extra decoupling. This metal wall also connects to the shield on metal 4 and 5.

Moreover, dummy exclusion shapes are used on the poly/oxide definition layers



(a) All Layers

(b) OD-M3 Transistors and Interconnects

(c) M4-M5 Shield

(d) M6-M7 CDAC/Vcm Bypass Capacitor

Figure 2.22: ADC Assembly Layout

at critical analog sections such as the comparator and the sample switch. Also, automatic metal fill is also disabled within the ADC's boundary. While the lower metal layers have enough metal density on their own, it is required to manually insert metal 8/9 shapes over the top of the non-critical portion (bypass capacitor and dummies) of the CDAC to satisfy the metal density design rules without compromising the CDAC performance.

As for port locations, analog and digital pins sit on two opposite edges of the

ADC, and all of them are on metal 2 and 3 layers. Concretely, the pin location is shown in Figure 2.23

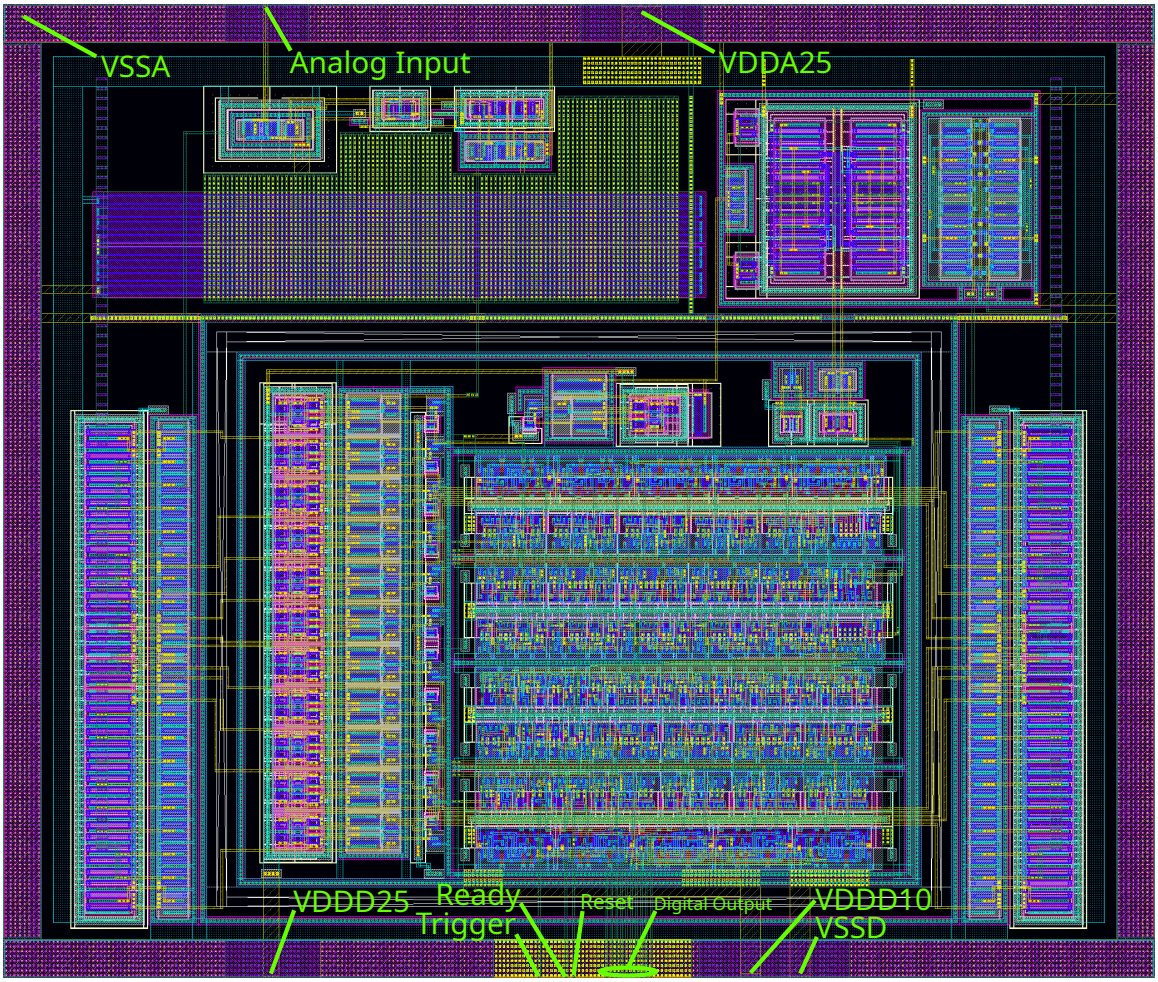


Figure 2.23: ADC Pin Location

2.6.3 Simulation

Top level ADC simulation was done mainly to examine the power consumption, the input range and the speed of the ADC. The simulation setup simply uses the ADC to sample DC voltages from 0 to 2.5 V. The simulation result is as follows. First, the energy consumed by each component in one conversion is listed in Table 2.4.

Table 2.4: Simulated ADC Power Consumption

Component	Power (pJ/conversion)
Sample Switch	0.17
Comparator	13.48
CDAC (with driver)	11.40 (Worst Case)
V_{cm} Generator	0.42
Level Shifters	6.61
Logic	1.55
Total	33.63

Second, the conversion phase and the reset phase in total take 24.29 ns. Assuming the sample and hold phase takes 10 ns, the maximum sampling frequency is around 29 MSPS.

For the input range, a transfer function from the input analog voltage to the digital code is plotted in Figure 2.24. From this plot, it can be seen that the ADC is perfectly linear and it can convert analog voltages from 0.5 V to 2.5 V, resulting in a range of 2 V.

Due to the lack of the CDAC mismatch model, the ADC's SINAD cannot be reliably simulated. Simulating the SINAD using the method, which will be discussed in the next section, results in a derived ENOB of 9.98 bits, which is overly ideal.

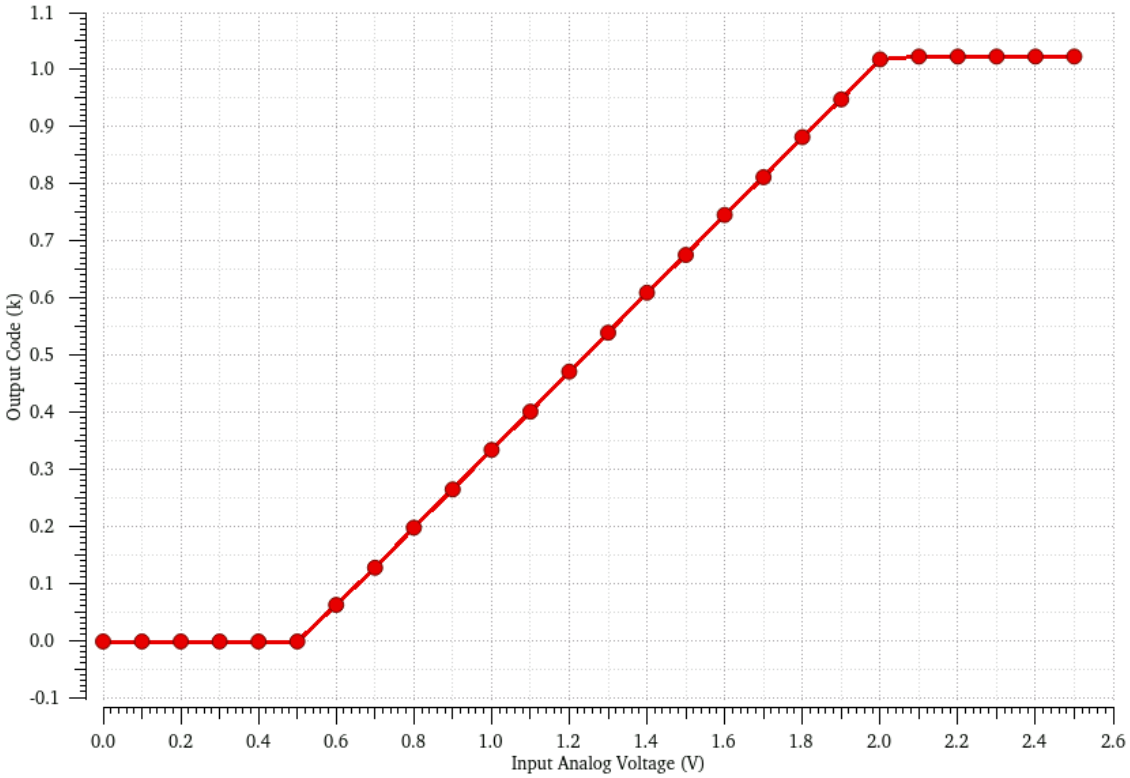


Figure 2.24: Simulated Analog to Digital Transfer Function Plot

Chapter 3

Testbench and Test Chips

3.1 Testbench

3.1.1 Hardware Setup

3.1.1.1 The Original Chip Testbench

Two ADC testbenches are set up for testing the ADCs' power consumption, linearity, SINAD, sampling rate, and analog input range. The testbench for the original test chip has been built, but only the schematic of the new chip testbench will be shown.

Ignoring the computer and all the lab bench equipment, the testbench consists of four main components: an ADC test PCB that interfaces with the test chip, a FIFO to USB3 (FTDI FT600Q-B) board that allows fast ADC data acquisition, an FPGA that sends the trigger signal to the ADC chip and bridges the ADC test chip and the FIFO to USB3 adapter, and a microcontroller (ESP32) to work as the SPI master. Putting all together, the testbench for the original test chip is shown in Figure 3.1.

The ADC test PCB provides connections to the ADC test chip using a ZIF socket. The connections include the the analog inputs, the power rails, the data outputs, and the trigger signal input. Shown in the picture, the PCB uses two Digilent PMOD connectors that can be directly plugged into the ARTY A7 FPGA board. There is

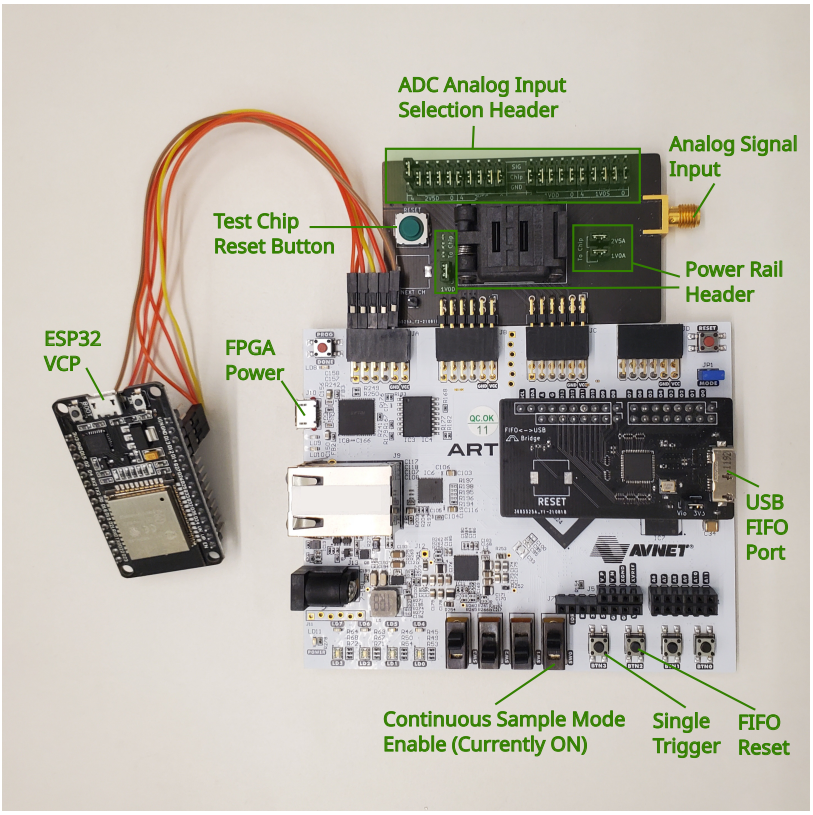


Figure 3.1: Testbench Boards for the Original Test Chip

also a coaxial terminal for analog signal input. This input is buffered by an opamp, and then sent to the top row of the ADC analog input selection pin headers. With the middle row of the headers being the ADC analog inputs and the bottom row being the analog ground, pin jumpers are placed between middle/top and middle/bottom rows to route the buffered signal or ground the ADC inputs. The ADC can also be driven externally by directly connecting signal and ground jumper wires to the middle and the bottom rows. For power rails, the 3.3 V digital IO voltage is sourced from the FPGA board, while the 1 V digital/analog power and the 2.5 V analog power are derived from the same source using low-dropout (LDO) regulators. Multiple sizes of bypass capacitors are used to filter the power rail noise across a wide bandwidth. Further, the digital and analog grounds are kept separate on the board but are joint

together at the PMOD connectors. During testing, to get an even quieter analog power rail or to measure power, external power can be supplied through the power header.

On the FPGA (Arty A7), a ping-pong buffer that is made of two 2048×10 bit asynchronous FIFO's is implemented to temporally store the ADC result. 2048 ADC samples are needed before a transfer to the FIFO to USB adapter board happens, and the samples can then be sent to the computer through the adapter. The FPGA board is also programmed to connect the trigger signal and the SPI wires from the microcontroller (ESP32) to the test chip through the PMOD connectors. Using a switch on the FPGA board, it can be chosen to have the ADC trigger signal generated by dividing down the 100 MHz clock from the USB to FIFO adapter for continuous sampling, or pass through the trigger signal from the ESP32 or manually trigger using a button for single sampling.

The microcontroller (ESP32) implements a USB/UART virtual COM port (VCP) command line interface. It executes the commands and communicates with the ADC test chip through the SPI bus and a standalone trigger signal wire. Functions including triggering a single sample and reading/writing the configurations on the test chip are realized.

The FIFO to USB3 adapter board uses a FTDI FT600Q-B chip working under 245 Synchronous FIFO mode.

3.1.1.2 The New Chip Testbench

In the testbench for the new chip, all the components except the ADC test board stay unchanged. Using a single analog input port for the same type of the ADCs instead of one analog input pin per ADC, the new test chip requires a redesign of the test board's input buffering circuit. The analog input selection header in the original board

is replaced with only four headers to allow each type of ADCs to select the input from the buffered signal, ground, or an external source. Interfacing with the differential ADCs is a single-ended to differential amplifier that has a voltage gain of 4.7 and bandwidth of 5.7 MHz. This makes it easier to use a signal generator as the signal source. In addition, the new ADC test board has a socket for ESP32, eliminating the need to pass signals through the FPGA board. Also, with the SPI serial data readout and the ability to generate sample triggers using the ESP32, this setup can now work at a lower sampling frequency on its own. For maximum throughput, the FPGA and FIFO/USB adapter combo is still required. With these modifications to the ADC test board applied, the system diagram of the new test setup is shown in Figure 3.2.

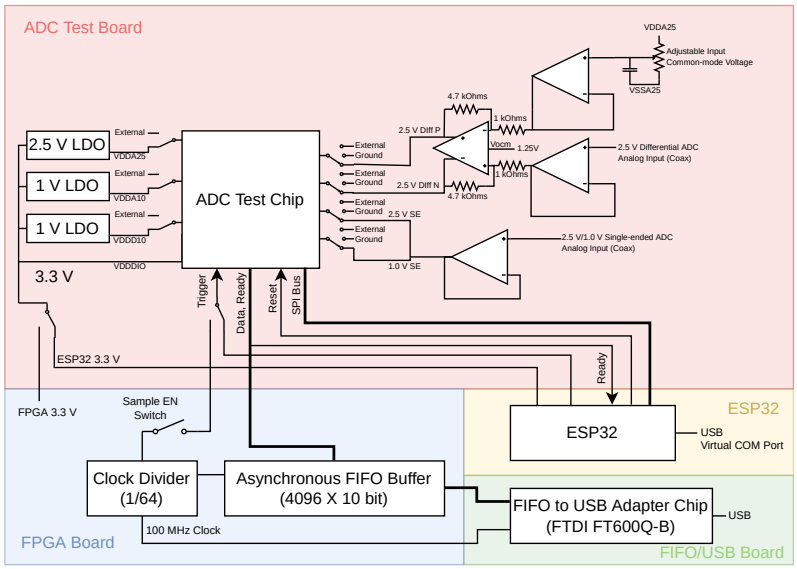


Figure 3.2: New Testbench Schematic Diagram

A picture of the new ADC test board is shown in Figure 3.3.

For reference, the full schematics of the original and the new ADC test board as well as the FIFO to USB adapter board are included in Appendix A.

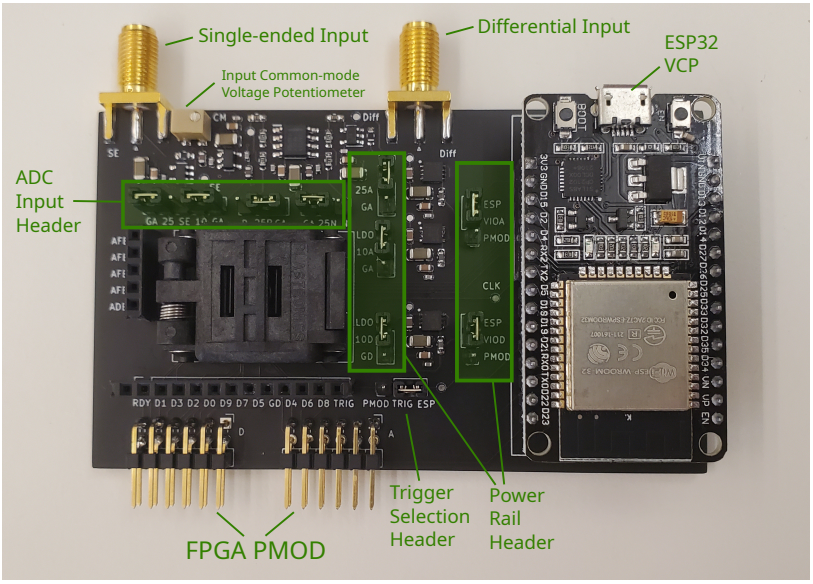


Figure 3.3: The New ADC Test Board

3.1.2 Test Method

For power consumption, it is hard to isolate the ADCs' idle power from all the leakage. Thus, the total quiescent power is assumed to be the measured power of the power rails divided by the number of ADCs. For example, in the original test chip (discussed in Section 3.2), a 2.5 V ADC's quiescent power is calculated by $P_{q,ADC25} = (P_{10VDDD}/20 + P_{25VDDA}/10)$ because, ignoring the controller, the 1 V digital power rail is shared across all 20 ADCs, while the 2.5V analog power rail is for the ten 2.5 V ADCs. A part of the idle power consumption comes from the voltage divider for generating the common mode voltage in each ADC, and it can be assumed that their real power matches the simulation value. This way, the leakage can be estimated using $P_{leakage,ADC25} = P_{q,ADC25} - P_{voltage\_divider,ADC25}$. Dynamic power is measured by taking the difference between the quiescent power and the average power draw when ADC is sampling at a high rate. Dividing the dynamic power by the sampling rate, the power can be converted into Joules per sample. In practice, the power is measured with a source meter. On the ADC test PCB, every power rail

(1.0 VDDD, 2.5 VDDA, 1.0 VDDA) can be either supplied from an internal LDO by putting on the jumper cap or from the external source meter by connecting jumper wires to the power pin. When measuring, only the power rail under measurement will be connected to the source meter, while the other two rails are connected to the LDOs. Thus, the process needs to be repeated for each power rail to find out the quiescent power and dynamic power for all types of the ADCs.

Maximum sampling rate can be found by measuring the negative pulse width of the ready signal output. Since this signal goes negative when sampling starts and becomes positive once reset finishes, its pulse width includes the duration of the sample and hold, conversion, and reset phases. It is important to know the converting and resetting time because sample/hold time is adjustable and it affects the maximum sampling rate. With a known sample and hold duration, the maximum sampling rate can be calculated by $F_{max} = 1/(t_{conversion,reset} + t_{sample\_hold}) = 1/t_{ready\_pulse}$. The easiest method to measure the conversion and reset time is to use the default trigger pulse pass-through mode that sends the external trigger pulse directly to the active ADC. This way, conversion and reset time is simply $t_{conversion,reset} = t_{ready\_pulse} - t_{trigger\_pulse}$.

The method for testing the analog input range is very straightforward. The ADC under test is set to sample to a variable DC voltage generated by a source meter. By manually adjusting the DC input, the voltages that cause the ADC output to change from 1 to 0 and from 1022 to 1023 can be found. The voltage range between these two points is the analog input range.

To measure INL and DNL, the ADC is set to continuously sample a lower frequency symmetrical triangle wave that sweeps back and forth within the ADC's full analog input range. The output codes are then used to build a histogram. Ideally, the equal chance of the input landing on a certain voltage indicates that, if having enough

samples, there will be very similar sample number in each bin in the histogram. With INL and DNL taken into account, the digital output is more likely to land on certain codes than others. To get the actual DNL and INL graphs, the following functions can be used:

$$DNL(code) = \frac{\#hits}{\#total\_sample/\#total\_code} - 1 = \frac{\#hits}{\#total\_sample/1024} - 1 \quad (3.1)$$

$$INL(code) = \sum_{0}^{code} DNL(code) \quad (3.2)$$

In the DNL equation, $\#hits$ is the number of samples that land on a certain code. $\#total\_sample$ is the total number of samples, and $\#total\_code$ is the number of code bins. In this case, the 10-bit ADCs have a total of 1024 codes.

The testing of SINAD and ENOB involves sampling a sine wave with an amplitude close to the full input range of the ADC and performing discrete Fourier transform on the output digital codes to find the power of the signal and the rest (noise and distortion). The frequency of the input sine wave needs to be lower than the Nyquist frequency and also at a frequency, by which the sampling rate is indivisible. This is to make sure that the digital outputs are spread over the full code range to reveal DNL/INL imperfections. For instance, when sampling at 10 MSPS, an input signal frequency of 1.228 MHz can be used. After getting enough samples, a frequency spectrum with desired resolution can be derived by performing FFT on the digital codes. Then, SINAD is calculated using the following equation:

$$SINAD = 10 \log_{10} \frac{P_f}{\sum P_i - P_0 - P_f} \quad (3.3)$$

In this equation, P_f is the power of the fundamental frequency, which is the power of

the 4.912 MHz sine wave in the example. The denominator is the total power minus the DC power (P_0) and the fundamental frequency power. With SINAD, ENOB can be calculated using the ENOB equation in Chapter 1.

3.2 The Original Test Chip

The original test chip was designed for testing the old ADC designs, and its layout is shown in Figure 3.1.

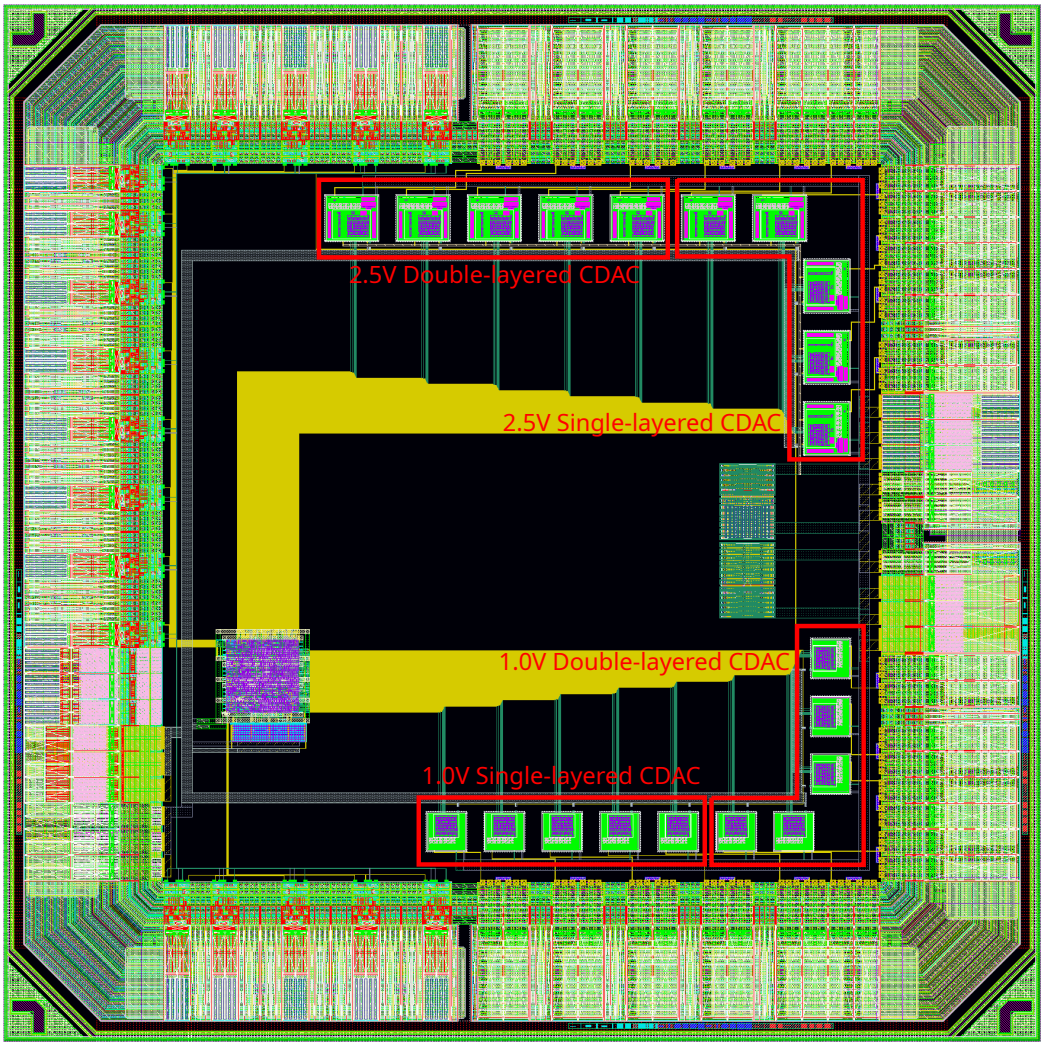


Figure 3.4: The Original Test Chip Layout

There are 20 ADCs of four different types, and each one of them has its dedicated analog input pin. In the layout, they are put alongside the chip seal ring. The purpose of having five ADCs per type is to statistically test the CDAC's matching performance. The four types are different in their operating voltage and the number of metal layers in the CDAC. There are 1 V ADCs for testing the lowest achievable power and 2.5 V ones for interfacing with the lab's previous analog front-end designs. Also, the CDACs are either made of a single metal 7 layer to reduce the total capacitance and the parasitic capacitance to the lower metal shield, or have metal 6 and 7 layers to achieve improved matching. The ADC types are the four combinations of these two differences.

There is also an ADC controller on board at the lower left corner in the layout. Its functions are mostly the same as the controller put onto the new chip that is discussed in Section 3.3. One difference is that, since all the ADCs on the original chips use asynchronous logic, no clock waveform generation circuit is included. Also differently from the new chip, this controller allows sending the trigger pulse simultaneously to multiple ADCs by enabling multiple ADC channels registers, and then using the "next channel" pin to quickly connect different ADC results to the parallel output for the maximum throughput. This function was not used in the test, and there was only one enabled ADC at a time to reduce the crosstalk and noise.

The original chip comes in a QFN44 package, and all of the 44 pins are used. The pin functions are listed in Table 3.1

3.2.1 Test Details and Results

Using the testbench and test methods talked in the previous section, the power consumption, maximum sampling rate, input range, and INL/DNL were tested. The testbench boards are shown in Figure 3.1 in the last section.

Table 3.1: Original Chip Pins

Pin#	Pin Name	Type	Notes
1-8	Debug [2:9]	Digital Out	Digital debug signal port that can also work as parallel data output
9	VDDIO	Power	3.3 V IO power rail
10	VDDD10	Power	1 V core digital power rail
11	VSSD	Ground	Digital Ground
12	Trigger	Digital In	Async sample trigger that starts internal pulse generation or directly pass through trigger to ADC
13	SCLK	Digital In	
14	MOSI	Digital In	
15	MISO	Digital Out	High impedance when CSN is high
16	CSN	Digital In	Active-low chip select
17-21	ADC 1V0S [0:4]	Analog In	Analog inputs to 1.0 V single-CDAC-layer ADCs
22-26	ADC 1V0D [0:4]	Analog In	Analog inputs to 1.0 V double-CDAC-layer ADCs
27	VDDA10	Power	1.0 V analog power rail
28	VSSA	Ground	Analog ground
29	VDDA25	Power	2.5 V analog power rail
30-34	ADC 2V5S [0:4]	Analog In	Analog inputs to 2.5 V single-CDAC-layer ADCs
35-39	ADC 2V5D [0:4]	Analog In	Analog inputs to 2.5 V double-CDAC-layer ADCs
40	Reset	Digital In	
41	Next Channel	Digital In	A positive edge on this pin connects the next enabled ADC output to the parallel data output port
42	ADC Ready	Digital Out	Same function of data available signal
43-44	Debug [0:1]	Digital Out	Same as pin 1-8

The power of the three rails were separately measured. Each measurement includes the quiescent power (leakage and V_{cm} generator power) and the dynamic power. The V_{cm} generator power is not measured, but derived from the simulation result. Also, SPI messages were sent to enable only one ADC during the dynamic power test. The test result is shown in Table 3.2.

Table 3.2: Original Test Chip ADC Typical Power at 1 MSPS

	1.0 V Single-layer CDAC (μW)	1.0 V Double-layer CDAC (μW)	2.5 V Single-layer CDAC (μW)	2.5 V Double-layer CDAC (μW)
Leakage (Digital+Analog)	1.78	1.78	1.16	1.16
V_{cm} Generator Power	2.35	2.35	11.77	11.77
Dynamic (Digital)	2.82	2.82	3.26	3.26
Dynamic (Analog)	0.83	1.02	13.12	13.82
Total	7.78	7.97	29.31	30.01

As for maximum sampling rate, the test result is listed below:

Table 3.3: Original Test Chip ADC Typical Speed

	1.0 V ADCs	2.5 V ADCs
Conversion/Reset Duration	22 ns	65 ns
Sampling Period Assuming 10 ns S/H Duration	32 ns	75 ns
Maximum Sampling Rate	31.25 MSPS	13.33 MSPS

In the 1.0 V ADCs, the dominating factor that affects the speed is the comparator, whereas in the 2.5 V ADCs, the level shifters also add significant delay. The assumed

10 ns sample and hold time is a typical value that was proven in simulation sufficient to fully charge the CDAC.

The input range test result is as follow:

Table 3.4: Original Test Chip ADC Typical Input Range

ADC Type	Input Range
1.0V Single CDAC Layer	0.70V
1.0V Double CDAC Layer	0.67V
2.5V Single CDAC Layer	1.82V
2.5V Double CDAC Layer	1.80V

The power, sampling rate, input range tests show similar results to the simulation.

In the linearity test, the sampling rate was set to 1.5625 MSPS (1/64 of the 100 MHz clock) and sample and hold duration was 10 ns. Input to the ADC was a symmetrical triangle wave with a frequency of 383.75 kHz, which the sampling rate is not an integer multiple of and is much lower than the Nyquist frequency. A total of 8,388,608 samples are used to build each histogram. The measurement results reveal significant nonlinearities within the ADC circuit. The histograms are included in Figure 3.5

Ideally, a uniform count in all ADC codes is expected, and it indicates equal mapping of voltage to bins. However, the histograms show that the output digital codes have significantly higher probability landing on certain codes than others, and the distribution becomes more uneven among higher codes. Seen from the less comb-like pattern in the left two plots, the double-layered CDACs have better linearity compared to the single-layered ones, especially among the lower binary bits. This matches the expectation of the design that the larger capacitor plate area results in less variation in capacitance and improves matching. Furthermore, there seems to be a large gap around the middle codes in every plot. This shows a significant mismatch

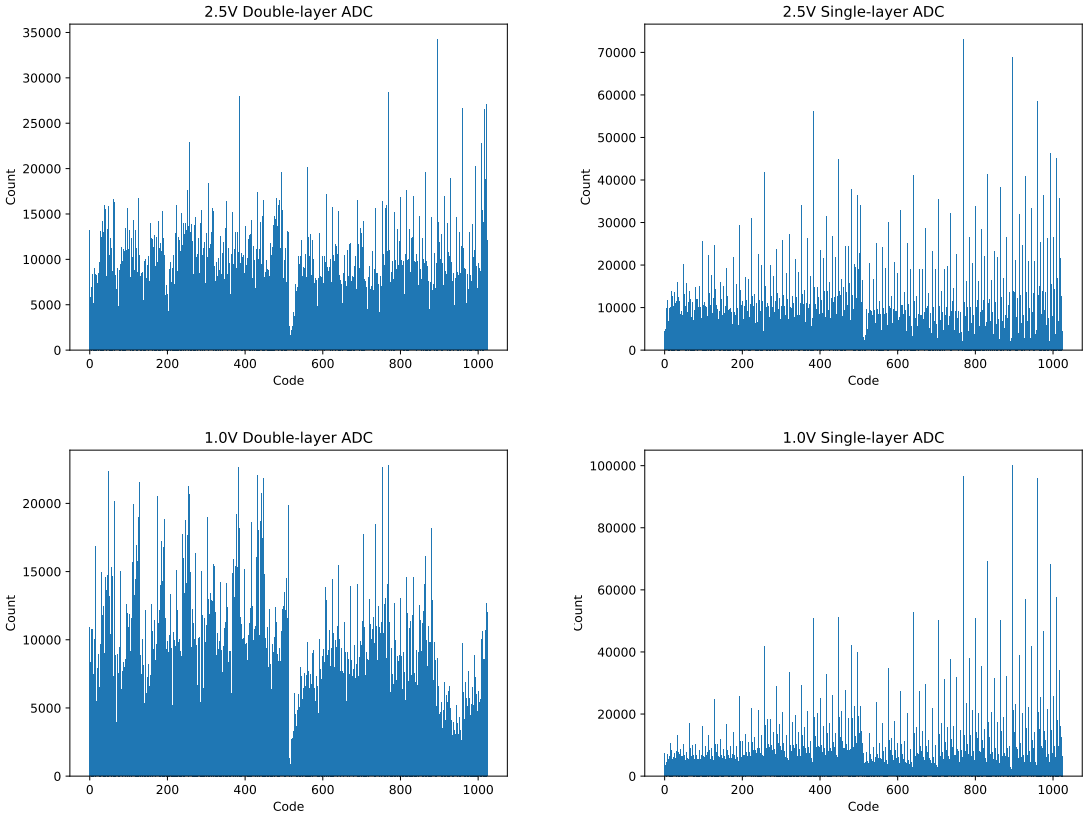


Figure 3.5: Original ADC Linearity Test Result Histograms

between the MSB capacitor and the rest. The corresponding DNL and INL plots are shown in Figure 3.6.

Concluded from the results of the four tests, it is unnecessary to use single-layered CDAC because the loss in the linearity far outweighs the small gain in the input range and power.

3.2.2 Problems

To find out the cause of the problems, the ADC is set to sample DC voltages that sweep across the whole range, and the latest 2,097,152 samples are plotted in real time on the histogram to see which digital code the input DC voltage is mapped to.

Surprisingly, when the input is at the middle of the range, the output codes appear

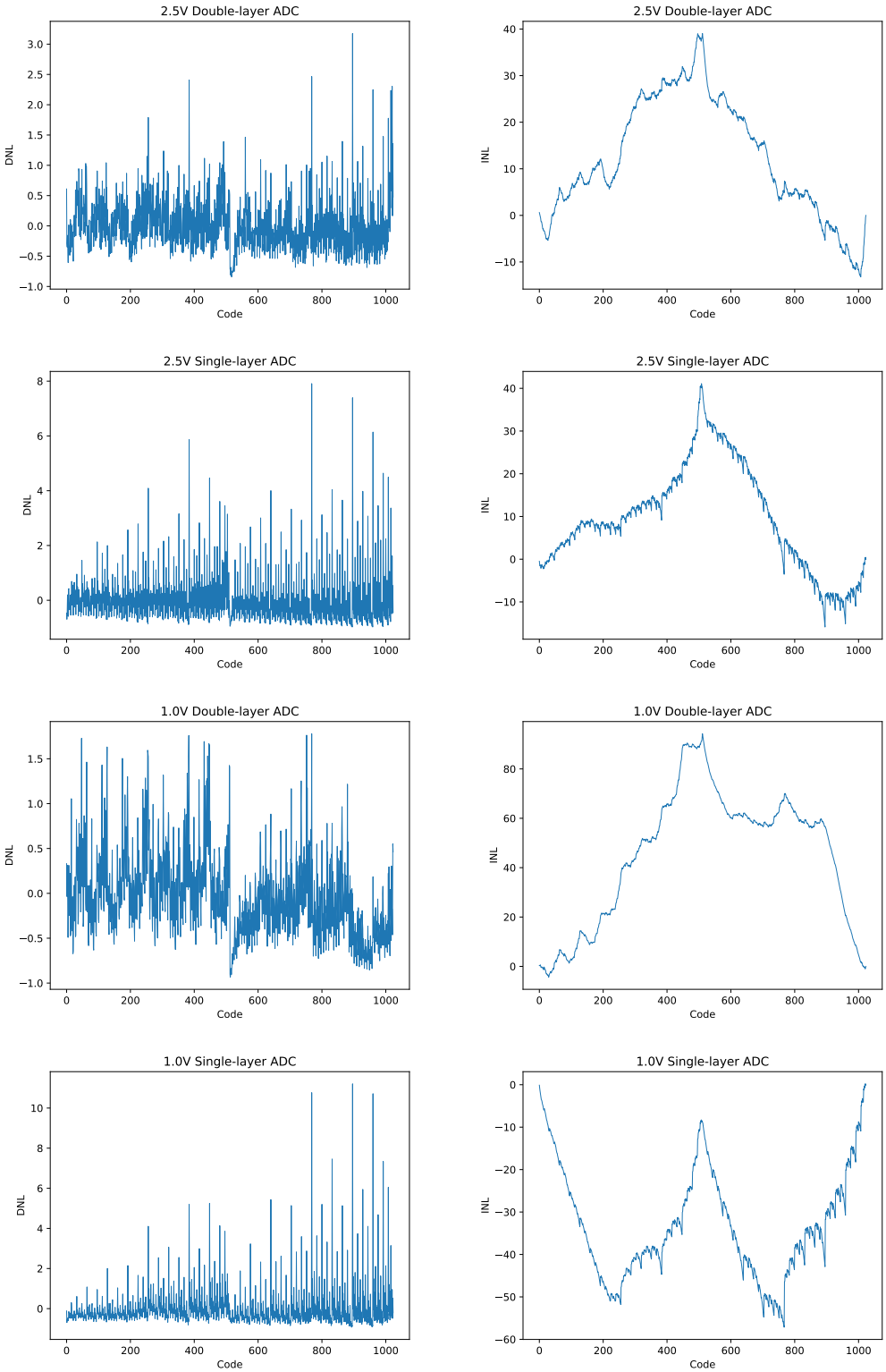


Figure 3.6: Original ADC Linearity (DNL/INL) Test Result

on multiple different spots. A similar effect also happens on some other codes. Two examples are shown in Figure 3.7.

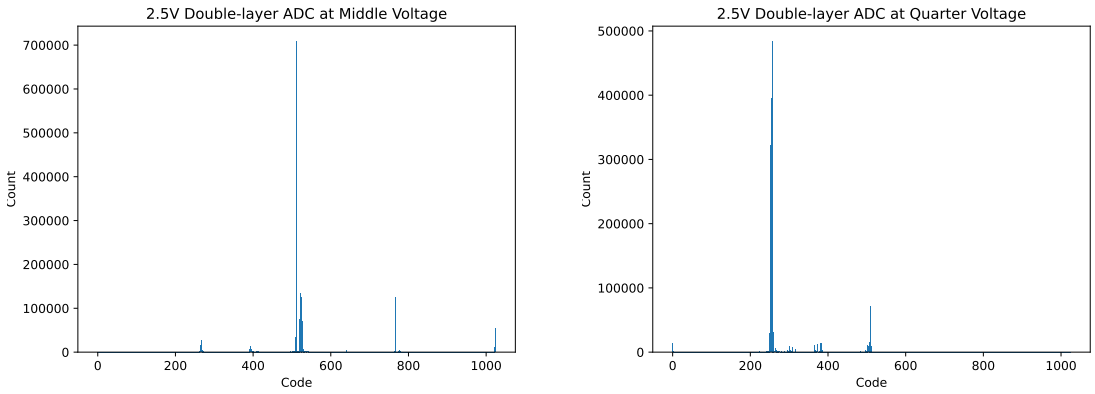


Figure 3.7: Original ADC False Codes Artifacts

Normally, when a bad DNL caused by mismatch in the CDAC manifests, a range of codes is mapped to a single bin near the expected ones, resulting in a gap in the histogram. Also, this gap is usually the widest at the middle code where all the bits flip, because the mismatch between the MSB and all the rest is taken into account. Looking at the histograms in Figure 3.7, it is likely that the mismatch exists in the middle code because of the gap at the center, but it is certain that the codes at the other locations are caused by something else. Because of this false code problem, the ADCs' SINAD and ENOB were not tested. Other than the false codes, the plot also shows unacceptable resolution as the output codes are not in a single bin, but a distribution centered around a bin. This can come from the noise within the ADC. In conclusion, it can be explained that the unevenness in the histogram in Figure 3.5 is contributed to by the false codes problem, the bad resolution, and the mismatch.

3.2.3 Possible Causes

3.2.3.1 False Code

Intuitively, the false code problem can be caused by setup or hold violations in the asynchronous logic block. During the design, the analog-extracted block passed the dynamic verification under all corners but was not put through a static timing analysis because of the difficulties in analyzing asynchronous logics. The fact that the logic is asynchronous also makes it harder to debug because it cannot be slowed down to at least identify the type of the violations (circuit starting to work under a lower clock frequency indicates setup violations, otherwise it can be hold violations).

Going through the logic, there are two most vulnerable spots. The first one is that the comparison ready signal may arrive too early at a bit logic block that the comparison data does not have enough time to be written back before the temporary data register is frozen. Another possible problem can happen when the result was transferred from the bit logic blocks' temporary data register to the output DFFs. The rising edge of the last bit logic's next bit start signal is used both as the output DFFs clock and as the reset signal for all the bit logic blocks. When the bit logic resets faster than the speed of the output DFFs latching the result, a hold violation happens and the result output may become undefined.

3.2.3.2 Low Resolution

The low resolution may be caused by the comparator. In the original chip, a different comparator topology was used (schematic shown in 3.8). Though having the same concept of putting the input transistors at the bottom to reduce the kickback noise, the transient noise level of the original design is significantly higher than the new topology with similar transistor sizing. In periodic noise simulation, the original

topology has a noise RMS value of 1.52 mV, exceeding half of the equivalent LSB voltage 0.977 mV. The transistor sizing in the original design is also far from ideal. The transistors are not at their minimal length, increasing the chance of memory effect affecting the conversion result of each succeeding bit because it becomes harder to fully discharge every node when resetting. This memory effect, in an extreme case when the comparison is stuck on the same result for multiple bits, can also lead to the noise and false code problems.

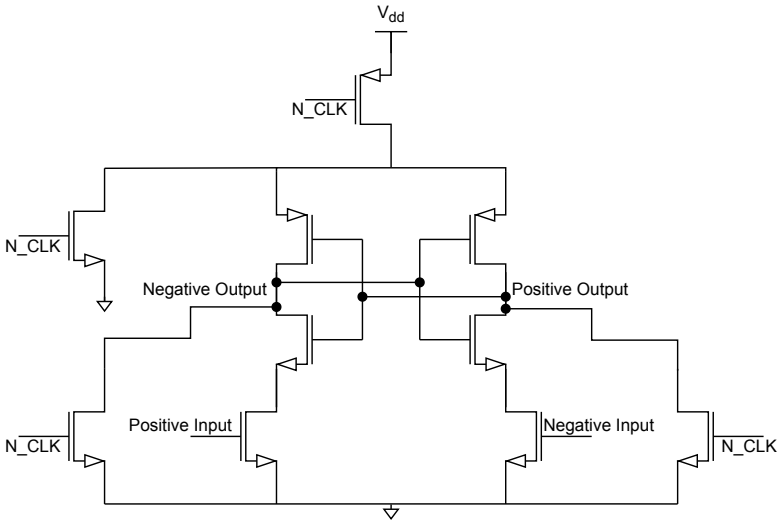


Figure 3.8: Original Comparator Schematic Diagram

Differently from the new topology, the original comparator idles with its outputs at ground instead of 2.5 V. When a comparison starts, the outputs will rise to the meta-stable voltage above 0.5 V, which, after shifted down to 1.0 V, causes both outputs to go to 1 V. Since the logic block expects a clean result without any intermediate state, this glitch can be problematic if not filtered. Shown in Figure 3.9, the original chip uses a filter circuit made of 2.5 V transistors and is slow enough to ignore the glitch. However, with PVT variations changing the speed of the circuit, the safest way is to use a comparator which idles with its outputs at 2.5 V like the new design

does.

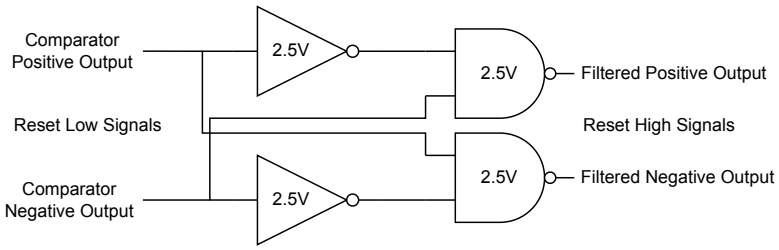


Figure 3.9: Original Comparator Output Filter Circuit

3.2.3.3 Mismatch

The mismatch problem can be related to the CDAC. First, the design from the original paper uses a differential setup. Compared to the single-ended topology used in this chip, the symmetry in a differential CDAC is naturally advantageous in canceling out some artifacts affecting both positive and negative halves. These includes the charge injection from the sample switch, the kickback noise from the comparator, and the process variation affecting the CDAC accuracy. Second, the original CDAC layout has very short negative fingers to reduce the negative capacitance. In the unary bits, the negative fingers are 1.31 μm and 1.07 μm for the 2.5 V and 1 V versions, respectively. This may lead to worse matching among the short negative fingers, and affect the accuracy of the unary bit unit. Third, the original single-ended CDAC has the bits laid out in an incrementing order, also meaning the unary and binary bits are at the two opposite sides of the layout. If a possible process variation applies a MOM capacitance density gradient across the CDAC, there will be significant capacitance error especially between the MSB and the rest. Also, to reduce the parasitic capacitance, dummies were only put outside the CDAC in the original chip. However, a single dummy at the each end of the CDAC is needed to preserve the layout pattern for better matching.

3.3 The New Test Chip

The new test chip is designed for the evaluation of the new ADCs and an analog front end (AFE) design for an unrelated research project. Knowing the problems discussed above, fixes are applied to the new ADCs on this chip. The fixes are namely:

- The new comparator with low noise and 2.5 V idle outputs is used.
- The layout of the CDAC is updated with binary bits between the MSB and the rest unary bits.
- Negative finger length is increased.
- Extra dummies are put at the two ends of the CDAC.
- Differential ADCs are designed.
- ADCs using synchronous logic blocks are designed as backups.
- V_t swap and transistor sizing methods are used to add delay to comparison ready signal in the asynchronous logic.
- Delay is added between output DFFs clock and the bit logic reset.

The whole chip layout is shown in 3.10. The area surrounded by the red box is dedicated for ADC testing, and 28 ADCs are labeled with their ID.

There are 28 ADCs in the ADC section on the new chip, each with its own unique configuration. For testing, a new controller is implemented to generate the trigger pulse or the clock for the ADCs and multiplex the digital result sent to the chip pins. All the functions can be accessed and configured through an SPI bus. Details will be given in the following subsections below.

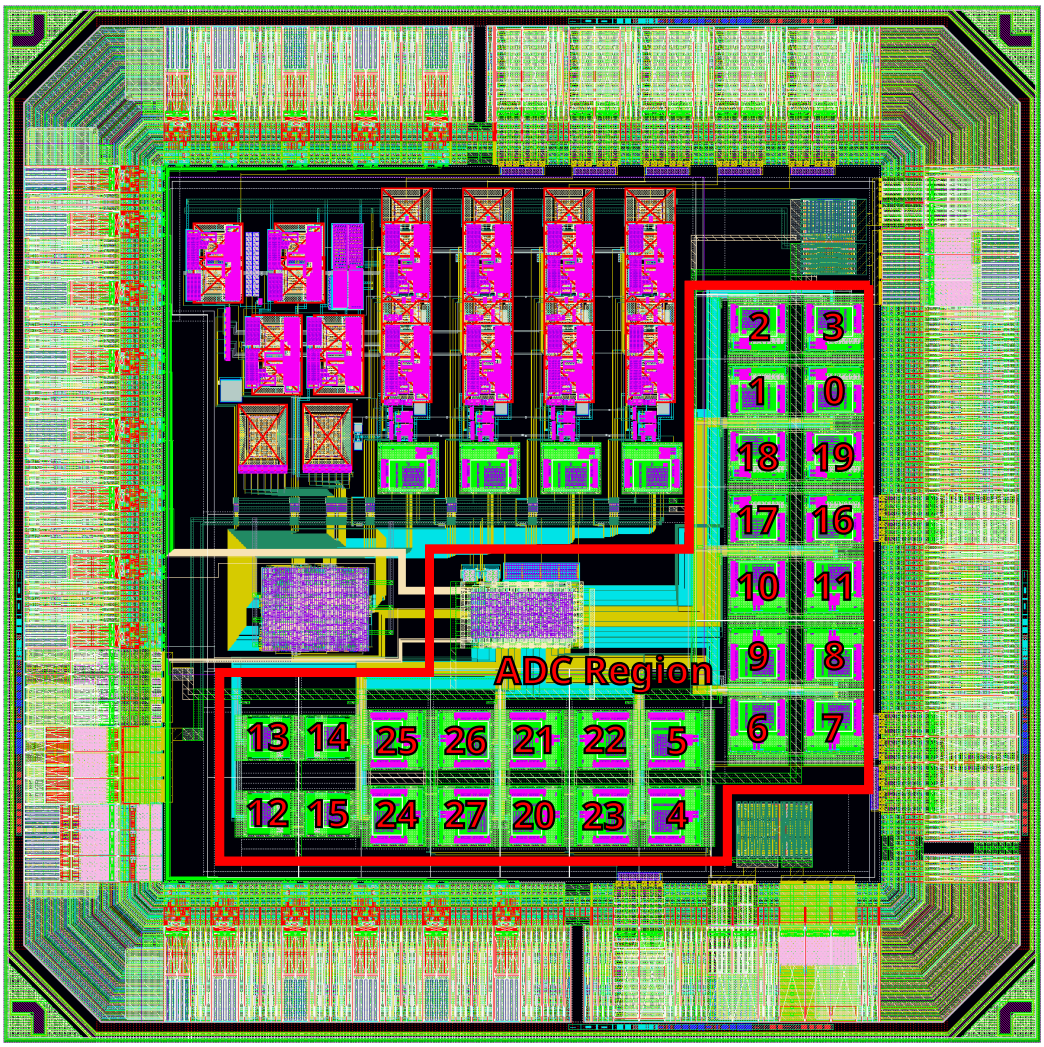


Figure 3.10: The New Test Chip Layout

3.3.1 ADC Configurations

Although the main focus of this thesis is the single-ended 2.5 V version, having had problems with the original test chip, 28 different ADCs are implemented on the new chip to pinpoint the cause of the previous issue as well as testing how different CDAC layouts performs. These ADCs are different mainly in four aspects: 1 V or 2.5 V, differential or single-ended, asynchronous or synchronous logic, and CDAC LSB effective capacitance and spacing between positive/negative strips. Table 3.5 lists all

the ADC configurations:

Table 3.5: ADC Configurations in the New Test Chip

ADC ID	Voltage	Topology	Logic	CDAC
0	2.5 V	Single-ended	Asynchronous	0.60 μm LSB length delta, 0.13 μm strip spacing
1	2.5 V	Single-ended	Asynchronous	0.50 μm LSB length delta, 0.13 μm strip spacing
2	2.5 V	Single-ended	Asynchronous	0.70 μm LSB length delta, 0.13 μm strip spacing
3	2.5 V	Single-ended	Asynchronous	0.60 μm LSB length delta, 0.50 μm strip spacing
4	2.5 V	Differential	Asynchronous	0.30 μm LSB length delta, 0.13 μm strip spacing
5	2.5 V	Differential	Asynchronous	0.25 μm LSB length delta, 0.13 μm strip spacing
6	2.5 V	Differential	Asynchronous	0.35 μm LSB length delta, 0.13 μm strip spacing
7	2.5 V	Differential	Asynchronous	0.30 μm LSB length delta, 0.50 μm strip spacing
8	2.5 V	Differential	Asynchronous	0.30 μm LSB length delta, 0.13 μm strip spacing, reduced LSB
9	2.5 V	Differential	Asynchronous	0.25 μm LSB length delta, 0.13 μm strip spacing, reduced LSB
10	2.5 V	Differential	Asynchronous	0.35 μm LSB length delta, 0.13 μm strip spacing, reduced LSB
11	2.5 V	Differential	Asynchronous	0.30 μm LSB length delta, 0.50 μm strip spacing, reduced LSB
12	1.0 V	Single-ended	Asynchronous	0.40 μm LSB length delta, 0.13 μm strip spacing
13	1.0 V	Single-ended	Asynchronous	0.30 μm LSB length delta, 0.13 μm strip spacing
14	1.0 V	Single-ended	Asynchronous	0.50 μm LSB length delta, 0.13 μm strip spacing
15	1.0 V	Single-ended	Asynchronous	0.40 μm LSB length delta, 0.50 μm strip spacing
16	2.5 V	Single-ended	Synchronous	0.60 μm LSB length delta, 0.13 μm strip spacing
17	2.5 V	Single-ended	Synchronous	0.50 μm LSB length delta, 0.13 μm strip spacing
18	2.5 V	Single-ended	Synchronous	0.70 μm LSB length delta, 0.13 μm strip spacing
19	2.5 V	Single-ended	Synchronous	0.60 μm LSB length delta, 0.50 μm strip spacing
20	2.5 V	Differential	Synchronous	0.30 μm LSB length delta, 0.13 μm strip spacing
21	2.5 V	Differential	Synchronous	0.25 μm LSB length delta, 0.13 μm strip spacing
22	2.5 V	Differential	Synchronous	0.35 μm LSB length delta, 0.13 μm strip spacing
23	2.5 V	Differential	Synchronous	0.30 μm LSB length delta, 0.50 μm strip spacing
24	2.5 V	Differential	Synchronous	0.30 μm LSB length delta, 0.13 μm strip spacing, reduced LSB
25	2.5 V	Differential	Synchronous	0.25 μm LSB length delta, 0.13 μm strip spacing, reduced LSB
26	2.5 V	Differential	Synchronous	0.35 μm LSB length delta, 0.13 μm strip spacing, reduced LSB
27	2.5 V	Differential	Synchronous	0.30 μm LSB length delta, 0.50 μm strip spacing, reduced LSB

The 1 V versions aim for the lowest power consumption, the highest sampling rate, and the smallest area. Thus, no synchronous 1 V version is included.

The differential ADCs are used to test whether the issues with the original chip are related to the asymmetry in the single-ended CDAC. The same traditional switching scheme is used for differential ADCs. In the CDAC column, "reduced LSB" means using one capacitor that is double the capacitance only in the positive or in the negative CDAC for the two least significant bits, instead of having regular sized capacitors on both CDACs. An example is given in Figure 3.11. This method reduces a large portion of negative capacitance in the lower bits. However, it will shift the common mode voltage of the two CDAC outputs when converting the last two bits,

and this may lead to wrong comparison results depending on how the comparator offset shifts according to the input common mode voltage. Also, "reduced LSB" only works on differential ADCs because it needs both positive and negative CDACs.

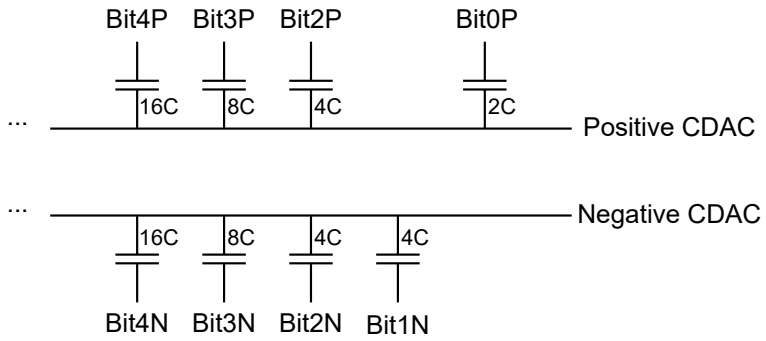


Figure 3.11: Reduced LSB Illustration

There are also synchronous ADCs that are clocked by a ring oscillator on the chip, and a typical clock frequency is 500 MHz. They are not expected to be low power because of the high frequency clock tree needed to distribute the clock, but having synchronous ADCs as a backup is helpful in isolating the potential problems with the asynchronous logic from the rest of the components, because it is difficult to reliably verify the timing of a custom asynchronous logic block.

These ADC configurations can also be partitioned into groups of four, with each ADC in it having a different CDAC LSB and finger spacing. Practically, the larger the LSB length delta is, the shorter the negative finger will be in the unary bits, but, at the same time, the less the negative capacitance that the CDAC will have. Short fingers do not match with each other as well as long ones, reducing the capacitance accuracy of the higher unary bits. However, it is also not desirable to have too much negative capacitance. Therefore, the different LSB length deltas are implemented to find a good balance point in this trade off. Furthermore, the configurations with different strip spacing between the positive and negative fingers are for testing its

effect on the capacitance accuracy. Ideally, the edge effect within a capacitor pair is canceled out because both fingers have the same edges. However, it is unknown if the inconsistency of the gap size around the fingers would cause worse matching.

3.3.2 Chip Pins

In Figure 3.12, the bonding diagram shows the connection between the bond pads and the QFN44 package, and Table 3.6 explains the function of each pin.

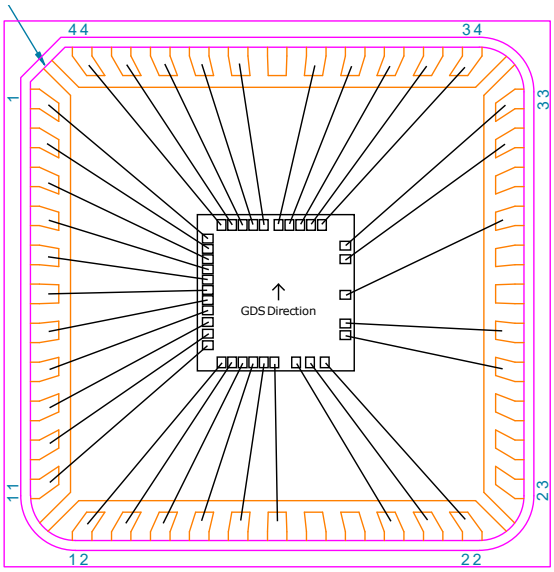


Figure 3.12: The New Test Chip Bonding Diagram

For the power and ground connections, the VSSA pins numbered 21 and 33 are joined together in the chip seal ring, but internally, pin 33 is for 2.5 V analog domain and pin 21 is for 1 V analog domain. Moreover, since there is no dedicated digital 2.5 V rail (VDDD25), the analog 2.5 V (VDDA25) with VSSD as ground is, instead, used for all the level-up-shifters. To reduce the noise coupled into the analog power rail, star wiring is applied to the digital and the analog branches of VDDA25.

Limited by the number of pins available, each ADC signal input pin is shared across multiple ADCs with the same input type (same voltage and single-ended/differential).

Table 3.6: New Chip Pins

Pin#	Pin Name	Purpose	Type	Notes
1-6	Debug [4:9]	Both	Digital Out	Digital debug signal port that can also work as parallel data output
7	Clock 32k	AFE	Digital In	
8	Reset	Both	Digital In	Active-high reset that resets all ADCs and the controller. Internal pull-down
9	VSSD	Both	Ground	Digital ground
10	VDDD10	Both	Power	1 V core digital power rail
11	VDDIO	Both	Power	3.3 V IO power rail
12	Trigger/Clock	ADC	Digital In	Async sample trigger that starts internal clock/pulse generation on rising edge, or directly pass the trigger/clock to ADC
13	SCLK	Both	Digital In	
14	MOSI	Both	Digital In	
15	MISO	Both	Digital Out	High impedance when CSN is high
16	CSN	Both	Digital In	Active-low chip select. Internal pull-up.
17	Slave Switch	Both	Digital In	Multiplex debug/data available/and SPI pins between AFE and ADC controllers. Hold high for ADC testing
20	Single Ended 10	ADC	Analog In	Analog input for 1 V single-ended ADCs
21	VSSA	Both	Ground	Analog Ground
22	VDDA10	ADC	Power	1 V analog power rail
26	Diff N 25	ADC	Analog In	Negative analog input for 2.5 V differential ADCs
27	Diff P 25	ADC	Analog In	Positive analog input for 2.5 V differential ADCs
30	Single Ended 25	ADC	Analog In	Analog input for 2.5 V single-ended ADCs
32	VDDA25	Both	Power	2.5 V analog power rail
33	VSSA	Both	Ground	Analog Ground
34-37	AFE [0:3]	AFE	Analog In	
38	Analog Debug	AFE	Analog Out	
40	Data Available	Both	‘ Digital Out	Active-high signal showing the ADC has done conversion when in ADC testing mode (“Slave Switch” is high)
41-44	Debug [0:3]	Both	Digital Out	Same as pin 1-6

The sample switch in the ADCs functions as the analog multiplexer, and there will be only one ADC actively sampling the input signal at a time. This setup reduces the number of signal input pins needed, at the same time, keeps the parasitic load on the pins way lower than using analog multiplexer made of transmission gates. In addition, no internal buffer is used given the low CDAC total capacitance.

The trigger/clock pin has two working modes depending on the pass-through configuration that can be changed through the SPI interface (discussed in Section 3.3.4). When in external mode, the pin passes the external signal directly to the active ADC. This is not ideal for synchronous ADCs, because the low bandwidth of the pin cell limits the maximum synchronous ADC clock frequency. Switching to internal mode, the chip generates the sample pulse or the clock depending on the logic type of the active ADC. For asynchronous ADCs, the logic sends out a sample/hold pulse with configurable width, whereas a specific clock waveform is generated for synchronous ADCs. Also in this mode, the trigger/clock pin only works as an asynchronous sampling request input. It reacts to a positive edge only when the active ADC is ready and triggers the exact ADC to perform one conversion. The three types of the

input signal waveform are shown as follows:

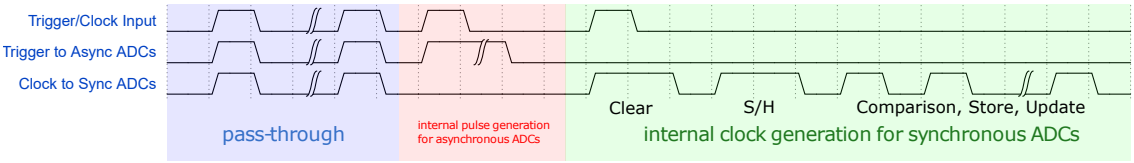


Figure 3.13: Three Trigger and Clock Modes

More on the synchronous ADC clock waveform, the first pulse clears the current result and restores the CDAC states for a new sample. The second pulse is the sample and hold pulse when the sample switch(s) closes. Its width is determined by the synchronous sample pulse width setting. Following these two pulses are another 10 pulses, whose positive edge starts a comparison, and the negative edge triggers result storing and CDAC updating.

3.3.3 The ADC Controller

The ADC controller has three main functions: 1) multiplexing the input and output pins, 2) passing through or generating the trigger pulse or clock for the active ADC, 3) writing and reading configuration registers or transmitting the active ADC results over SPI.

The first function is applicable to all the debug pins, data available pins and the SPI bus pins. Using the slave switch input, all these pins can be connected either to the ADC controller when slave switch is high or the AFE controller when low. In the ADC mode, the active ADC's result is sent to the debug pins for parallel output unless in debug mode (discussed in Section 3.3.4). Also, the data available pin reflects if the active ADC is ready.

The asynchronous trigger pulse is generated using the circuit in Figure 3.14. Starting with pulse generation, it uses an externally triggered D flip-flop that is asyn-

chronously reset by its delayed output. The delay is realized using a chain of delay cells, and signals are tapped off the stages in the chain to make multiple outputs with different delays. These outputs can be multiplexed and turned into a single asynchronous reset signal to get the variable pulse width. In the chip, there are 32 stages in the delay chain, and each stage has around 700 ps of delay under typical corner.

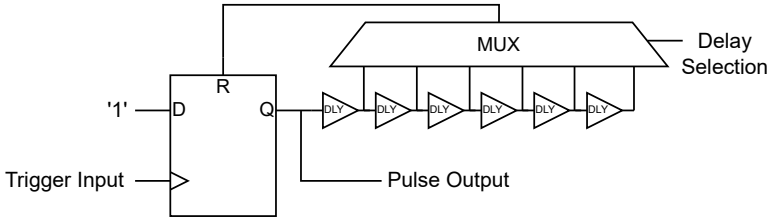


Figure 3.14: Pulse Generator Schematic

The clock generation for the synchronous ADCs requires a clock source other than the clock gating logic. The focus of the discussion here is the ring oscillator with adjustable frequency and duty cycle. In the schematic in Figure 3.15, all the transistors are kept at their minimal size, and 2.5 V MOSFETs running under 1 V V_{dd} are used in the inverters and the NAND gate to get lower power consumption as well as the desired lower intrinsic clock frequency without increasing the length of the transistors.

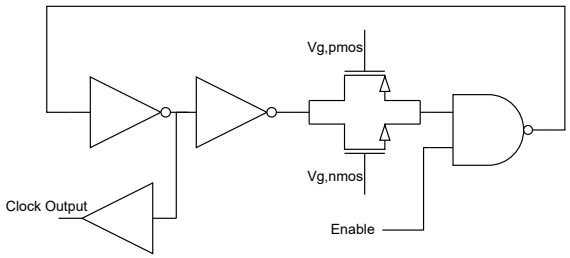


Figure 3.15: Ring Oscillator Schematic

The MOSFETs in the transmission gate are controlled by two 5-bit R2R DACs.

Their gate voltage can be adjusted to achieve different conductivity, changing the speed of the signal propagation, thus varying the oscillating frequency of the ring. Changing only one of the two gate voltages affects both the oscillating frequency and the duty cycle. Generally, a higher NMOS gate voltage results in faster switching and lower duty cycle (duration of "1" in a clock cycle), and a higher PMOS gate voltage has the opposite effects on both. It is obvious how the frequency increases with the lowered propagation delay, but for the change in duty cycle, it is because the NMOS and PMOS are really slow at passing through a voltage that is, respectively, higher than and lower than the overdrive voltage. When purposely setting the pass transistors' gate voltage, desired delay of the falling and rising edge can be achieved to set the ring oscillator's frequency and duty cycle. Through the test, under typical corner, the highest achievable frequency is 938 MHz and the duty cycle roughly ranges from 10% to 90% (the range may change under different frequency).

For reference, lookup tables are included in Appendix B to show the simulated oscillating frequency and dutycycle (typical corner) under different positive and negative DAC code combinations.

3.3.4 The SPI Slave and the Registers

An SPI slave that operates under mode 0 and uses 16-bit frames is implemented to control all the ADCs. It is activated when the slave switch pin is pulled high. A data transfer starts with the chip-select pin (CSN) going from high to low, and resets whenever the CSN is driven high. The slave reads 9 bits at the beginning and outputs 10 bits at the end of the frame. The waveform of a frame is shown in Figure 3.16.

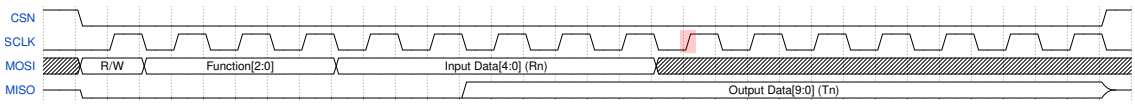


Figure 3.16: SPI Frame

In the diagram, the rising edge highlighted in red triggers a register writing in the finite state machine when the input command requests one.

Figure 3.16 and the following text use Rn to represent the n'th input (MOSI pin) data bit and Tn to denote the n'th output (MISO pin) bit. With a general SPI command format shown in the figure above, all the commands are listed in Table 3.7.

Table 3.7: SPI Commands

R/W	Function	Data Bits	Command Function
1	000	R4-R0 (5 bits)	Write active channel
1	001	R4-R0 (5 bits)	Write asynchronous trigger pulse width
1	010	R2-R0 (3 bits)	Write synchronous sample pulse width
1	011	R2-R0 (3 bits)	Write configurations
1	100	R4-R0 (5 bits)	Write ring oscillator transmission gate NMOS gate voltage
1	101	R4-R0 (5 bits)	Write ring oscillator transmission gate PMOS gate voltage
0	000	T4-T0 (5 bits)	Read active channel
0	001	T4-T0 (5 bits)	Read asynchronous trigger pulse width
0	010	T2-T0 (3 bits)	Read synchronous sample pulse width
0	011	T2-T0 (3 bits)	Read configurations
0	100	T4-T0 (5 bits)	Read ring oscillator transmission gate NMOS gate voltage
0	101	T4-T0 (5 bits)	Read ring oscillator transmission gate PMOS gate voltage
0	110	T9-T0 (10 bits)	Read ADC result

In the table, the R/W and the function columns correspond to the initial two fields in a frame. The following data bits column specifies the indices of the bits containing the actually data. In case of a reading command, the data is sent by the SPI slave on the MISO pin, thus Tn bits are used rather than Rn bits.

Here is more detail about the commands. All the following discussion uses active high signaling unless specifically specified.

Starting with the active channel, the data bits are the ADC number denoted in Table 3.5. Depending on the ADC type, the clock or the trigger will be sent to the active ADC when the trigger/clock pin is activated. Also, the active ADC's conversion results and ready signal will be routed to the debug pins and the "data available" pin for parallel output. Since the data bits can address 32 ADCs, when the active ADC

number is set above 27 (the last ADC), no trigger/clock will be generated and all the result/ready output signals are pulled to "0". The default active ADC is number 0.

When sending the clock or the trigger to the ADC, an important consideration is the sample and hold timing. The duration of this period is controlled by the asynchronous trigger pulse width and the synchronous sample pulse width registers. The former is used to pick the length of the delay cell chain to generate different pulse widths, and the latter decides how many clock cycles to wait before moving on to the conversion phase. Both default to the longest setting (all 1's) after reset.

The configuration register is made up of three bits. Bit 0 is for enabling debug mode. When in this mode, the debug output pins no longer output the ADC result. Instead, the 9th bit of the debug port outputs the trigger or the clock that is sent to the active ADC, allowing for measurement of the sample and hold duration for tuning reference. The debug port now also outputs on the 8th bit, the divided clock that is 1/32 of the ring oscillator frequency. This makes it easier to set the desired clock frequency. Bit 1 in the configuration register is for turning on and off the ring oscillator when needed. Lastly, the bit 2 is for enabling external triggering mode. By default, debug mode and the ring oscillator are turned off, while the external trigger clock mode is turned on.

To control the frequency and the duty cycle of the ring oscillator, the PMOS and NMOS gate voltage of the transmission gate in the ring oscillator can be set through the SPI commands. The data in the command sets the R2R DAC voltages that drive the gates. A high code on the NMOS gate and a low code on the PMOS gate grant faster oscillating, vise versa. The duty cycle changes when only one of the two codes changes, and it can be picked intentionally for a desired value. However, there is no way to measure the duty cycle from the outside because the divided clock output in the debug mode only reveals the clock frequency and the original fast clock is not

able to pass through the pin cell because of the bandwidth limitation. Thus, the best estimate of the duty cycle comes from the simulation result. Additionally, the default DAC code for the NMOS gate voltage is “10000” , and for PMOS, it is “01111”.

The only function that is read-only is the ADC result. This function should only be used after receiving a ready signal on the data available pin to prevent possible timing violation.

For reference, Table 3.8 is a summary of all the registers, and example microcontroller pseudocode for interfacing with the test chip is included in Appendix C.

Table 3.8: Registers Summary

Name	Length (bits)	Default Value in Binary
Active Channel	5	00000
Asynchronous Trigger Pulse Width	5	11111
Synchronous Sample Pulse Width	3	11111
Configurations	3	100
Ring Oscillator Transmission Gate NMOS Gate Voltage	5	10000
Ring Oscillator Transmission Gate PMOS Gate Voltage	5	01111

Chapter 4

Conclusion

This thesis research has investigated the design, fabrication, and test of a recent and innovative CDAC design that greatly reduces the area and power consumption of SAR ADCs. In order to adapt the design methodology for research applications, this work starts with the design of a single-ended 10-bit SAR ADC that consumes 30.01 pJ/sample yielding a power consumption of only 300.1 μW at 10 MSPS.

The fabricated chip was tested using a custom PCB test fixture and verified to operate within the expected low power budget. However, the ADC exhibited signinficant nonlinearities that warranted a second fabrication run. The nonlinearities were characterized, and the circuit was revised to both address known issues and to allow enhanced testing and analysis to better characterize the circuit's performance.

At the time of writing, the second chip is in fabrication, and an updated test fixture PCB has been designed and assembled in preparation for the chip arrival. Given the knowledge gained from the first round of testing, this revised version is expected to resolve the linearity performance of the first, while also exhibiting the excellent area and power characteristics of the first.

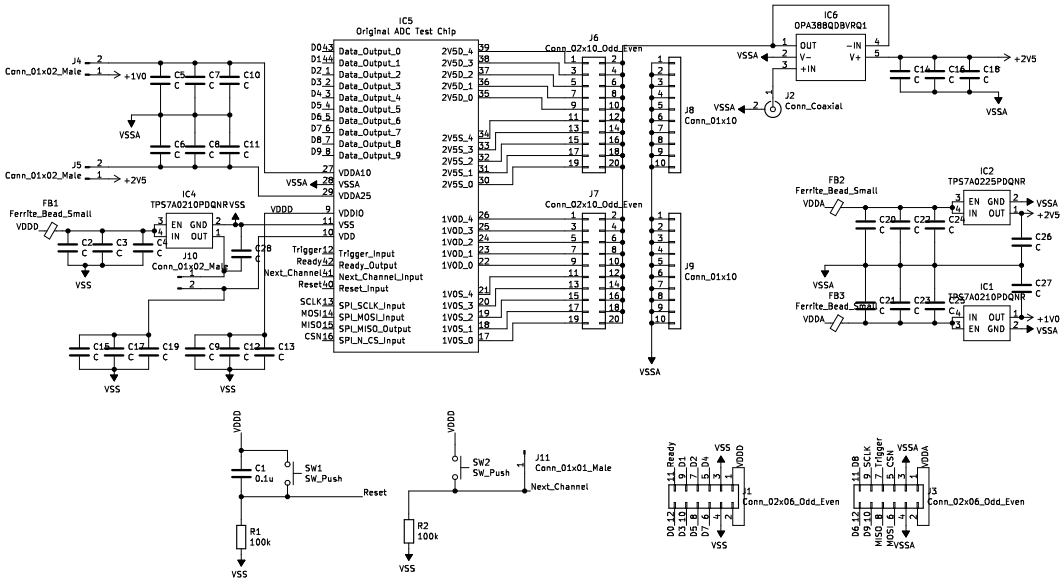
Future work will first characterize the ADCs performance, then comparing the performance trade-offs of the multiple instances present on the chip. Finally, ADCs based on this work will be integrated across multiple projects to support the power

and area demands of those applications.

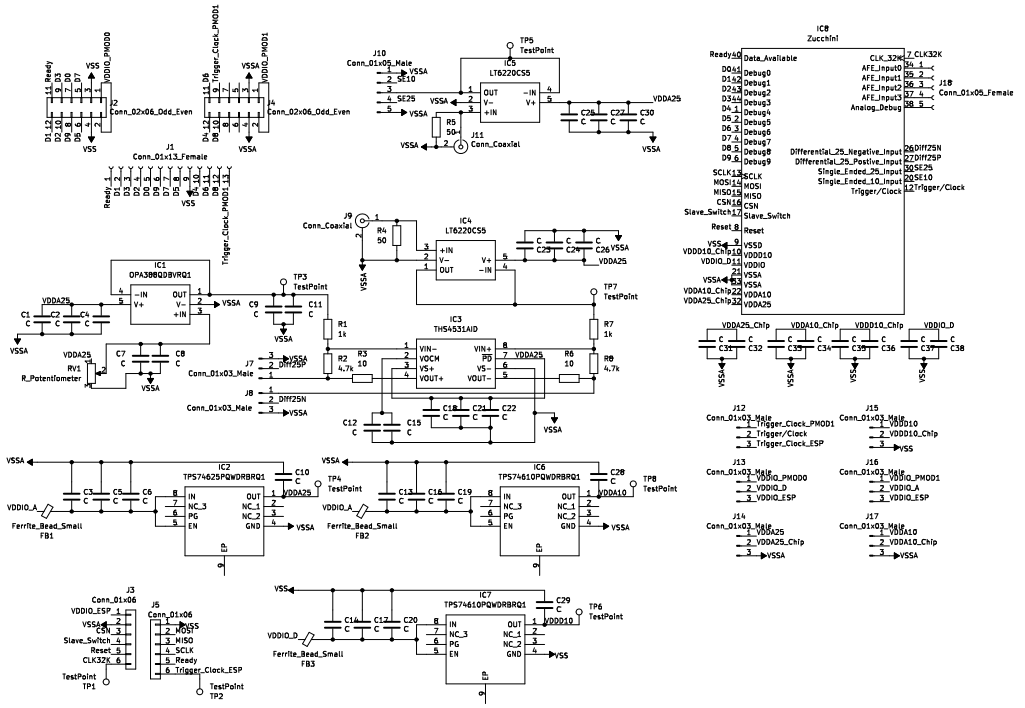
Appendix A

Testbench Board Schematics

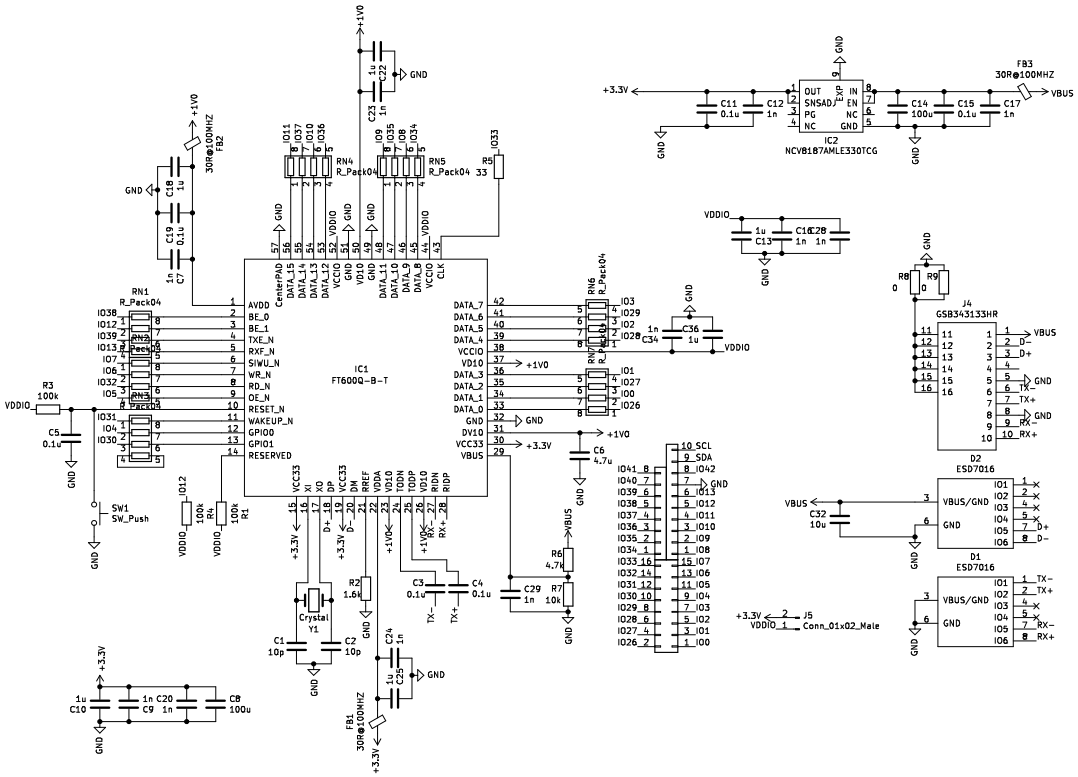
A.1 Original ADC Test Board Schematic



A.2 New ADC Test Board Schematic



A.3 FIFO to USB Board Schematic



Appendix B

Ring Oscillator Lookup Tables

In the following lookup tables, the horizonal axis corresponds to the DAC code for the PMOS, and the vertical axis is the NMOS DAC code.

DAC code combinations that result in a "DNU" (Do Not Use) should not be used, because they make both the PMOS and NMOS work in cut-off region, resulting in a floating node on the transmission gate output.

B.1 DAC Codes VS Frequency (MHz)

N \ P	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	665.7	624.4	579.1	529.6	476.2	419.2	359.3	297.3	235.0	175.0	121.1	78.7	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
1	665.8	624.6	579.3	530.0	476.7	419.9	360.1	298.6	236.8	177.5	124.6	82.8	78.5	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
2	666.0	624.9	579.8	530.7	477.7	421.2	362.1	301.3	240.6	182.9	131.9	91.7	66.1	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
3	666.6	625.7	580.9	532.2	479.8	424.1	366.1	306.9	248.5	193.7	146.4	109.7	84.2	68.3	59.1	55.0	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
4	667.7	627.3	583.1	535.3	484.0	430.1	374.2	318.1	263.9	214.5	173.0	141.4	119.0	103.6	93.0	85.3	79.7	76.8	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
5	670.1	630.6	587.6	541.4	492.5	441.6	390.0	339.5	292.2	250.8	217.0	191.1	171.7	157.2	145.9	136.8	129.3	123.4	120.5	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
6	674.6	636.8	596.1	553.1	508.3	463.0	418.4	376.5	339.0	307.0	280.9	259.9	242.9	228.9	217.1	206.8	197.9	190.5	185.9	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
7	683.0	648.2	611.5	573.6	535.7	498.6	463.8	432.3	404.7	381.0	360.7	343.2	328.0	314.4	302.2	291.1	280.8	271.6	265.3	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
8	697.2	667.1	636.6	606.2	577.0	549.5	524.4	501.8	481.5	463.3	446.8	431.8	417.8	404.7	392.1	379.9	368.0	356.5	347.0	343.5	343.3	339.3	326.7	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
9	719.0	695.2	671.9	649.6	628.4	608.9	590.7	573.9	558.3	543.5	529.4	516.0	502.9	489.8	476.7	463.2	449.0	434.2	420.3	409.8	398.8	380.3	350.1	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
10	746.6	729.1	712.2	696.0	680.8	666.3	652.4	639.1	626.3	613.6	601.2	588.6	575.8	562.5	548.3	533.1	516.3	497.8	478.5	460.0	437.9	405.9	361.2	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
11	776.4	763.4	751.0	738.7	726.9	715.5	704.2	693.0	681.9	670.6	658.8	646.8	634.0	619.9	604.8	587.6	568.0	545.8	521.4	495.4	463.7	420.9	365.7	300.0	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
12	804.5	794.5	784.8	775.2	765.5	756.1	746.5	736.6	726.5	716.0	704.9	693.0	680.2	665.8	649.4	630.8	609.0	583.7	555.2	523.5	484.6	434.3	372.3	301.1	226.3	156.6	DNU	DNU	DNU	DNU	DNU	DNU
13	829.9	822.2	814.0	806.1	798.0	789.9	781.5	772.6	763.4	753.5	743.0	731.2	718.3	703.7	686.8	667.1	643.8	616.4	584.9	549.1	505.2	450.1	383.3	308.1	230.4	158.5	100.5	DNU	DNU	DNU	DNU	DNU
14	851.7	845.2	838.4	831.6	824.6	817.3	809.7	801.8	793.1	783.8	773.5	762.1	749.2	734.4	717.1	696.7	672.3	643.5	609.8	570.9	523.4	464.6	394.5	316.4	236.4	162.8	103.2	61.6	DNU	DNU	DNU	DNU
15	868.7	863.2	857.6	851.6	845.4	838.8	832.0	824.4	816.5	807.4	797.4	786.2	773.4	758.7	741.1	720.3	695.2	665.2	630.0	589.0	538.9	477.5	404.9	324.7	243.1	168.1	107.2	63.8	DNU	DNU	DNU	DNU
16	882.0	877.2	872.2	866.9	861.3	855.4	849.0	842.0	834.3	825.8	816.1	805.2	792.6	777.8	760.2	739.1	713.6	682.9	646.7	604.2	552.3	489.1	414.9	333.3	250.5	174.3	112.1	67.4	DNU	DNU	DNU	DNU
17	892.4	888.3	883.6	879.1	873.9	868.6	862.6	855.8	848.5	840.3	830.9	820.2	807.9	793.2	775.7	754.5	728.8	697.7	660.8	617.3	564.3	499.9	424.7	342.2	258.5	181.5	118.2	72.3	47.6	DNU	DNU	DNU
18	900.6	896.8	892.8	888.7	883.8	878.8	873.1	866.9	860.0	852.1	843.0	832.5	820.3	805.9	788.5	767.4	741.7	710.4	673.2	629.0	575.3	510.3	434.5	351.6	267.5	189.9	126.0	79.1	50.6	DNU	DNU	DNU
19	907.2	904.1	900.2	896.3	892.0	887.4	881.9	876.1	869.3	861.9	852.9	842.8	830.9	816.6	799.5	778.5	752.8	721.7	684.3	639.8	585.8	520.6	444.7	361.7	277.7	200.1	135.9	88.8	58.9	DNU	DNU	DNU
20	912.7	909.8	906.3	902.9	898.7	894.4	889.4	883.6	877.3	869.8	861.4	851.5	839.9	825.9	809.0	788.3	762.8	731.8	694.5	650.0	596.0	530.9	455.4	372.9	289.5	212.7	149.5	103.5	74.4	59.7	64.0	DNU
21	917.2	914.5	911.4	908.2	904.3	900.2	895.4	890.0	884.1	876.8	868.6	859.0	847.5	834.0	817.4	797.0	771.8	741.1	704.1	660.0	606.3	541.6	466.8	385.4	303.5	228.7	168.4	125.7	99.6	85.4	78.4	75.2
22	921.0	918.6	915.7	912.8	909.1	905.2	900.9	895.7	889.7	883.0	875.0	865.6	854.5	841.2	824.9	805.2	780.3	749.8	713.4	669.6	616.6	552.8	479.2	399.5	320.3	249.6	194.7	157.9	136.3	125.0	119.4	116.9
23	924.5	921.9	919.4	916.5	913.4	909.5	905.3	900.4	894.8	888.3	880.6	871.5	860.8	847.8	831.9	812.3	788.2	758.3	722.5	679.4	627.1	564.7	492.7	415.8	340.9	276.6	229.7	200.2	183.7	175.4	171.4	169.5
24	927.1	924.9	922.6	919.8	916.8	913.3	909.3	904.8	899.2	893.0	885.6	876.9	866.4	853.8	838.4	819.3	795.7	766.5	731.3	689.2	638.1	577.3	507.9	434.8	366.1	310.6	272.9	250.6	238.7	232.8	230.0	228.8
25	929.4	927.6	925.3	922.7	919.9	916.8	912.8	908.5	903.5	897.3	890.2	881.9	871.8	859.6	844.6	826.0	803.0	774.5	740.3	699.2	649.7	591.0	524.9	457.1	396.6	351.2	322.2	306.0	297.6	293.5	291.6	290.7
26	931.4	929.7	927.7	925.5	922.7	919.6	916.1	911.8	907.2	901.4	894.4	886.3	876.7	864.9	850.6	832.5	810.1	782.5	749.3	709.6	662.0	606.0	544.1	483.2	432.2	396.6	375.2	363.5	357.6	354.8	353.5	352.9
27	933.3	931.5	929.7	927.6	925.1	922.3	918.9	914.9	910.3	905.0	898.4	890.7	881.3	870.0	856.3	839.0	817.3	790.6	758.6	720.6	675.1	622.7	566.2	513.3	472.1	445.1	429.5	421.3	417.1	415.2	414.2	413.8
28	934.7	933.3	931.5	929.6	927.5	924.6	921.5	917.8	913.5	908.3	902.2	894.9	886.0	875.2	861.9	845.2	824.6	798.9	768.3	732.1	689.5	641.0	590.9	546.9	514.8	494.9	483.7	477.8	474.9	473.5	472.9	472.6
29	936.1	934.7	933.3	931.4	929.4	926.8	923.9	920.5	916.3	911.4	905.7	898.7	890.2	879.9	867.2	851.4	831.7	807.3	778.4	744.4	704.8	661.4	618.6	583.2	558.9	544.3	536.3	532.2	530.2	529.2	528.8	528.6
30	937.3	936.1	934.6	933.0	931.1	928.8	926.2	922.9	919.1	914.7	909.2	902.5	894.6	884.9	872.9	857.8	839.1	816.1	788.8	757.3	721.7	683.7	648.4	620.9	602.8	592.2	586.7	583.8	582.3	581.7	581.4	581.3
31	938.3	937.3	936.0	934.6	932.9	930.8	928.2	925.2	921.8	917.6	912.4	906.3	898.8	889.8	878.4	864.2	846.6	825.1	799.9	771.2	739.6	707.6	679.5	658.7	645.6	638.1	634.1	632.1	631.1	630.7	630.5	630.4

B.2 DAC Codes VS Dutycycle (Positive%)

N \ P	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	64.05	66.30	68.70	71.24	73.89	76.64	79.47	82.38	85.33	88.21	90.83	92.89	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
1	64.04	66.29	68.69	71.22	73.87	76.61	79.43	82.33	85.25	88.10	90.69	92.78	91.90	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
2	64.02	66.26	68.66	71.18	73.82	76.54	79.34	82.20	85.08	87.87	90.39	92.45	93.77	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
3	63.99	66.21	68.59	71.10	73.71	76.41	79.16	81.96	84.74	87.40	89.78	91.71	93.14	94.09	94.65	94.84	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
4	63.91	66.11	68.46	70.93	73.50	76.12	78.79	81.45	84.05	86.48	88.58	90.25	91.47	92.32	92.90	93.29	93.52	93.54	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
5	63.75	65.90	68.20	70.59	73.06	75.56	78.05	80.47	82.75	84.78	86.46	87.77	88.73	89.43	89.91	90.23	90.42	90.45	90.21	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
6	63.44	65.51	67.68	69.93	72.21	74.47	76.65	78.68	80.49	82.02	83.25	84.21	84.92	85.44	85.80	86.00	86.03	85.88	85.37	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
7	62.86	64.76	66.73	68.70	70.65	72.50	74.21	75.72	77.00	78.04	78.89	79.54	80.03	80.36	80.53	80.52	80.31	79.82	78.86	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
8	61.85	63.47	65.08	66.64	68.10	69.42	70.57	71.56	72.38	73.06	73.60	73.99	74.25	74.36	74.31	74.05	73.52	72.64	71.15	68.48	64.36	58.85	51.80	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
9	60.26	61.48	62.64	63.71	64.66	65.51	66.23	66.84	67.34	67.73	68.02	68.19	68.25	68.15	67.87	67.35	66.52	65.26	63.32	60.16	55.63	49.86	42.84	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
10	58.10	58.93	59.68	60.36	60.96	61.48	61.91	62.26	62.54	62.72	62.82	62.81	62.68	62.39	61.90	61.16	60.08	58.52	56.26	52.85	48.23	42.56	35.96	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
11	55.71	56.25	56.73	57.14	57.51	57.81	58.06	58.24	58.35	58.38	58.33	58.17	57.89	57.44	56.80	55.89	54.62	52.87	50.43	46.96	42.45	37.07	30.99	24.55	DNU	DNU	DNU	DNU	DNU	DNU	DNU	DNU
12	53.47	53.82	54.12	54.39	54.61	54.78	54.89	54.96	54.96	54.89	54.73	54.47	54.10	53.56	52.82	51.81	50.45	48.61	46.12	42.73	38.44	33.42	27.85	22.03	16.47	11.74	DNU	DNU	DNU	DNU	DNU	DNU
13	51.61	51.84	52.04	52.20	52.33	52.41	52.45	52.44	52.37	52.23	52.02	51.70	51.26	50.68	49.90	48.85	47.45	45.60	43.15	39.88	35.84	31.16	26.00	20.65	15.54	11.16	7.78	DNU	DNU	DNU	DNU	DNU
14	50.20	50.35	50.47	50.56	50.63	50.65	50.64	50.57	50.46	50.27	50.01	49.66	49.20	48.58	47.77	46.71	45.30	43.46	41.06	37.93	34.09	29.67	24.83	19.81	15.02	10.90	7.68	5.47	DNU	DNU	DNU	DNU
15	49.17	49.26	49.34	49.38	49.40	49.38	49.33	49.23	49.08	48.87	48.58	48.20	47.71	47.08	46.25	45.18	43.79	41.96	39.61	36.58	32.91	28.70	24.08	19.31	14.75	10.82	7.72	5.52	DNU	DNU	DNU	DNU
16	48.41	48.47	48.51	48.52	48.51	48.46	48.38	48.25	48.08	47.84	47.53	47.14	46.64	46.00	45.16	44.10	42.70	40.90	38.60	35.66	32.13	28.08	23.64	19.05	14.66	10.86	7.86	5.70	DNU	DNU	DNU	DNU
17	47.85	47.89	47.89	47.88	47.84	47.77	47.67	47.52	47.33	47.08	46.76	46.35	45.85	45.20	44.37	43.31	41.93	40.15	37.89	35.04	31.63	27.71	23.41	18.95	14.70	11.02	8.09	5.98	5.22	DNU	DNU	DNU
18	47.42	47.43	47.42	47.39	47.33	47.25	47.12	46.97	46.76	46.50	46.18	45.77	45.26	44.61	43.79	42.73	41.37	39.62	37.40	34.63	31.31	27.51	23.33	19.00	14.87	11.29	8.45	6.40	5.33	DNU	DNU	DNU
19	47.07	47.08	47.05	47.00	46.93	46.84	46.71	46.54	46.33	46.07	45.73	45.33	44.82	44.17	43.36	42.32	40.97	39.25	37.07	34.37	31.15	27.45	23.38	19.16	15.15	11.69	8.96	6.99	5.86	DNU	DNU	DNU
20	46.81	46.80	46.76	46.71	46.62	46.53	46.39	46.21	45.99	45.72	45.39	44.99	44.48	43.85	43.04	42.02	40.70	39.00	36.87	34.24	31.10	27.49	23.53	19.44	15.55	12.23	9.65	7.85	6.80	6.51	7.93	DNU
21	46.60	46.58	46.53	46.47	46.38	46.27	46.13	45.95	45.74	45.47	45.14	44.73	44.23	43.61	42.82	41.81	40.51	38.85	36.76	34.20	31.14	27.63	23.79	19.81	16.08	12.95	10.60	9.04	8.17	7.75	7.58	7.52
22	46.43	46.40	46.34	46.28	46.19	46.07	45.94	45.75	45.53	45.27	44.95	44.54	44.05	43.44	42.66	41.68	40.41	38.78	36.74	34.24	31.27	27.86	24.13	20.31	16.77	13.90	11.86	10.62	9.94	9.62	9.46	9.40
23	46.29	46.25	46.20	46.13	46.04	45.92	45.77	45.60	45.38	45.12	44.80	44.41	43.93	43.33	42.57	41.60	40.37	38.77	36.79	34.35	31.46	28.16	24.56	20.92	17.64	15.11	13.45	12.50	12.01	11.78	11.67	11.61
24	46.18	46.14	46.08	46.00	45.91	45.80	45.65	45.49	45.27	45.01	44.70	44.32	43.85	43.26	42.52	41.58	40.37	38.82	36.88	34.52	31.73	28.54	25.10	21.68	18.73	16.59	15.29	14.59	14.24	14.08	14.00	13.96
25	46.08	46.05	45.98	45.91	45.82	45.71	45.56	45.39	45.19	44.93	44.63	44.27	43.81	43.24	42.52	41.60	40.43	38.92	37.03	34.74	32.06	29.00	25.75	22.61	20.04	18.31	17.32	16.81	16.55	16.43	16.37	16.35
26	46.01	45.97	45.91	45.84	45.75	45.63	45.50	45.33	45.14	44.89	44.59	44.23	43.79	43.24	42.55	41.66	40.52	39.06	37.23	35.03	32.45	29.55	26.52	23.72	21.56	20.20	19.45	19.07	18.88	18.79	18.75	18.73
27	45.96	45.90	45.85	45.78	45.69	45.59	45.45	45.29	45.10	44.87	44.58	44.24	43.80	43.27	42.61	41.76	40.65	39.24	37.48	35.37	32.91	30.19	27.44	25.01	23.26	22.20	21.64	21.35	21.21	21.15	21.12	21.10
28	45.91	45.87	45.81	45.74	45.66	45.55	45.42	45.27	45.09	44.86	44.59	44.26	43.85	43.35	42.70	41.88	40.82	39.45	37.77	35.76	33.45	30.93	28.48	26.46	25.07	24.27	23.85	23.64	23.53	23.48	23.46	23.45
29	45.87	45.83	45.78	45.71	45.64	45.53	45.41	45.27	45.09	44.88	44.62	44.30	43.91	43.42	42.81	42.03	41.01	39.71	38.11	36.21	34.05	31.78	29.68	28.04	26.97	26.37	26.04	25.88	25.80	25.76	25.75	25.74
30	45.85	45.81	45.76	45.70	45.62	45.52	45.41	45.27	45.11	44.91	44.67	44.36	44.00	43.53	42.95	42.20	41.24	40.00	38.48	36.70	34.74	32.74	30.98	29.69	28.88	28.42	28.19	28.07	28.01	27.98	27.96	27.96
31	45.83	45.80	45.75	45.69	45.62	45.53	45.42	45.30	45.14	44.95	44.72	44.44	44.09	43.66	43.11	42.40	41.49	40.32	38.90	37.26	35.50	33.79	32.37	31.36	30.76	30.42	30.25	30.16	30.11	30.10	30.09	30.08

Appendix C

Pseudocode

C.1 SPI Interfacing Examples

```
uint8_t write_active_channel(uint8_t adc_id){
        uint16_t rx_data, tx_data;
        if (adc_id <= 28) {
                // write mode
                tx_data = 0b1 << 8;
                // function: active channel
                tx_data += 0b000 << 5;
                // input data: ADC ID
                tx_data += adc_id;
                // shift everything left for alignment
                tx_data <<= 6;
                // send
                rx_data = SPI_transceive(tx_data);
                return OK;
        }
        return ERROR;
```

```
}

uint16_t read_active_channel(){
        uint16_t rx_data, tx_data;
        // read mode
        tx_data = 0b0 << 8;
        // function: active channel
        tx_data += 0b000 << 5;
        // shift everything left for alignment
        tx_data <<= 6;
        // send
        rx_data = SPI_transceive(tx_data);

        return rx_data;
}
```

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