TOWARDS HIGH EFFICIENCY INVERSION LAYER CELLS BASED ON ION-CHARGED DIELECTRICS

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ABSTRACT: This work investigates the production and performance of p-type Inversion Layer (IL) Si solar cells, manufactured with an ion-injection technique that produces a highly charged dielectric nanolayer. Ions are applied to the front dielectric layer and then driven towards the c-Si/SiO_2 interface by an electric field before stabilisation with an anneal. As this process can be performed in minutes at temperatures below 500 °C, it potentially provides a fast, yet controllable way for IL cell manufacturing. We demonstrate by simulations using Sentaurus TCAD that for the 1 Ω·cm p-type Si/thermal oxide model defined in this work, the sheet resistance of the field-induced electron layer can reach 1.1 kΩ/sq in the dark by reducing band-tail interface state density to below 10^{14} $eV^{-1}cm^{-2}$ and increasing the dielectric charge density to above 2×10^{13} cm^{-2}. Additionally, we present a proof-of-concept p-type IL cell on a non-gettered, non-hydrogenated substrate with an efficiency of 10.8%, and an open-circuit voltage (V_{OC}) equivalent to that in a cell with a diffused phosphorous emitter. Lastly, we perform Sentaurus TCAD simulations to assess the efficiency potential of such IL cells. By incorporating optimal passivation, gettering, hydrogenation and metallisation, IL cells are predicted to reach an efficiency of 24.5% on 5 Ω·cm, and beyond 24.8% on 10 Ω·cm p-type substrates, provided the dielectric charge density reaches 2×10^{13} cm^{-2}, which has been experimentally demonstrated to be possible. IL cells are therefore, in principle, a potential competitive candidate in the photovoltaic industry.

Keywords: Inversion-layer, Dielectric Charge, Laser Processing, Interfaces, Silicon Solar Cell

1 INTRODUCTION

In p-type IL (inversion layer) cells, the pn junction is formed by introducing positive charges into a front dielectric layer, such that an n-type inversion layer is formed in the underlying p-type base. IL cells have been studied in detail two decades ago, yet they did not progress to successful commercialisation. In such IL cells intrinsic charge in the dielectric layer was used to induce the emitter [1]–[5]. Their development was limited by the high emitter resistivity due to the low intrinsic dielectric charge. The ion-injection technique in this work allows embedding of ionic charge into the dielectric, thus has the potential of reaching charge densities beyond the highest (>10^{13} cm^{-2}) obtained before [6]. Compared with a P-diffused emitter, the induced emitter would inherently lead to less Auger, or dopant-mediated recombination. The conditions required for the technique includes an application of ion precursor, a strong electric field across the dielectric, and a temperature below 500 °C. Considering the low cost and the high compatibility of the process to the mainstream technology, the induced emitter can be a viable replacement for the P-diffused emitter.

In a p-type IL cell, the p-n junction is formed by introducing positive charges into a front dielectric layer such that an n-type inversion layer is formed in the underlying p-type base. Previously, fixed charge in titanium oxide, silicon oxide, tantalum oxide, and aluminium oxide thin-films have been used to induce inversion layers in silicon [1], [2], [7]. Silicon nitride was first used in IL cells in the 1980s and has since been widely studied due to its high charge density and good charge stability [4]. Introducing cesium before nitride deposition was found to boost the charge density up to nearly 10^{13} cm^{-2} [8]. However, this concentration was not high enough to induce a sufficiently conductive emitter to compete with P-diffused emitters at the time. Therefore, it is necessary to produce high enough charge densities in the dielectric layer to reduce lateral resistive losses. In this study, we use a technique that embeds ionic charge into the dielectric layer, with the potential of reaching a charge density beyond 10^{13} cm^{-2} [9]. We aim to develop an IL cell with a charge-induced emitter that is comparable to, or beyond, a P-diffused emitter in performance while maintaining simpler and lower temperature (hence lower-cost) manufacturing processes.

This paper is composed of two main results sections. In section 2, various aspects of the inversion layer induced by ion injection are discussed. Modelling is employed to investigate the impact of surface charge on the characteristics of the emitter. Such structures are then demonstrated experimentally. In section 3, a proof-of-concept inversion layer solar cell is fabricated. Further modelling indicates the efficiency potential of this cell design.

2 FIELD-INDUCED INVERSION LAYER

2.1 Ion migration method

The ion migration technique involves delivery of ion precursors, application of a corona discharge to generate an electric field across the dielectric, and an anneal to migrate the ions into the dielectric and reach the semiconductor-dielectric interface. Fig. 1 shows the processing method and a schematic of the wafer with a field-induced electron layer. Our previous work [10] has

demonstrated that the ion-injection technique can produce a field-induced electron accumulation layer with a dark sheet resistance of as low as 0.95 kΩ/sq on 1 Ω·cm n-type silicon substrates, which is the lowest reported in the literature.

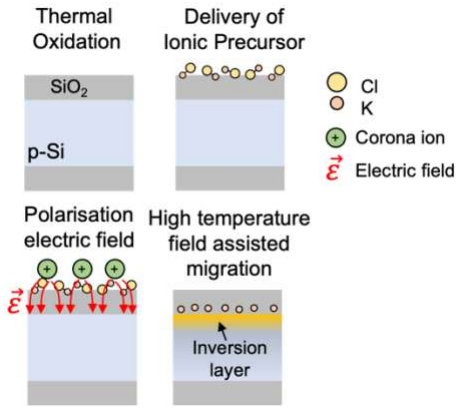

Figure 1: Processing of migration of ions into surface dielectrics: ion precursor delivery, applying electric field, and anneal.

2.2 Simulating conductivity of inversion layers

A model was developed in Sentaurus TCAD to simulate the interface carrier conditions of field induced layers. The model comprises a 200 µm thick, 1 Ω·cm p-type Si substrate, with an oxide passivating layer on both sides. Dielectric fixed charge was defined at the front Si/SiO_2 interface. The interface was defined following the common parametrisation as reported in [11], with interface state densities at midgap and band tails as primary parameters. The Lombardi model [12], [13] was used to model the mobility throughout the sample bulk and in the space charge layer. A modified local-density approximation (MLDA) quantum-mechanical model was used to account for the confined carrier distributions occurring near semiconductor–insulator interfaces [14]. It has been demonstrated that in the case of strong band bending, the band-tail interface states are able to store charged carriers and can therefore compensate the dielectric charge, leading to a reduced net charge density to induce the inversion layer [10], [15], [16]. In the model, the band-tail interface state density is described by Eq. 1 and Eq. 2:

$$D_{it}(acc) = D_{it}\text{CB} \times e^{-\frac{(E_g - E)}{E_{0,CB}}} \quad (1)$$

$$D_{it}(don) = D_{it}\text{VB} \times e^{-\frac{E}{E_{0,VB}}} \quad (2)$$

where D_{it} (acc) and D_{it} (don) represent the acceptor/donor band-tail interface state density. D_{it}-CB and D_{it}-VB are the maximum interface state density at conduction/valence band edge. E_g is the band gap of crystalline Si (1.12 eV). E is the energy from valence band edge in eV. $E_{0,CB}$ and $E_{0,VB}$ represent the slope of the tail at the conduction band and valence band, respectively. Here $E_{0,CB}$ and $E_{0,VB}$ were set to 0.028 eV and 0.024 eV, respectively, to reflect average values extracted from previous works [17]–[19]. In this model, D_{it}-midgap was set to 5×10^{10} $eV^{-1}cm^{-2}$. D_{it}-CB and D_{it}-VB were set to 10^{14} and 5×10^{13} $eV^{-1}cm^{-2}$, respectively [16]. Fig. 2 shows the schematic of the model and the band diagram of the model near the interface. To calculate the inversion layer sheet resistance from the model, the equilibrium state was simulated, and the carrier density and mobility in bulk silicon were extracted as a function of the distance from the Si/SiO_2 interface. The thickness of an inversion layer is defined by where the hole density exceeds that of electrons. The sheet resistance can then be calculated using the following equation:

$$R_{sh} = \frac{1}{\int_0^{thickness} (nq\mu_n + pq\mu_p)\, dt} \quad (3)$$

where n and p are electron/hole density, μ_n and μ_p are electron/hole mobility, and q is the elementary charge.

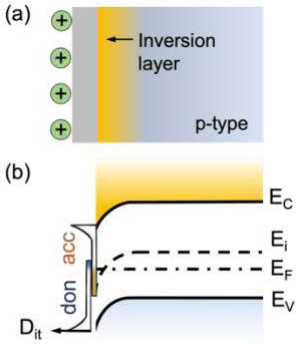

Figure 2: (a) Schematic of the model developed in Sentaurus TCAD. (b) Band diagram of p-type Si substrate near Si/SiO_2 interface in the presence of positive surface charge.

Fig. 3 shows the simulated inversion layer sheet resistance and its reciprocal, inversion layer sheet conductance, as a function of positive surface charge density. It is shown that the inversion layer sheet resistance decreases with increased charge density. The conductivity plateauing at high charge densities indicates that extra charge introduced in this range does not lead to an as significant increase in conductivity. Since conductivity is dependent on both the carrier mobility and the carrier density (as shown in Eq. 3), the plateauing effect can be attributed to two factors. The first is that the quasi-Fermi level of the trapped charges in the band-tail states will reach the band-tail near the conduction band edge at high enough charge densities. This will allow field-induced electrons to occupy band-tail interface states rather than remaining in the bulk and contribute to conductivity in the inversion layer, thus resulting in a smaller slope in the conductivity curve in the high charge density range. The other factor is the increased surface scattering, and therefore reduced carrier mobility, with increased dielectric charge density. The profiles of electron density, mobility, and the product of electron density and mobility near the interface with varied dielectric charge densities are plotted in Fig. 4. Fig. 4a shows that the electron density profile increases with charge density. Fig. 4b shows the reduced electron mobility near the interface with increased charge density. As a result, Fig. 4c shows the product of electron density and mobility. This demonstrated that the increase in conductivity induced by extra charge reduces with charge density. The simulation results demonstrate that the conductivity in the inversion layer is limited by the high density of interface states at the band-tail and the reduced carrier mobility due to increased surface scattering. It is noted that the lowest sheet resistance of the field-induced electron layer obtained (0.95 kΩ/sq) from our previous work [10] is close to the inversion layer sheet resistance expected at a charge density of $2-4 \times 10^{13}$ cm-

[2]. This suggests that the charge density obtained with the ion migration method is sufficiently high for the sheet resistance to plateau.

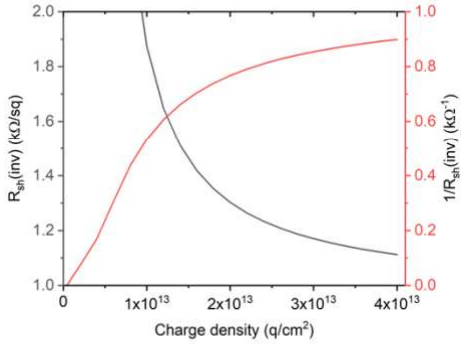

Figure 3: Simulated inversion layer sheet resistance (left axis) and conductivity (right axis) on a 1 Ω·cm p-type Si base as a function of positive interface charge density.

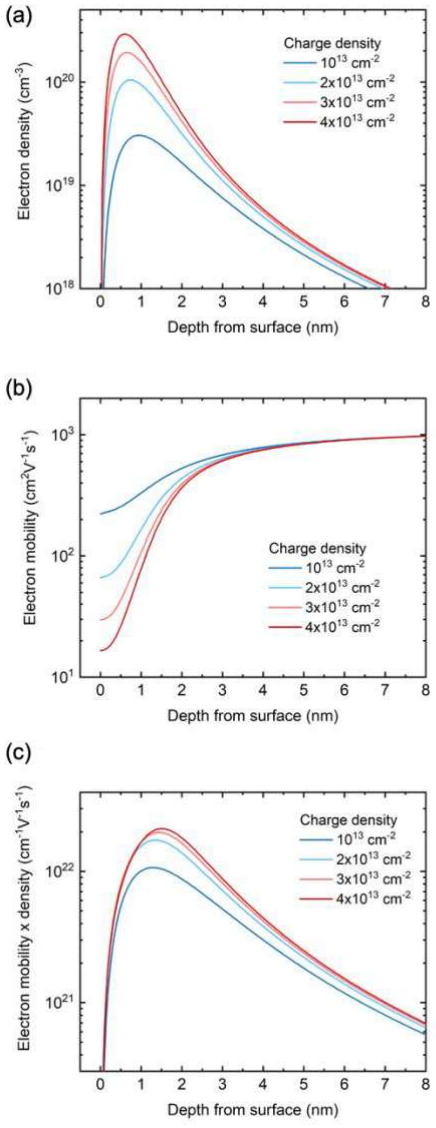

Figure 4: (a) Electron density, (b) electron mobility, and (c) electron density × mobility profiles near the interface on a 1 Ω·cm p-type base in the presence of varied positive interface charge density.

Since the surface scattering and therefore the reduced carrier mobility cannot be avoided, the impact of band-tail interface state density on the conductivity is explored. Fig. 5a shows the inversion layer conductivity as a function of charge density with varied D_{it}-CB. A significant increase in conductivity can be observed by reducing the D_{it}-CB from 10^{15} to 10^{14} eV^{-1}cm^{-2}, and further to 10^{13} eV^{-1}cm^{-2}, such that less interface states are available to accommodate the field-induced electrons. Fig. 5b demonstrates that passivating the band-tail interface states is an effective way to improve the inversion layer conductivity, yet it plateaus upon reducing the D_{it}-CB further. Since the band-tail interface states originate from termination of the periodicity of the bulk silicon, and that the energy slope has been demonstrated to be a function of overall bulk defect density [20], the band-tail interface states reflect the level of disorder. A characterisation technique has been developed in our previous work to detect D_{it}-CB [15], [16], which can be used to explore methods to passivate D_{it}-CB.

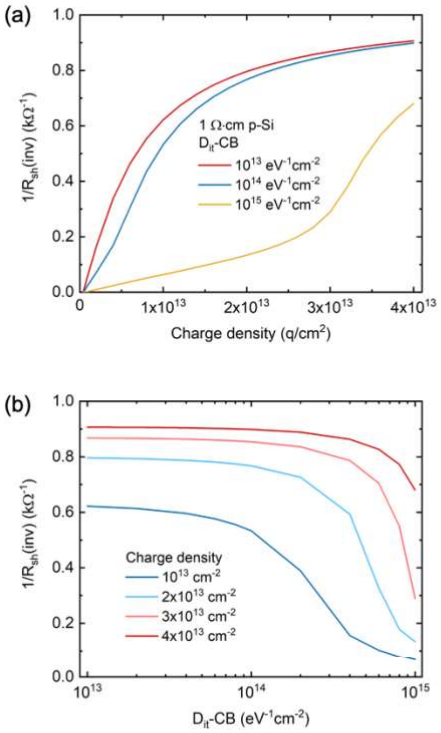

Figure 5: (a) Calculated inversion layer conductivity on a p-type base as a function of positive interface charge density with varied D_{it}-CB. (b) Calculated inversion layer conductivity on a p-type base as a function of D_{it}-CB with varied positive interface charge density.

Fig. 6 shows the simulated carrier density profile near the interface of both a field-induced inversion layer with a charge density of 2 × 10^{13} cm^{-2}, and a phosphorus diffused emitter in the dark and under illumination. The generation profile was obtained from ray tracing using Sunrays [21] and altered to mimic a pyramid surface with 0.1 µm height. A positive charge density of 10^{12} cm^{-2} is defined at the semiconductor-dielectric interface for the P-diffused emitter, which is the typical charge density of a SiN_x passivating layer [22]. D_{it}-midgap was set to 5 × 10^{10} eV^{-1}cm^{-2}. D_{it}-CB and D_{it}-VB were set to 10^{14} and 5 × 10^{13} eV^{-1}cm^{-2}, respectively [16]. The conductivity of the emitter is calculated by integrating the product of carrier density and

mobility over the thickness of the pn junction. The depth of the pn junction is defined by where the hole density exceeds that of electrons. In the dark, the electron density in the inversion layer drops rapidly with the distance from the interface, whereas the phosphorus diffused emitter depends on the doping profile, which leads to a much deeper junction. Under illumination, both the majority and the minority carrier density will be increased by the light injection, increasing the local conductivity. As shown in Fig. 6, the pn junction depth will also be altered by light injection. The junction shifted from ~375 to 340 nm for the diffused emitter (reduction by 10%), and from ~100 to 60 nm for the field-induced emitter (reduction by 40%). As a result, the sheet resistance of the diffused emitter dropped from 196.6 to 195.1 Ω/sq upon illumination, corresponding to a 0.8% increase in conductivity. For the field-induced emitter, the sheet resistance dropped from 1.30 to 1.21 kΩ/sq, corresponding to a 7.4% increase in conductivity. This will lead to reduced resistive losses under operating conditions with illumination. Compared with the standard diffused emitter, the field-induced emitter appears to be thinner, more resistive with the sheet resistance more sensitive to light injection. For the induced emitter, the region with high carrier concentration that leads to strong Auger recombination is thinner, which leads to an overall reduced Auger recombination compared with the deep diffused emitter. As shown in Fig. 5, the sheet resistance can be reduced by increasing the charge density and further passivating the band-tail interface states. In the cell design, a smaller metal contact pitch can be used to compensate the resistive losses in the emitter. The efficiency potential of the inversion layer cell will be discussed in Section 3.

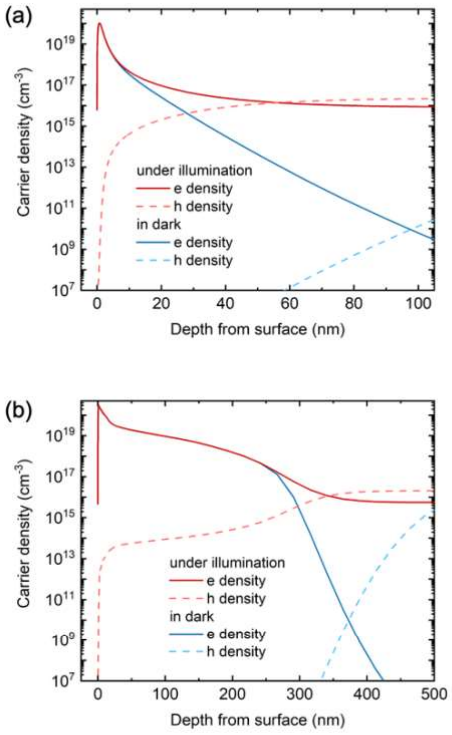

Figure 6: Simulated carrier density profiles of (a) a field-induced inversion layer with a positive charge density of 2×10^{13} cm^{-2}, and (b) a P-diffused emitter near the interface in dark and under illumination.

2.3 Field-induced electron accumulation layer

The Van der Pauw method is used to measure the sheet resistance of the induced electron layer [23], [24]. Fig. 7a shows the sample structure designed for the measurement. Direct electrical contact to the induced layer is required to measure the sheet resistance. For an inversion layer, as illustrated in Fig. 7b, the electrical contact to the inversion layer requires local doping underneath the meta contact. Due to the experimental difficulty in measuring the sheet resistance of an inversion layer, an electron accumulation layer was induced on an n-type Si substrate using the ion migration method. A 200 µm thick, 1 Ω·cm n-type Si substrate with 100 nm of thermal oxide on both sides was used for the experiment. Our previous work has shown an accumulation layer sheet resistance of as low as 950 Ω/sq on the n-type Si substrate but with enhanced chemical passivation by a forming gas anneal in 5 % hydrogen ambient at 425 °C for 30 min [10]. In this work, the ionic charge was introduced by spin coating of 0.05 M KCl solution (DI water:IPA 30:70) followed by a drive-in process consisting of 8 cycles of corona (30 kV, 30 s) – anneal (430 °C, 10 s). The KCl spin coating plus drive-in was repeated 4 times. Fig. 8 shows the average accumulation layer sheet resistance measured from four identical samples after drive-in of K^+ ions by each spin coating/drive-in step. The samples were then stored at room temperature in dark until the sheet resistance stabilised. In equilibrium, the sheet resistance is determined by the charge density and the D_{it} profile. However, the recorded sheet resistance shows a decay within the 25 days after processing. The hypothesis is that the high voltage and anneal involved in the ion migration process drives electrons in bulk Si into the interface states, or states in the dielectric material, compensating the net ionic charge. The gradual decay of such electrons leads to an increase in net dielectric charge and therefore a reduction in sheet resistance. The stability of the sheet resistance was then tested against elevated temperature and UV irradiation separately for a period of 2 months. During the period, no increase is observed for the samples kept at 120 °C nor the ones kept under UV irradiation, demonstrating a promising stability of conductivity in the field-induced electron layer.

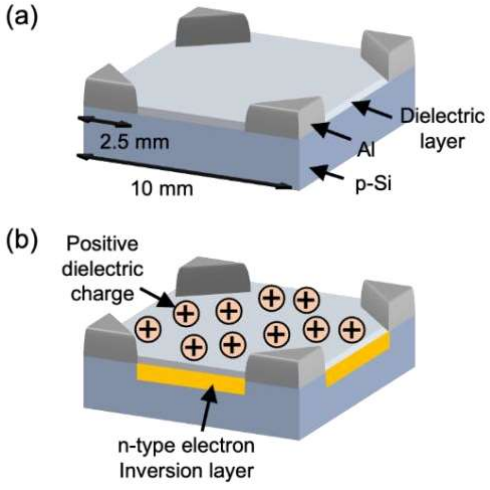

Figure 7: (a) Structure of sample designed for Van der Pauw measurement. (b) Schematic of electron inversion layer on a Van der Pauw sample structure with p-type Si substrate.

The impact of the K^+ ions on surface passivation is explored by characterising D_{it}-midgap prior to and after the ion migration. D_{it}-midgap was obtained by an analytical fitting of effective lifetime of the sample as a function of surface potential. A detailed description of this method can be found in [25]. Fig. 9a shows the schematic diagram of the experimental setup. A transparent PEDOT:PSS gate electrode was applied on both surfaces to monitor the surface potential, while effective lifetime of the sample was recorded as a function of surface potential using the lifetime tester. Fig. 9b shows the experimental data and the analytical fitting of one fresh sample and one with K^+ ions introduced on both sides by one spin coating and the subsequent driven-in. The interface parameters used in the fitting are listed in Table I. The shift in gate bias in Fig. 9b corresponds to an increase in charge density by 9.6×10^{12} cm^{-2}. Upon drive-in of the K^+ ions introduced by one spin coating, D_{it}-midgap increased from 2.8×10^{10} to 3.6×10^{11} $eV^{-1}cm^{-2}$, demonstrating the damage of the K^+ ions to the surface passivation. One hypothesis is that the accumulation of K^+ ions at the interface causes a strain that generates more defects and therefore leads to an increase in D_{it}-midgap. The Si substrates used in this experiment are passivated solely by thermal oxide without any hydrogenation steps. A natural subsequent experiment is the addition of hydrogenation introduced by depositing a SiN_x or AlO_x layer and conducting an activation anneal for improved surface passivation. Such methods will be explored in future work.

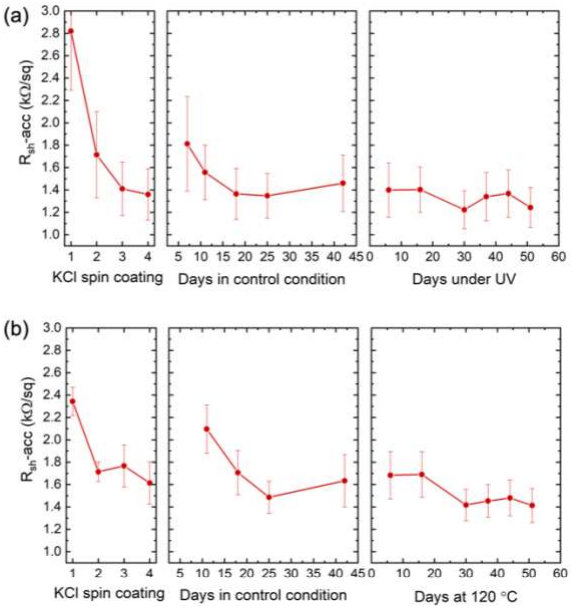

Figure 9: Calculated accumulation layer sheet resistance on the n-type samples upon introduction of ionic charge by spin coating of KCl solution by 4 times and kept (a) under UV irradiation, (b) at 120 °C for 2 months.

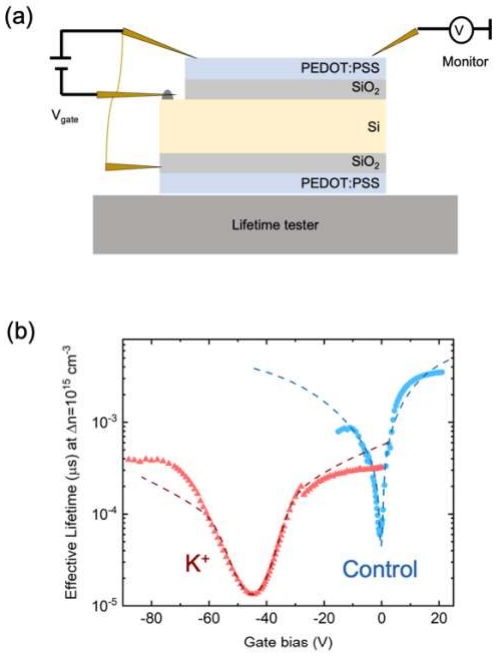

Figure 8: (a) Schematic diagram of experimental setup to obtain effective lifetime of a sample as a function of surface potential. (b) Experimental data (dotted line) and its analytical fitting (dashed line) of effective lifetime of one fresh sample and one sample with K^+ ions introduced by one spin coating and the subsequent drive-in.

Table I: Interface parameters used in the analytical model to fit the experimental lifetime data as a function of surface potential of one fresh sample and one sample with K^+ ions applied by one spin coating driven in.

	Control	**K^+ ions introduced**
D_{it}-midgap ($eV^{-1}cm^{-2}$)	2.8×10^{10}	3.6×10^{11}
D_{it}-CB ($eV^{-1}cm^{-2}$)	9×10^{13}	7.5×10^{14}
D_{it}-VB ($eV^{-1}cm^{-2}$)	5×10^{13}	3.5×10^{14}
Q_f (cm^{-2})	10^{11}	9.7×10^{12}

3 P-TYPE INVERSION LAYER CELLS

3.1 Proof-of-concept inversion layer cell

In IL cells the inversion layer is interrupted at regions beneath the metal contacts, hence local doping is necessary to ensure the continuity of the n-type layer. Laser doping is a fast and cost-effective way to achieve this. Fig. 10a shows a schematic of a prototype IL cell. The prototype cells start with 180 μm thick, 1 Ω·cm, p-type Cz Si wafers. These wafers were pyramid textured at the front surface and had 20 nm thermal oxide on both sides. The effective lifetime of this sample structure is ~50 μs since they were made in solar grade silicon without gettering. Rear openings were produced using a laser scriber prior to rear screen-printing of aluminium paste. The wafers were then fired at ~750 °C for 3 s in a belt furnace. A localised emitter was fabricated across the front surface by laser

doping. An 85% H_3PO_4 solution was spin coated onto the sample surface at 12,000 rpm for 50 s as a phosphorus source. A 355 nm nanosecond pulsed laser was scanned across the sample surface according to the pattern shown in Fig. 10b to both ablate the oxide and melt the silicon beneath to allow in-diffusion of phosphorus atoms to dope the molten region. The fingers were 10 mm long and were spaced apart by 1 mm. Two busbars of 0.5 mm wide with a line spacing of 30 µm were designed at the two ends of the fingers. The samples were then rinsed in DI water to remove the phosphorous residues. An anneal at 560 °C for 1 hour was found necessary to allow regeneration of the laser-doped and damaged region as shown in Fig. 10a, so that optimal availability of K^+ ions is ensured. An inversion layer emitter was induced by spin coating of a KCl solution 4 times each followed by 8 Corona anneal cycles as described in Section 2. Before metallisation, the oxide in the laser doped grooves formed during laser doping and anneal was etched off by 1% HF solution. Fig. 10c shows a schematic of the process of light-assisted nickel electroplating. A voltage of 1.1 V was applied between a Ni wire and the rear metallisation of the sample for 4 min while the front is illuminated by a white LED lamp. A ready-for-use commercial nickel sulfamate solution (NB Semiplate Ni 100) was used as the electrolyte. Since prior to front metallisation, the inversion layer emitter has been formed with its electrical connection to the local doped region ensured, upon illumination, the photocurrent contributes to the electroplating current, accelerating the process. A 10 × 10 mm^2 proof-of-concept IL cell is fabricated in this manner including Ni electroplated metallisation.

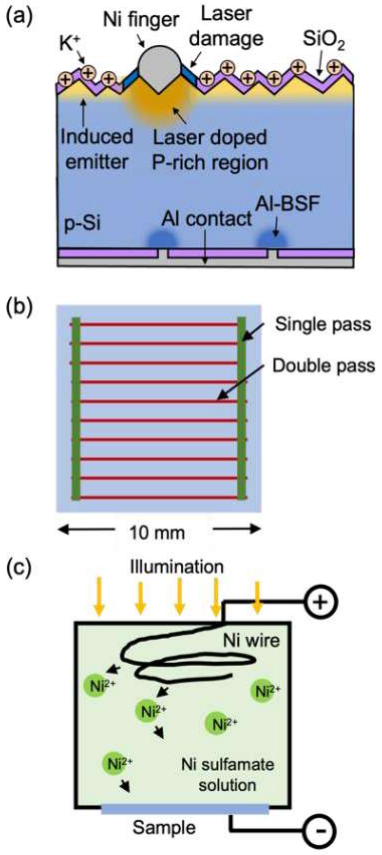

Figure 10: Schematic of a p-type cell precursor in (a) cross section and (b) plan view from top surface. (c) Process of light-assisted Ni electroplating.

The formation of the inversion layer emitter was monitored by Suns-V_{OC} and is shown in Fig. 11a. After the drive-in of K^+ ions introduced by the first spin coating, the V_{OC} increased by about 35 mV to 590 mV. No evident increase of V_{OC} was observed while further K^+ ions were embedded after the 2nd, 3rd and the 4th KCl spin coating, with the highest V_{OC} reaching 600 mV. Fig. 11b shows an LBIC image of 500 × 500 μm^2 area of the IL cell with the pixel size being 2 × 2 μm^2, as described in [26]. The contrast in the image indicates the photocurrent collected by the cell while a red laser is scanned across the sample surface. The blue low-photocurrent region (3-5 µA) in the middle represents a Ni finger. The region adjacent to the Ni finger with a photocurrent of 11-13 µA is affected by the recombination sites introduced by the laser-induced damage. The large area with high photocurrent (13-14 µA), together with the increase in V_{OC} upon introducing K+ ions, indicates the presence of a uniform inversion layer emitter and the continuity of the n-type layer beneath the dielectric film. Fig. 11c shows the IV curve of a device with both the busbars and the fingers doped by single laser pass. The IV curve gives a V_{OC} of 559 mV, a J_{SC} of 33.9 mA/cm^2, and an efficiency of 10.8%. These experiments demonstrate the potential of fabricating IL cell using the ion migration method. This cell represents a proof-of-concept for the ion injection inversion layer solar cell. However, there were several aspects of the cell design, shown schematically in Fig. 10a, which limited the performance. Better performance is expected if the following issues are addressed: (i) Start with Si substrates with lifetime in ms level (rather than 50 µs as in the proof-of-concept cell) and high resistivity (5/10 Ω·cm); (ii) Add SiN_x coating for hydrogenation and anti-reflection; and (iii) Anneal Ni-Si contact to form NiSi alloy for reduced contact resistance. Although an efficiency of only 10.8% is obtained by the proof-of-concept IL cell, the potential of IL cells is evaluated by simulations in Section 3.2.

The stability of V_{OC} of the precursor cells was monitored against elevated temperature and UV irradiation. Performance of the cells were monitored by taking Suns-V_{OC} measurements throughout the 2-month period. Fig. 12 shows the recorded V_{OC} of the cells during drive-in of the K^+ ions and its stability against elevated temperature, UV radiation, and a control sample set kept in dark at room temperature for comparison. In all 3 groups of samples, during the ion migration process, a tendency that V_{OC} decreases with the number of ions embedded is observed. This agrees with the finding observed in Section 2.3 that the interface is damaged during the ion injection process. There is hence a trade-off between improved emitter conductivity and limiting the damage to the interface. Methods to introduce atomic hydrogen are to be tested for improved interface passivation. One point to note is that the V_{OC} values measured after K^+ drive-in is 50-60 mV lower than that measured in Fig. 11a. This can be explained by the increased laser damage caused by the non-optimised laser parameters. Upon keeping the samples at 120 °C, under UV irradiation, and at the control condition, a reduction in V_{OC} ranging from 3 to 8 mV is observed for all 3 groups within 7 days. The variations afterwards are not significant enough to show any further degradation. Since similar trends are observed in all of the three figures in Fig. 12, the conclusion is that the degradation in V_{OC} caused, or accelerated at elevated temperature and under UV irradiation is minor in the 2-month period.

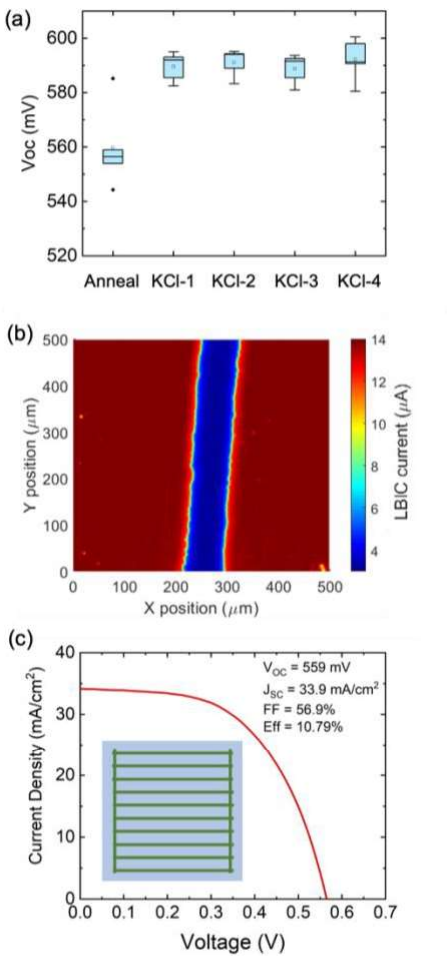

Figure 11: (a) Recorded V_{OC} of IL cell precursors after anneal and introducing ionic charge. (b) LBIC photocurrent map of an IL cell. (c) IV curve of an IL cell with a single laser-doped line as busbar and a single laser pass for laser doping.

3.2 Simulating the maximum potential of inversion layer cells

Next, we turn our attention to the efficiency potential of the proposed inversion layer cell design. A model was developed in Sentaurus TCAD to simulate the performance of p-type IL cells. The model comprises a 170 µm, boron-doped silicon substrate, with both surfaces passivated by dielectric layer. Base resistivity of 1, 5, and 10 Ω·cm was simulated to reflect the influence of doping density. The bulk lifetime was set to $\tau_p=10\cdot\tau_n=3.7$ ms for 1 Ω·cm, as may be reached in Ga-doped wafers if Fe concentration is sufficiently small, and $\tau_p=10\cdot\tau_n=15$ ms for 5 Ω·cm, $\tau_p=131$ms, $\tau_n=1.14$ ms for 10 Ω·cm wafers as referred from [27]–[29]. Dielectric charges were defined at the silicon-dielectric interface, with the positive charge at the front dielectric to induce the inversion layer, and the negative charge at the rear dielectric to limit the access of electrons to the rear surface for reduced carrier recombination. The front finger width was set to 25 µm since recent progress in metallisation technologies shows that such thin metal fingers are possible using screen printing, or a combination of laser doping and electroplating [30], [31]. Due to the absence of charge-induced inversion layer beneath the front metal contact, n-type local doping is required for the inversion layer to connect to the fingers via an n-type local contact. A phosphorous doping profile measured from an industrial phosphorus diffused emitter was defined beneath the contact. Similarly, an aluminium profile was defined beneath the rear contact to resemble Al-BSF for reduced contact resistivity. While a flat surface is defined in the model, the generation profile was obtained from ray tracing using Sunrays [21] and altered to mimic a pyramid surface with 0.1 µm height. Despite the potential of developing a bifacial cell, in this work, only light injection from the front surface is considered. A summary of parameters used to describe the model is listed in Table II.

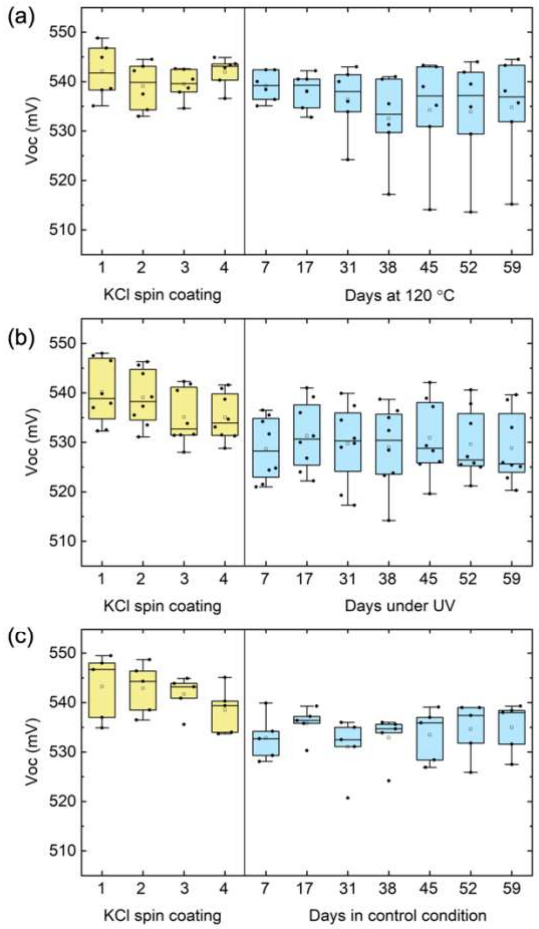

Figure 12: Recorded V_{OC} of IL cell precursors kept (a) under UV irradiation, (b) at 120 °C, and (c) at room temperature in dark for 2 months.

Fig. 13 shows the simulated IL cell efficiency with wafer resistivity being 1/5/10 Ω·cm at various charge densities and finger spacings. At the interface, D_{it}-midgap was set to 5×10^{10} $eV^{-1}cm^{-2}$. D_{it}-CB and D_{it}-VB were set to 10^{14} and 5×10^{13} $eV^{-1}cm^{-2}$, respectively. A negative charge density of 5×10^{12} cm^{-2} was defined at the rear interface, which is typical for a SiO_2/AlO_x passivating stack [32]. It is noted that higher efficiency is expected for substrates with higher resistivity. This is due to the higher bulk lifetime estimated for more resistive bulk. Another point to note is that the increase in efficiency with higher charge density is not evident, especially for 5/10 Ω·cm substrates. This can be explained by noting that with D_{it}-CB of 10^{14} $eV^{-1}cm^{-2}$ defined, the increase in emitter conductivity with charge density is not as effective for charge densities beyond 2×10^{13} cm^{-2}, which agrees with the conclusion drawn from Fig. 5a. Considering that the

accumulation of K^+ ions at the interface damages the passivation as demonstrated in Fig. 9, it might be beneficial to maintain a relatively low charge density. Further studies on the interface and simulations are required to determine the optimum charge density. The peak in the efficiency vs. finger spacing curve occurs when the performance-gain due to reduced shading losses is outweighed by the increased resistive losses at large finger spacings. The efficiency peak shifting from < 0.8 mm for the 1 Ω·cm base to about 1.4-1.6 mm for the 5/10 Ω·cm base indicates a more conductive emitter, and therefore less resistive losses. This is because for a high resistivity substrate, the initial hole density is lower for the field-induced electrons to compensate and eventually turned into n-type. Low emitter conductivity has been considered as one of the major concerns for IL cells. For the 5/10 Ω·cm base, with the efficiency peak expected to appear beyond 1.4 mm in finger pitch on a well passivated cell, and that 0.7-1.6 mm [33] was used in industry for the mainstream PERC, emitter resistivity is no longer limiting the efficiency potential for IL cells. These simulation results suggest: 1) the necessity of moving to high resistivity substrates; 2) with well passivated surfaces, increasing the charge density to beyond 2×10^{13} cm^{-2} is less effective in improving the cell performance; and 3) and internal efficiency of 24.8% can be obtained with optimised processing.

Table II: Summary of cell parameters used for simulation of full inversion layer cells in Sentaurus TCAD.

Parameter	Value
Cell thickness	170 µm
Bulk base resistivity	1/5/10 Ω·cm
SRH bulk lifetime	1 Ω·cm: $\tau_n = 0.371$ ms, $\tau_p = 3.71$ ms 5 Ω·cm: $\tau_n = 1.5$ ms, $\tau_p = 15$ ms 10 Ω·cm: $\tau_n = 1.14$ ms, $\tau_p = 131$ ms
Front finger width	25 µm
Rear finger width	67 µm
Finger spacing	0.8-1.8 mm
SRV at front contacts	$S_n = 10^7$ cm/s, $S_p = 10^7$ cm/s
SRV at rear contacts	$S_n = 4 \times 10^4$ cm/s, $S_p = 10^7$ cm/s
Front contact resistivity	2 mΩ·cm^2
Rear contact resistivity	5 mΩ·cm^2
D_{it}-midgap	5×10^{10}-10^{11} $eV^{-1}cm^{-2}$
D_{it}-tail	CB: 10^{13}-10^{15} $eV^{-1}cm^{-2}$ VB: 10^{13}-5×10^{14} $eV^{-1}cm^{-2}$

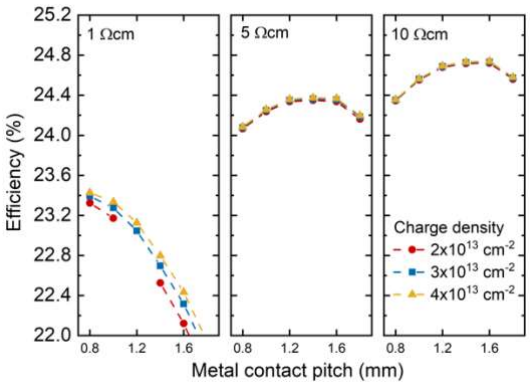

Figure 13: Simulated IL cell efficiency with wafer resistivity being 1/5/10 Ω·cm at various charge densities and finger spacings. D_{it}-midgap, D_{it}-CB, and D_{it}-VB were set to 5×10^{10}, 10^{14}, and 5×10^{13} $eV^{-1}cm^{-2}$, respectively.

D_{it}-CB was varied and efficiency plotted in Fig. 14. As concluded from Fig. 5b that the emitter conductivity reaches its maximum from D_{it}-CB of 10^{14} $eV^{-1}cm^{-2}$ and does not increase further at lower D_{it}-CB. In Fig. 14, an evident increase in efficiency is observed by reducing D_{it}-CB from 10^{15} to 10^{14} $eV^{-1}cm^{-2}$, while the improvement is minor by further reducing the D_{it}-CB to 10^{13}. One other point to note is that by reducing D_{it}-CB from 10^{15} to $10^{14}/10^{13}$ $eV^{-1}cm^{-2}$, the efficiency peak shifts from 1.2 mm to 1.4-1.6 mm in finger pitch, indicating an increase in emitter conductivity, which agrees with the conclusion drawn from Fig. 5b.

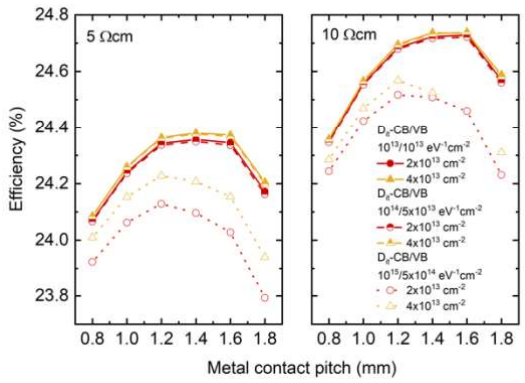

Figure 14: Simulated IL cell efficiency with wafer resistivity being 5/10 Ω·cm at various charge densities, finger spacings, and D_{it}-CB/VB.

In the model, negative charge is defined at the rear interface for field-effect passivation. A typical value of 5×10^{12} cm^{-2} was used in previous simulations. However, charge densities of above 10^{13} cm^{-2} have been demonstrated at a c-Si/AlO_x interface [34] and a c-Si/SiO_2/AlO_x stack [35]. In Fig. 15, simulations with rear negative charge densities as high as the front positive charge densities were plotted for comparison. No significant improvement in efficiency is observed by increasing the rear negative charge density from 5×10^{12} to 2×10^{13} cm^{-2} for a front positive charge density of 2×10^{13} cm^{-2}. This is due to the already well passivated surfaces and that the recombination at the rear surface is not the limiting factor. For the front positive charge density of 4×10^{13} cm^{-2}, more prominent improvement is

observed upon increasing the rear negative charge density. This is due to the recombination at the front surface being further reduced, so that stronger field-effect passivation at the rear leads to an increase in efficiency. Since the resistive losses in the emitter and therefore the optimum finger spacing is determined by finger width, the advancement in metallisation technology needs to be considered. The finger width by screen printing in industry is expected to be narrowed down to 18 µm by 2032 [36]. Cu plating allows narrower fingers down to 12 um has been demonstrated [37]. For the last group of data with hollow symbols and dashed lines in Fig. 15, the finger spacing was set to 15 µm, which allows reduced shading losses and therefore more room for the finger spacing to be reduced for lower resistive losses. This leads to a shift in peak efficiency from 1.6 to 1.2 mm finger pitch, and an increase in efficiency to beyond 24.8%.

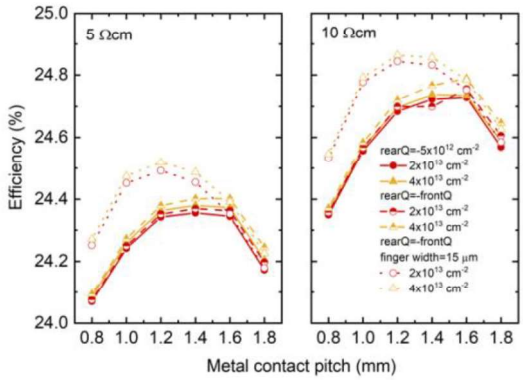

Figure 15: Simulated IL cell efficiency with wafer resistivity being 5/10 Ω·cm at various charge densities, finger spacings, and negative rear charge densities for field-effect passivation. Band-tail interface states are assumed to be well passivated, with Dit-CB/VB both set to 10^{13} $eV^{-1}cm^{-2}$.

The D_{it}-midgap of 5×10^{10} $eV^{-1}cm^{-2}$ and Dit-CB/VB of $10^{14}/5 \times 10^{13}$ $eV^{-1}cm^{-2}$ used in the above simulations were measured from a float zone Si substrate with a planar {1 0 0} plane passivated by thermal oxide. Since pyramid-textured surfaces are mostly used in commercial solar cells and that the interface passivation will be compromised because of the {1 1 1} facets [38]. In Fig. 16, D_{it}-midgap, D_{it}-CB, and D_{it}-VB were increased to values of 10^{11}, 10^{15}, and 5×10^{14} $eV^{-1}cm^{-2}$, respectively. The simulations show significant increase in efficiency by increasing the front charge density from 2×10^{13} to 4×10^{13} cm^{-2}, and by increasing the rear charge density for stronger field-effect passivation. This again suggests the importance in passivating the interface and maintaining high charge densities at both the front and the rear for reduced surface recombination.

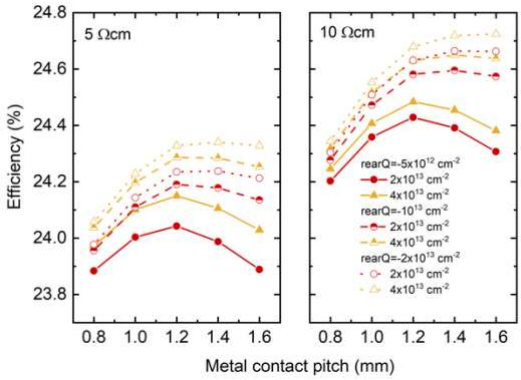

Figure 16: Simulated IL cell efficiency with wafer resistivity being 5/10 Ω·cm at various charge densities, finger spacings, and negative rear charge densities for field-effect passivation. D_{it}-midgap, D_{it}-CB, and D_{it}-VB were set to 10^{11}, 10^{15}, and 5×10^{14} $eV^{-1}cm^{-2}$, respectively.

4 CONCLUSIONS

In this work, the formation of field-induced electron surface layers and the potential of inversion layer cells is explored. For inversion layer cells, simulation results indicate that higher cell efficiencies are expected for substrates with higher resistivities due to improved bulk lifetime and lower doping density. This suggests the necessity of fabricating inversion layer cells on substrates with resistivity above 5 Ω·cm. Both high charge densities and well passivated surfaces are necessary to obtain high emitter conductivity and therefore cell efficiency, with the best efficiency reaching beyond 24.8%. However, further increasing the charge density to beyond 2×10^{13} cm^{-2} and reducing D_{it}-CB to below 10^{14} $eV^{-1}cm^{-2}$ are not as effective in improving the emitter conductivity. Beyond the charge density of 2×10^{13} cm^{-2}, the effect of increased electron density on emitter conductivity is balanced by the reduced carrier mobility due to increased surface scattering. For D_{it}-CB below 10^{14} $eV^{-1}cm^{-2}$, the released electrons from the interface states are too little compared with the electron density in the emitter to lead to an observable improvement. It is noted that the accumulation of K^+ ions at the interface damages the passivation. Further research on the damaged interface is required to determine its effect on the cell performance. The optimum finger spacing of 1.2-1.6 mm for 5/10 Ω·cm substrates is equivalent to that of the mainstream PERC. This suggests that although the field-induced emitter is more resistive, the optimised finger spacing does not lead to significantly higher shading losses than that of the cells with a P-diffused emitter. A 10.8% efficient proof-of-concept inversion layer cell is fabricated. It is observed that the sheet resistance of a field-induced electron layer and V_{OC} of a precursor cell with K^+ ions embedded in the same method show good stability against elevated temperature (120 °C) and UV irradiation within 2 months. Although the efficiency of the prototype cell is low, an internal efficiency of beyond 24.8% is expected by simulations with optimised processing.

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6 DATA AVAILABILITY

All data created during this research and published in this article is openly available from the Oxford University Research Archive and can be downloaded free of charge from http://ora.ox.ac.uk.

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