FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Fast Loop for a Capless LDO

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Resumo

A evolução de Circuitos Integrados e gestão de potência na indústria de semicondutores tem vindo a forçar circuitos eletrónicos a permitirem uma maior integração em soluções de sistemas em *chip*.

Reguladores de tensão convencionais de baixa queda possuem um condensador externo de dimensões elevadas para compensar a resposta em frequência e em variações transientes. De forma a ser integrado em aplicações de sistemas em *chip*, o condensador externo tem de ser removido.

A solução apresentada dispõe de um caminho rápido de regulação para compensação de respostas transientes do regulador de tensão de baixa queda sem condensador externo, para uma tecnologia de processo CMOS de 28nm. O regulador de tensão de baixa queda sem condensador externo com caminho rápido de regulação é alimentado com uma tensão nominal de 1.8V, sendo capaz de regular tensões de saída de 1.2V, 1.1V, 1V, 0.9V, 0.8V e 0.7V. A partir de uma arquitetura genérica, sem compensação, de um regulador de tensão de baixa queda sem condensador externo, um condensador interno de Miller com valor de 5pF é implementado no amplificador de erro com o objetivo de gerar compensação em frequência no sistema e garantir a estabilidade em corrente alternada do mesmo. Um esquema de compensação de um caminho rapido de regulação é estudado e implementado para a compensação de uma resposta transiente a uma variação máxima da corrente de carga de 1mA com uma capacidade de carga equivalente a 1pF.

Os resultados das simulações mostram que o regulador de tensão de baixa queda é competitivo entre as arquiteturas do estado da arte, passando algumas, registando um valor de variação transiente positiva e negativa na tensão de saída de 48mV e 49.8mV, respetivamente, com 0.5μs de tempo de recuperação.

simulações de casos extremos de *PVT (Process, Voltage, Temperature)* e análises de Monte Carlo feitas posteriormente, mostram que o sistema desenhado cumpre com a norma ISO 26262.

O desenho do *layout* do sistema proposto é apresentado para uma futura integração do mesmo.

Palavras-chave: CMOS, LDO, regulador de tensão, tensão de queda, caminho rápido de regulação, sem condensador externo, compensação transiente, compensação em frequência, regulação de carga.

Abstract

The evolution of Integrated Circuits (IC) and power management in the semiconductor's industry has pushing circuit designs to allow for more integration in system-on-chip (SoC) solutions.

Conventional LDO voltage regulator topologies have a large external capacitor to compensate frequency and transient response. In order to be integrated in SoC applications, the external capacitor has to be removed.

The presented solution provides a fast loop for transient compensation for a capacitor-less LDO voltage regulator, in a 28nm CMOS process technology. The proposed fast loop capacitor-less LDO voltage regulator is supplied with a nominal voltage of 1.8V with the ability to regulate an output voltage of 1.2V, 1.1V, 1V, 0.9V, 0.8V and 0.7V. From a generic, uncompensated, architecture of a LDO voltage regulator without a bulky external capacitor, a 5pF internal Miller capacitor is implemented in the Error Amplifier in order to provide frequency compensation to the system and guarantee the systems AC stability. A Fast loop compensation scheme is studied and implemented for transient compensation of 1mA maximum load current step and a load capacitance of 1pF.

Simulation results show that the proposed LDO voltage regulator is competitive among the state-of-the-art architectures, exceeding some in transient response, reporting an output voltage overshoot and undershoot of 48mV and 49.8mV, respectively, with 0.5μs of settling time.

PVT (Process, Voltage, Temperature) corner simulations and further Monte Carlo analysis show that the designed system complies with the ISO 26262 standard.

A layout design of the proposed fast loop capacitor-less LDO voltage regulator is presented, for future integration.

Keywords: CMOS, LDO, voltage regulator, dropout voltage, fast loop, dual loop, capless, capacitor-less, transient compensation, frequency compensation, load regulation

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Filipe Oliveira

"Knowledge is a skyscraper.
You can take a shortcut with a fragile foundation of memorization,
or build slowly upon a steel frame of understanding."

Naval Ravikant

Contents

List of Figures

List of Tables

Abbreviations and Symbols

β	Feedback Factor
CD	Common Drain
C_{gd}	Gate-Drain Capacitance
C_L	Load Capacitor
C_M	Miller Capacitor
CMOS	Complementary Metal–Oxide–Semiconductor
CMRR	Common-Mode Rejection Ratio
CS	Common Source
C_{out}	Output Capacitance
C_{ox}	Oxide Capacitance per unit area
DRC	Design Rule Check
EA	Error Amplifier
FL	Fast Loop
FoM	Figure of Merit
FVF	Flipped Voltage Follower
g_m	Transistor's Transconductance
IC	Integrated Circuits
I_L	Load Current
I_Q	Quiescent Current
L	Channel Length of a transistor
LDO	Low-Dropout
LR_{line}	Line Regulation
LR_{load}	Load Regulation
LVS	Layout VS Schematic
MC	Monte Carlo
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-channel metal-oxide semiconductor
ODC	Overshoot Detection Circuit
PMOS	P-channel metal-oxide semiconductor
PM	Phase Margin
PSRR	Power Supply Ripple Rejection
PT	Pass Transistor
PVT	Process, Voltage, Temperature
R_L	Load Resistor
R_{out}	Output Resistance
SoC	System on Chip
SSF	Super Source Follower
TF	Transfer Function
T_{fall}	Fall Time
T_{rise}	Rise Time

UDC	Undershoot Detection Circuit
V_{DD}	Supply Voltage
V_{DO}	Dropout Voltage
V_{DSAT}	Transistor's Saturation Voltage
V_{EA}	Error Amplifier output Voltage
V_{FB}	Feedback Voltage
V_G	Gate Voltage
V_{in}	Pass Transistor's Input Supply Voltage
V_{out}	Output Voltage
V_{ref}	Voltage Reference
V_{SD}	Source-Drain Voltage
V_{SG}	Source-Gate Voltage
W	Channel Width of a transistor
$\mu_{p/n}$	Transistor's Mobility

Chapter 1

Introduction

The evolution of Integrated Circuits (IC) and semiconductor's industry has pushing circuit designs to allow for more integration in system-on-chip (SoC) solutions. Power management systems have been thoroughly studied in the last few years, not only for the increasing usage of portable and handheld battery operated devices [3], but also in regard to high-performance desktop and server applications [4]. Power management systems aim to improve power efficiency in a given device, in order to prolong battery life and operating time [3] of battery-operated devices and, ultimately, to satisfy packaging and cooling requirements [4].

1.1 Voltage Regulators

The low-dropout (LDO) voltage regulator is an essential power management circuit that typically follows a DC-DC switching converter [1], as shown in Figure 1.1.

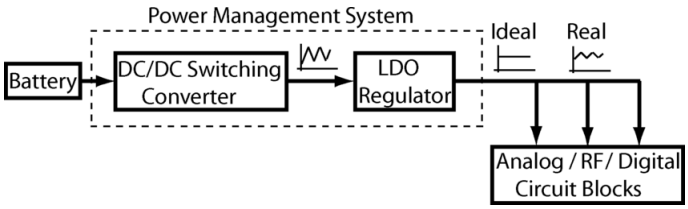


Figure 1.1: Block diagram of a typical power management system, taken from [1]

Low dropout voltage regulators come from the fact that a linear voltage regulator's efficiency is inversely proportional to the voltage drop across the control element. So, DC-DC switching converters are used to minimise the voltage drop of LDO regulators, as they buck the battery supplied voltage to any desired output voltage with a high grade of efficiency [5]. However, an SoC employs analog and other circuit blocks that are sensitive to supply voltage variations and supply noise [2], that cannot be supplied by switching regulators due to their high output ripple which degrades the performance of the blocks to be supplied [6]. LDO regulators are then used to provide high power supply rejection (PSR) and high accuracy power rails, under all load

conditions, to the circuit blocks. Figure 1.1 is also able to illustrate how the described voltage ripple of both the converter and the regulator work.

1.2 Motivation

Conventional LDO voltage regulator topologies use a large external capacitor, within the range of few microfarads (μF), to provide a good regulation of the output voltage during fast load transient variations and also, to set a dominant pole in the system to ensure a stable output voltage. However, in current SoC design technologies that aim to reduce chip area, this amount of capacitance cannot be integrated in silicon which leads to an external pin to mount an external capacitor in the board, resulting in an inefficient board area usage [7]. So, there is a need to remove this large external capacitor that unavoidably makes the LDO voltage regulator uncompensated, degrading its transient performance and system stability. Thus, an uncompensated capacitorless LDO voltage regulator requires internal frequency and transient compensation techniques in order to maintain the stability of the system and also a good and accurate transient response.

1.3 Objectives and Approach

The objectives established for this dissertation include the study of the state-of-the-art frequency compensation techniques and, also, state-of-the-art components that are part of the LDO voltage regulator's system. The study of prior state-of-the-art fast loop architectures is mandatory in order to implement the best suited architecture for the proposed capacitor-less LDO voltage regulator, and prove the concept that a fast loop is able to compensate the lack o an external output capacitor.

Based on a given general architecture of a frequency compensated capacitor-less LDO voltage regulator, the focus of this dissertation is to implement and develop a fast loop in order to compensate fast transient response. The purpose of the fast loop is to compensate the low bandwidth of the main loop, to regulate transient responses within the frequency range that are not covered by the bandwidth of the main loop. The results should aim for very low output voltage spikes, these being overshoots and undershoots caused respectively by fast high-to-low and low-to-high load current steps, as well as their own settling times. A low dropout voltage across the control device is also an important requirement so that the LDO voltage regulator is able to operate at a low input supply voltage, being aware also of the effects that voltage ripple have on input supply voltage.

Later, it is introduced extra add-on configurations such as a variable feedback factor and a start-up circuit in order to enrich and give a creative factor to the dissertation.

1.4 System Specifications

Table 1.1: Capacitor-less LDO Voltage Regulator initial specifications

Parameter	Value
Technology	28nm
V_{supply}	1.8V $\pm$10%
V_{out}	1.2V
ΔV_{out}	1.2V $\pm$10%
V_{DO}	0.36V
I_L	0 - 1 mA
$T_{L_{rise}}$	1 ns
C_L	0 - 1 pF
Loop DC Gain	60dB
Phase Margin	50 deg
PSRR (C_L=1pF)	-60dB @1kHz
	-40dB @1MHz
	-20dB @1GHz
LR_{line}	10 mV/V
LR_{load}	10 mV/mA

1.5 Structure of the Document

The dissertation presented is composed by six chapters. Chapter 1 gives the context of the presented problem. Chapter 2 shows the study of state-of-the-art architectures already developed for a fast loop. Chapter 3 shows a literature review and preliminary work done around a capacitor-less LDO voltage regulator, diving into the characteristics of the capless LDO voltage regulator and their components, as well as some basic theory review on negative feedback and stability. Chapter 4 further explores the mentioned state-of-the art fast loop architectures by implementing and comparing them from a more objective point of view. The final design is analysed and developed in the same chapter as well as the introduction of some extras to the system. Chapter 5 shows the most relevant results obtained from the final integration, given the LDO voltage regulator characteristics and specifications, including PVT corner simulations and Monte Carlo analysis. The last chapter concludes the work done throughout this dissertation with some final insights regarding future work around fast loops for capless LDO voltage regulators and also some suggestions that would improve the work developed.

Chapter 2

State of the Art

The EA presents high DC gain but a low bandwidth and slew-rate, which means that the LDO might have a slow response for higher transient load current variations. In order to do this kind of transient compensation, so the LDO is able to react faster and reduce voltage values of overshoots and undershoots, the LDO needs to provide adequate power instantaneously by increasing the bandwidth and slew rate at the gate of the pass transistor [27]. A faster loop acting directly at the gate of the pass transistor is the solution proposed in this work. Some state of the art studies were made in order to find out which approaches may be best for the implementation of a fast loop in a generic capacitor-less LDO architecture.

2.1 Literature Review

2.1.1 Overshoot Detection Circuit, implemented by Liu and Chen (2020)

The work developed in [27] introduces two different approaches for an ultra-fast transient response of the LDO presented in the paper, one for low-to-high load steps (undershoots) and the other for high-to-low load steps (overshoots).

When dealing with undershoots, the paper focuses on achieving quick transient responses without consuming large amounts of quiescent current. So, it is implemented a fast local loop based on a super source follower (SSF), acting as a buffer, and a cascoded flipped voltage follower (FVF) topology to increase the bandwidth at the gate of the pass transistor [27]. The fast local loop mentioned is shown in Figure 2.1.

With this configuration, M_1 and M_2 sense the undershoot at the output of the LDO, amplifying it to the node V_2 [27]. As the output voltage of the EA charges the gate of M_1, this fast local loop stays dependent of the EA's generic slow loop which means that the slew rate of the EA limits the transient response at V_G. This limitation is then attenuated by the SSF that ensures ultra-low output impedance and premium sink capability to quickly discharge the pass transistor and thus, turning it off [27].

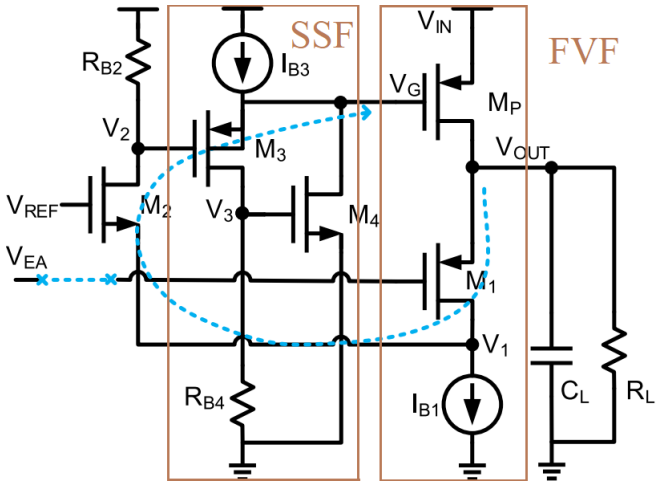


Figure 2.1: Fast local loop including load, [27]

In order to compensate high-to-low load steps, the paper suggests the implementation of an overshoot detection circuit (ODC), presenting various possible configurations. For the sake of simplicity and power consumption through quiescent current, a robust ODC, shown in Figure 2.2, was introduced in [27].

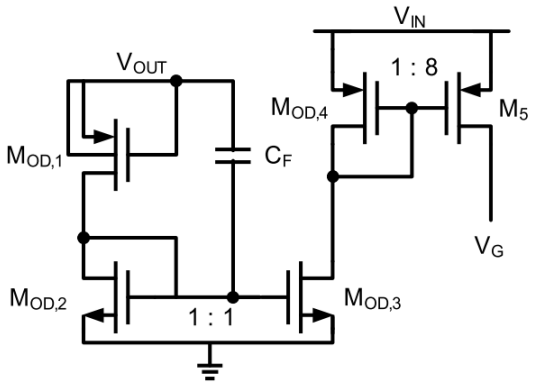


Figure 2.2: Robust Overshoot Detection Circuit, [27]

This configuration has the ability to compensate fast transient responses without EA's slew-rate limitation, as it is independent from it. According to [27], connecting the gate of the PMOS transistor $M_{OD,1}$ to its source forces this ODC to be in off mode, letting enough leakage current through to bias transistor $M_{OD,3}$ near threshold voltage. This way, upon coupling an overshoot at V_{out} to the gate of $M_{OD,3}$ with the capacitor C_F, transistor $M_{OD,3}$ is able to sink a large dynamic current. This current is then amplified by the 8 to 1 size ratio of the current mirror of M_5 and $M_{OD,4}$ respectively, that rises the voltage value at V_G, turning off the pass transistor of the LDO.

The LDO mentioned above is implemented in a 65nm CMOS technology and, can be supplied from 1.05V to 1.2V in order to regulate an output voltage (V_{out}) of 0.9V, with a dropout voltage (V_{DO}) of 150mV under a load current step (I_L) of 20mA.

The simulation results presented in [27] showed that the architecture was able to achieve undershoots from 290mV with 10pF load capacitance (C_L) down to 120mV with a 100pF load capacitance, at a load current step rise time (T_{rise_L}) of 500ps. However, as observed in Figure 2.3, the increase of load capacitance makes the overshoot settling time increase. For different T_{rise_L} with C_L = 10 pF, the simulation results in Figure 2.3 show a 100mV of undershoot at a T_{rise_L} of 5ns, up to 290mV at a T_{rise_L} of 500ps.

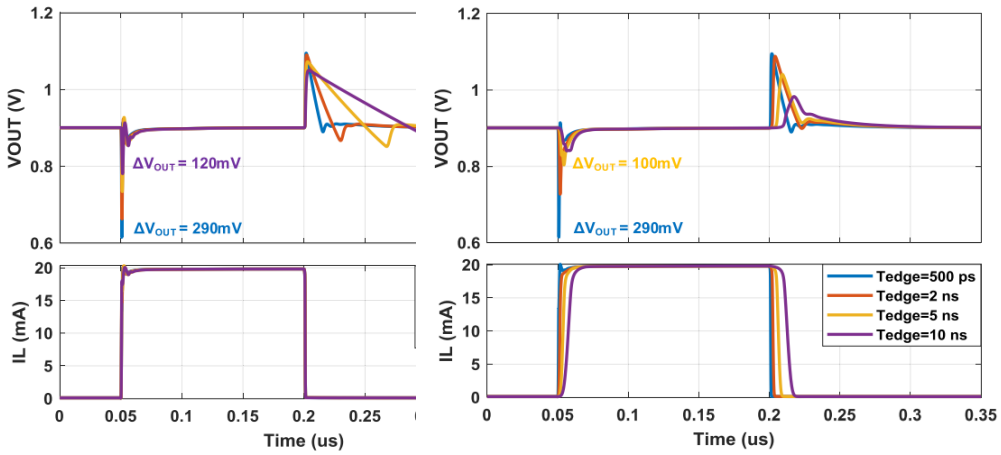


Figure 2.3: Simulation results obtain in [27]

Overall, including biasing circuits, this architecture was able to achieve 99.7% of current efficiency with a quiescent current (I_Q) equal to 65μA. The fast local loop has the most power consumption of the presented LDO, as the cascoded FVF consumes 35μA and the SSF buffer consumes 15μA to boost the bandwith of the LDO. The EA consumes 8.5μA of quiescent current and the overshoot detection circuit ended up consuming only 1.5μA.

2.1.2 Fast differential stage architecture, implemented by Yosef-Hay *et al.* (2017)

The work presented in [10] is an extended version of the work developed in [28] that aims to satisfy the challenges of hearing aids devices, including specifications such as fast transient performance and small overshoots and undershoots under fast load current step variations [10].

As shown in Figure 2.4, the architecture presented is based on a dual feedback loop topology in which, the configuration adopted for the fast loop, is set to be dependent of the slow loop defined by the EA.

The fast loop consists in a differential stage that drives the gate of the pass device Q_1. Q_2 and Q_3 are controlled by the slow loop of the EA while the differential pair of Q_4 and Q_5 acts as a fast transient detection stage. According to [10], this design allows for an easy and area efficient implementation because of its simplicity and is still able to demonstrate a good performance. The low transistor count of this architecture also allows the system to have a very limited number of poles and zeros, that makes it easier to achieve and maintain stability [10].

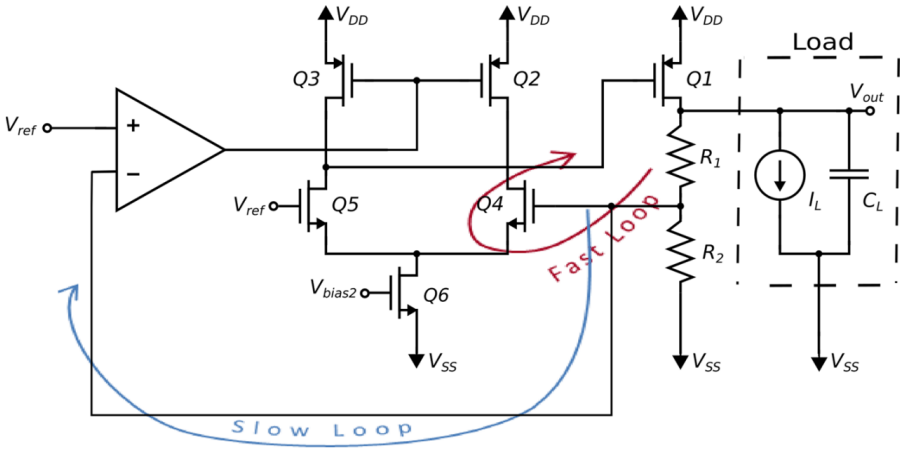


Figure 2.4: Fast loop and slow loop of the LDO proposed in [10]

The voltage regulator, implemented in a 180 nm CMOS process, is supplied with 1.2 V and has an output voltage of 0.9 V. The load current step is 250 μA, from 250 μA to 500 μA, with 1 ns of load current step time and a load capacitance up to 100 pF [10]. Post layout simulations showed overshoots/undershoots of 64 mV without load capacitance and 56 mV with C_L = 100 pF, both for a rise/fall time of 1 ns. The settling time of this simulations is not available. Both post layout simulation and measurement of load transient response for a rise/fall time of 1.5 μs were performed in order to evaluate both results fairly. The first one generated 18 mV of overshoot and undershoot with a settling time, t_s, of 3 μs and, the measures showed that the voltage regulator was able to achieve 26 mV of both undershoot and overshoot for t_s equal to 1.5 μs and 3.5 μs respectively [10].

The post layout simulations also showed the LDO has a PSRR value of 63 dB at 1 kHz, which was further tested by measuring the line transient response of a 0.3 ms supply step from 1.0 V to 1.4 V, achieving a ΔV_{out} of 5 mV [10]. The fast loop and EA consume 8.256 μA and 1.05 μA of quiescent current, respectively, of a total quiescent current consumption of 10.3 μA [10].

2.1.3 Transient Enhancement Circuit based on a Differentiator, designed by Yu Peng *et al.* (2021)

The fast loop architecture proposed in [26], Figure 2.5, aims to achieve fast transient responses while solving the stability constraints from the removal of the LDO output capacitor. This configuration is labelled as a class AB transient enhancement circuit based on a differentiator, which is composed by a current amplifier connected in series with a capacitor C_F, forming an independent fast loop emerging at the output node and closing at the gate of the pass transistor M_P.

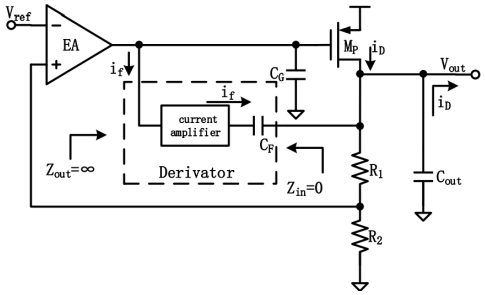


Figure 2.5: Derivator separation poles frequency compensation schematic, [26]

The C_F is used to produce a Miller compensation scheme by executing a separation of the primary and secondary frequency poles and thus, ensure the stability of the system. This capacitor is also able to detect overshoots and undershoots whenever there is a high-to-low or low-to-high load current step, respectively. The spikes detected are then amplified by the current amplifier [26].

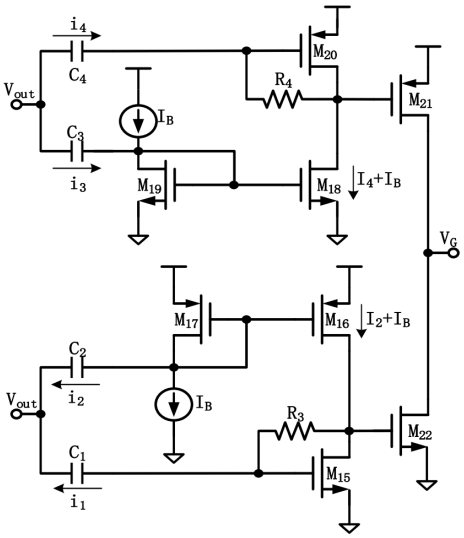


Figure 2.6: Class AB transient enhancement circuit based on a differentiator, [26]

The LDO presented in [26] is implemented in a 180 nm CMOS technology and, can be supplied from 1.4 V to 1.8 V in order to regulate an output voltage (V_{out}) of 1.2 V. This load regulation setup allows the circuit to compensate a maximum load current step of around 300 mA, while maintaining an output voltage offset of 522 μV.

The simulation results presented in [26] showed that, for the mentioned load current step, the LDO achieves a maximum undershoot value of 50.3 mV with 1.12 μs of settling time (t_s) and, a maximum overshoot value of 51.1 mV with t_s equal to 1.58 μs. This results can be observed in Figure 2.7.

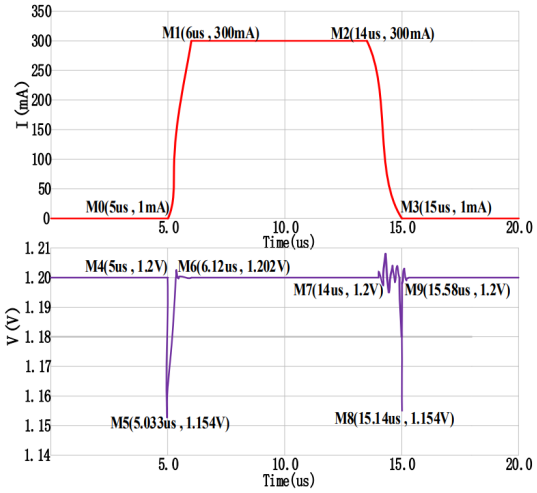


Figure 2.7: Simulation results of load transient characteristics, [26]

2.1.4 Common Source Stage, design by N. Deleuran *et al.* (2015)

The LDO voltage regulator's design proposed in [28], has a similar approach to [10] for implementing a fast loop, as it has nearly the same dependency level of the slow loop. Although the LDO design uses a NMOS as the pass transistor, with a common drain stage, this architecture showed enough potential to be considered due to its simplicity and direct approach to a fast transient spike suppression. The simplicity of the design has major relevance as the paper aims for an easy and space efficient implementation, while still providing good regulation performance [28].

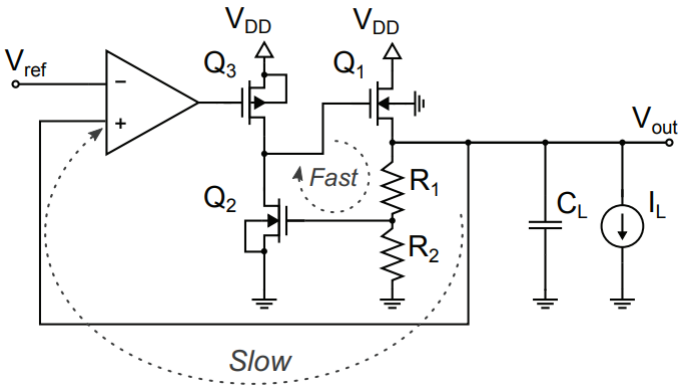


Figure 2.8: Functional diagram of the LDO, [28]

As shown in Figure 2.8, the fast loop consists in a common source (CS) amplifier formed by transistors Q_2 and Q_3, that will charge or discharge the gate of the pass transistor Q_1 [28]. Despite starting at the gate of Q_2, the dependency of this loop lies at the gate of Q_3 driven by the EA. The goal of this CS stage is to achieve a great Gain Bandwidth Product (GBWP), through the maximisation of Q_2's transconductance, in order to compensate fast transient load current steps [28].

The simulations presented in [28] were performed under typical temperature and process corner of a 180 nm CMOS technology. The LDO is supplied with 3.3 V and generates an output voltage of 1.8 V. The load transient analysis was tested with a load current step of 50 mA with a rise and fall time of 1 μs and a maximum load capacitance of 20 pF [ref paper]. Load transient simulations were done at the schematic level and at the layout level. The first one showed that, under no load capacitance conditions, the undershoot voltage is 140 mV for a transient recovery time, T_R (refered in [28] as being the load response rise time), of 39 ns and, for a reduction of the load current step time to 10 ns, the undershoot voltage increased to 640 mV and T_R decreased to 20.4 ns. Simulations at the layout level, with extracted parasitics included, showed that for a load current step time of 1ns, the undershoot voltage value was 160 mV with T_R of 1.158 μs.

2.1.5 Summary

Table 2.1 compiles the most relevant performance parameters of the state-of-the art architectures.

Table 2.1: Specifications' comparison for the state-of-the-art work presented

Parameters	ODC, Liu and Chen [27]	ODC, J. Tang *et al.* [19]	Fast Diff. Stage [10]	Transient Enhancement Circuit [26]	CS Fast Loop [28]
Technology (nm)	65	130	180	180	180
V_{in} (V)	1.05-1.2	2.5-3.6	1.0-1.4	1.4-1.8	3.3
V_{out} (V)	0.9	1.2	0.9	1.2	1.8
V_{DO} (mV)	150	1300[2]	100	200	1500[2]
I_{load_MAX} (mA)	20	20	0.5	300	50
C_L (pF)	0-100	0-100	0-100	N/A	20
Overshoot (mV)	N/A	97	26	51.1	N/A
$T_{s_{overshoot}}$ (μs)	N/A	1.5	3.5	1.12	N/A
Undershoot (mV)	290[1]	98	26	50.3	160
$T_{s_{undershoot}}$ (μs)	0.1	1.2	1.5	1.58	1.16
I_q (μA)	65	7.2	10.5	132	98.3
FOM	3.9 ps	0.175[2] ps	218.4[2] ps	0.69[2] ns	2.281 ns
Area (mm^2)	0.01	-	0.012	-	0.0093

[1] For minimum C_L and maximum I_L load conditions
[2] Values taken from calculations

Results given by the authors suggest that the transient enhancement loop delivers the best performance despite its quiescent current value. Although the absolute value of the overshoots/undershoot generated in the fast differential stage architecture is lower, the maximum load current that the transient enhancement loop is able to regulate is about 600 times higher.

Chapter 3

LDO Voltage Regulator

A generic uncompensated capacitor-less LDO voltage regulator architecture is implemented by several sources [3],[8] and, it is composed by a pass device used as a control element, a negative feedback network and an error amplifier used as an error detection mechanism, as shown in Figure 3.1.

As the name suggests, an LDO voltage regulator has the purpose to maintain an accurate output voltage independently of the given load. This means that at a fast high-to-low load step, the output voltage, V_{out}, will naturally overcompensate the new load current value which will generate an overshoot. This overshoot is seen at the feedback voltage node, V_{FB}, and will be compared to the reference voltage, V_{ref}, in the error amplifier (EA), increasing the voltage in the output node of the EA, V_{EA}. Once V_{EA} increases, the gate of the PMOS transistor gets charged making $V_{SG_{PT}}$ decrease. When the voltage value of V_{SG} decreases, the drain current flowing through the pass transistor will also decrease accordingly to the active load, regulating the output voltage back to the desired value. When V_{out} decreases, due to a low-to-high load current step, the opposite logic is applied and, like so, this whole process is done recursively so that the system regulates itself.

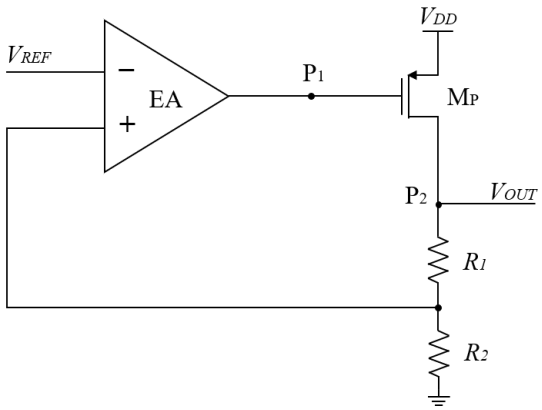


Figure 3.1: Proposed uncompensated LDO voltage regulator

3.1 Components

3.1.1 Pass Transistor

The main three criteria aspects associated with the pass transistor in a LDO voltage regulator is the maximum allowable current that flows through it, its dropout voltage and power consumption. Studies provided by [10], [9] and [11] show that some voltage regulators that use a NMOS transistor as pass device, even though it requires less area for the same amount of drain current due to its higher mobility, the dropout voltage required to maintain it in saturation region is greater than the one required for PMOS transistors, which means that the supply voltage needs to be significantly higher than the output voltage. The dropout voltage over a NMOS transistor can be reduced by increasing its gate voltage above the supply voltage, as stated in [9] however, in order for this to happen, some NMOS pass device configurations add a charge pump circuit to increase the headroom of the NMOS pass transistor.

Another aspect to take into account is the consumption of the pass device, where the dropout voltage plays a huge role in power efficiency. The less dropout voltage there is, the less power dissipation there will be, leading the PMOS to consume less quiescent current than the NMOS as a pass transistor [10].

From this point of view, the PMOS transistor was chosen as pass device for the LDO voltage regulator with the goal of achieving low dropout voltage. The pass transistor design is shown in Figure 3.2.

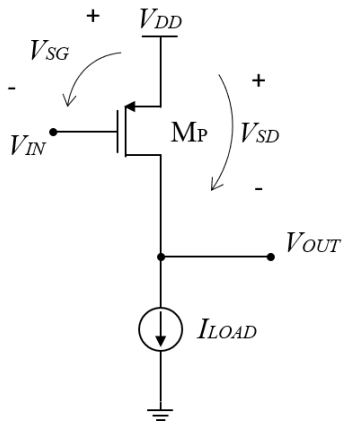


Figure 3.2: Pass Transistor design

The pass transistor determines the maximum load current that the LDO voltage regulator is able to regulate so, from drain current equation for saturation region it is possible to determine the transistor dimensions for the desired maximum load current, as presented in Equation 3.1.

$$I_{load_{max}} = \frac{1}{2}\mu_p C_{ox}\left[\frac{W}{L}\right]_{PT} V_{dsat}^2 \tag{3.1}$$

$I_{load_{max}}$ defines the maximum load current, forcing the dimensions of the pass transistor, W/L, for the saturation voltage specified. The hole mobility, μ_p, and gate oxide capacitance per unit area, C_{ox}, are device parameters set by the technology in use.

Equation 3.1 was rearranged to equation 3.2 to better show how the pass transistor dimensions can be found. Computer simulations were used to complement the mentioned equations and obtain the right W/L ratio for the specified maximum load current of the proposed work. The W/L ratio is presented in Table 3.1.

$$\left[\frac{W}{L}\right] = \frac{2I_{load_{max}}}{\mu_p C_{ox} V_{dsat}^2} \tag{3.2}$$

Table 3.1: Pass Transistor sizing of the proposed LDO

	M_P (hv)
W ($\cdot 1\frac{}{W_{min}}$)	1
L ($\cdot 1\frac{}{L_{min}}$)	1
Multiplicity	400

Analysing the small-signal model of PMOS transistor [12], the DC gain of the pass transistor is found to be

$$A_{PT} = -g_{m_{PT}} ro_{PT} \tag{3.3}$$

As the PMOS transistor presents a negative gain, the feedback voltage is applied to the positive input terminal of the error amplifier and the reference voltage to the negative input terminal, as shown in Figure 3.1. Although it seems to be a positive feedback system, due to the gain properties of the PMOS transistor, it is in fact a negative feedback system.

3.1.2 Error amplifier

The implemented Error Amplifier (EA) is based on a typical two-stage operational amplifier [14], [15], [16] and is used to amplify the error between the input differential pair. The proposed Error Amplifier is shown in Figure 3.3.

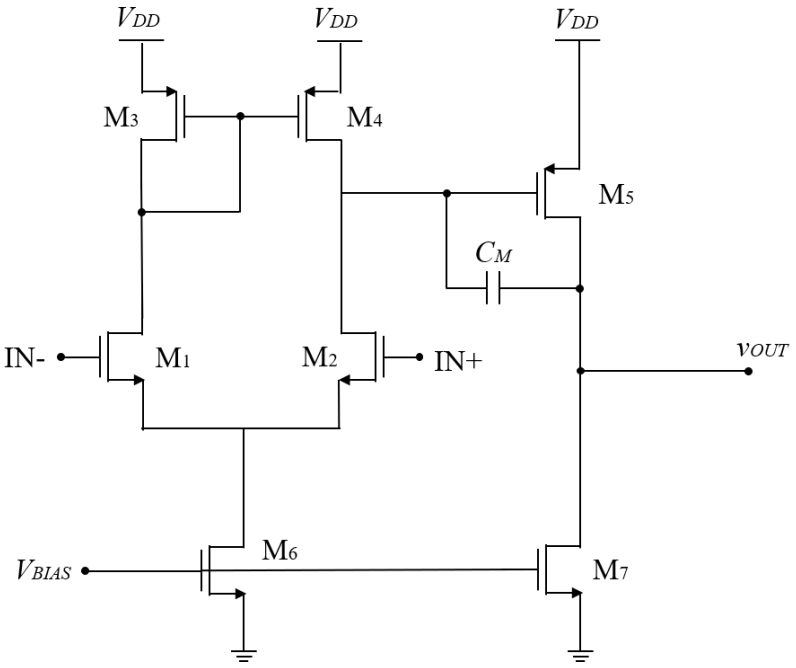


Figure 3.3: Error Amplifier - Two stage Operational Amplifier

The first stage of the EA is based on a simple current mirror loaded differential pair configuration. As analysed in detail in [12] and [18], the small-signal model of the first stage, the open-circuit differential gain (A_d) can be found as the product of the short-circuit transconductance of the differential input (G_m) with the output resistance of the circuit (R_{OUT}) as shown in Equation 3.4.

$$A_d = G_m \cdot R_{OUT} \tag{3.4}$$

Considering the size of both transistors in the differential pair, M_1 and M_2, is the same for an equal distribution of the bias current flowing through M_6, the analysis done in [18] show that

$$G_m = -g_{m_{1,2}} \tag{3.5}$$

where $g_{m_{1,2}}$ represents the transconductance of M_1 and M_2. The output resistance of the first stage is defined by the circuit equivalent resistance seen at the output node and is shown in 3.6 to be the parallel equivalent of the output resistance of the differential pair and the output resistance of the current mirror.

$$R_{OUT} = (r_{o_{1,2}} || r_{o_{3,4}}) \tag{3.6}$$

That being said, the open loop differential gain of the first stage is expressed as

$$A_{stage1} \equiv \frac{v_{OUT}}{v_{IN}} = -g_{m_{1,2}}(r_{o_{1,2}} || r_{o_{3,4}}) \tag{3.7}$$

The second stage of the error amplifier is a PMOS common source amplifier. Its purpose is to amplify the voltage seen at the gate of the transistor M_5 and, in order to calculate the DC gain of this second stage, a small signal analysis illustrated in Figure 3.4 is done.

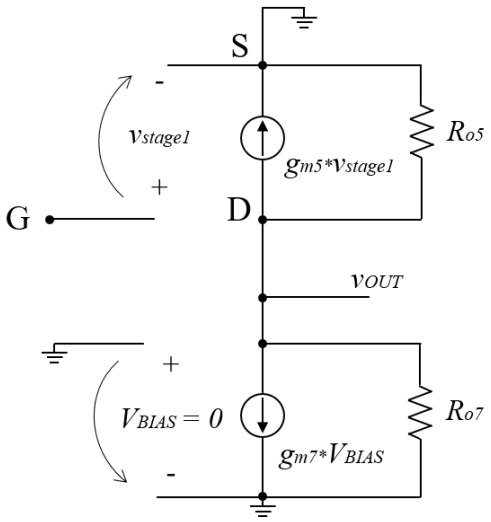


Figure 3.4: Small Signal Model of the 2nd stage of the EA

Applying the Kirchhoff's Current Law (KCL) in the common source shows that

$$\frac{v_{OUT}}{r_{o_5}} + g_{m_5} v_{stage1} + \frac{v_{OUT}}{r_{o_7}} = 0 \tag{3.8}$$

which leads to a common source gain of

$$A_{stage2} \equiv \frac{v_{OUT}}{v_{stage1}} = -g_{m_5}(r_{o_5} || r_{o_7}) \tag{3.9}$$

The assemble of the entire open loop gain of the error amplifier (A_{EA}) is given by the product of its stages so,

$$A_{EA} = A_{stage1\,stage2} = g_{m_5} g_{m_{1,2}} \cdot [(r_{o_5} || r_{o_7}) \cdot (r_{o_{1,2}} || r_{o_{3,4}})] \tag{3.10}$$

In addition, it is integrated a capacitor between the two stages in the error amplifier to introduce a miller compensation for stability purposes. The miller compensation is based on the miller effect explained in [17], illustrated in Figure 3.5, to generate a technique called pole splitting that increases the dominant pole capacitor by (1 - A_{device}), bringing it to lower frequencies, and decreases the second pole capacitor by (1 - $\frac{1}{A_{device}}$), pushing it to higher frequencies.

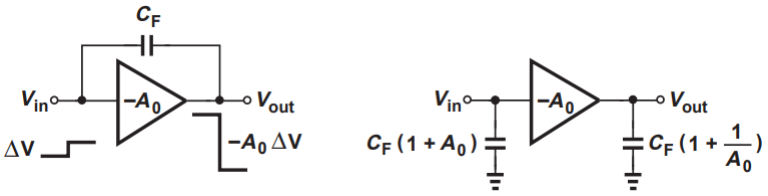


Figure 3.5: Miller's effect, [17]

From an AC stability analysis point of view, this action is intended to achieve adequate phase margin by forcing the system transfer function to behave like a single pole system [15]. An intuitive illustration is showed in Figure 3.6.

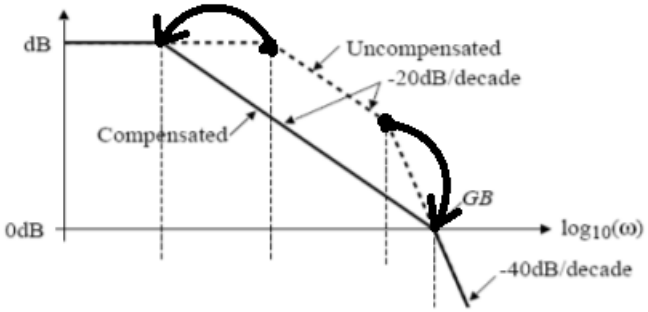


Figure 3.6: Bode Plot of Miller Compensation, adapted from [16]

The components' sizing for the Error Amplifier is presented in Tables 3.2 and 3.3.

Table 3.2: Transistor sizing of the Error Amplifier implemented in the proposed LDO

	M_1 (hv)	M_2 (hv)	M_3 (hv)	M_4 (hv)	M_5 (hv)	M_6 (lvt)	M_7 (lvt)
W $(\cdot 1\frac{}{W_{min}})$	4	4	9	9	1	18	1
L $(\cdot 1\frac{}{L_{min}})$	2	2	1	1	2	16	10
Multiplicity	1	1	1	1	100	1	70

Table 3.3: Miller capacitor value

Parameter	Value
C_M	5 pF

The results gathered from the Error Amplifier simulations are presented in Table 3.4.

Table 3.4: Proposed Error Amplifier Specifications

Parameter	Value
Loop DC Gain	46.5dB
Phase Margin	88.4º
BW	14.5 kHz
CMRR gain	47.1dB
PSRR (C_L=1pF)	-49dB @1kHz
	-12.3dB @1MHz
	-921mdB @1GHz

Since the capacitor-less LDO voltage regulator supports a load capacitance up to 1pF, the miller capacitor, C_M, has to be higher so that the dominant pole is not significantly affected by the load capacitance and thus the system's stability is not load dependent. The Miller effect on the capacitance C_M sets the phase margin of the EA at 87.9º in order to prevent stability issues when adding the equivalent capacitance of the miller effect on C_GD of the pass transistor to the node of its gate terminal. Based on the size of the pass transistor, the value of the mentioned equivalent capacitance at the gate terminal is around 500fF.

3.1.3 Feedback Network

The feedback network represents a frequency independent feedback factor, β, given by the voltage divider of R2. Since the feedback voltage, V_{FB}, is connected to the differential pair of the EA, it is assumed that its voltage value is equal to V_{REF} considering an ideal analysis of the system and the operational amplifier. The DC gain of the feedback network is then calculated through Equation 3.11.

$$\beta = \frac{V_{REF}}{V_{OUT}} = \frac{R_2}{R_1 + R_2} = \frac{1}{2} \tag{3.11}$$

3.1.4 Stability

A LDO voltage regulator in analog circuits works as a negative feedback system in order to regulate the desired output voltage. The system block diagram of an LDO voltage regulator is shown in Figure 3.7, with the Error Amplifier, EA(s), and Pass Transistor, PT(s), forming the feed-forward network and the feedback factor, β, being the previously mentioned feedback network. The input signal X(s) represents the voltage reference, V_{REF}, as it is the primarily signal for comparison and tracking of the output value of the signal Y(s) that represents the output voltage of the LDO, V_{OUT}.

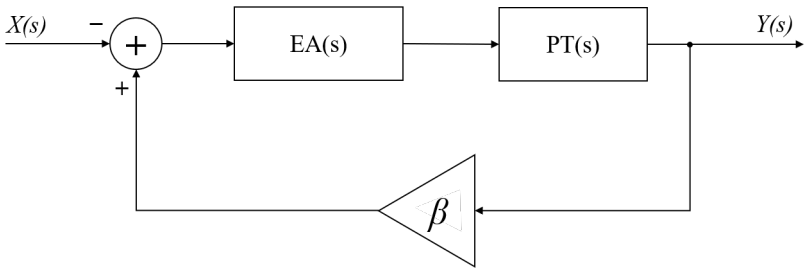


Figure 3.7: System Block Diagram of the proposed LDO voltage regualtor

Through the system block diagram analysis, the transfer function of the system is found to be

$$\frac{Y(s)}{X(s)} = \frac{EA(s)PT(s)}{1+\beta EA(s)PT(s)} \tag{3.12}$$

Like any negative feedback system, stability has a huge role when designing and implementing the system and, for the case of a capacitor-less LDO voltage regulator, this one is prone to become unstable due to its pole composition. The poles of the LDO can be identified by inspection in Figure 3.1. With the removal of the external capacitor, the dominant pole is no longer at the output node of the LDO voltage regulator. The first pole, P_1, is now found at the gate of the pass transistor with in order not to make the stability of the LDO voltage regulator load dependent. The second pole, P_2, is in the output node of the LDO, preferably at high frequencies so it doesn't impact the stability of the circuit [19], [20]. Analysis by inspection are very useful to have a clear vision on where are the critical points in the circuit and from there, proceed to a more focused and detailed analysis. The bode plot shown in Figure 3.8, illustrates how an uncompensated capacitor-less LDO is on the edge of instability, having in mind that, to be stable, the system needs to have a positive phase margin at unity gain frequency.

The goal in a capacitor-less LDO voltage regulator is to promote the first pole to be the dominant pole, whereas before the external capacitor set the second pole as the dominant pole, so that the system is able to maintain stability independently of the load capacitance to be regulated, noting that the load capacitance adds up to the second pole of the LDO. In order to achieve this kind of stability for the capless LDO, the miller compensation technique is used to make the first pole dominant as explained previously.

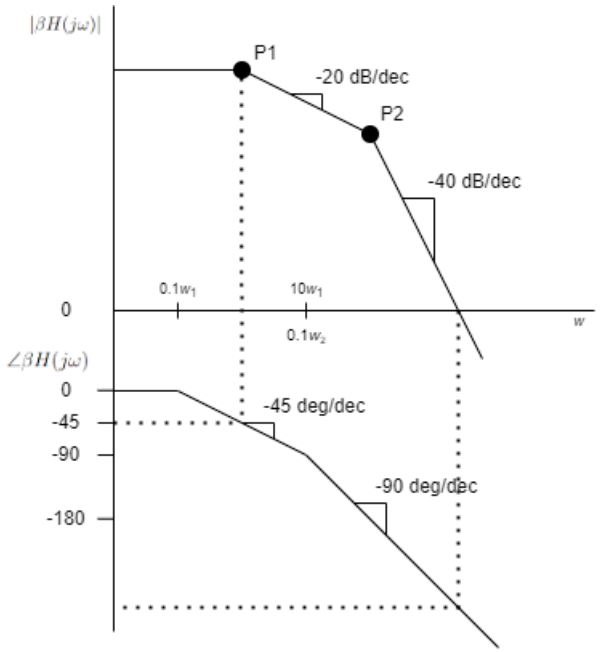


Figure 3.8: Gain and Phase Bode Plot of an uncompensated LDO voltage regulator, [16]

3.2 Characterisation

The LDO voltage regulator has to generate a constant output voltage while dealing with dynamic variations, this is, it should be the most independent of supply variations and also able to adapt quickly to load changes of the circuit that uses this regulated power supply. So, the system needs to meet some static-state analysis to ensure good steady state operation, dynamic-state analysis to be able to regulate the output voltage during load and line transient conditions, and high-frequency analysis to see how the LDO is able to reject high-frequency noise sources such as non linearities in the voltage supply [21].

The design of the LDO voltage regulator aims to be ready for integration so, the characterisation process and design of the circuit needs to take into consideration Process, Voltage and Temperature (PVT) variations to make sure the proposed design works in all extreme corners, as it is going to be explained further in section 3.3.

3.2.1 Static-State Specifications

3.2.1.1 System Gain

The next set of equations show the system gain in steady state where V_{out} is the output signal of the system and V_{ref} the input signal that serves as reference for the output regulation.

$$\frac{V_{out}}{V_{ref}} = \frac{A_{OL}}{1+A_{OL}\beta} \tag{3.13}$$

$$\frac{V_{out}}{V_{ref}} = \frac{A_{EA}A_{PT}}{1+A_{EA}A_{PT}\beta} \tag{3.14}$$

$$\frac{V_{out}}{V_{ref}} = \frac{g_{m_5}g_{m_{1,2}}g_{mPT}\cdot[(r_{o_5}||r_{o_7})\cdot(r_{o_{1,2}}||r_{o_{3,4}})_{oPT}]}{1+g_{m_5}g_{m_{1,2}}g_{mPT}\cdot[(r_{o_5}||r_{o_7})\cdot(r_{o_{1,2}}||r_{o_{3,4}})_{oPT}]\cdot(\frac{R_2}{R_2+R_1})} \tag{3.15}$$

3.2.1.2 Dropout Voltage

Dropout voltage is understood to be the minimum headroom required for the pass transistor to be able to flow the maximum load current specified. It is difference between the maximum generated output voltage and the minimum supply voltage available to the system in order to keep the pass transistor in saturation region so the device can operate properly without any unwanted performance degradation [21]. Coming from the fact that the supply voltage connects to the source of the PMOS pass transistor and the output voltage to the drain of the PMOS pass transistor, the voltage dropout of the LDO voltage regulator can be defined as the saturation voltage of the pass transistor that will further be designed to obtain the desired value of this specification, based on its maximum load current as previously shown. In spite of V_{DO} being set through Equation 3.16, Equation 3.17 presented in [5] shows another way to get the value of the LDO's dropout voltage.

$$V_{DO} = V_{Dsat_{PT}} = V_{DD_{min}} - V_{out_{max}} \tag{3.16}$$

$$V_{DO} = I_{load_{max}}o_{PT} \tag{3.17}$$

3.2.1.3 Load Regulation

Load regulation measures the ability of the LDO voltage regulator to maintain a constant output voltage under DC varying load conditions. The load variations are represented by variations in the load current as shown in equation 3.18, where $A\beta$ is the loop gain and $r_{o_{PT}}$ is the output resistance of the pass transistor [5].

$$LR_{load} = \frac{\Delta V_{out}}{\Delta I_L} \approx \frac{r_{o_{PT}}}{1+A\beta} \tag{3.18}$$

3.2.1.4 Line Regulation

Line regulation measures the ability of the LDO voltage regulator to maintain a constant output voltage under DC varying supply voltage conditions applied in the source terminal of the pass transistor as shown in Equation 3.19. The voltage supply variations also imply the measurement of the output voltage for different voltage dropout values [5].

$$LR_{line} = \frac{\Delta V_{out}}{\Delta V_{in}} \tag{3.19}$$

3.2.1.5 Power Efficiency

The measurement of power efficiency in a LDO voltage regulator, and many other circuits, is useful to determine various energy related aspects, such as battery life in portable devices for example. This measurement can be calculated in percentage of the ratio between the power consumption over the power supplied as shown in Equation 3.20.

$$E_{ff_{power}}(\%) = \frac{P_{output}}{P_{supply}} = \frac{V_{out} I_L}{V_{DD}(I_L + I_Q)} \cdot 100 \tag{3.20}$$

3.2.2 Dynamic-State Specifications

Based on the small signal model of the proposed LDO voltage regulator, illustrated in figure 3.9, the analysis of the system's dynamic state is done through the transfer functions presented in the following set of equations. The analysis of the small signal model was focused on the main nodes of the regulator in order to study and find the most influential poles of the system already mentioned in previous subsections. $G_{m_{EA}}$ and $G_{m_{EA}}$ represent the transconductances of the Error Amplifier and the pass transistor, respectively.

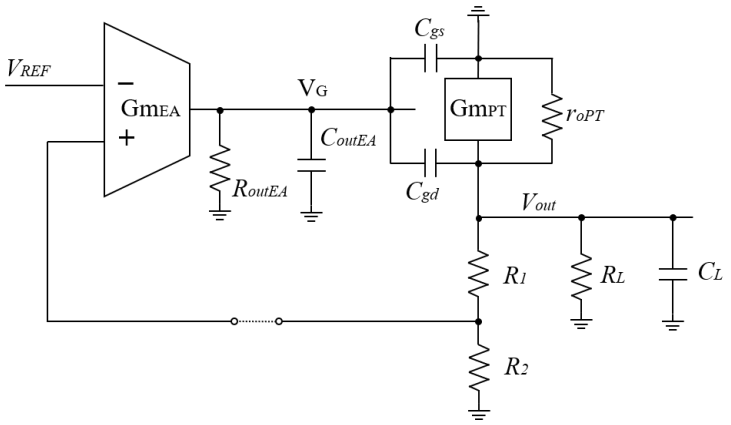


Figure 3.9: Small Signal Model of the proposed LDO voltage regulator

$$TF_{LDO}(s) = \frac{V_{FB}}{V_{ref}}(s) = \frac{V_G}{V_{ref}}(s) \cdot \frac{V_{out}}{V_G}(s) \cdot \frac{V_{FB}}{V_{out}}(s) \tag{3.21}$$

$$\frac{V_G}{V_{ref}}(s) = \frac{Gm_{EA}(s)_{out_{EA}}}{1 + s[C_{out_{EA}} + C_{gs_{PT}} + C_{gd_{PT}}(1 - A_{PT})]_{out_{EA}}} \tag{3.22}$$

$$\frac{V_{out}}{V_G}(s) = \frac{Gm_{PT}(s) \cdot [R_L || (R_1 + R_2) || r_{o_{PT}}]}{1 + s[C_{gd_{PT}}(1 - \frac{1}{A_{PT}}) + C_L] \cdot [R_L || (R_1 + R_2) || r_{o_{PT}}]} \tag{3.23}$$

$$\frac{V_{FB}}{V_{out}}(s) = \frac{R_2}{R_1 + R_2} \tag{3.24}$$

3.2.3 High-Frequency State Specifications

3.2.3.1 PSRR

Power Supply Rejection Ratio, PSRR, measures the ability of the LDO voltage regulator to reject supply variations, that can be seen as noise to the desired output on the circuit input supply voltage, it has the same value as line regulation [2] but, it is measured through an AC simulation, expressed by the ratio between the transfer function of the system's open loop gain over the transfer function of the gain between the output node and the input supply node, as shown in the following equation.

$$PSRR = 20 \cdot log_{10}(\frac{V_{outripple}(s)}{V_{in_{ripple}}(s)}) \tag{3.25}$$

3.2.4 Figure of Merit (FoM)

The Figure of Merit (FoM) calculation is a method used to compare the performance of several architecture for a capless LDO voltage regulator. This collective measurement can be calculated through different equations depending on the performance parameter of which the LDO voltage regulator is designed for [22]. For the proposed specifications and objectives of the implemented capless LDO voltage regulator, the FoM will be calculated based on the load transient performance in order to be further compared to state-of-the-art architectures.

According to the study provided by [22] following the work developed in [23], [24] and many others, Equation 3.26 is the most established equation used for general purpose performance comparison, which is focused on load transient and efficiency parameters, where C_{out} refers to the output load capacitance, ΔV_{out} to the output voltage difference during a full load transient step with I_q and $I_{L_{MAX}}$ being the quiescent current and maximum load current respectively.

$$FoM = T_{settle} \cdot \frac{I_Q}{I_{L_{MAX}}} = \frac{C_{out} \cdot \Delta V_{out}}{I_{L_{MAX}}} \cdot \frac{I_Q}{L} \tag{3.26}$$

3.3 PVT Variability

The IC and semiconductor fabrication process has a strong impact in determining the circuit's behaviour and, when considering the circuit's behaviour after fabrication, it must be taken into account environmental and manufacturing variations, that impose different operating conditions. So, a circuit must be designed to operate properly and reliably, for a long period of time, over extreme corner variability of three main parameters, Process, supply Voltage and operating Temperature (PVT) [25], in order to avoid failure, degradation and customer dissatisfaction.

3.3.1 Process Variation

The Process variation is a manufacturing variation and may be caused by dependencies on precision factors, such as film thickness and optical deviations that may affect the channel length of MOS transistors, and also by different doping concentrations affecting essentially the threshold

voltage, and charge mobility of transistors [25]. This variations in process causes changes in the propagation delay of transistors and, for that, MOS transistors are categorised as being fast (F), slow (S) or typical (T). In this way, process corners can be set as:

Table 3.5: Process Corners

NMOS	PMOS	Corner Designation
Slow	Slow	SS (slow-slow)
Slow	Fast	SF (slow-fast)
Typical	Typical	TT (typical-typical)
Fast	Slow	FS (fast-slow)
Fast	Fast	FF (fast-fast)

3.3.2 Supply Voltage

The supply voltage variation is an environmental variation that the IC is subjected to, such as IR drops along supply rails and supply noise [25]. The impact around the nominal voltage value, caused by these effects, is typically $\pm 10\%$ [25] which means that, for the proposed circuit the supply voltage variation corners are going to be in the following range:

Table 3.6: Supply Voltage Corners

Parameter	MIN	TYP	MAX
Supply Voltage (V)	1.62	1.8	1.98

3.3.3 Operating Temperature

The operating temperature variation is also an environmental variation that the IC might be exposed, it could be either by different ambient temperatures in certain industries and also by different levels of power dissipation that causes the temperature to rise [25]. According to the referred paper, as the temperature increases, drain current of MOS transistors decreases. In order to support a wide range of applications, the operating temperature variation corners are set as shown in Table 3.7.

Table 3.7: Temperature Corners

Parameter	MIN	TYP	MAX
Temperature (°C)	-40	25	125

In order to analyse a circuit in detail for a specific setup and application, before getting into the layout design and fabrication stages, PVT corner simulations are done by crossing all of these parameters variations.

3.3.4 Monte Carlo Analysis

As illustrated in Figure 3.10, upon simulating all the most extreme PVT corners, the Monte Carlo statistical model is used to evaluate the impact of these corner variations. This Analysis creates a random variation, based on the worst corner simulated in PVT, in the model intrinsic parameters in a way that it will skew it's behaviour into a more realistic device. This type of simulation usually follows a Gaussian deviation with a target sigma defined by the designer to fulfil a specific yield, expecting that the results will follow the same distribution trend. The results collected from all the scenarios describe the effect of variation on the system, through histogram plots or Q-Q plots, that then allows for an estimation of the fabrication yield of the design [25].

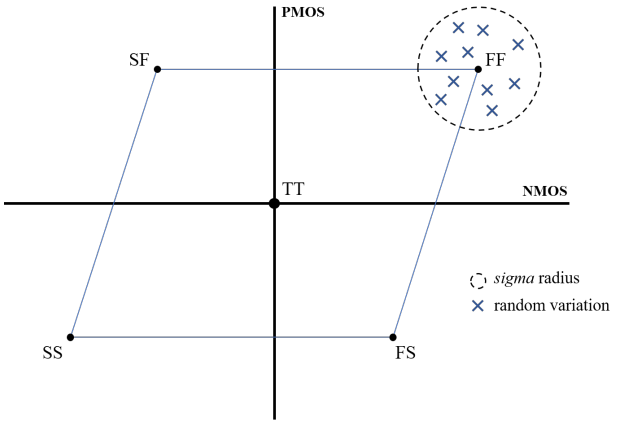


Figure 3.10: Monte Carlo Analysis' set up illustration

3.4 Summary

A preliminary implementation of a capacitor-less LDO voltage regulator was made to measure its initial performance and later on, compare with the performance of a fast loop transient compensation scheme implemented in the capless LDO voltage regulator.

Frequency compensation has a big role in a capacitor-less LDO voltage regulator to maintain stability of the system and provide a good load regulation. The Miller capacitance between the stages of the error amplifier, sets the dominant pole at low frequencies so that the stability of the LDO voltage regulator is not load dependent. The maximum load current required determines the width of the pass transistor that might result in a high gate capacitance and bring the pole at the gate of the pass transistor to lower frequencies. For the proposed capacitor-less LDO voltage regulator, the gate capacitor connected to the ground is around 500f F, calculated using the same Miller effect applied to $C_{gd_{PT}}$, which does not impact the dominant pole. However, if a higher specified maximum load current value and $C_{g_{PT}}$ starts to move its pole closer to the dominant pole, the pole-splitting is put at risk and the phase margin decreases, affecting the stability of the capacitor-less LDO voltage regulator.

The system's characterisation lays out the most relevant performance parameters of a LDO voltage regulator, with details on, simulating PVT corner variations and performing a Monte Carlo analysis. The simulation results of the proposed capacitor-less LDO voltage regulator, based of the system's characterisation, are shown in the figures below below, compiling the specifications of some performance data in Table 3.8.

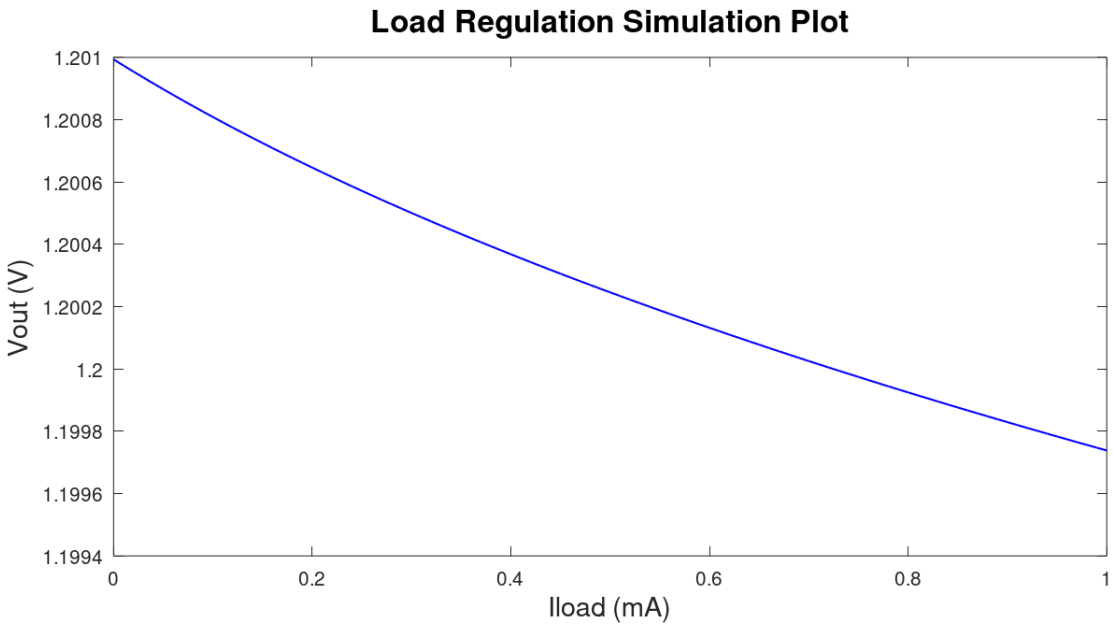


Figure 3.11: Load Regulation simulation results for V_{in}=1.8V and C_L=0 F

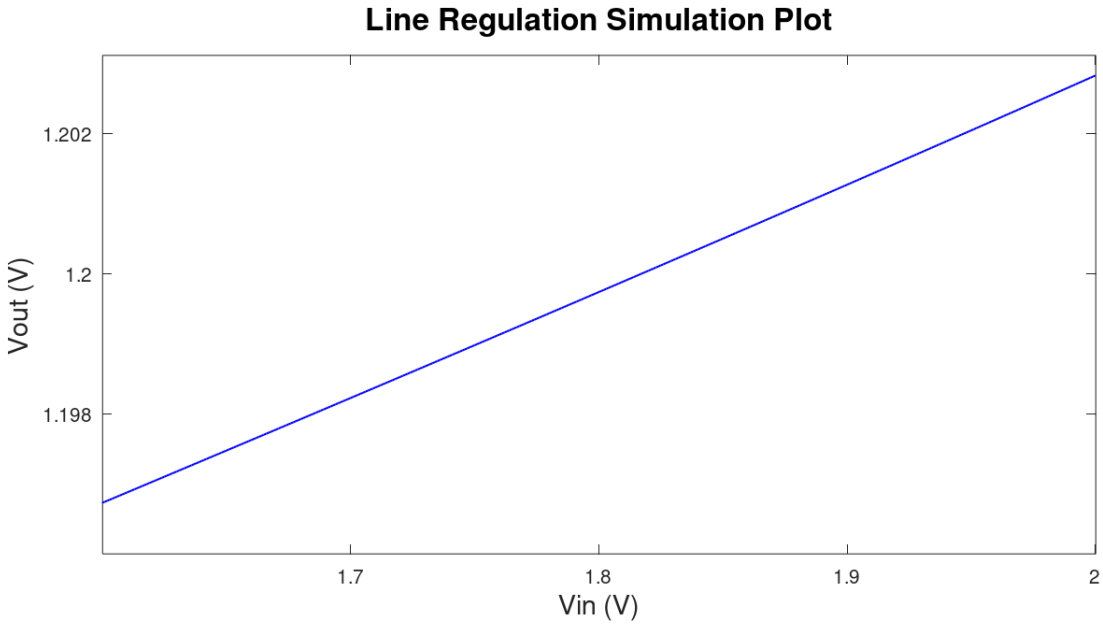


Figure 3.12: Line Regulation simulation results for I_L=1mA and C_L=0 F

The load transient simulation was performed with a load current step of 1mA with a t_{rise} and t_{fall} of 1ns.

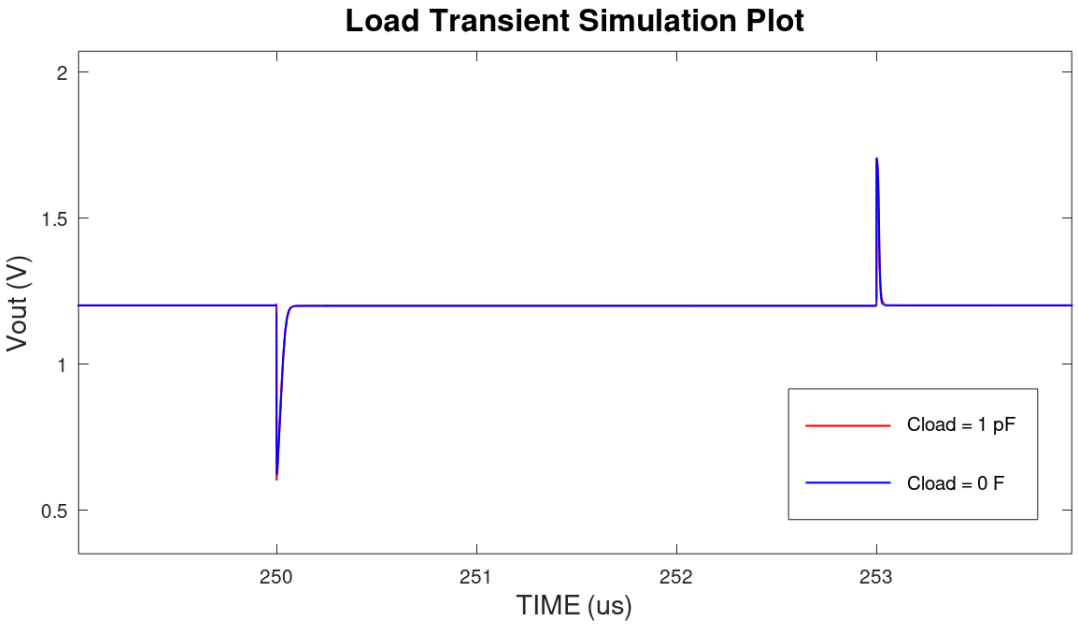


Figure 3.13: Load transient simulation results for I_L=1mA with C_L=0, 1 pF

The line transient simulation was performed with an input supply step from 1.8V to 2V, with a t_{rise} and t_{fall} of 1ns.

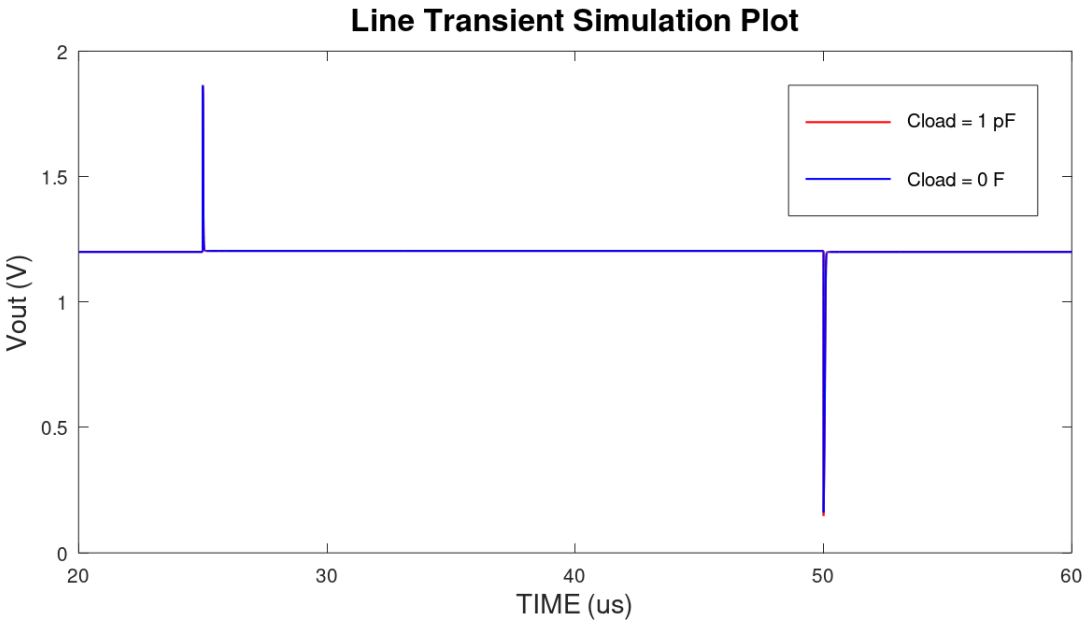


Figure 3.14: Line transient simulation results for I_L=1mA with C_L=0, 1 pF

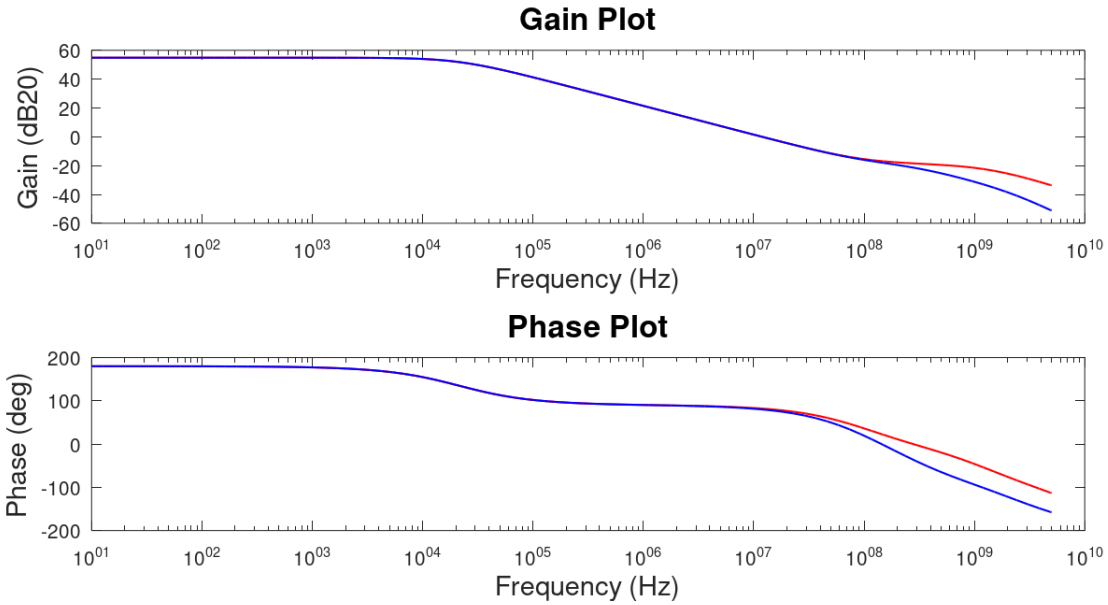


Figure 3.15: AC simulation results for I_L=0mA with C_L=0, 1pF

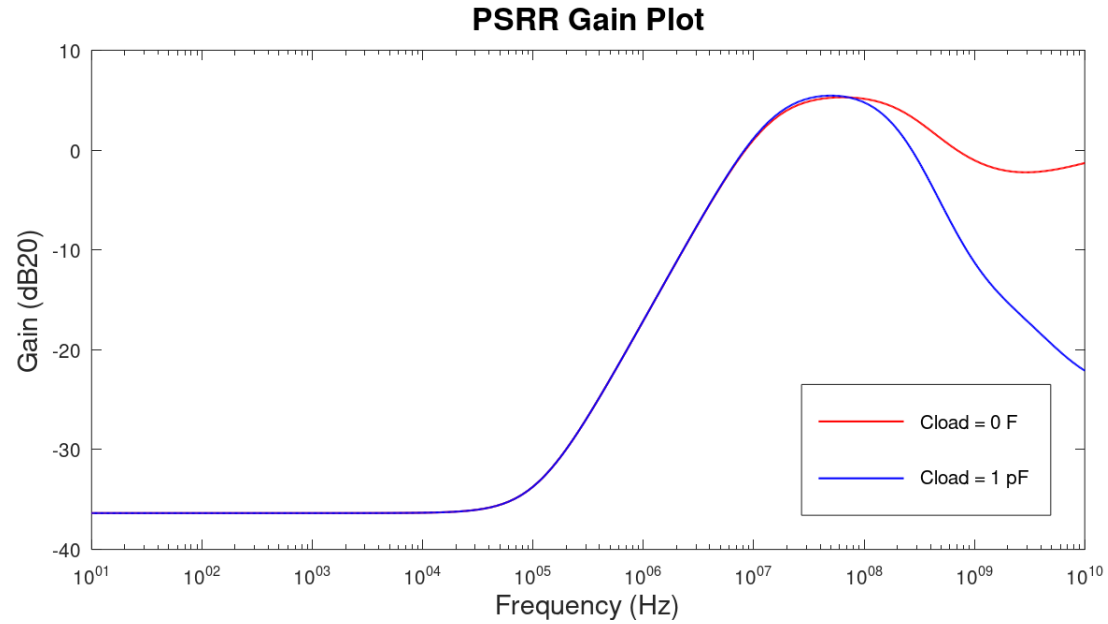


Figure 3.16: PSRR simulation results for I_L=0mA with C_L=0, 1pF

Table 3.8: Capacitor-less LDO Voltage Regulator Specifications

Parameter	Value
Technology	28nm
V_{supply}	1.8V $\pm$10%
V_{out}	1.2V
V_{DO}	0.28V
$I_{L_{max}}$	1mA
Loop DC Gain	55.3dB
Phase Margin (C_L=1pF)	71°
$\Delta V_{out_{MAX}}$	1.2V
PSRR (C_L=1pF)	-35.9dB @1kHz
	-17.1dB @1MHz
	-15.1dB @1GHz
I_Q	600μA
LR_{load}	1.3mV/mA

Chapter 4

Fast Loop Design

In this chapter the state-of-the-art architectures, studied previously, are implemented in the proposed LDO voltage regulator in order to further explore their performance in an environment setup that offers a more objective comparison between each other. Upon choosing the most optimal architecture of the goals specified for this work, it is analysed in detail to make further improvements. Next up, a startup circuit for the fast loop is introduced as well as a variable feedback network capable of providing different output voltages to regulate. A sizing methodology scheme is presented to show how the transistor dimensions were selected for each design.

4.1 Sizing Flow

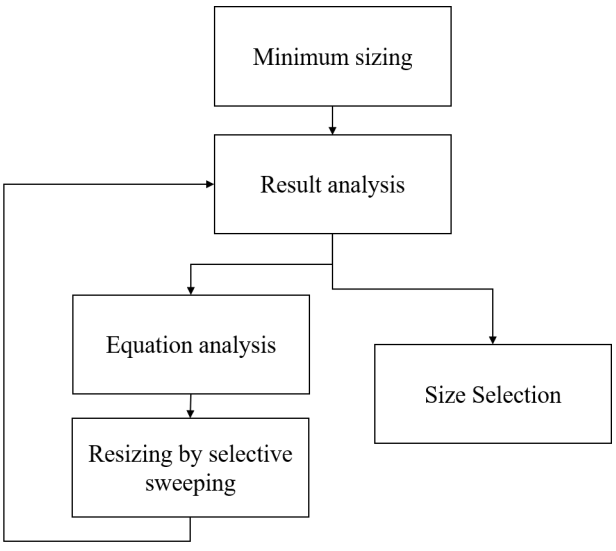


Figure 4.1: Sizing flow used to select components' dimensions of the circuit at hand

The sizing flow presented in figure 4.1 shows the methodology used to select transistor sizing and other components parameters. When implementing and assessing a certain architecture or circuit, first it is simulated with minimal sizing followed by the analysis of the respective results.

If the results do not satisfy firstly good operating point conditions and then, further requirements and specifications such as stability and load transient performance, the circuit and its equations are analysed in detailed in order to perform a localised and selective parametric sweep among components. After doing a resize of the components the results are analysed once again, repeating this method until the results satisfy the target specifications.

4.2 Literature Assessment

As each reviewed state-of-the-art architecture is design over different CMOS process technologies and every one of them integrates error amplifiers with different characteristics and specifications, the comparison made in the previous chapter becomes subjective to the principles used and concepts applied. Given the proposed EA and LDO voltage regulator design, for a more accurate comparison between these state of the art configurations, the concept of each one of them was applied to the proposed capacitor less LDO to objectively analyse the effects and results for the given integrated architectures in order to satisfy the desired specifications. Only load transient simulations were done in their implementations as the achievement of minimal values of overshoots and undershoots are the main purpose of the proposed LDO voltage regulator.

4.2.1 Overshoot/Undershoot Detection Circuit

The architecture presented in [27] showed an intuitive way to compensate the low bandwidth of the main loop formed by the error amplifier, in case of very fast transient load current step variations that this last one is not able to detect. Having in mind a typical low pass filter gain bode plot, in order to reach a broad range of bandwidth in the frequency spectrum, the compensation goes through the implementation of a high band-pass filter achieving a complementary behaviour on stability which. The high band-pass filter has to be implemented in the right frequency range so that its bandwidth does not detect general noise frequency values.

The high band-pass filter in the fast loop is achieved through a capacitor in series, that creates a zero in the frequency response, followed by a current mirror that imposes a pole through the intrinsic capacitance of transistor M_5. This configuration allows the LDO voltage regulator to react faster to load current step variations.

In figure 4.2, taken from [27] for analysis, is an overshoot detection circuit with a more illustrative understanding of its behaviour that was already explained in the previous chapter.

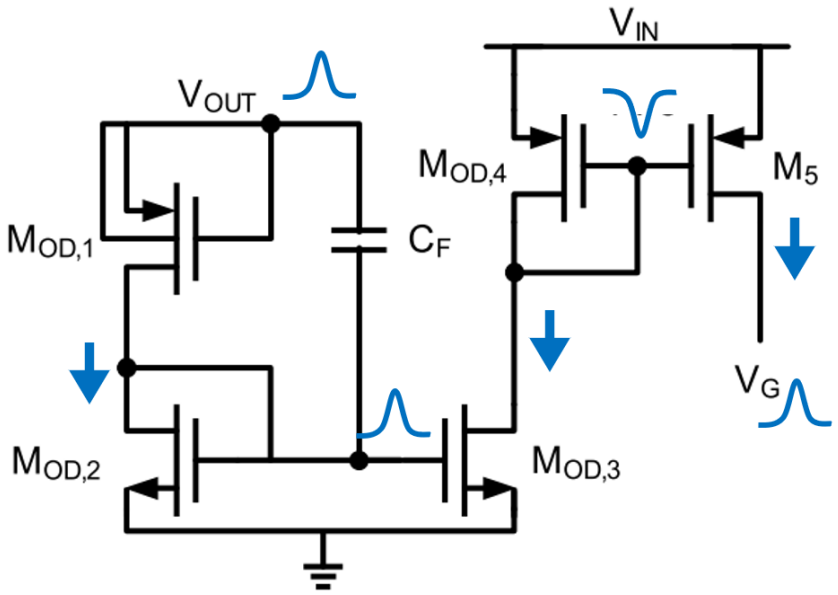


Figure 4.2: Robust Overshoot Detection Circuit, adapted from [27]

Based on this analysis, it was possible to recreate the concept for an undershoot detection circuit, UDC, presented in figure 4.3 where, from the same perspective, the capacitor C_U detects a low-to-high current step through an undershoot. This output voltage reduction will put the PMOS transistor M_9 in saturation, providing a current flow to the current mirror of M_{10} and M_{11} in which, that same current is amplified in order to pull down the node V_G and discharge the gate of the pass transistor. This action will put the pass transistor also in saturation mode, enabling its drain current to flow to the output node and regulate V_{out} back to the desired value.

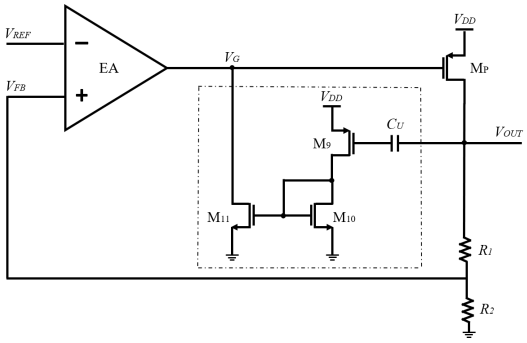


Figure 4.3: Undershoot Detection Circuit

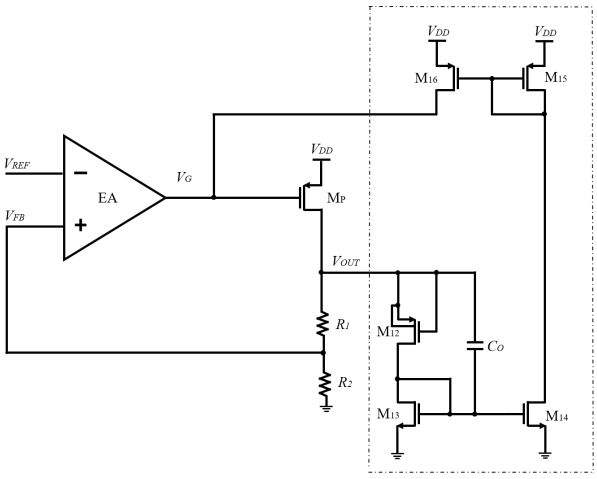


Figure 4.4: Overshoot Detection Circuit

The selected component sizes were the following:

Table 4.1: Transistor sizing for UDC implemented in the proposed LDO

	M_9 (hv)	M_{10} (lvt)	M_{11} (lvt)
W ($\cdot 1\frac{}{W_{min}}$)	1	1	15
L ($\cdot 1\frac{}{L_{min}}$)	10	10	10

Table 4.2: Transistor sizing for ODC implemented in the proposed LDO

	M_{12} (lvt)	M_{13} (lvt)	M_{14} (lvt)	M_{15} (hv)	M_{16} (hv)
W ($\cdot 1\frac{}{W_{min}}$)	1	1	5	1	15
L ($\cdot 1\frac{}{L_{min}}$)	1	1	1	2	2

Table 4.3: Capacitor parameters for UDC and ODC implemented in the proposed LDO

Component	Parameter
C_U	500 fF
C_O	500 fF

The next set of figures, show the simulation results of the load transient response for the UDC and ODC implemented in the proposed LDO voltage regulator. First the UDC and the ODC are simulated individually to see the effects of each one in the response of the LDO, then, in figure 4.7, the simulation results show the implementation of both in the same circuit to analyse how they compensate and complete each other in a maximum load current step transient response with a t_{rise} and t_{fall} of 1ns.

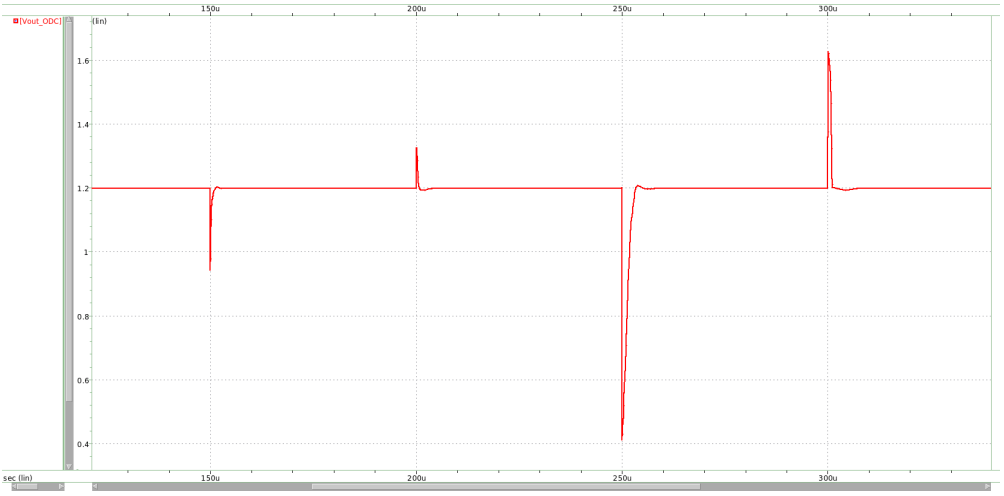


Figure 4.5: Load transient simulation of the ODC

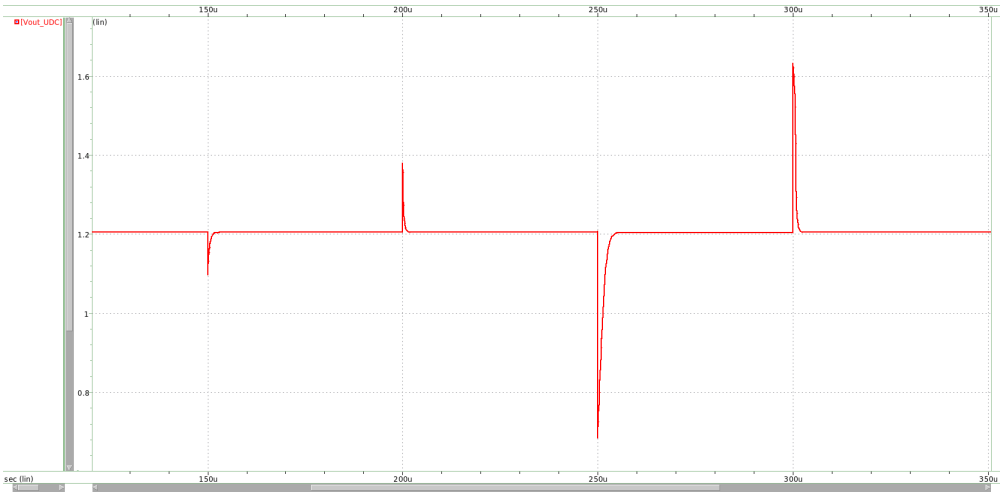


Figure 4.6: Load transient simulation of the UDC

Figure 4.7: Load transient simulation of the Full Spike Detection Circuit

4.2.2 Fast and Slow Loop Architecture

The fast differential stage presented in [10] has a noticeable dependency on the slow loop of the error amplifier which, at a certain point, limits the slew-rate enhancement provided by the fast loop at the get of the pass transistor. This dependency makes it more difficult to isolate either loops from each other in order to analyse the frequency response of the fast loop.

Nevertheless, the circuit behaviour analysis was made in the same way of the ones done for other architectures. Following the implementation done in [10], the feedback network needs to be connected to the negative input terminal of the error amplifier as the fast differential loop presents a signal inversion at the gate of pass transistor from the output of the error amplifier. As it is shown in Figure 4.8, his inverting stage allows the error amplifier to increase the voltage at the gate of Q_3 and Q_2 whenever there is an undershoot at the output of the LDO voltage regulator, making both

transistor enter in cut-off region. At the same time, a decrease of the feedback voltage also puts transistor Q_4 in the cut-off region. Since transistor Q_6 acts as a current source its drain current is constant which means that, when Q_4 is not conducting, the majority of Q_6's drain current will be flowing through transistor Q_5, pulling down the node V_G and discharging the PMOS pass transistor in order to provide current to the output and compensate for the low-to-high current load step.

In case of an overshoot in the output voltage, the analysis of the fast loop becomes less clear as the transistors Q_3 and Q_5 clash with each other in order to control the voltage at the node V_G. In the event of a high-to-low current load step, the voltage seen at the output of the error amplifier decreases, making Q_3 and Q_2 conduct. At the same time, an overshoot at V_{out} also makes Q_4 to conduct. In this case, transistors Q_4 and Q_5 are now both draining current, so the node V_G is getting pulled-up and pulled-down at the same time. However, in relation to steady state conditions, as transistor Q_6 acts as a current source, its drain current is constant which means that, the current flowing through transistor Q_5 will be less than when the fast loop is working in steady state, i.e. when V_{FB} is equal to V_{ref}. At this operating point, the drain terminal of transistor Q_5 is set with a higher voltage value at the same time that transistor Q_3 charges up the same node, V_G. This response towards overshoots requires the fast loop to have a well calibrated operating point in order to properly charge the gate of the PMOS pass transistor so it enters in the cut-off region and the overshoot at V_{out} is compensated.

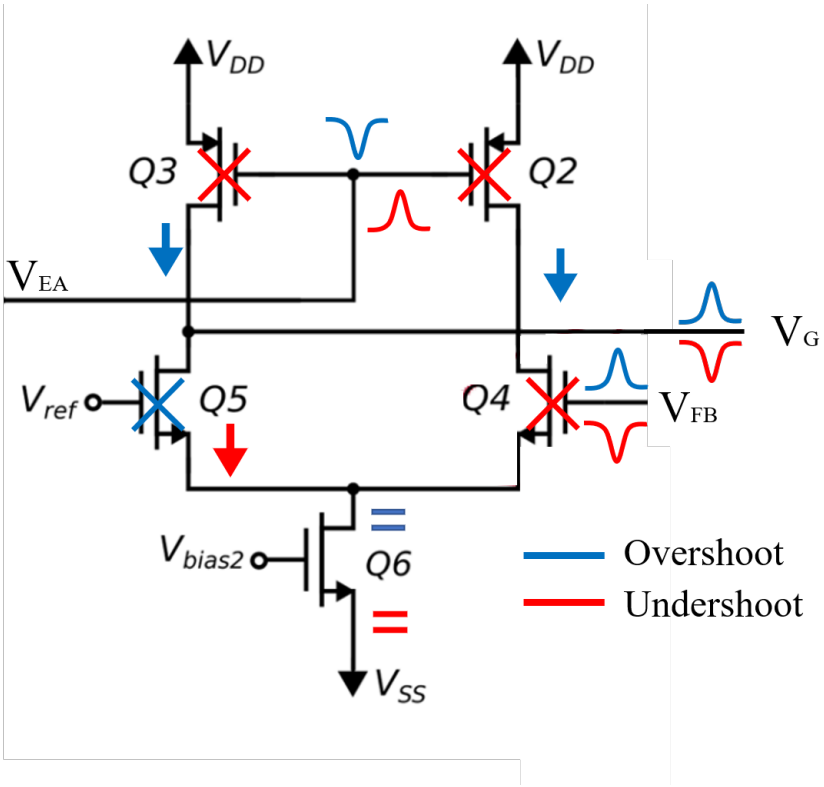


Figure 4.8: Fast loop configuration and analysis of the LDO proposed in [10]

Figure 4.9 shows the implementation of the fast differential stage in the proposed LDO voltage regulated, which didn't suffered any changes from the initial architecture of the paper.

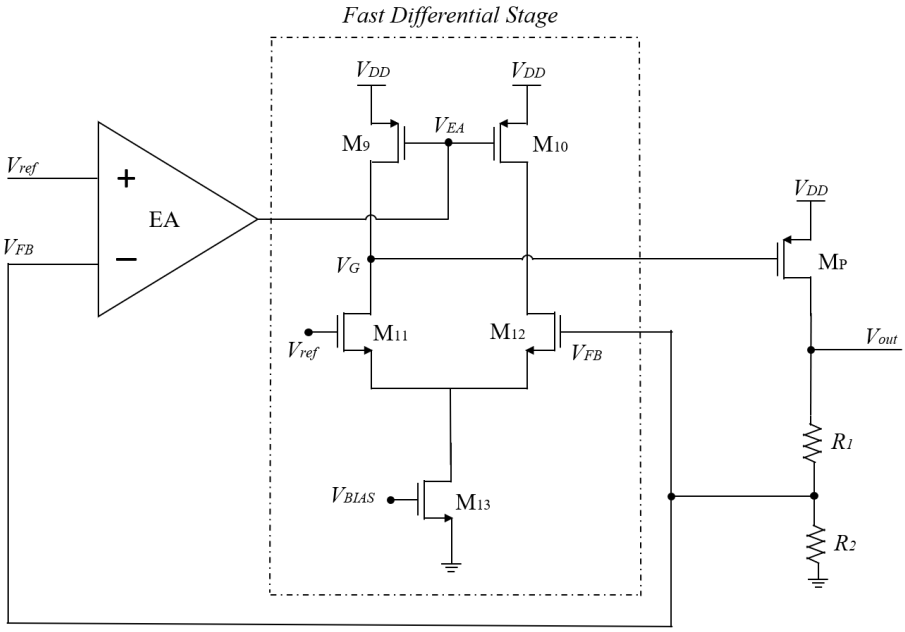


Figure 4.9: Fast Differential Stage implemented in the proposed LDO

Following the sizing approach of [10], where the transistor pairs in the differential stage have the same size ratio, the sizing results obtained with parametric sweeps through computer simulations are presented in table 4.10

Table 4.4: Transistor sizing of the fast differential stage implemented in the proposed LDO

	M_9 (hv)	M_{10} (hv)	M_{11} (lvt)	M_{12} (lvt)	M_{13} (lvt)
W ($\cdot 1\frac{}{W_{min}}$)	5	5	20	20	6
L ($\cdot 1\frac{}{L_{min}}$)	1	1	1	1	1
Multiplicity	1	1	1	1	1

The load transient result of the implemented architecture, for a load current step of 100μA and 1mA with a t_{rise} and t_{fall} equal to 1ns, simulated in the proposed LDO is presented in Figure 4.10.

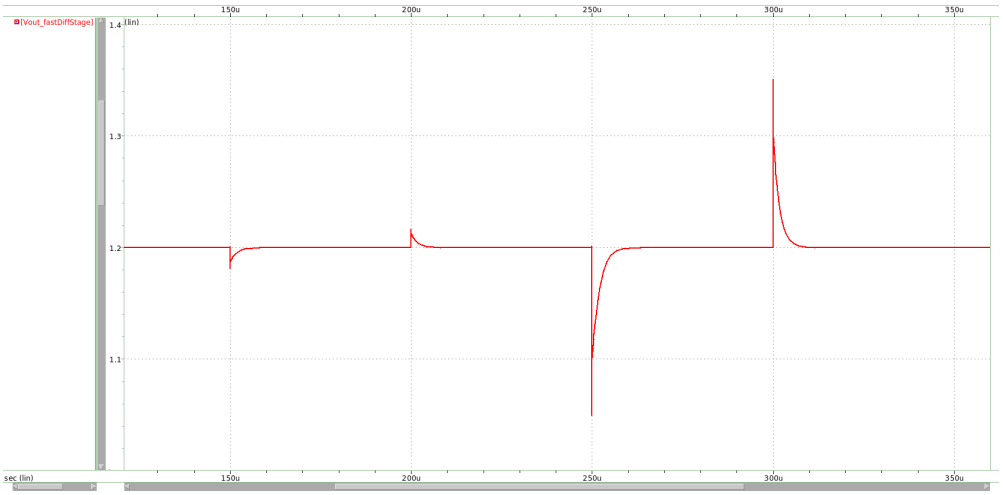


Figure 4.10: Load transient simulation of the Fast Differential Stage

4.2.3 Transient Enhancement Circuit based on a Differentiator

The C_F is used to produce a Miller compensation scheme by executing a separation of the primary and secondary frequency poles and thus, ensure the stability of the system. This capacitor is also able to detect overshoots and undershoots whenever there is a high-to-low or low-to-high load current step, respectively [26]. The spikes detected are then amplified by the current amplifier, as illustrated in Figure 4.11, to charge or discharge the pass transistor depending on the desired response behaviour. For an overshoot scenario the current amplifier behaves as follows, once capacitor C_3 detects the spike, it will charge the gate of M_{18}, which is biased by the current source I_B. Depending on the ratio of the current mirror, transistor M_{18} will pull a large amount of dynamic current at the gate of M_{21}, discharging it, and therefore turning on the transistor, leading to a voltage increase at the gate of the pass device, V_G. At the same time, an overshoot lets transistor M_{15} fully discharge the gate of the NMOS transistor M_{22}, so that it enters in cut-off region, and is able to only pull leakage current from the node V_G. The response of the circuit for an undershoots is the complement of the last one, illustrated in red in Figure 4.11.

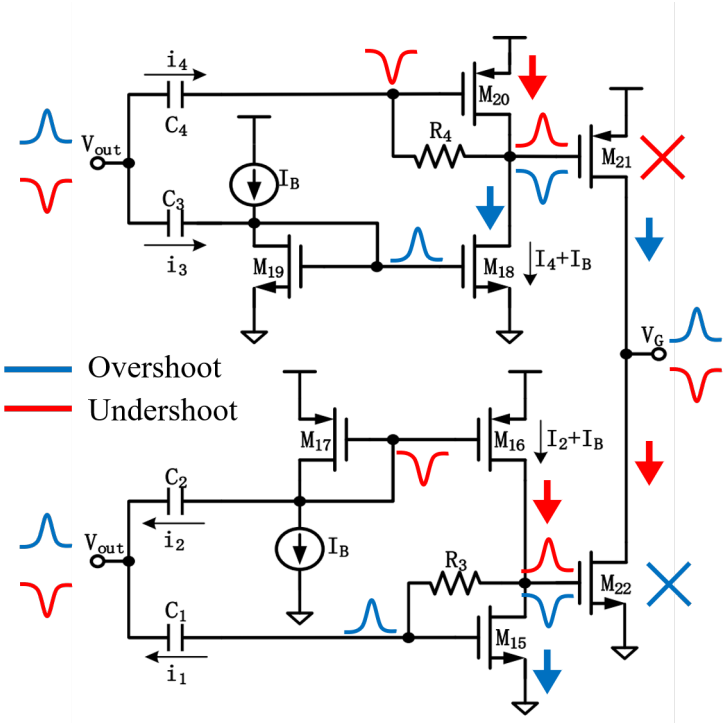


Figure 4.11: Class AB transient enhancement circuit based on a differentiator, adapted from [26]

The differentiator implemented, based in [26], is shown in Figure 4.12.

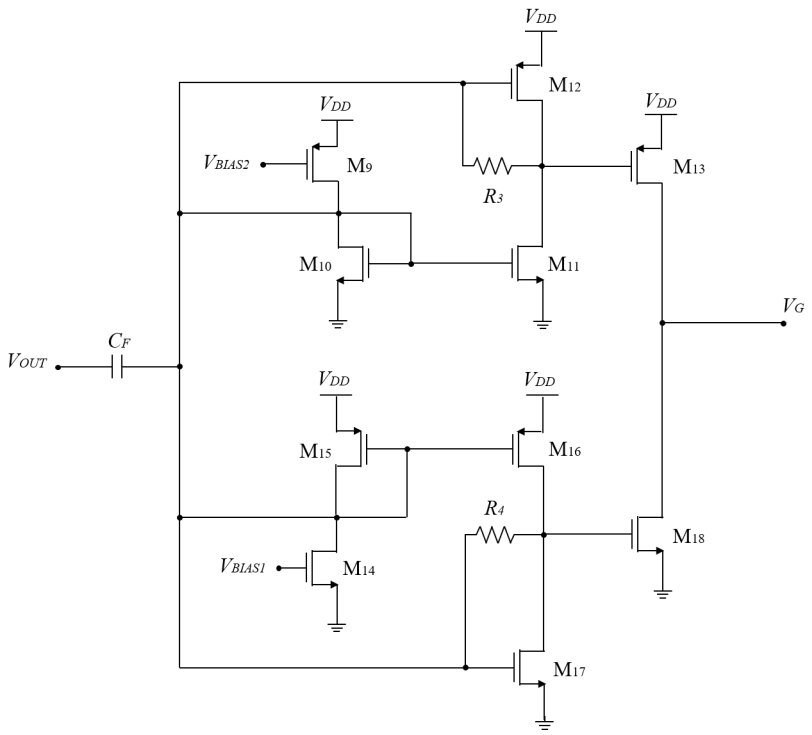


Figure 4.12: Fast Loop based on a Differentiator

The selected component sizes were the following:

Table 4.5: Transistor sizing of the differentiatior's overshoot path implemented in the proposed LDO

	M_9 (hv)	M_{10} (hv)	M_{11} (hv)	M_{12} (hv)	M_{13} (hv)
W ($\cdot 1\frac{}{W_{min}}$)	1	1	5	1	5
L ($\cdot 1\frac{}{L_{min}}$)	2	2	2	2	2

Table 4.6: Transistor sizing of the differentiatior's undershoot path implemented in the proposed LDO

	M_{14} (hv)	M_{15} (hv)	M_{16} (hv)	M_{17} (hv)	M_{18} (hv)
W ($\cdot 1\frac{}{W_{min}}$)	5	1	5	9	10
L ($\cdot 1\frac{}{L_{min}}$)	2	2	2	2	2

Table 4.7: Capacitor and resistors' sizing of the differentiatior implemented in the proposed LDO

Component	Parameter
C_F	10 fF
R_3	1 $k\Omega$
R_4	1 $k\Omega$

The load transient results of the implemented architecture, for a load current step of 100μA and 1mA with a t_{rise} and t_{fall} equal to 1ns, simulated in the proposed LDO is presented in Figure 4.13.

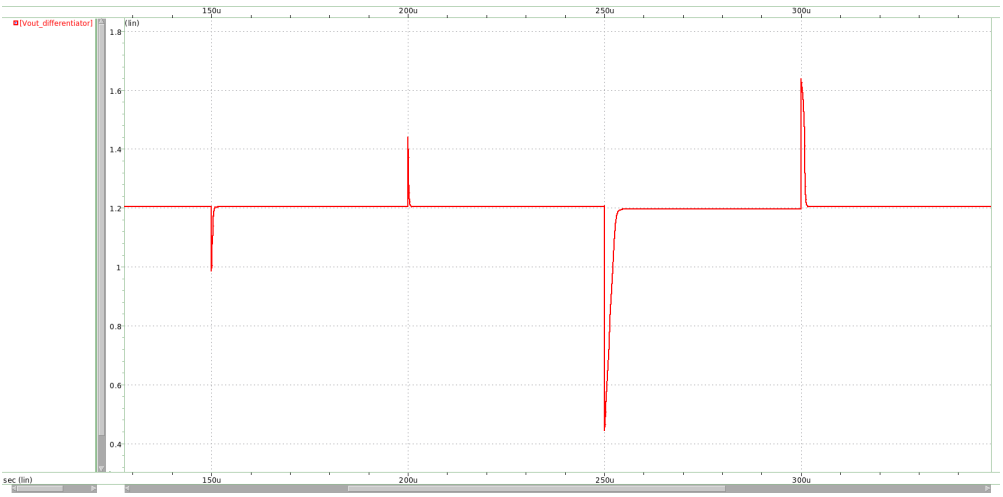


Figure 4.13: Load transient simulation of the differentiator

4.2.4 Common Drain Fast Loop

The configuration implemented in [28] is similar to the one presented in [10] but, with a common source configuration. This architecture offers more simplicity due to the lower number of transistors used in the fast loop [28]. However, the configuration used by Deleuran *et al.* is designed to generate a signal inversion in the presented common source stage that will drive the NMOS pass transistor properly.

The use of this inversion stage in a LDO voltage configuration with a PMOS pass transistor would not be compensating the transient variations applied to the system. So, the fast loop configuration implemented in [28] was redesigned in order to provide an amplifying stage without any signal inversion, while still following the concept introduced. Figure 4.14 shows the redesigned common source stage for the fast loop where, in case of an overshoot transistor M_{10} is cut-off by the feedback voltage while transistor M_9 pulls up the voltage at the gate of the PMOS pass transistor, V_G, allowing it to compensate the detected overshoot. In case of an undershoot, the transistor M_{10} pulls the node V_G down, while M_9 is in cut-off region, allowing the M_P to flow current through its drain and compensate the undershoot.

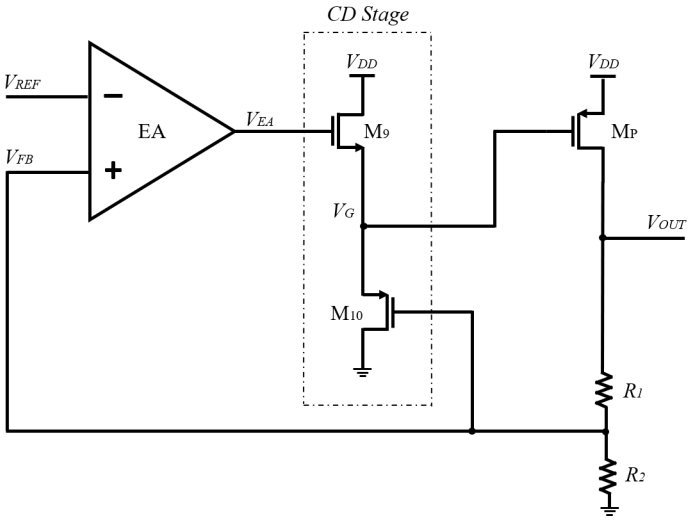


Figure 4.14: Common Source Fast Loop Stage

Upon performing a parametric sweep, the selected sizes for the assessed configuration are presented in Table 4.8.

Table 4.8: Transistor dimensions of the implemented CS stage

	M_9 (hv)	M_{10} (lvt)
W ($\cdot 1\frac{}{W_{min}}$)	1	1
L ($\cdot 1\frac{}{L_{min}}$)	2	1
Multiplicity	30	10

The load transient results of the implemented architecture, for a load current step of 100μA and 1mA with a t_{rise} and t_{fall} equal to 1ns, simulated in the proposed LDO is presented in Figure

4.15.

Figure 4.15: Load transient simulation of the Common source fast loop

4.2.5 Preliminary conclusions

On an initial implementation design level, the results given in Table 4.9 show that all state-of-the-art fast loop configurations are functional when implemented in the proposed capacitor-less LDO voltage regulator. However, assuming the followed sizing, the Fast Differential Stage configuration proved to have a better transient compensation over the transient enhancement circuit and the other architectures.

That being said, the fast differential stage architecture has been chosen to be further developed and implemented in the proposed system, given its preliminary results and its potential for optimisation.

Table 4.9: Specifications' comparison for the presented literature assessment

Parameters	ODC	Fast and Slow Loop	Transient Enhancement Circuit	CS Fast Loop
Overshoot (mV)	425.3	150.4	437.2	401.6
$T_{s_{overshoot}}$ (μs)	7	12	4	8.4
Undershoot (mV)	657.4	150.6	756.7	511.4
$T_{s_{undershoot}}$ (μs)	10.4	13	5	9.4

4.3 Design Modeling

Upon finishing preliminary implementations of the state-of-the-art architectures in the proposed LDO voltage regulator, the architecture based on the fast differential stage has shown to be the one with the most potential for reducing the overshoots and undershoots, under load transient variations, and also for possible improvements and optimisations.

The dependency of the fast loop from the error amplifier means that this sub-system has 2 inputs, one directly from the feedback network and the other one from the output of the error amplifier itself. The work developed in [ref paper] describes the transfer function of the fast loop as follows

$$TF_{FL}(s) = -g_{m_{11}} R_{outDiff} \frac{(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{pa}})(1+\frac{s}{\omega_{pb}})} \tag{4.1}$$

where ω_{pa} is the dominant pole of the fast loop, due to the large gate capacitance of the pass transistor, and it is located at the node V_G and, ω_{pb} is the second pole and is located at the node V_{EA} which connects to the gate of the transistors M_8 and M_9 [10]. The next set of equations show a simplified version of the values of the poles and the zero of the fast loop. This approximations are based on the relative influence of the components to each critical node, in regard to the desired analysis which, in this case, is the general open loop frequency response of the fast loop.

$$\omega_{pa} \approx \frac{1}{R_{outDiff} C_{gd_{PT}}} \tag{4.2}$$

$$\omega_{pb} \approx \frac{g_{m_9}}{C_G} \tag{4.3}$$

$$\omega_z \approx \frac{2g_{m_9}}{C_G} \tag{4.4}$$

So has it is seen from Equation 4.2 and 4.4, highlighting the fact that ω_z is inversely proportional to the numerator of the transfer function $TF_{FL}(s)$, decreasing the transconductance of the transistor M_9 makes the gain of the fast loop increase. This means that, decreasing the width of the transistor M_9 might have a potential increase on the gain of the fast loop and thus, improve the performance of the Fast Loop capless LDO voltage regulator.

The fact that the fast loop is so dependent on the slow loop, formed by the error amplifier, makes it very challenging to isolate the fast loop from the slow loop and thus, analyse its contribution through the compensation in frequency and transient response. Figure 4.16 shows the block diagram of the system, to better illustrate the dynamics of the system between its component blocks.

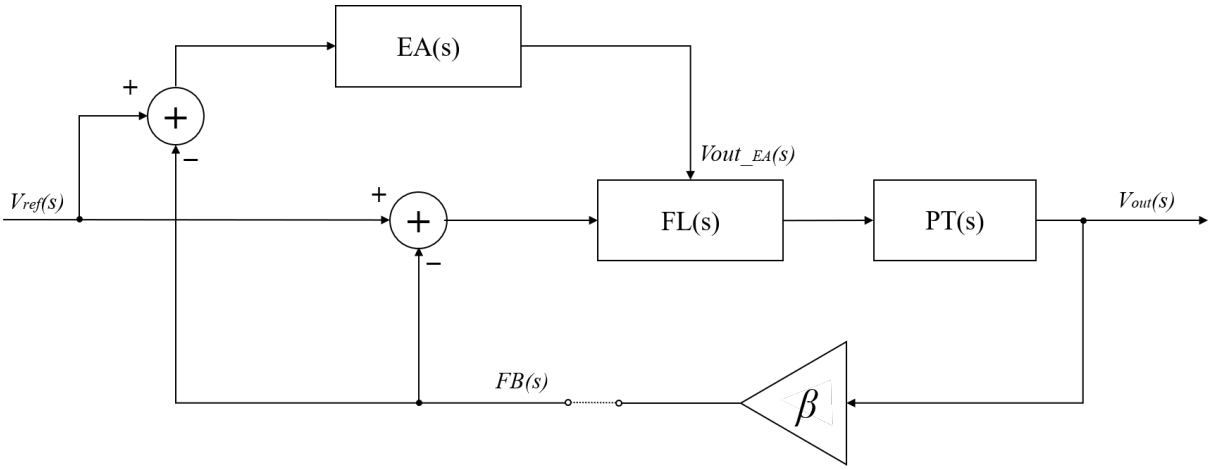


Figure 4.16: Block Diagram of the system proposed

As the block diagram suggests, the loop is opened at the output of the feedback factor's analog block in order to analyse the stability of the whole system regarding the two inputs of the fast loop, EA(s) and FB(s). To see how the fast loop compensates the frequency response of the slow loop for fast load transient variations, the two loops where isolated from one another. From the diagram presented in Figure 4.16, the output relation between $V_G(s)$ and the inputs coming from the EA and the feedback network is

$$V_{ref}(s) - FB(s) = V_{in}(s) \tag{4.5}$$

$$\frac{V_{out}(s)}{V_G(s)}) = PT(s) \tag{4.6}$$

$$\frac{Vout_{EA}(s)}{V_{in}(s)}) = EA(s) \tag{4.7}$$

$$\frac{V_G(s)}{V_{in}(s)}) = FL(Vout_{EA}(s), s) \tag{4.8}$$

The simulation setup implemented for the open loop frequency response analysis of each isolated loop is shown in figures 4.17 and 4.5. For the frequency response analysis of the slow loop, the feedback input of the fast loop was cancelled by generating an ideal voltage value of 0.6V without any AC properties and, the frequency response of the fast loop was obtained by replacing the EA with an ideal unity gain amplifier in order to cancel the impact of the EA input in the fast loop.

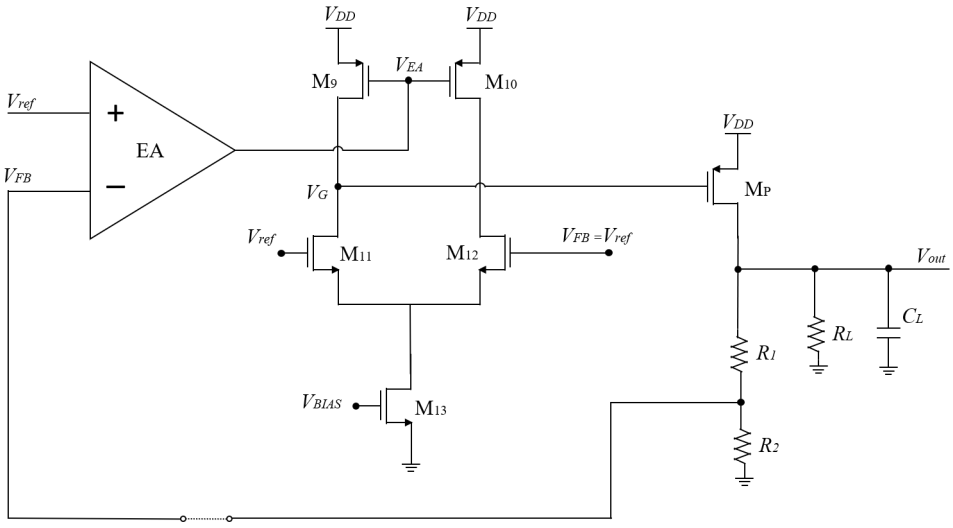


Figure 4.17: Simulation setup for the open loop frequency response analysis of the slow loop

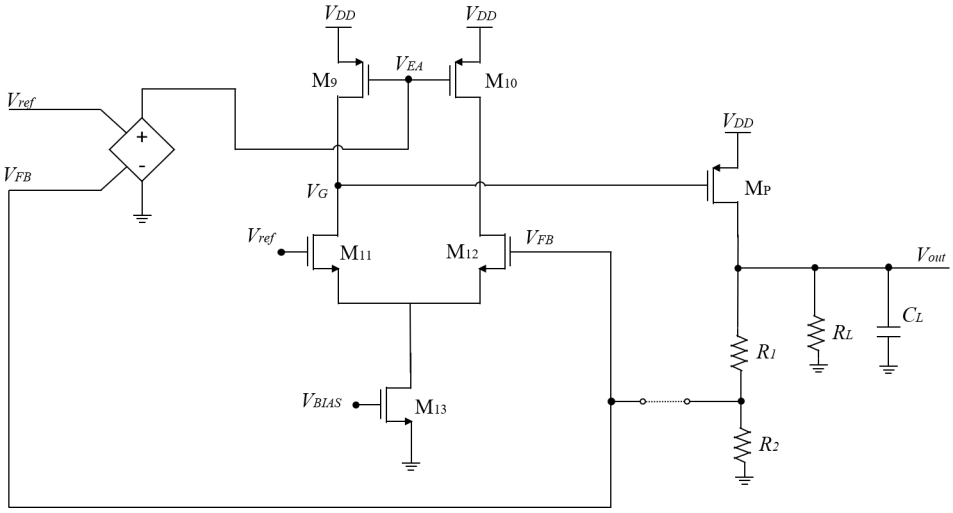


Figure 4.18: Simulation setup for the open loop frequency response analysis of the fast loop

The simulation results of the open loop frequency response of each isolated loop are presented in the following figures. The presented simulations were done with C_L= 0 F so the results to be analysed are not affected by the load capacitance. The simulations were set up also for a load current of 1 mA to see how the system behaves towards its maximum current conditions.

The first simulation, in Figure 4.19, shows the frequency response of the slow and fast loops for the sizing presented in subsection 4.2.2. Already from this results, it is clear how the fast loop is able to compensate the bandwidth of the slow loop.

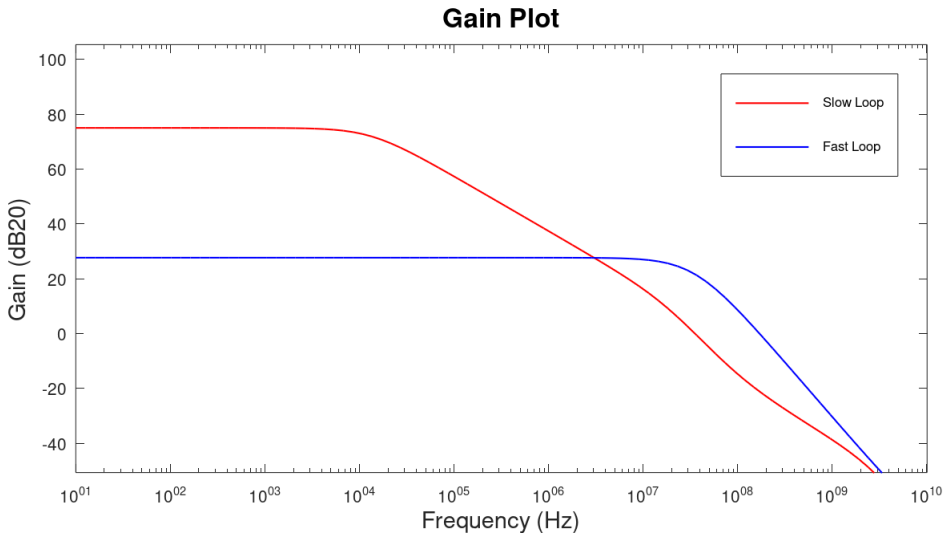


Figure 4.19: Stability simulation results of the Slow Loop and the Fast Loop for I_{load}=1mA with C_L=0 F

However, the phase margin captured from the fast loop frequency response showed a potential for improvement of the fast loop in general. For that matter, the width of the transistors of the fast loop was increased in a proportion of 20 so the fast loop is able to support bigger currents overall, flowing through its transistors. The increase of width in transistors make their intrinsic capacitances also to increase, generating a move down in frequency of the poles associated to the nodes of the transistors. As Figure 4.20 presents the AC simulation results for a width increase of 20 times showing, as expected, a decrease of bandwidth from the fast loop AC contribution. For the proposed LDO voltage regulator architecture, specifically the error amplifier, the fast loop ceases to compensate the bandwidth curve of the slow loop, ironically. However, according to the AC simulation results given by [10], the bandwidth of the fast loop is not being limited by the increase of the fast loop's transistors width but rather, it is the entire systems frequency compensation that is limited by the characteristics of the error amplifier.

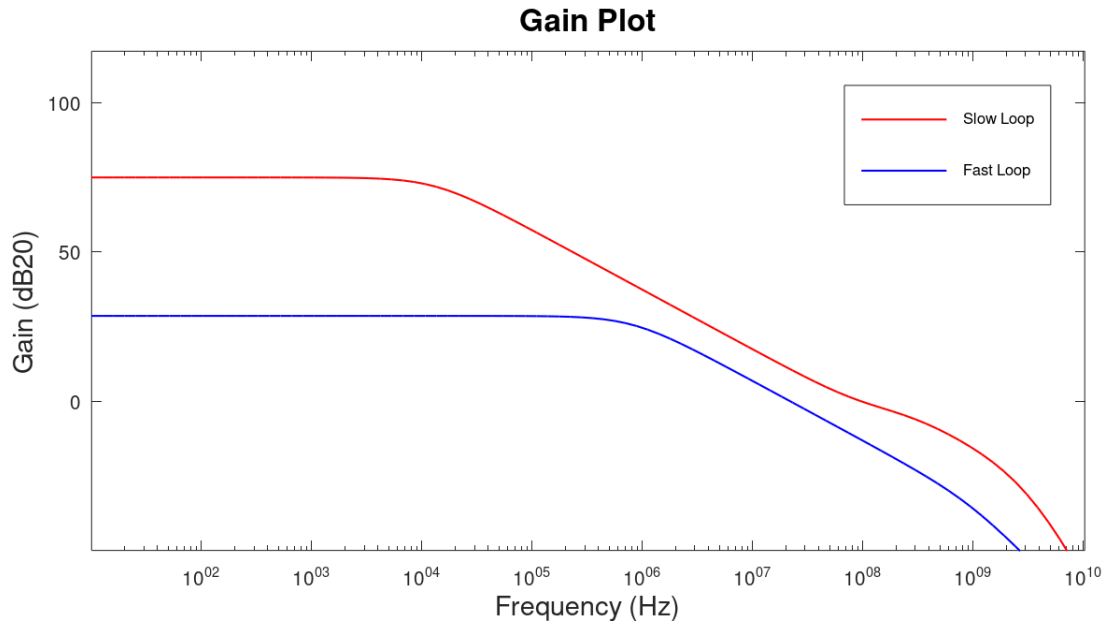


Figure 4.20: Stability simulation results of the Slow Loop and the Fast Loop for I_{load}=1mA with C_L=0 F

Upon performing a parametric sweep on the widths of the M_9 and M_{10} transistors pair, the best performance was extracted from a relative decrease of the size of the transistor M_9 towards transistor M_{10}. The overall width increase of the transistors allows more current to flow in the system and thus, the fast loop is able to compensate the transient variations even more. However, increasing overall width of the transistors also increases their parasitic gate capacitance, which slows down the circuit and makes the settling time to be longer. Doubling length of transistors M_9 and M_{10} makes them less sensitive to the power supply ripple that these transistors are directly connected to. The final sizing of the transistors of the fast loop is presented in table 4.10, with the AC simulation results being presented in Figure 4.21.

Table 4.10: Transistor sizing of the fast differential stage implemented in the proposed LDO

	M_9 (hv)	M_{10} (hv)	M_{11} (lvt)	M_{12} (lvt)	M_{13} (lvt)
W ($\cdot 1\frac{}{W_{min}}$)	5	20	20	20	6
L ($\cdot 1\frac{}{L_{min}}$)	2	2	1	1	1
Multiplicity	20	20	20	20	20

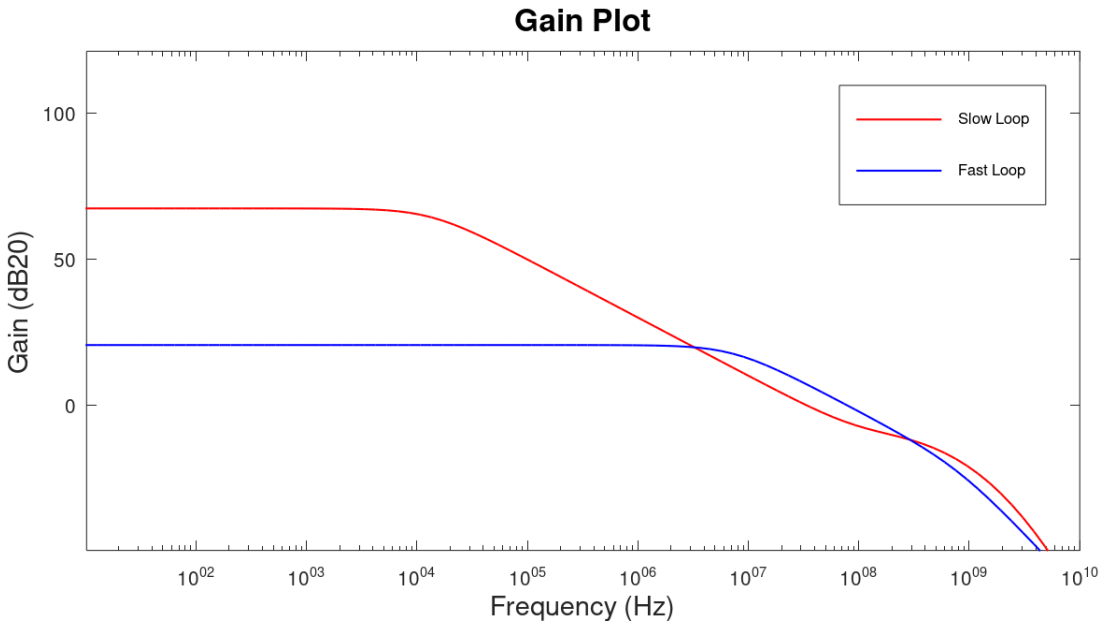


Figure 4.21: Stability simulation results of the Slow Loop and the Fast Loop for I_{load}=1mA with C_L=0 F

4.3.1 Biasing Circuits

Up to this point, the biasing of the transistors M_6, M_7 and M_{13} was provided with voltage polarisation by an independent voltage source, that defines the current flowing through the mentioned transistors based on the voltage value applied to their gate terminal. However, in PVT corner simulations, specially with variations in the voltage supply, the headroom of the transistors will change, as well as their operating point, and thus having a drain current very sensitive for these operating conditions, showing the example of the M_{13} biasing in Figure 4.22.

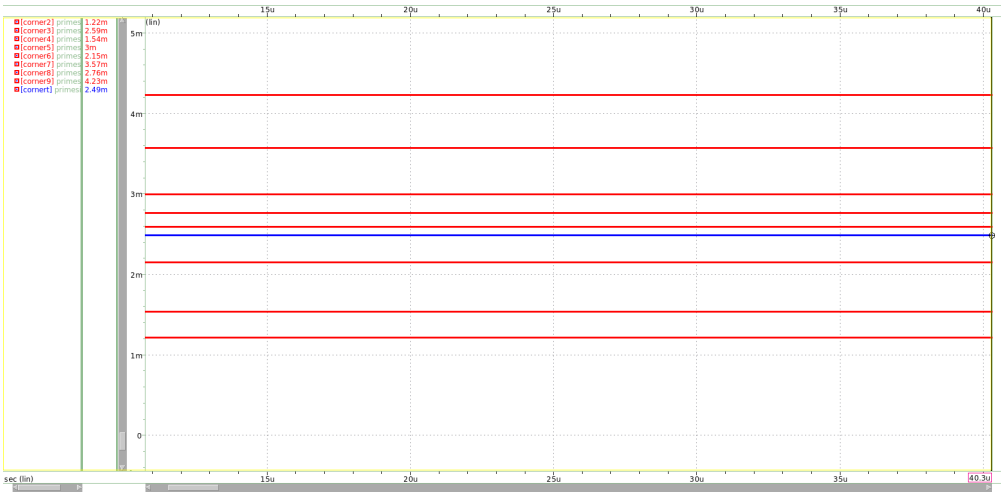
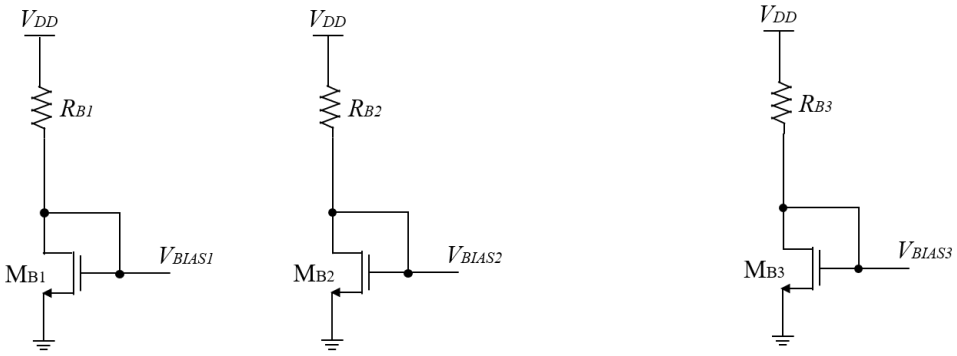


Figure 4.22: Current simulations under PVT corner variations when applying a bias voltage in M_{13}

In order to reduce these current variations, a bias circuit based on a current mirror configuration was applied to the gates of the transistors M_6, M_7 and M_{13}, as shown in Figure 4.23, where the value of the bias resistors and the size of the bias transistors are presented in tables 4.11 and 4.12.



a) Error Amplifier b) Fast Loop

Figure 4.23: Implemented Bias Circuits

Table 4.11: Resistor values of the presented bias circuits

Parameter	Value (Ω)
R_{B1}	40k
R_{B2}	100k
R_{B3}	355

Table 4.12: Transistor sizes of the presented bias circuits

Parameter	Width Proportion
M_{B1}	1_6
M_{B2}	$\frac{1}{70}7$
M_{B3}	1_{13}

The implementation of a current mirror to bias the transistors M_6, M_7 and M_{13} forces their drain current to be the same as the one defined by the transistor and resistor of the bias circuit. With this biasing configuration, further current variations will now be triggered mainly by variations in the process and temperature of the transistors that inevitably change the device characteristics. The simulation results of the current variations, applied in the same example, with the transistor M_{13} is biased through the proposed current mirror configuration, are shown in Figure 4.24.

The current variations presented in Figure 4.24 could be even less significant, in the example showed, by increasing the value of the bias resistor R_{B3}, that would make it less sensible to voltage variations that supply the bias circuit of M_{13}.

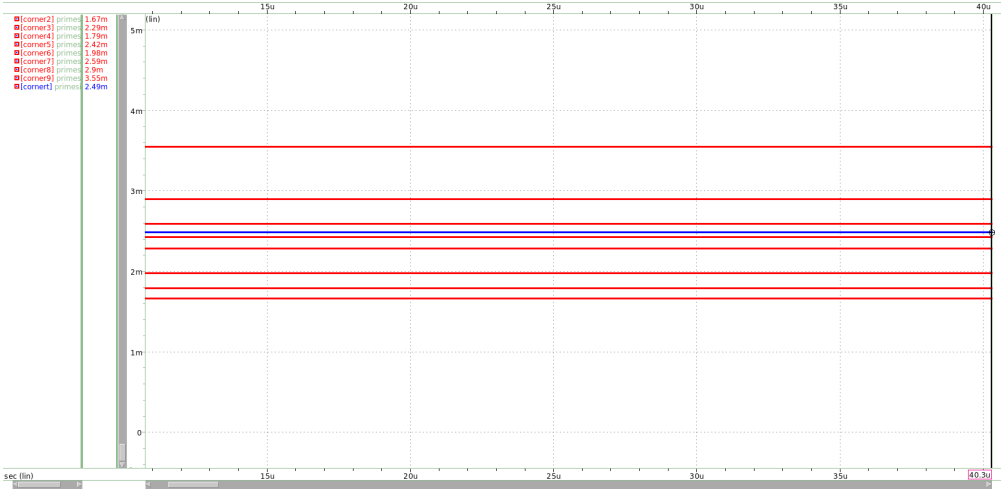


Figure 4.24: Current simulations under PVT corner variations when biasing transistor M_{13} through a current mirror

4.4 Variable Output

The proposed LDO voltage regulator is set to regulate an output voltage of 1.2V. However, an adaptable voltage divider configuration implemented in the feedback network allows the LDO to regulate different output voltage values. The developed configuration is presented in Figure 4.25, using a combinational set of resistors in series with NMOS transistors controlled by input voltage sources, V_{swi}, in order to function as analog switches.

The implemented configuration is combinational to allow for a wider range of possible output voltage values, as well as to reduce leakage through the transistors as much as possible.

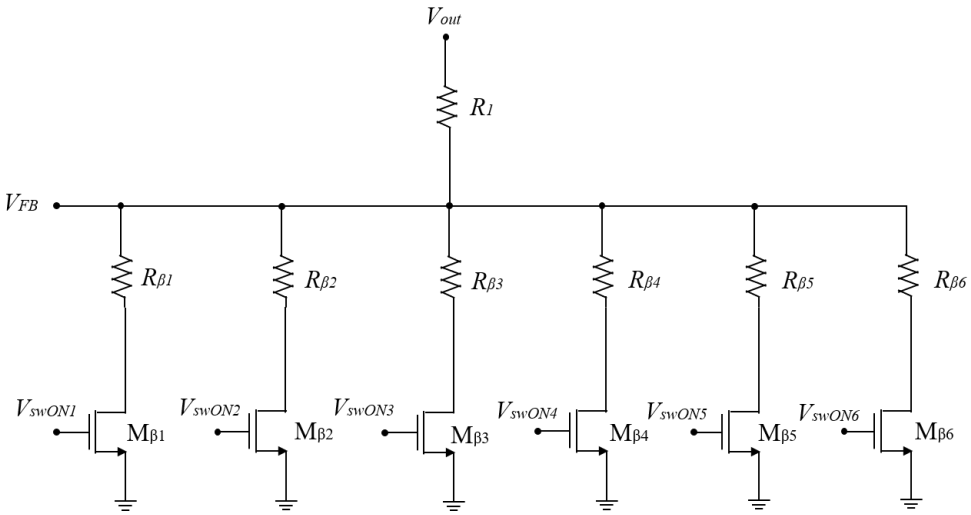


Figure 4.25: Adaptable β

The approach towards this implementation of a combinational feedback factor started based on the voltage divider method, where

$$V_{FB} = \frac{R_{\beta eq}}{R_1 + R_{\beta eq}} V_{out} \tag{4.9}$$

As the feedback voltage has to be equal V_{ref} in steady state, V_{FB} = 0.6 V and, R_1 remains 1k Ohms, the previous equation leads to the following expression

$$V_{out_{new}} = \frac{600}{R_{\beta eq}} + 0.6 \tag{4.10}$$

To have an equal distribution of current through the β resistors and a linear combinational setup, all β resistors have the same value, meaning that the equivalent β resistor, $R_{\beta eq}$, is given by equation 4.11, where N_{Ron} is the number of β resistors active in the feedback network.

$$\frac{1}{R_{\beta eq}} = N_{Ron} \cdot \left(\frac{1}{R_{\beta i}} \right) \tag{4.11}$$

Due to the defined dropout voltage, the maximum output voltage available is the specified nominal output voltage value of 1.2 V meaning that, ultimately, $R_{\beta eq}$ has to be equal to 1k Ohms. So, the value of each β resistor is measured in relation to the total number of resistors used: $R_{\beta i} = N_{Rtotal} \cdot 1k$. Equation 4.12 shows the final deducted expression to calculate $R_{\beta eq}$.

$$R_{\beta eq} = \frac{N_{Rtotal} \cdot 1k}{N_{Ron}} \tag{4.12}$$

The final expression to select a certain value of output voltage is given by

$$V_{out_{new}} = \frac{0.6_{Ron}}{N_{Rtotal}} + 0.6 \tag{4.13}$$

The deduction where $V_{out_{new}} = V_{out_N} - \Delta V_{step}$ allows the manipulation of previous expressions in order to find the delta step between the output voltages available, shown in equation 4.14.

$$\Delta V_{step} = \frac{0.6}{N_{Rtotal}}, \qquad \text{for} \quad N_{Rtotal} > 1 \tag{4.14}$$

The output voltage step implemented in the proposed LDO voltage regulator is 0.1 V, being able to regulate out voltages from 0.7 V up to 1.2 V. So, the total number of beta resistors is 6 to achieve these output voltage values, as illustrated in Figure 4.25.

The implemented configuration is combinational to allow for a wider range of possible output voltage values, as well as to reduce leakage through the transistors as much as possible. Initially, a transmission gate was used to act as non-ideal switches but, despite showing to be very effective in theory, in practice the transmission gates generated a lot of leakage currents that would change the desired output voltage value. This way, since the beta resistors are connected to ground, a simple NMOS transistor was used between the β resistors and the ground terminal, designed to work in saturation region when $V_{swi} = 1.8V$ and in cut-off region when $V_{swi} = 0V$. The designed transistors set their output resistance value around the 200 Omhs. This means that, for a total resistance of 6k Ohms in each branch, each β resistor as a total value of $R_{\beta i}$ = 6k - 200 = 5.8k Ohms.

Table 5.3 shows the V_{swi} combinations for each output voltage value available.

Table 4.13: Switching setup for the defined output voltages

V_{out} (V)	$V_{sw1}(V)$	$V_{sw2}(V)$	$V_{sw3}(V)$	$V_{sw4}(V)$	$V_{sw5}(V)$	$V_{sw6}(V)$
1.2	1.8	1.8	1.8	1.8	1.8	1.8
1.1	0	1.8	1.8	1.8	1.8	1.8
1.0	0	0	1.8	1.8	1.8	1.8
0.9	0	0	0	1.8	1.8	1.8
0.8	0	0	0	0	1.8	1.8
0.7	0	0	0	0	0	1.8

The results presented in Figure 4.26 show that the proposed LDO voltage regulator, was able to regulate every output voltage value with the same precision of the 1.2V output voltage regulation in steady state. The transient behaviour of these combinational beta resistors showed that for lower output voltages, the overshoot and undershoot values tend to decrease ever so slightly while the phase margin of the system also decreases as the equivalent beta resistor is about 6x higher, observing a ringing increase in the response to load current step variations.

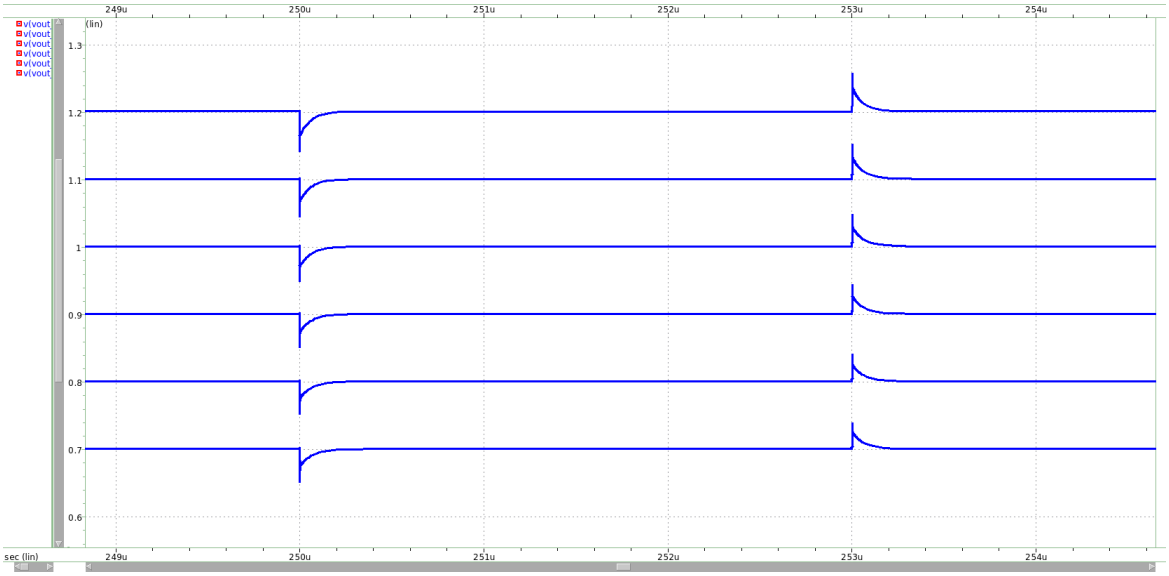


Figure 4.26: Transient response of the proposed LDO voltage regulator for the available output values, with a load current step of 1mA

4.5 Start up circuit

The start up circuit for the fast loop provides isolation the fast loop from the main system loop of capacitor-less LDO voltage regulator. This switch on/off implementation allows the main system of the capacitor-less LDO voltage regulator to turn on the fast loop whenever it is need, for example in a fast load transient step, and also, switch between different fast loop configurations. For a well designed capless LDO generic architecture, the opportunity to switch between different fast loop

configurations is good to implement a fast loop re-configurable system in various applications with different specifications.

The proposed Start-up circuit is presented in Figure 4.27

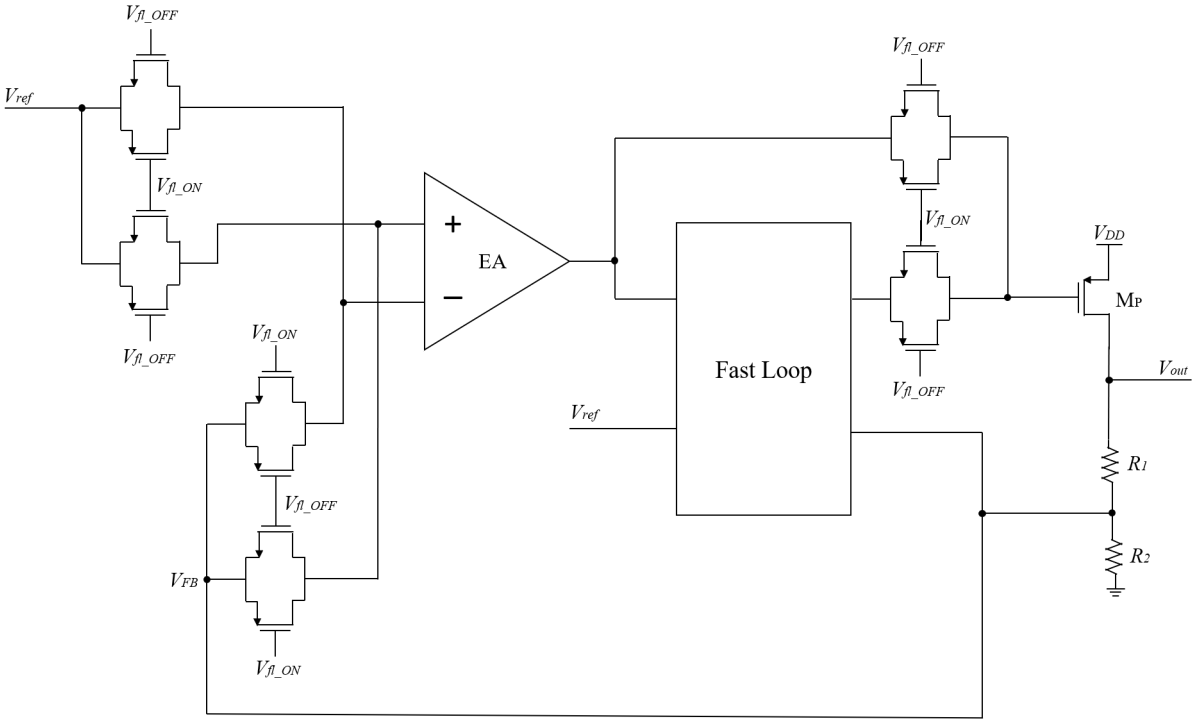


Figure 4.27: Proposed Start-up Circuit

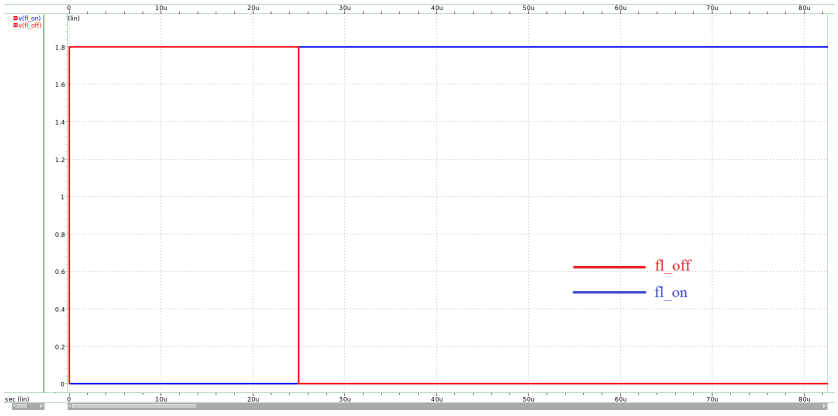


Figure 4.28: Control Signals of the Start-up circuit

The result for the transient simulation of start up circuit is presented in Figure 4.29.

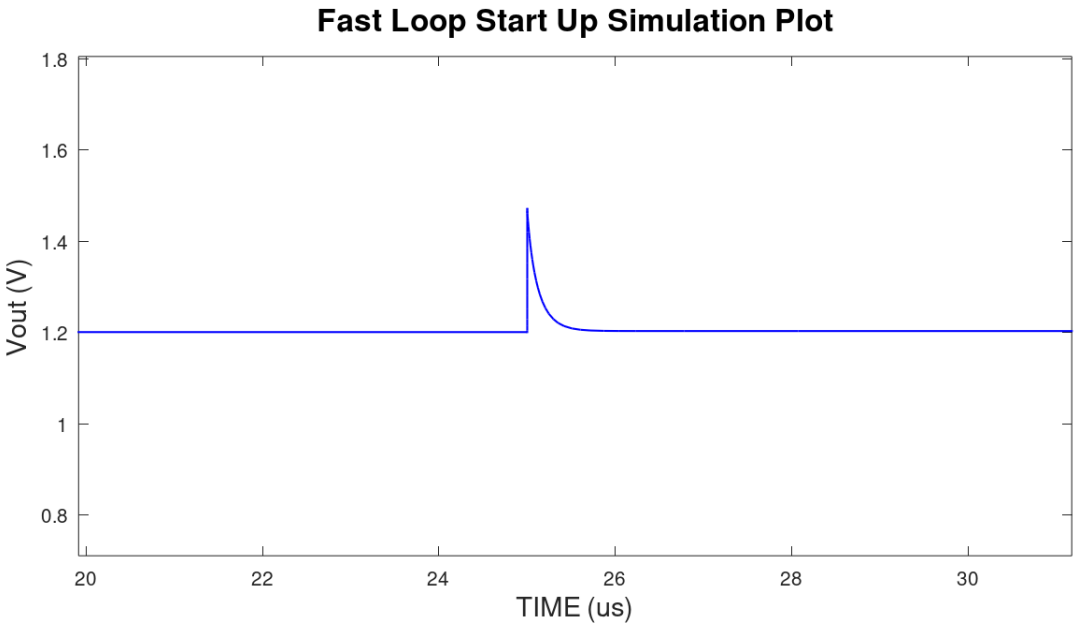


Figure 4.29: Transient response for the start up circuit under no load conditions

Both the output of the error amplifier ($V_{out_{EA}}$) and the output of the fast loop ($V_{out_{FastLoop}}$) connect to the gate of the pass transistor. At the switching point between the general LDO voltage regulator architecture and the fast loop block the nodes conflict with each other by holding different voltage values, as shown in Figure 4.30. This clash of voltage values generate a voltage drop from the node at the gate of the pass transistor to the output node of the fast loop until this last one recovers up to the voltage value needed to drive the gate of the pass transistor in steady state, which in this case is 1V. Figure 4.30 is zoomed in in order to observe the effect at the switching point so the gate voltage settling is not included in the range of simulation.

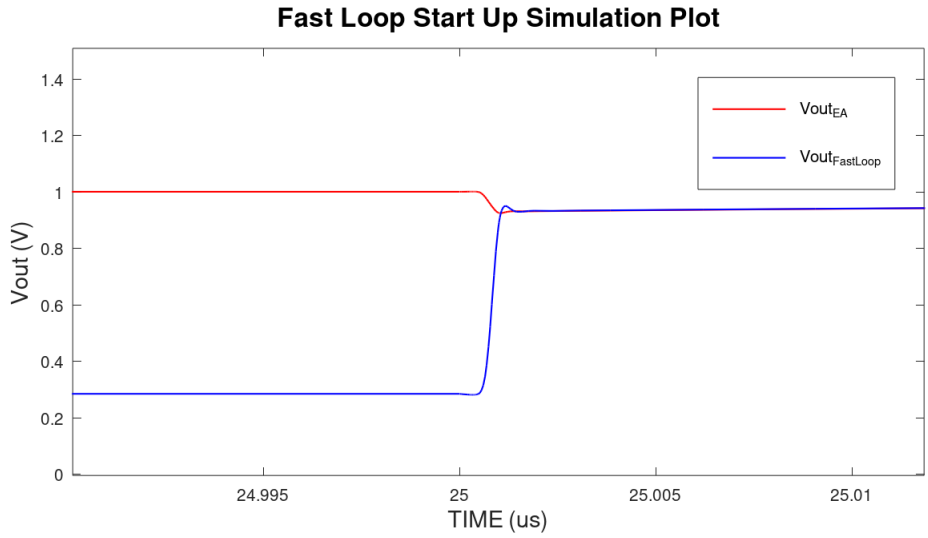


Figure 4.30: Transient response for the start up circuit under no load conditions

The mentioned voltage drop at the gate of the pass transistor, makes the pass transistor to

drain current to the system's output voltage node generating an overshoot of 272 mV as showed in Figure 4.29. The switching action takes up to 500 ns to settle. This overshoot value and settling time can be reduced with the ability to increase the fast loop's output voltage through pre-charging of the respective node or by setting an initial condition for a predictable switch between the general configuration and the fast loop of the LDO voltage regulator.

4.6 Layout Design

This section introduces the layout of the proposed fast loop capacitor-less LDO voltage regulator. The layout design of the circuit allows the designer to evaluate the impact of parasitic capacitance generated by the circuit blocks and other effects caused by the routing and interconnection between block elements.

Figure 4.31 shows a diagram that represents the layout flow used to design the LDO voltage regulator in a 28nm CMOS silicon process.

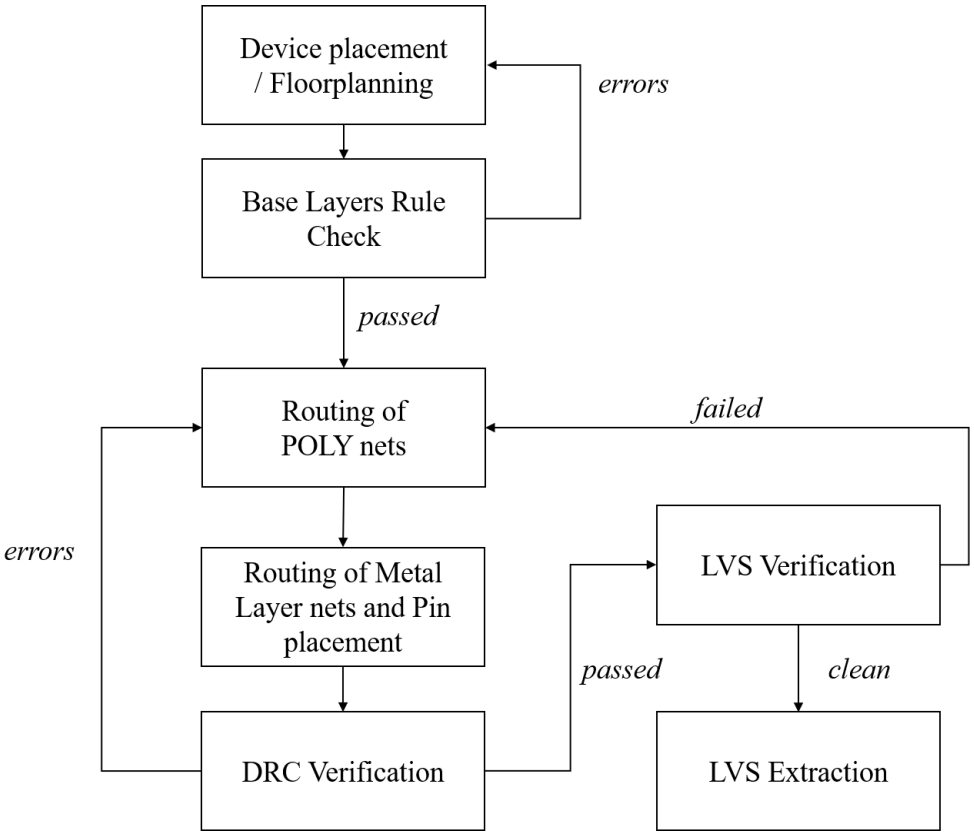


Figure 4.31: Layout Design Flow

Each device is instantiated with matching in order to minimise area usage and mismatch effects inherent to the fabrication process. After being placed, a preliminary Design Rule Check (DRC) verification is done to see if the placement of the base layers of the devices comply with the rules provided by the foundry, in the working process technology.

With the base layers laid out, the routing of the device nets starts with interconnecting the polysilicon, *POLY*, nets with metal, instead of using an all polysilicon layer routing, in order to minimise unwanted voltage drop between routing.

The routing between contacts of source and drain device nets is done after the routing of *POLY* nets given the fact that they are more flexible to interconnect. Since the vias used, in source and drain terminals, to navigate between metal layers are more isolated that the ones used for *POLY* routing, that are more prone to be crossed by metal layers used for different signals.

Upon passing all DRC verification, the LVS verification is performed to verify if the layout matches with the respective schematic designed. Once LVS verification is clean, the layout of the circuit can be extracted.

The layout design developed for the proposed fast loop capacitor-less LDO voltage regulator is presented in Figure 4.32.

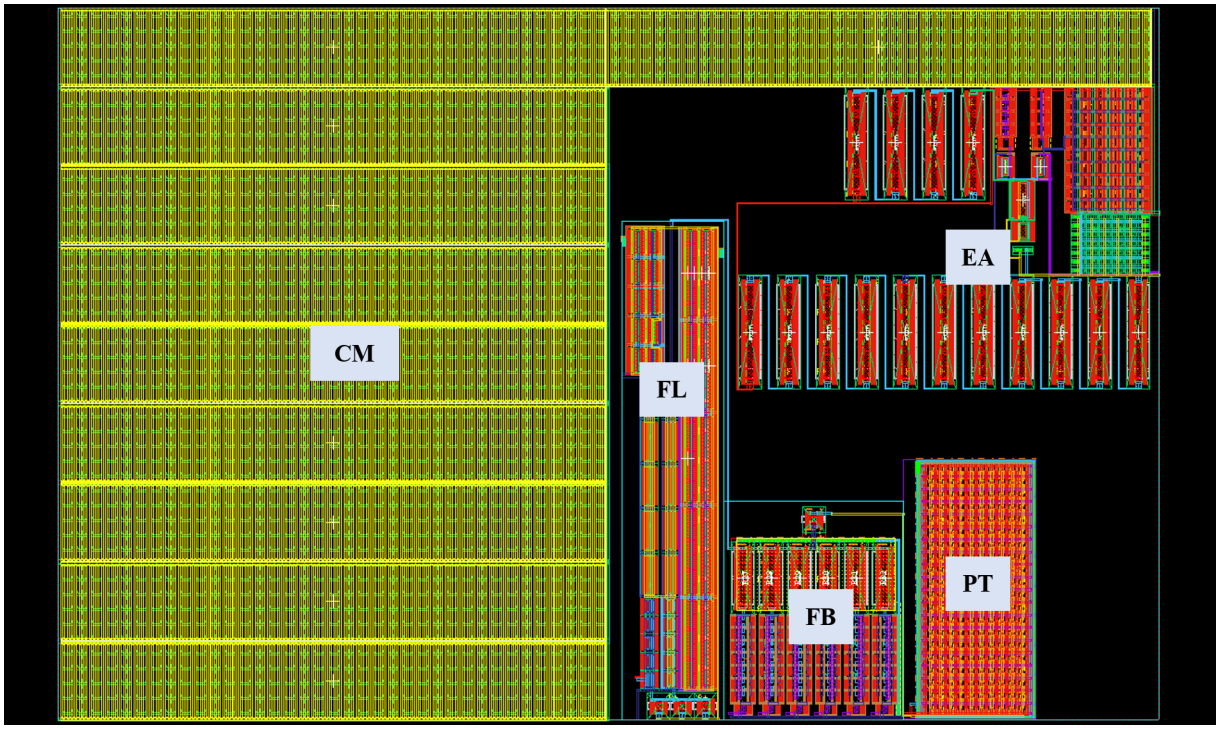


Figure 4.32: Layout Design of the proposed fast loop capless LDO voltage regulator

The total area usage achieved for the proposed design is 0.0032 ^{2} with the miller capacitance representing more that 50% of the total area consumption of the LDO.

Chapter 5

Final System's Results

5.1 Testbench setup

The final results were measured with an approximation to what can be a real load condition provided by an analog building block. For that reason, an ideal current source representing the load current, used until now for circuit testing purposes, is replaced by a switching combination of resistors able to provide 0 A, 10 μA, 100 μA, 1 mA and more, with a t_{rise} and T_{fall} of 1ns. The method used to implement the load resistor block was the same used in the previous chapter for the adaptable voltage divider of the feedback factor. The load setup used for circuit simulation in Figure 5.1.

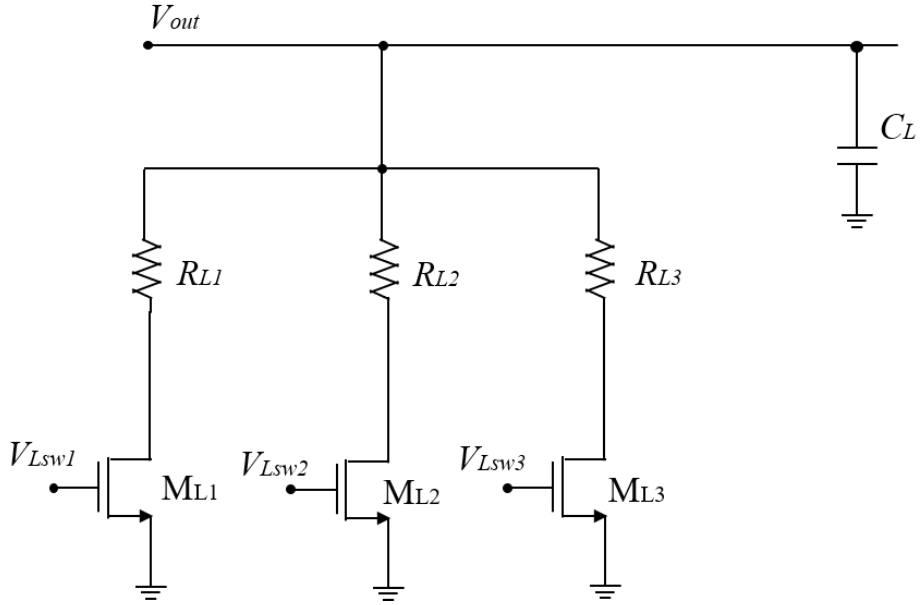


Figure 5.1: Load circuit block

Based on the current divider principle, the equivalent resistance for each branch in order to achieve the specified currents is $R_{L1_{eq}}$ = 1.33kΩ, $R_{L2_{eq}}$ = 13.33kΩ and $R_{L3_{eq}}$ = 120kΩ.

Considering the NMOS switches, as done for the configurable feedback network resistor block, the exact resistor values for each load resistor is presented in Table 5.1 and the transistor sizes in Table 5.2.

Table 5.1: Load Resistor values

Parameter	Value
R_{L1}	1.33 kΩ
R_{L2}	13.33 kΩ
R_{L3}	120 kΩ

Table 5.2: Load transistor sizing

	M_{L1} (hv)	M_{L2} (hv)	M_{L3} (hv)
W ($\cdot 1\frac{}{W_{min}}$)	1	1	1
L ($\cdot 1\frac{}{L_{min}}$)	2	2	2
Multiplicity	15	30	40

The length of the load transistors is doubled in order to provide higher output resistance and decrease leakage current through them. The goal is to keep transistor sizing minimal to keep the transistor output resistance high but, to be able to flow 10 μA, 90 μA and 902 μA through each resistor branch, the width of the transistors have to be increased 15, 30 and 40 times higher, respectively.

Table 5.3 shows the set up of switch combinations for different load currents.

Table 5.3: Switching setup for the defined output voltages

I_L	$V_{Lsw1}(V)$	$V_{Lsw2}(V)$	$V_{Lsw3}(V)$
0 A	0	0	0
10 μA	0	0	1.8
100 μA	0	1.8	1.8
1 mA	1.8	1.8	1.8

5.2 Results

5.2.1 Dropout Voltage

A parametric sweep simulation over the input supply voltage (V_{in}), from 0 to 2V, was performed in order to see which is the minimum V_{in} required to the LDO voltage regulator is able to regulate an output voltage of 1.2 V. The minimum input voltage measured in the simulation result is 1.247V which means that the dropout voltage (V_{DO}) is 47 mV.

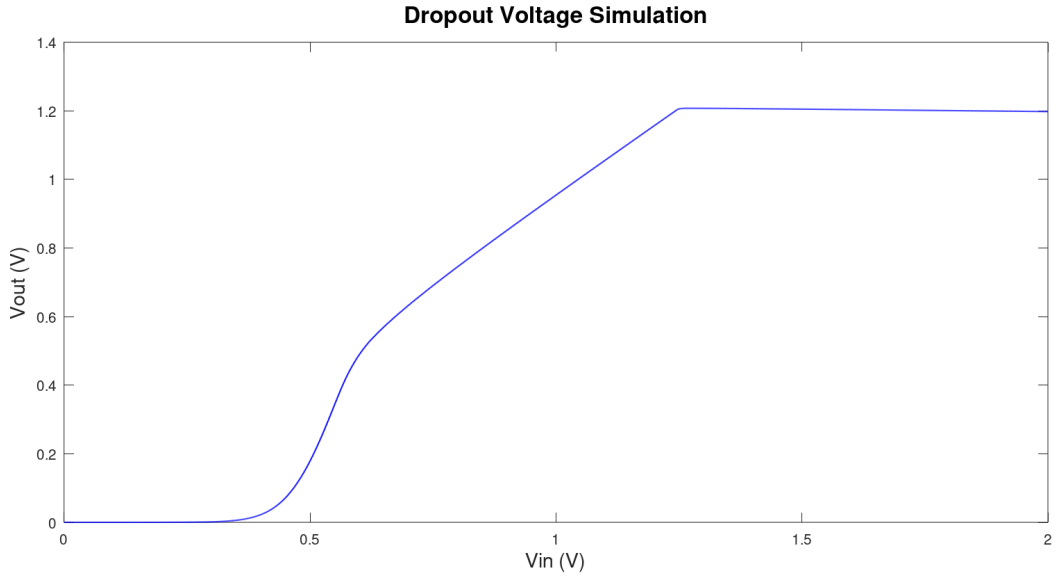


Figure 5.2: Voltage Dropout simulation results for I_L=1 mA with C_L= 0 F

5.2.2 Transient Behaviour

The load transient behaviour of the Fast Loop capless LDO voltage regulator, presented in Figure 5.3, was simulated by applying a load current variation from 0 A up to a maximum load current of 1 mA, with a rise and fall time of 1 ns. The ideal input voltage was set to the nominal value, V_{dd}=1.8 V, and the load capacitance is equal to 1 pF.

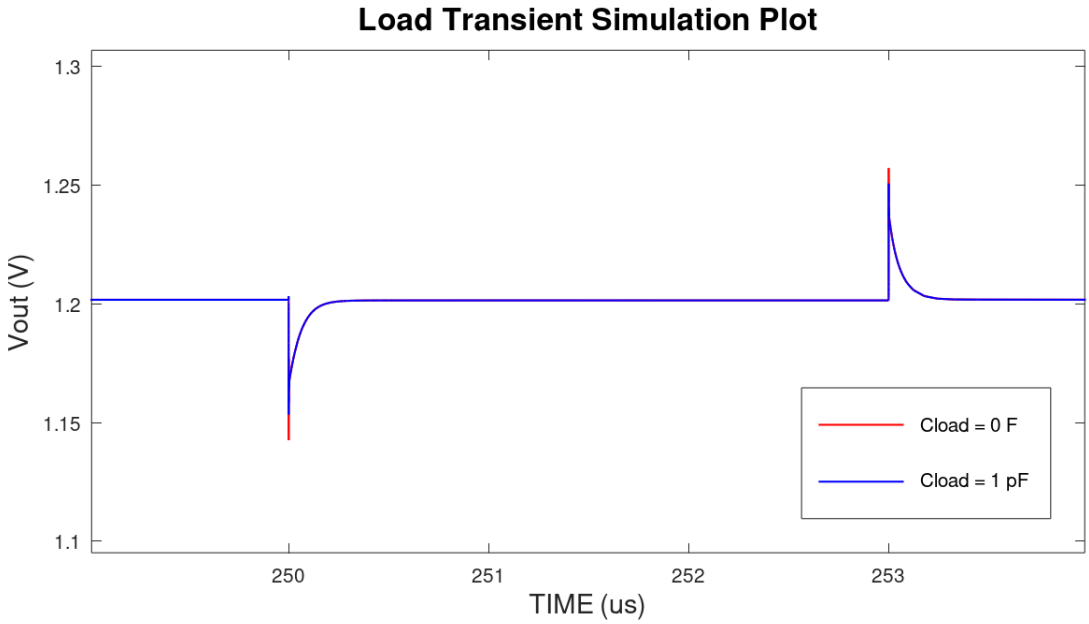


Figure 5.3: Load transient simulation results for V_{in}=1.8V with C_L=0, 1p F

The results in Figure 5.3 showed an overshoot and undershoot of 48mV and 49.8mV, respectively, for the set up testbench while, for an ideal load current source, the proposed LDO voltage

regulator generated 38.5mV of overshoot and 37mV of undershoot.

The line transient behaviour of the Fast Loop capless LDO voltage regulator, shown in Figure 5.10, was simulated by applying a input supply voltage variation, of the pass transistor, from 1.8 V to 2 V, with a rise and fall time of 1 ns. The load current was set to the maximum value, I_L=1 mA, and the load capacitance is equal to 1 pF.

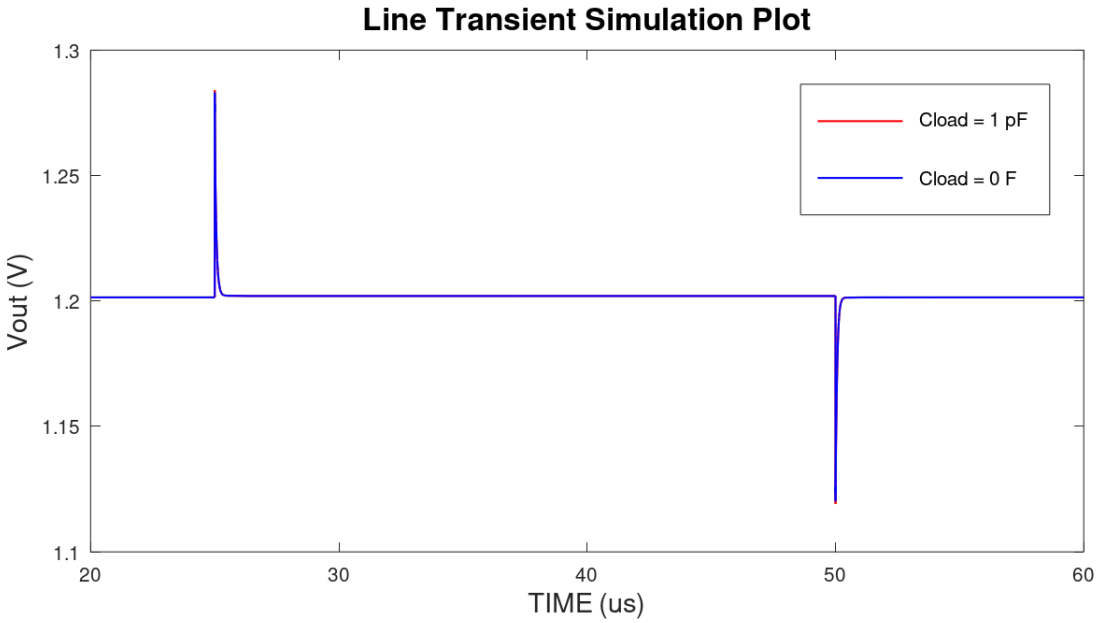


Figure 5.4: Line transient simulation results for I_{load}=1mA with C_L={0, 1p} F

Figure 5.10 presents the load transient response for a load current step of 1mA with a parametric sweep of 500ps, 1ns, 5ns, 10ns and 50ns of t_{rise} and t_{fall}.

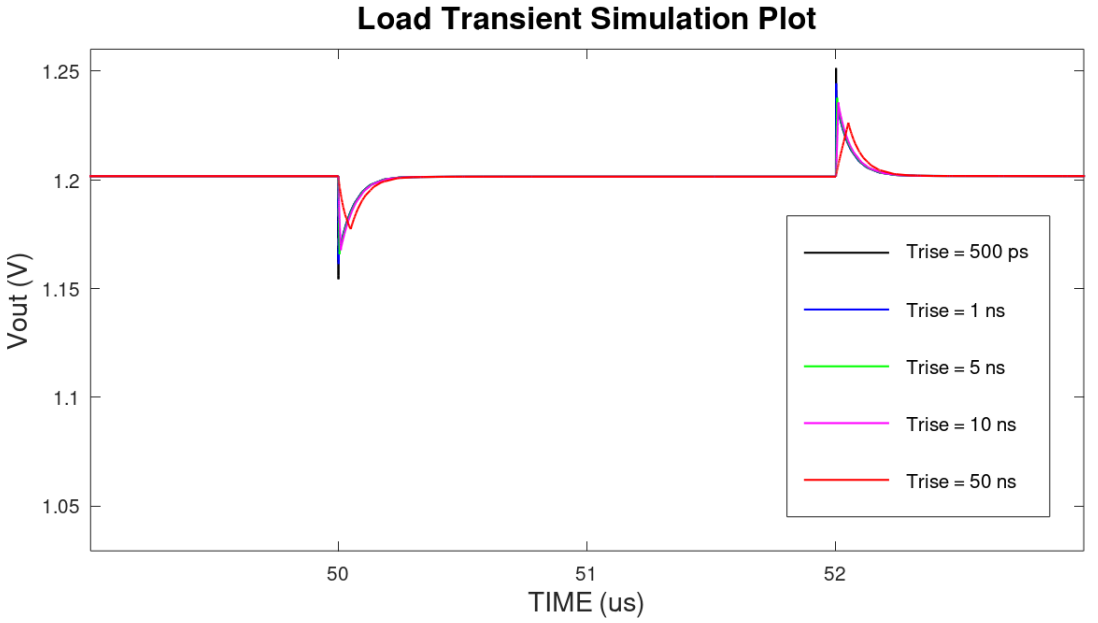


Figure 5.5: t_{rise} sweep load transient simulation results for I_{load}=1mA with C_L=0 F

5.2.3 Output Regulation

The load regulation of the fast loop capless LDO was simulated by running a parametric sweep of the load current from 0 mA to 1 mA, with 101 points measured, over load transient simulations for a supply input voltage of 1.8 V. This type of simulations measure the output voltage value at a determined point in time where it is already in steady state, for every point of the sweep range. Then, the plot in Figure 5.6 shows the regulated output voltage value for each active load current in the circuit, containing the regulation delta around 465 μV in the load current range of 0 to 1 mA. The load regulation can also be measured in voltage percentage by dividing the output regulation delta by the nominal output voltage value, achieving a load regulation of 0.03 %/V.

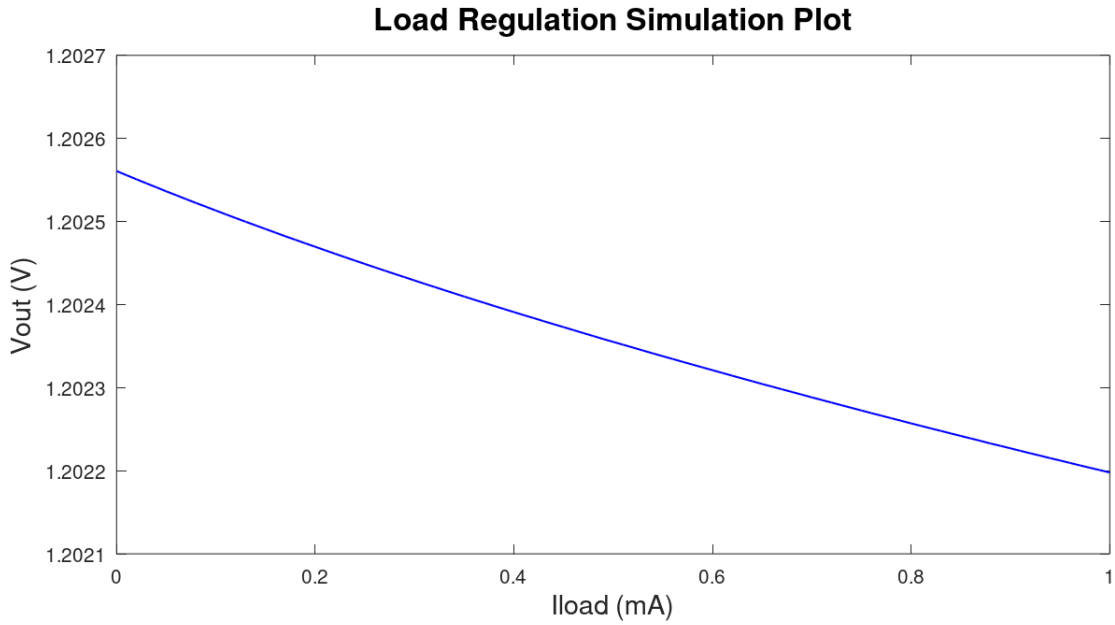


Figure 5.6: Load Regulation simulation results for V_{dd}=1.8V

The line regulation of the fast loop capless LDO was simulated with the same method of the load regulation simulation. This time, the load current is fixed at the maximum value, $I_L = 1mA$, and the parameter swept was the pass transistor supply voltage in the range from 1.6 V up to 2 V with 21 points measured. The plot in Figure 5.7 shows the regulated output voltage value for each active input voltage value, containing the regulation delta around 6 mV in the input voltage range of 1.6 V to 2 V. The line regulation can also be measured in voltage percentage by dividing, in the same way as for the load regulation, the output regulation delta by the nominal output voltage value, achieving a line regulation of 0.5 %/V.

5.2.4 Stability of the Fast Loop capless LDO voltage regulator

The open loop stability parameters were measured with an open loop AC simulation analysis, opening the loop at the common node of the feedback network. The testbench was set with a suuply voltage of 1.8 V and a load curent of 0 A. The simulations presented in Figure 5.8 were

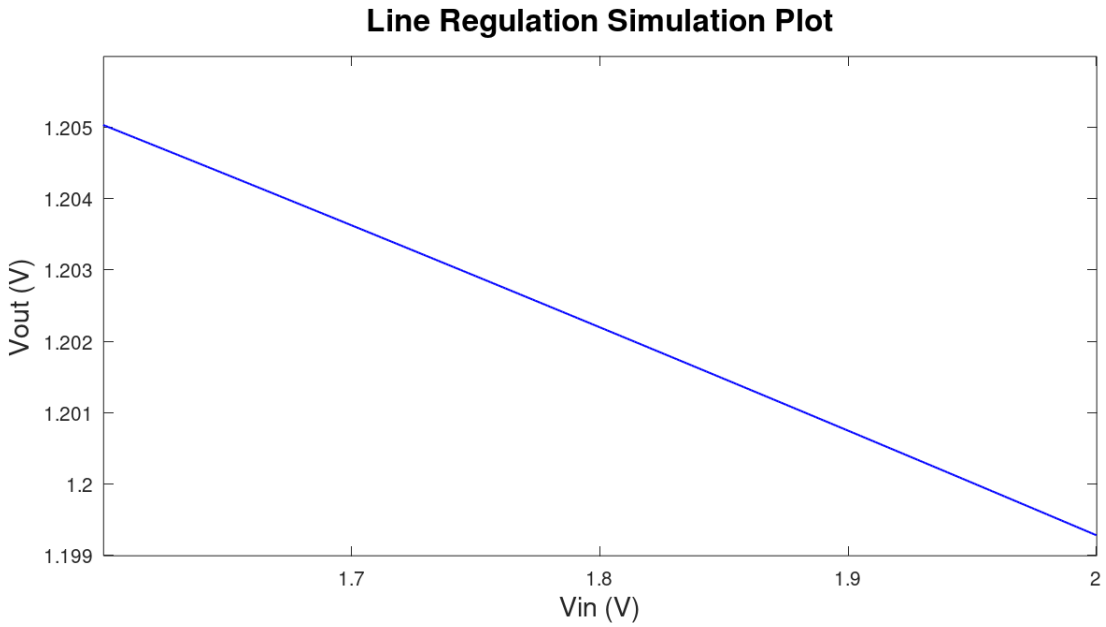


Figure 5.7: Line Regulation simulation results for I_{load}=1mA

done for a C_L=0 F, in red, and C_L=1 pF, in blue, in order to see the impact of the load capacitance on the stability of the fast loop capless LDO voltage regulator.

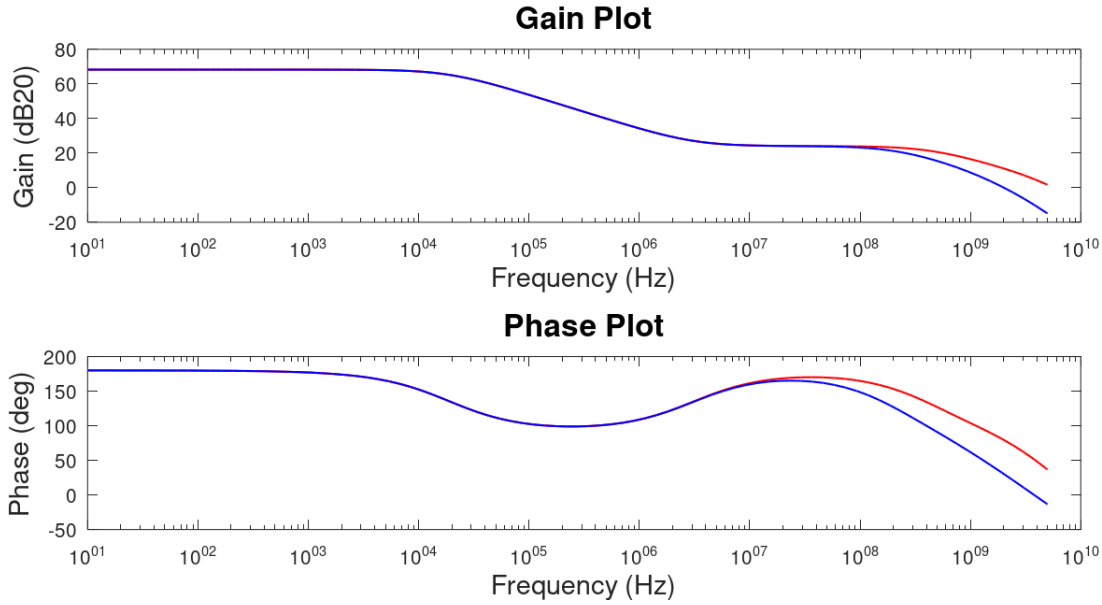


Figure 5.8: AC simulation results for I_{load}=1mA with C_L= 0 in red and C_L= 1pF in blue

Overall, the circuit has an open loop gain of 67.5 dB and a bandwidth of 13.3 kHz and, a phase margin equal to 25.7 deg for C_L=1 pF and 28.8 deg for C_L=0 F.

5.2.5 Ripple Rejection Behaviour

The Power Supply Ripple Rejection is simulated by applying an AC supply voltage with 1.8V DC voltage value and a magnitude of 1V, to find the amount of input ripple that the proposed LDO voltage regulator is able to attenuate in its output node. The AC value of the output voltage was converted into a $20log_{10}$ scale of decibels and then plotted over the frequency spectrum as shown in Figure 5.9.

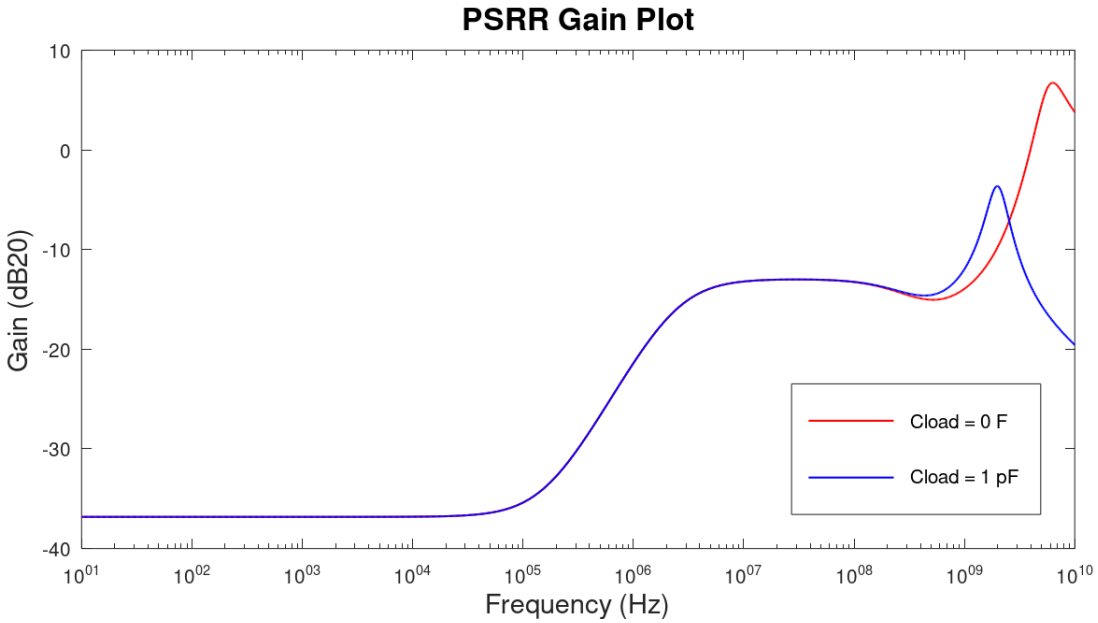


Figure 5.9: PSRR simulation results for I_{load}=1mA with C_L=0, 1pF

For a load current value of 1 mA the plot shows an identical ripple attenuation until 1 GHz, having a better rejection with C_L=1 pF, in blue, than with C_L=0 F, in red. The best ripple rejection achieved is -36.8dB at low frequencies and, the worst is -3.64dB at 1.98 GHz and 6.72dB around 6.23 GHz, for C_L=1 pF and C_L=0 F respectively.

The PSRR plot of C_L=0F maintains a supply ripple rejection up to 4.5GHz. However, as the operating range of frequency of the proposed LDO voltage regulator is only up until 1GHz, the amplification above the mark of 4.5GHz is not considered for the given LDO applications.

The rejection gain, given by the simulation results, in the standard frequency points of measurement are the following:

- 1MHz : -21.4dB
- 10MHZ : -13.2dB
- 1GHz : -12dB for C_L= 0 F and -13.9dB for C_L=1 pF
- 10GHz : -2.78dB for C_L= 0 F and -19.6dB for C_L=1 pF

The previous results were simulated for the maximum load current. In order to observe how the proposed LDO voltage regulator is able to reject supply ripple for lower load currents, a simulation

for a given set of load currents, 10 uA, 100 uA and 1 mA was performed. The results of the last mentioned simulation are presented in Figure 5.10.

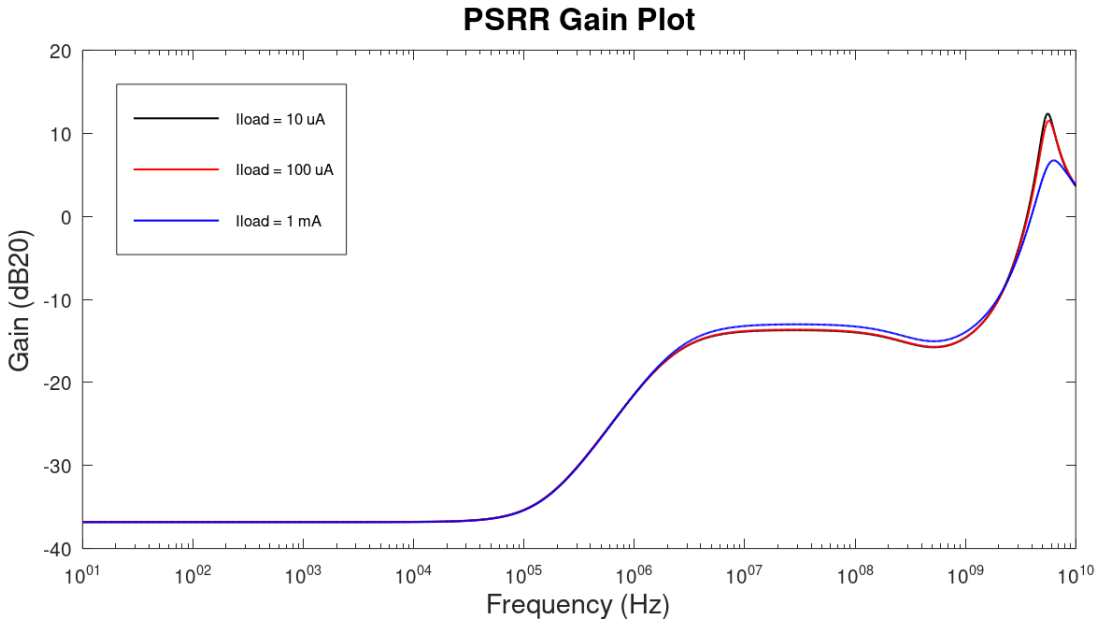


Figure 5.10: PSRR simulation results for I_{load}=10u, 100u, 1m A with C_L=0 F

The results show that PSRR of the proposed LDO voltage regulator improves with a load current decrease, as the equivalent load resistance is higher when the load current is lower.

5.2.6 Power Up

This next simulation measures the power up of the proposed LDO voltage regulator. This measurement determines the time required for the LDO to turn-on, while the output voltage reaches steady state at 1.2 V. The measured settling time is about 0.5 μs meaning that the capacitor-less LDO voltage regulator takes up t0 0.5 μs to turn-on.

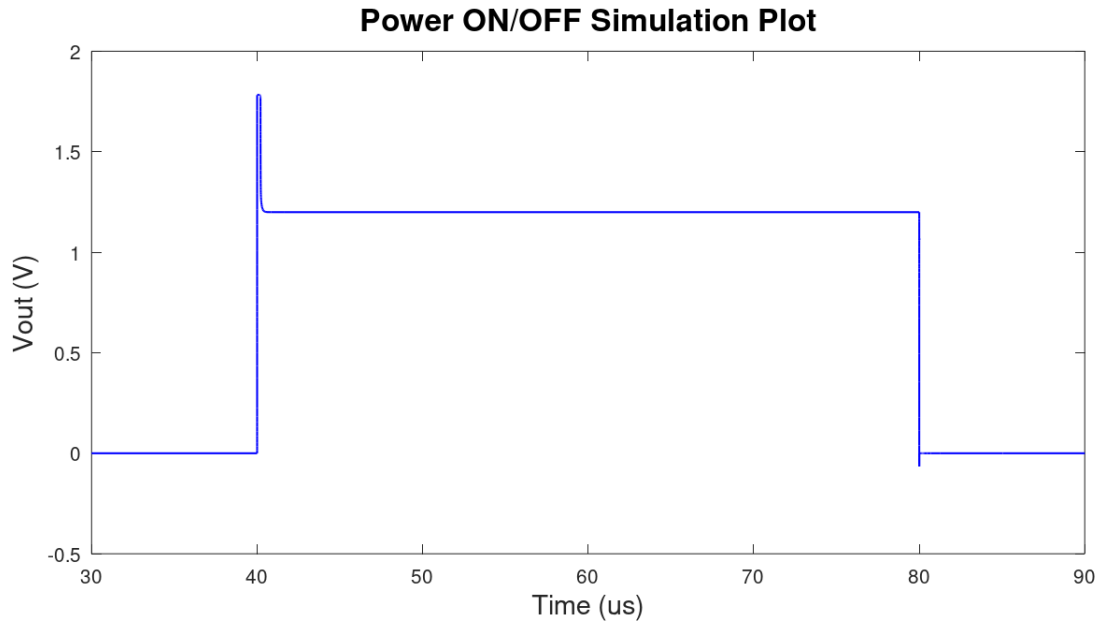


Figure 5.11: Power ON/OFF simulation results for I_{load}=0mA with C_L=0 F

5.2.7 Efficiency

Given the fact that the quiescent is 60% of the maximum regulated load current, it will be defining the efficiency of the voltage regulator. Therefor, The efficiency of the LDO voltage regulator is

$$E_{ff} = \frac{1.201 \cdot 0.001}{1.247 \cdot (0.001 + 0.0006)} = 60.2\% \tag{5.1}$$

5.2.8 PVT corner variations

PVT variation measurements were performed by simulating, for the desired parameters, the set of extreme corners described in chapter 3

Figure 5.12 shows the PVT corner variations for a load transient simulation with a load current step variation from 0 to 1 mA, with a t_{rise} and a t_{fall} of 1ns, and C_L=0 F.

The simulation results showed an output voltage regulation between 1.155 V and 1.241 V achieving a maximum overshoot value of 56.8 mV and a maximum undershoot value of 63.5 mV. The worst case corner simulated was found to be in an environment of temperature equal to 125º Celsius, a supply voltage of 1.62 V over a fast-fast process, regulating an output voltage value of 1.155V that might limit the headroom available, for example, for the components of eventual analog load blocks.

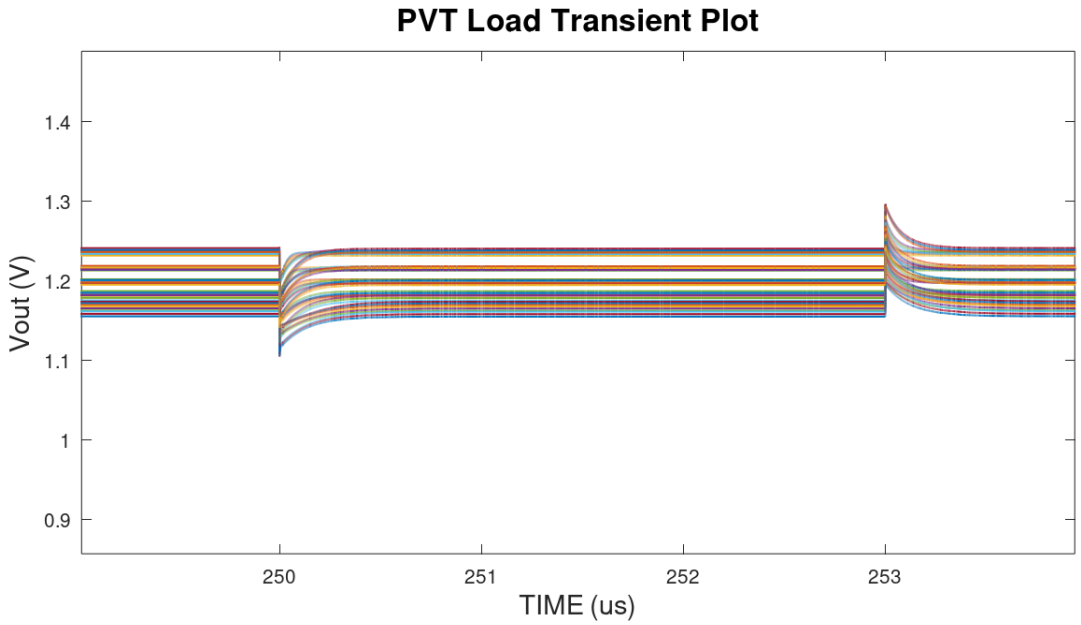


Figure 5.12: Load Transient PVT simulation results for I_{load}=1mA with C_L= 0 F

Figure 5.13 shows the PVT corner variations for an open loop AC simulation with a load current of 1 mA and no load capacitance.

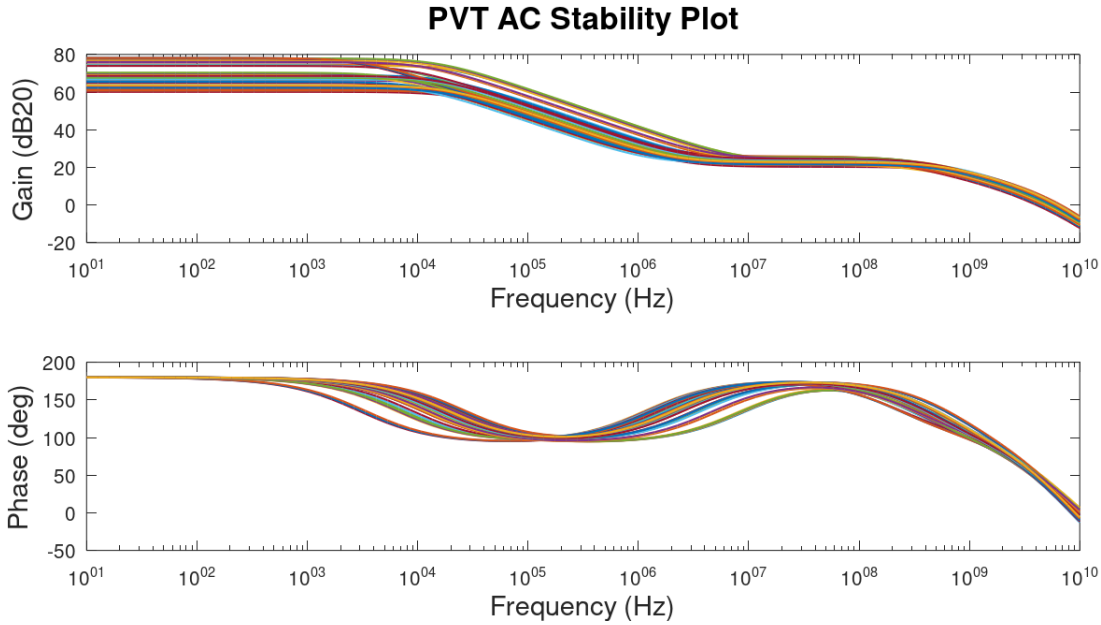


Figure 5.13: AC PVT simulation results for I_{load}=1mA with C_L=0 F

The simulation results showed a DC gain variation between 61.1dB and 78.2dB and a phase margin ranging between 22.8 degrees and 46.6 degrees. The worst case corner simulated was found to be in an environment of temperature equal to 125º Celsius, a supply voltage of 1.98 V over a fast-slow process, by delivering the lowest phase margin detected with the value of 22.8

degrees. This result proves that the system guarantees its stability even at the worst operating environment.

Figure 5.13 shows the PVT corner variations for the power supply ripple rejection simulation with a load current of 1 mA and no load capacitance.

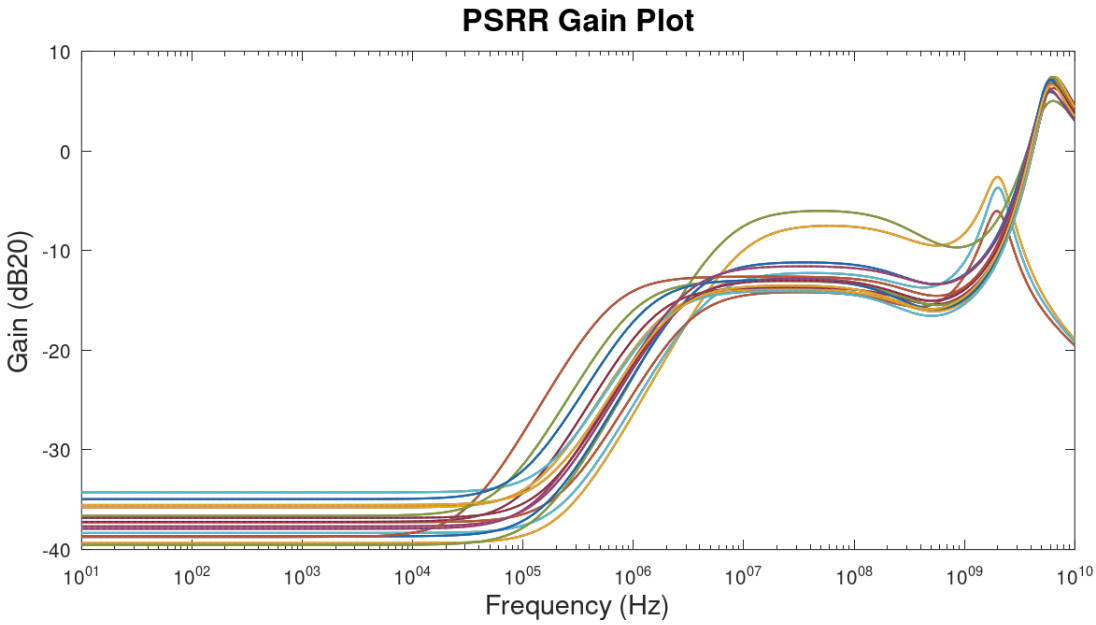


Figure 5.14: PSRR PVT simulation results for I_{load}=1mA with C_L=0 F

The PVT corner simulation results for PSRR showed a supply ripple rejection ranging from -44.9dB to -36.8dB at a frequency of 1kHz, from -26.1dB to -13.7dB at 1MHz and from -15.9dB to -6.76dB at 1GHz. Some corners show a positive sipple rejection near 10MHz of frequency. The worst corner was found to be in a simulated environment of 25º Celsius of temperature, a supply voltage of 1.98 V and a SS process corner.

5.2.9 Monte Carlo Analysis

Monte Carlo Analysis was performed to study the sensitivity of the proposed fast loop capacitorless LDO voltage regulator to process variations. To comply with ISO26262 safety and reliability standards, the measured device should have a maximum of 1000 *dppm* [29], defective parts per million, which is corresponds to a 3.09 sigma. Monte Carlo simulations were performed using a 4.5 *sigma* for 330 iterations in order to cover a yield percentage of 99.997%, which represents 3.4 *dppm*. The set of Monte Carlo simulations were done under the same conditions as the PVT corner simulations.

Results presented in Figure 5.15 for load regulation showed a centered Gaussian distribution with an output voltage median of 1.17 V and a standard deviation of 46.6mV.

Monte Carlo analysis was also performed for the phase margin of the proposed LDO to verify the stability of the system. Results presented in Figure 5.16 show a phase margin median of 23.9 degrees and a standard deviation of 2.85 degrees. Phase margin was able to achieve more than 35

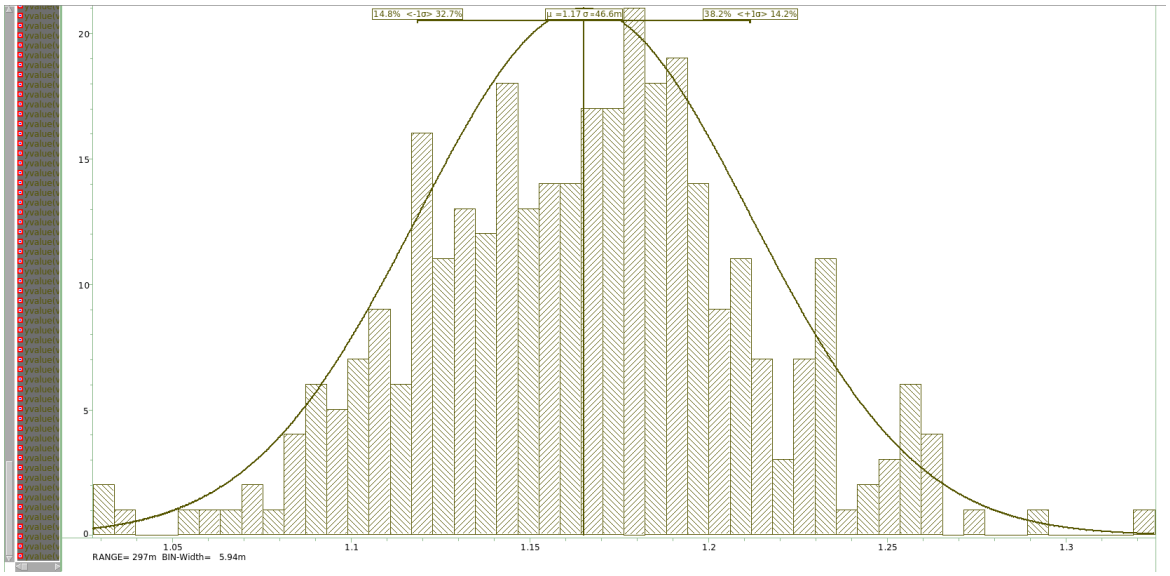


Figure 5.15: Worst Case Load regulation Monte Carlo simulation results for I_{load}=1mA with C_L=0pF

degrees for some iterations due to DC gain increase in the respective process variations, as seen for the PVT corner simulations.

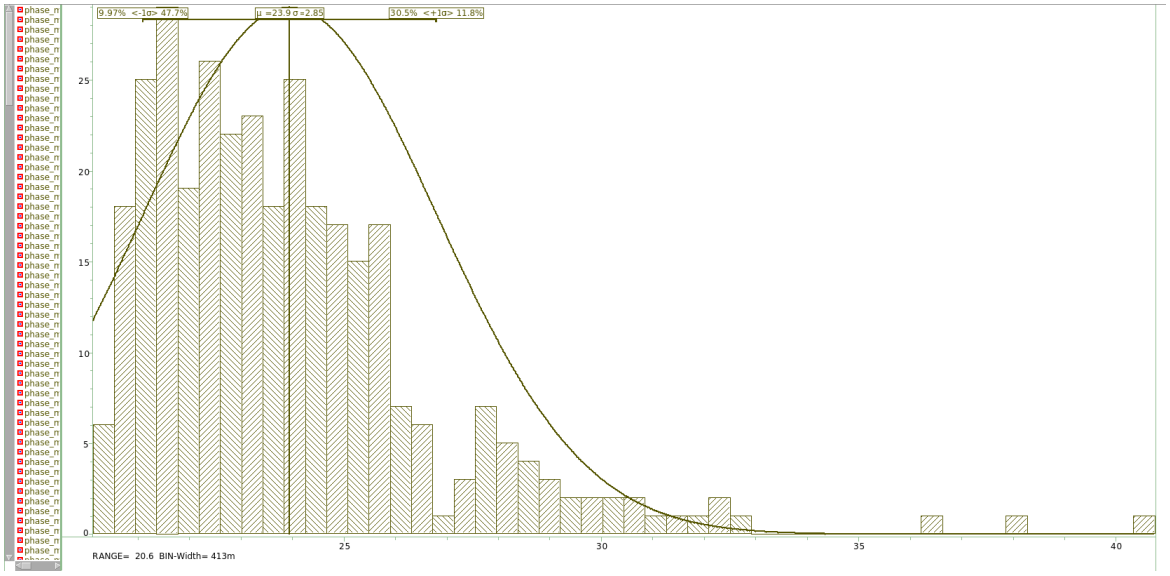


Figure 5.16: Worst Case Phase Margin Monte Carlo simulation results for I_{load}=1 mA with C_L=0 pF

Results presented in Figure 5.17 for power supply rejection ratio showed a centred Gaussian distribution for 1kHz frequency a median of -26.7dB and standard deviation of 276mdB. For 1MHz the median is -15dB with a standard deviation of 1.22dB and for 1GHz the registered median was -14.1dB with a standard deviation of 1.9dB.

At 10MHz of frequency, the PVT simulations showed a very weak rejection from the fast loop

capacitor-less LDO voltage regulator. So, from there, the performed Monte Carlo simulation over that frequency, with a median of -12.1dB and a standard deviation of 2.98dB, shows indeed an amplification in a few number of iterations.

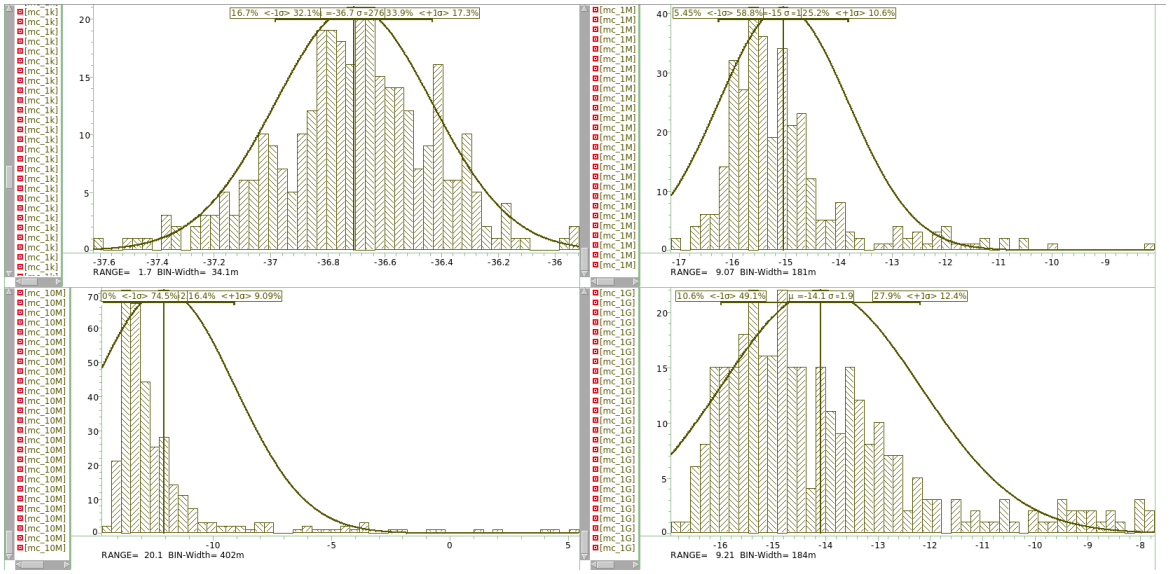


Figure 5.17: Worst Case PSRR Monte Carlo simulation results for I_{load}=1 mA with C_L=0pF

5.3 System Validation and Datasheet

After performing the presented simulations, a datasheet of the proposed fast loop capacitor-less LDO voltage regulator is presented in Table5.4, detailing the final system's specifications.

Table 5.4: Datasheet of the electrical characteristics of the Fast Loop capacitor-less LDO voltage regulator

Parameter	MIN	TYP	MAX	
Input Voltage V_{in}	1.62	1.8	1.98	V
Load Current I_L	0		1	mA
System's DC Gain	61.1	68.5	78.2	dB
System's Bandwidth	2.95k	14.8k	27k	Hz
System's Phase Margin	22.8	28.6	46.6	deg
Output Voltage (V_{out})	1.155	1.199	1.241	V
Dropout Voltage (V_{DO})		47		mV
Load Regulation	93.9	241	755	μV/mA
Line Regulation	10.7	14.3	18.7	mV/V
Load Transient Overshoot	45	48	56.8	mV
Load Transient Undershoot	48	49.8	63.5	mV
Line Transient Overshoot	73	82	240	mV
Line Transient Undershoot	72	82.8	432	mV
Quiescent Current		600		μA
PSRR @1kHz	36.8	40.2	44.9	dB
@1MHz	13.7	21.1	26.1	
@1GHz	6.76	13.1	15.9	
Efficiency		60.2		%
FoM		0.028		ns
Silicon Area		0.0032		mm^2

Chapter 6

Conclusion

A proof of concept for transient compensation of a capless LDO voltage regulator through a fast loop configuration has been developed and presented. An uncompensated capacitor-less LDO has performance limitations in stability and transient response therefore, a capacitor-less LDO with frequency compensation scheme, using a Miller capacitor for a pole splitting technique, was initially studied and developed in order to guarantee stability and a functional performance for a maximum load step range of 1mA. The slow loop composed by the error amplifier, essentially, provides the system with high gain and low bandwidth while, the fast loop provides high bandwidth so the system is able to react faster to load transient variations in a wider range of the frequency spectrum.

Four fast loop architectures have been studied and implemented to see their effects, objectively, on the proposed capacitor-less LDO voltage regulator. Each architecture is designed for the purpose and certain performance specification and, a fast loop architecture based on a differential stage showed the best potential for a good load transient performance.

Two extra featured applications were developed for the LDO voltage regulator: an adjustable feedback network that allows for the regulation of 6 different output voltage values, and a fast loop start up circuit that provides isolation and the switch on/off of the fast loop from the main loop of the system.

The proposed fast loop for a capless LDO voltage regulator has shown a successful transient compensation compared to the initial start off generic architecture with an improvement over 500mV on output voltage spikes, in load transient response. Compared to other fast loop architectures, the proposed configuration has shown to be the third best configuration in transient performance and fourth in dropout voltage. One fact worth noticing is that, state of the art architectures were implemented in much bigger CMOS process technologies than the one proposed, which means that they are able to support higher voltage inputs as well as a higher current flow in the circuit, thus expecting to have a better performance right from the start. The trade off for a good transient performance was felt in the power supply ripple rejection performance where the system could only achieve a rejection of 40.2dB at low frequencies and, without any load capacitance, was not able to reject the voltage supply ripple between 1GHz and 10GHz. A quiescent

current of 600uA for a maximum load current of 1mA resulted in low efficiency and low FoM. which means that the device should consume less quiescent current or have a higher maximum load current specification. Nevertheless, with the specifications presented, the proposed capacitor-less LDO voltage regulator with fast loop is still a viable solution for low-voltage SoC applications with a big reduction in silicon area, pin count and overall cost.

6.1 Future Work

For further development of the work proposed in this dissertation, there are a few improvements to keep in mind:

- Quiescent current (I_Q) should be reduced in order to improve the efficiency of the LDO voltage regulator. In order to do that, the value of the feedback resistors should increase, at least, towards the hundred thousand Ohms range, so that the system' quiescent current consumption is within the micro ampere range for an output voltage value of 1.2V.
- For a better rejection of the power supply ripple, an overall increase of the lenght of the transistors could be applied to the transistors [ref paper arch2]. This increase would also reduce the impact of the process fabrication in the results as the devices become less sensitive to variations, relatively.
- The proposed error amplifier should also be improved as it happens to be a big limitation on the performance and area of the LDO voltage regulator. The error amplifier has still potential to provide a bigger gain with an adequate topology and also, potential to decrease the miller capacitance while maintaining the stability of the system. In spite of being much smaller than an external capacitor, the miller capacitor used in the error amplifier still occupies more than 50% of the area of the proposed LDO voltage regulator. Since that every stage introduces a pole in the system, a good suggestion would be to design an operational amplifier with only one stage, as for example a folded cascode or a telescopic amplifier, that would deliver high DC gain with a very low bandwidth, and then to either increase the size of the pass transistor, increasing its C_{gd} capacitance, or introduce a much smaller miller capacitor connected to the gate and the drain of the pass transistor which, with the high gain provided by the pass transistor would induce a much bigger pole splitting effect. With the increase of the pass transistor width, even if the area stays the same, its use would me more optimal given the fact that the pass transistor would be able to drain much higher current values.

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