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# Ge-modified Si(100) substrates for the growth of 3*C*-SiC(100)

Ch. Zgheib[a)]
*Department of Electrical Engineering, Notre Dame University, P.O. Box 72, Zouk Mikhayel, Zouk Mosbeh 2211 4501, Lebanon*

L. E. McNeil
*Department of Physics and Astronomy, University of North Carolina at Chapel Hill, Chapel Hill, North Carolina 27599-3255*

P. Masri
*Groupe d'Etude des Semi-conducteurs, CNRS-UMR 5650, GES, Université de Montpellier II, cc 074, 34095 Montpellier, France*

Ch. Förster, F. M. Morales, Th. Stauden, O. Ambacher, and J. Pezoldt
*Department of Nanotechnology, Center of Micro- and Nanotechnologies, TU Ilmenau, PF 100565, 98684 Ilmenau, Germany*

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An alternative route to improve the epitaxial growth of 3*C*-SiC(100) on Si(100) was developed. It consists in covering the silicon wafers with germanium prior to the carbonization step of the silicon substrate. Transmission electron microscopy and $\mu$-Raman investigations revealed an improvement in the residual strain and crystalline quality of the grown 3*C*-SiC layers comparable to or better than in the case of 3*C*-SiC grown on silicon on insulator substrates. These beneficial effects were reached by using a Ge coverage in the range of 0.5–1 monolayer. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2206558]

The increasing demands to integrate diverse electronic and optoelectronic devices operating at high temperatures and harsh environments[1] where silicon (Si)-based technologies cannot operate have motivated great improvements in alternative heteroepitaxial systems. Silicon carbide (SiC) compared to silicon exhibits a larger band gap, a higher breakdown field, and a higher thermal conductivity. These properties make it profitable to replace Si with SiC in these restrictive applications. Besides the advantages described above, SiC presents disadvantages when compared to Si, i.e., the high cost of SiC substrates and the smaller size of commercialized wafers, which prevent its integration in the device market. The challenge is to combine the favorable physical properties of SiC with the low-cost, mature Si technology; and the cubic phase, 3*C*-SiC, appears as the most plausible candidate.

However, due to the large lattice mismatch ($\approx 20\%$) and the high difference in thermal expansion coefficients ($\approx 8\%$), it has been difficult to obtain a coherent interface between the two cubic materials. The standard deposition process to achieve single-crystalline SiC on Si consists in a two-step epitaxial process and was originally published by Nishino *et al.* in 1983.[2] The first process step consists in the formation of a thin 3*C*-SiC layer by converting the Si in the near-surface region into SiC at 1400 °C, while the second step consists in the subsequent epitaxial growth, at the same temperature, on the formed SiC pseudosubstrate. The obtained 3*C*-SiC layers are normally tensile strained, which affects the device properties. Up to now, different methods have been developed in order to modify the strain in the grown 3*C*-SiC layers. They consist in the tuning of the crystalline properties[3] or the carbonization conditions,[4,5] or in the use of different types of compliant substrates.[6–9]

Another consequence of the standard growth method is the development of voids in the silicon substrate just beneath the SiC layer due to Si out-diffusion. The void formation can be stopped by adjusting the conversion conditions and selecting the Si-to-C ratio during the subsequent epitaxial growth.[10–12] Both effects, the strain and related defect formation as well as the voids, deteriorate the electrical properties of the grown SiC.[13] Furthermore, since usually the temperature required for growing good SiC approaches the melting point of Si, low temperature growth is preferred even at the cost of a lower 3*C*-SiC crystalline quality.[14] The previous arguments (reduced crystalline quality, high strain inside 3*C*-SiC and the presence of voids) have prevented the development of a large scale 3*C*-SiC integration on Si substrates.

With the aim to obtain better 3*C*-SiC/Si heteroepitaxy, our approach consists in the deposition of Ge prior to the carbonization step in order to create a modulated transition at the interface. In the case of Si(111) it has already been shown that Ge plays the role of a diffusion barrier for Si out-diffusion from the substrate through the growing SiC layer suppressing void formation.[15]

In the present study it will be demonstrated that Ge predeposition prior to the conversion process of Si(100) into 3*C*-SiC(100), combined with 3*C*-SiC epitaxial growth by chemical vapor deposition (CVD), reduces the residual strain in the heteroepitaxial 3*C*-SiC/Si system up to values previously achieved only by using silicon on insulator (SOI) substrates.

Si(100) 10 $\Omega$ cm *p*-type boron doped wafers were used as substrates. In the first step, the wafers were subjected to a Radio Corporation of America (RCA) cleaning with a finishing dip in buffered HF. Subsequently, the wafers were introduced in an UMS 500 Balzers molecular beam epitaxy chamber. After annealing steps of 1 h at 400 and 750 °C

[a)]Author to whom correspondence should be addressed; electronic mail: czgheib@ndu.edu.lb

 

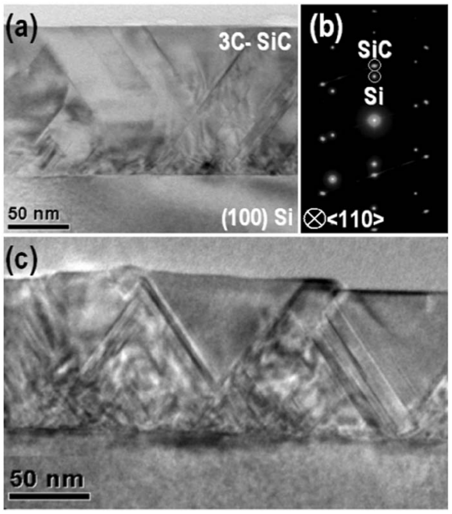


FIG. 1. TEM micrographs of samples with 1 ML of Ge (a) and without Ge (c), and SAED pattern (b) of the interface region shown in (a).

leading to a clean $(2\times 1)$-Si (001)Si reconstructed surface, the temperature was set to 530 °C. After temperature stabilization Ge was deposited on the $(2\times 1)$-Si reconstructed surface in amounts varying from 0 to 4 ML (ML are monolayers with respect to the Si surface). The Ge-modified wafers were transferred to an ultra high vacuum chemical vapor deposition (UHVCVD) chamber where the carbonization and 3*C*-SiC epitaxial overgrowth were carried out. The growth temperature was 1050 °C. The detailed growth procedure is described elsewhere.[16] The 3*C*-SiC layers were chosen to be thin (around 120 nm) to gain insight into the impact of the substrate modification on the early growth stages.

To extract the values of residual strain inside the 3*C*-SiC layers, $\mu$-Raman measurements were performed in backscattering geometry with an Ar-ion laser operating at 488 nm and a spot size of $\approx 4$ $\mu$m. The crystalline quality of the structures was also assessed by transmission electron microscopy (TEM) in both image and diffraction modes, using a TECNAI 20S electron microscope.

Figure 1(a) shows a bright-field TEM micrograph of a sample with 1 ML of Ge presenting a very flat surface. Figure 1(b) displays a selected-area electron diffraction (SAED) pattern taken at the interface region of the same sample on the $\langle 110\rangle$ zone axis. The perfect alignment of both Si and SiC related reflection spots gives an idea of the good epitaxial relationship and crystalline quality of the grown SiC layer. For comparison, a bright field TEM image of the reference sample, i.e., without Ge deposition, was recorded. Figure 1(c) illustrates a surface with distorted terraces and higher surface roughness, indicating the improved crystallinity due to the modification of the silicon substrate by Ge. This observed beneficial effect of the Ge predeposition corresponds to the effect observed in the case of Si(111) substrates and 3*C*-SiC layers grown by molecular beam epitaxy.[15]

In order to extract the strain values inside the 3*C*-SiC layers and to evaluate its variation with the Ge coverage ($Q_{Ge}$) prior to the conversion process of Si into SiC, $\mu$-Raman measurements were carried out. In the Raman spectra the LO and TO modes were evident. According to the selection rule for the (100) surface of a zinc-blende crystal, the LO mode is allowed but the TO mode is forbidden. The

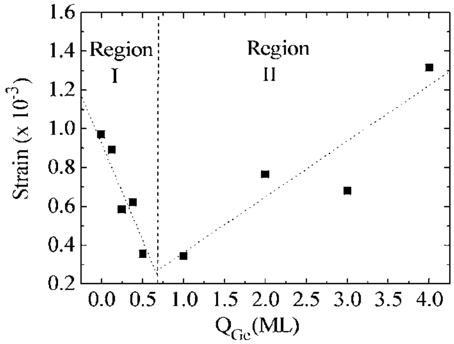


FIG. 2. Strain variation vs Ge coverage $Q_{Ge}$. The solid line shows the border between the two strain regions of strain decrease and increase. The dashed line is a guide for the eyes.

appearance of the TO mode could be due to a certain degree of disorder, i.e., the defect densities, in this epitaxial films and also partially due to a non-perfect backscattering geometry due to the finite focusing angle of the objective of the microscope in the measurements.[5,17] The strain was determined using the method developed by Feng *et al.*[18] after the extraction of the transverse and longitudinal optical phonon modes (TO and LO) by using a Lorentzian fit. Figure 2 shows the effect of the Ge coverage on the strain inside the grown 3*C*-SiC layers.

Two strain regions, I and II, are clearly observed. The strain state inside the 3*C*-SiC layers is always tensile and decreases with increasing Ge coverages, if the predeposited Ge amount is below 1 ML (region I). If the Ge predeposition exceeds 1 ML (region II), the strain increases again. At precoverages above 2 ML Ge (region II) the residual strain in the epitaxial 3*C*-SiC layer grown on Si(100) exceeds the value obtained on substrates without Ge predeposition. The strain reduction reaches a minimum in the 0.5–1 ML precoverage region. The strain value obtained for the reference sample, i.e., without Ge predeposition, is comparable to the values obtained for thicker layers grown at temperatures above 1300 °C,[6] where the strain approaches $2\times 10^{-3}$. In the case of Ge precoverages around the optimum value, the residual strain is lower than in the case of thick 3*C*-SiC layers grown on SOI substrates,[6] where values between $5.0\times 10^{-4}$ and $8\times 10^{-4}$ in dependence on the used SOI substrate were found.

Strain reduction is normally connected to dislocation generation, i.e., higher defects densities. An increase in the defects densities normally lowers the electronic and optical properties of the grown layers. In TEM investigations in the upper part of the 3*C*-SiC layer a substantial change in the defect densities could not be observed with respect to the reference sample, i.e., without Ge. In the interface region the defect densities were too high to formulate a reliable conclusion. For this reason another parameter, which gives access to the overall crystal quality and therefore to the electronic and optical properties, was used: the intensity ratio of the LO and TO phonon modes ($I_{LO}/I_{TO}$).[5,17] This ratio increases with the improvement of the crystalline quality. Figure 3 shows the $I_{LO}/I_{TO}$ intensity ratio as a function of the Ge coverage. The intensity ratio increases up to a Ge predeposition of 2 ML where it reaches a maximum (improvement regime). If this Ge precoverage is exceeded, the 3*C*-SiC quality decreases (deterioration regime; see Fig. 3). Therefore, it can be concluded that the strain reduction is not due

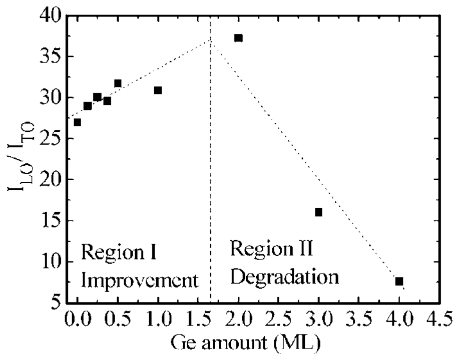


FIG. 3. Dependence of the LO/TO intensity ratio vs Ge coverage $Q_{Ge}$. The solid line shows the border between the regions of crystallinity improvement and deterioration. The dashed line is a guide for the eyes.

to a deterioration of the overall crystalline quality.

Two components of the strain reduction must be considered: (i) extrinsic, i.e., thermal strain caused by the difference in thermal expansion coefficients between Si and 3*C*-SiC, and (ii) intrinsic, also known as the growth strain.[19] The extrinsic part of the residual strain is lowered in the current growth method by lowering the growth temperature to around 1000 °C. The intrinsic part of the residual stress can be and is indeed affected by the presence of a buffer layer between the grown layer and the substrate which reduces the stress in the early stages of the heteroepitaxy. Such a layer can effectively improve the crystalline quality of the grown layer[20] and is affected by the Ge predeposited prior to the conversion of Si into SiC. In the case of Si(111) and molecular beam epitaxy (MBE) growth conditions, it was shown that during the conversion process an ultra thin buffer layerlike structure is formed.[21] This buffer layer and the Ge incorporation into the Si substrate improve the interface properties[22] and the residual stress.[23] So, the heteroeptaxial relationship in a pair of materials with extremely large lattice and thermal expansion mismatch can be improved through the matching of the elasticity-related properties at the interfaces by introducing a Ge-containing buffer layer. This effect was predicted theoretically in an earlier publication.[24]

Based on Fig. 2, it can be concluded that the optimum strain and crystalline quality is reached by using 1ML of Ge. If this amount is exceeded, the nucleation conditions tend to roughen the surface and interface of the conversion layer due to a reduced nucleation density and a pronounced three-dimensional nucleation of the 3*C*-SiC on Si.[25] These effects in turn lead to an increase of the intrinsic stress and to the reduction of the $I_{LO}/I_{TO}$ ratio.

In conclusion, an alternative type of substrate for the heteroepitaxy of 3*C*-SiC on Si(100) has been developed. These substrates consist of a Si(100) wafer with a chemically Ge-modified surface. It allows a reduction of the stress and an improvement of the crystalline quality of the grown 3*C*-SiC layer comparable or better than achieved by using SOI substrates, if the Ge coverage is in the range of 0.5–1 ML. These results can provide a promising route towards the optimization of the heteroepitaxial growth of 3*C*-SiC on silicon substrates.

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