A Describing Function for Resonantly Commutated H-Bridge Inverters

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***Abstract*—The paper presents the derivation of a describing-function to model the dynamic behavior of a metal oxide semiconductor field effect transistor-based, capacitively commutated H-bridge, including a comprehensive explanation of the various stages in the switching cycle. Expressions to model the resulting input current, are also given. The derived model allows the inverter to be accurately modeled within a control system simulation over a number of utility input voltage cycles, without resorting to computationally intensive switching-cycle level, time-domain SPICE simulations. Experimental measurements from a prototype H-bridge inverter employed in an induction heating application, are used to demonstrate a high degree of prediction accuracy over a large variation of load conditions is possible using the simplified model.**

***Index Terms*—Metal oxide semiconductor field effect transistor (MOSFET)-based capacitively commutated H-bridge, switching cycle.**

NOMENCLATURE

C_1	Capacitor across top-side, load commutated power switch.
C_2	Capacitor across top-side, PWM-controlled power switch.
C_3	Capacitor across bottom-side, load commutated power switch.
C_4	Capacitor across bottom-side, PWM-controlled power switch.
$\{C_1 \dots C_4\}$	Capacitance of $\{\mathrm{C}_1 \dots \mathrm{C}_4\}$.
C_{comm}	Capacitance involved in the commutation of the switch.
$C'_{\mathrm{comm(PWM)}}$	Equivalent capacitance involved in the commutation of the PWM leg.
$C'_{\mathrm{comm(Load)}}$	Equivalent capacitance involved in the commutation of the load-commutated leg.
C_{oss}	Parasitic capacitance across the device.
D_1	Antiparallel diode across top-side, load commutated power switch.
D_2	Antiparallel diode across top-side, PWM-controlled power switch.
D_3	Antiparallel diode across bottom-side, load commutated power switch.
D_4	Antiparallel diode across bottom-side, PWM-controlled power switch.
$F_c(V_{\mathrm{dc}})$	Function relating the charge held in the parasitic capacitance of the MOSFET to the dc-link voltage.
f_s	Switching frequency.
I_{cos}	"quadrature" component of the output current vector.
I_{dc}	Input current to the H-Bridge.
I_{out}	Magnitude of the equivalent sinusoidal representation of the output current.
I_{sin}	"in-phase" component of the output current vector."
i_{out}	Time-domain representation of output current from the H-Bridge.
q_1	Charge transferred from the dc-link to the H-bridge during period 1.
q_2	Charge transferred form the dc-link to the H-bridge during period 2.
q_3	Charge transferred form the dc-link to the H-bridge during period 3.
q_4	Charge transferred form the dc-link to the H-bridge during period 4.
q_5	Charge transferred form the dc-link to the H-bridge during period 5.
q_6	Charge transferred form the dc-link to the H-bridge during period 6.
q_7	Charge transferred form the dc-link to the H-bridge during period 7.
q_8	Charge transferred form the dc-link to the H-bridge during period 8.
R_d	On-state resistance of the diode.
R_{on}	On-state resistance of the switch.
SW_1	Top-side, load commutated power switch.
SW_3	Bottom-side, load commutated power switch.
SW_2	Top-side, PWM-controlled power switch.
SW_4	Bottom-side, PWM-controlled power switch.
T_{on}	On-time of the switch.
q_{com}	Charge stored in the total leg capacitance.
$q_{\mathrm{com\ limit}}$	Angle at which the commutation cycle finishes as the opposing switch turns on.
V_d	Time-domain representation of the generic leg voltage during the time that the switches' antiparallel diodes are carrying the output current.
V_{dc}	dc-link voltage.
V_{diode}	Forward voltage of the diode.
V_t	Voltage across the switch at the point of turn-off.
V_{tr}	Forward voltage of switch.
V_{Leg}	FMA equivalent representation of the leg voltage.
v_{com}	Time-domain representation of the generic leg voltage during the time that the commutation capacitors are carrying the output current.

Manuscript received January 27, 2003; revised December 11, 2003. Recommended by Associate Editor B. Fahimi.

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Digital Object Identifier 10.1109/TPEL.2004.830081

$v_{\rm cond}$	Time-domain representation of the generic leg voltage during the time that the switches are carrying the output current.
$v_{\rm ds}$	Voltage across the drain and source terminals of the MOSFET switch.
$v_{\rm LC}$	Time-domain representation of the load commutated leg voltage.
$v_{\rm Leg}$	Time-domain representation of the generic leg voltage.
$v_{\rm PWM}$	Time-domain representation of PWM-controlled leg voltage.
$v_{\rm out}$	Time-domain representation of output voltage from the H-Bridge.
$v_{\rm to}$	Time-domain representation of the generic leg voltage during the time that the switches are turning off.
θ_1	Angle at which the switch starts to turn off.
θ_2	Angle at which the switch completes turn-off.
θ_3	Angle at which the commutation finishes.
θ_d	Phase of the equivalent sinusoidal representation of the output current.
α_1	Angle at which $\rm SW_4$ starts to turn off.
α_2	Angle at which $\rm SW_4$ completes turn-off.
α_3	Angle at which the commutation of $\rm SW_4$ finishes.
β_1	Angle at which $\rm SW_1$ starts to turn off.
β_2	Angle at which $\rm SW_1$ completes turn-off.
β_3	Angle at which the commutation of $\rm SW_1$ finishes.

I. Introduction

THE MOST common high-frequency inverter circuit employed in an industrial environment consists of a capacitively commutated metal oxide semiconductor field effect transistor (MOSFET)-based H-bridge, a dc-link smoothing filter, Fig. 1, together with monitoring and feedback electronics. For high-frequency applications, the basic H-bridge is often augmented with capacitors $(\rm C_1 \ldots C_4)$ in parallel with the power switches, to facilitate zero-voltage commutation of the inverter legs; a feature that has been shown to be advantageous in both IGBT and MOSFET-based bridges [1] since it allows high efficiency operation with very low switching loss. It also permits some control of $dv_{\rm out}/dt$ at the output, thereby mitigating EMC problems. However, the incorporation of commutation capacitors has significant impact on the dynamic operation of the circuit, as the bridge commutation period becomes a significant proportion of the switching period. This substantially increases the complexity of models that can accurately predict circuit behavior, since they are required to describe the output voltage characteristics during the commutation periods, when the commutation capacitors support the output current. Although modeling the operation of low-power LCC resonant converters with half-bridge switch networks [3] has been addressed with some success, the dynamic effects of commutation components in a full H-bridge, for high power systems, remains outstanding.

Here then, the complex commutation effects within the H-bridge inverter are described, along with time-domain and static performance characteristics. From this, a describing-function to model the input/output characteristics of inverter operation, is derived, and subsequently employed to predict system output current against PWM duty, thereby providing a macro-model of the H-bridge; a feature necessary to accurately, and rapidly, model an inverter within a control system simulation, for instance. Indeed, the proposed model typically executes some 10 000 times faster than component-based simulation packages such as Spice. Additionally, the resulting model is sufficiently detailed to provide enhanced predictions of efficiency throughout the circuit, and facilitate optimized design and performance sensitivity results with respect to component values and tolerances. To provide a practical focus to the paper, application of the presented techniques is considered for modeling a 2.5-kW inverter employed in an induction heating system.

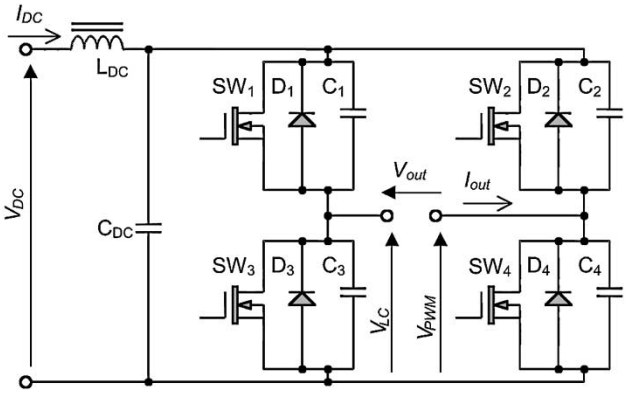

Fig. 1. Inverter circuit.

II. Circuit Operation

The preferred use of high switching frequencies to reduce the size of reactive system components (or to achieve specific heating patterns in the case of induction heating), means that device switching can become the most significant loss mechanism within the inverter. Low-loss commutation strategies are therefore desirable, the most effective being zero-voltage commutation [2].

Since PWM is a requirement for control of power to the load, only one leg of the inverter ($\rm SW_1$ and $\rm SW_3$, for instance) can switch at the zero-crossing times of the load current, while the remaining leg must commutate appropriately to provide the effective duty-cycle at the output, under zero-voltage commutation. This facilitates controlled power transfer without additional power preprocessing stages. To minimize switching losses in the fixed, "load commutated" leg, $\rm SW_1$ and $\rm SW_3$ are turned off as the output current is about to pass through zero. Although this appears to utilize zero current commutation, the devices are, in fact, commutated under reduced voltage by virtue of the presence of the commutation capacitors $\rm C_1$ and $\rm C_3$. This combination of low current and low voltage at the switching instant significantly reduces switching losses, and constitutes operation under optimal conditions described by Dede *et al.* [2]. However, since the output voltage is controlled using pulse width modulation (PWM), $\rm SW_2$, and $\rm SW_4$ cannot be load commutated in the same manner. Consequently, capacitors $\rm C_2$ and $\rm C_4$ are included to allow zero-voltage commutation

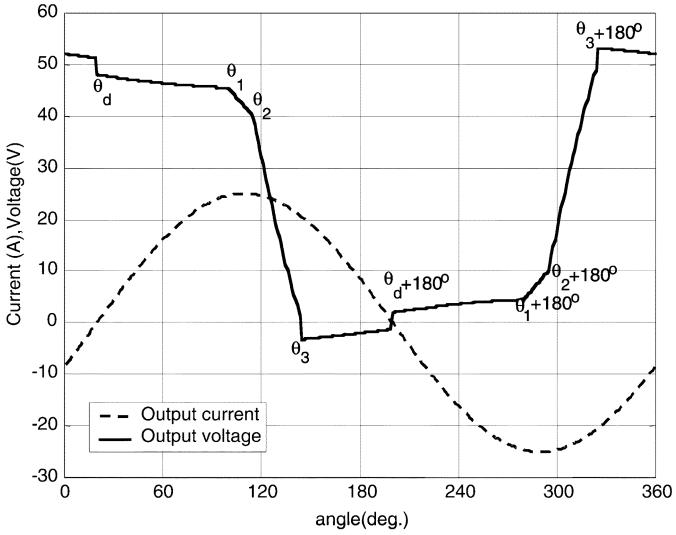

Fig. 2. Inverter leg voltage and load current.

of SW_2 and SW_4, thereby reducing the switching losses and decreasing the dv/dt across the switches. C_2 and C_4 are larger than C_1 and C_3, as the potential instantaneous currents they are to handle are higher, given that the instantaneous maximum in the output current may occur during the commutation event. The resulting inverter output voltage is then given by the difference between the inverter bridge-leg voltages (1) (see Fig. 1)

$$v_{\rm out} = v_{\rm LC} - v_{\rm PWM}. \tag{1}$$

The characteristics of both $v_{\rm LC}$ and $v_{\rm PWM}$ may be analyzed independently and subsequently combined to give the overall describing function for the inverter output voltage.

III. Generic Model of Leg Voltage

Typical leg-voltage $(v_{\rm Leg})$ and current $(i_{\rm out})$ waveforms during steady-state operation of the inverter are shown in Fig. 2, where the output of the leg is loaded by a sinusoidal current sink [see Fig. 3(a)] and time has been normalized based on the switching period to provide waveforms as a function of angle. A describing function modeling the behavior of the leg of the inverter is obtained by considering the piecewise time-domain operation of the inverter between the various mode transition angles θ_n shown in Fig. 2.

The phase reference for the voltage, $\theta = 0$, coincides with the turn-on of the upper top-left switch, SW_1 in Fig. 1, and occurs while the anti-parallel diode is conducting. The anti-parallel diode ceases to conduct at θ_d, which also defines the phase-shift between the output voltage and the sinusoidal output current, described by

$$i_{\rm out}(\theta) = I_{\rm out}\sin(\theta - \theta_d). \tag{2}$$

During the period $\theta_d \rightarrow \theta_1$, SW_1 is forward conducting and the leg voltage during this time, $v_{\rm cond}$, is modeled as a quasisquare

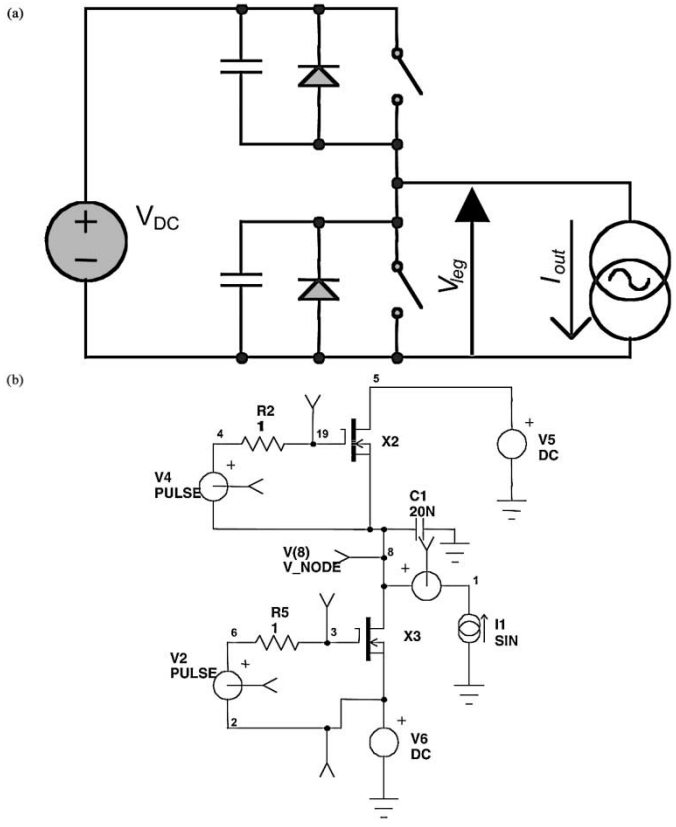

Fig. 3. (a) Generic inverter leg model and (b) Spice model circuit.

wave modified by a sinusoidal perturbation to account for conduction resistance of the switching device

$$v_{\rm Leg}(\theta) = v_{\rm cond}(\theta) = \begin{cases} V_{\rm DC} - V_{\rm tr} - i_{\rm out}(\theta)R_{\rm on} & \theta = \theta_d \ldots \theta_1 \\ V_{\rm tr} - i_{\rm out}(\theta)R_{\rm on} & \theta = \pi + \theta_d \ldots \pi + \theta_1 \end{cases} \tag{3}$$

where the forward-conduction voltage drop of the device, $V_{\rm tr}$, is included to allow for either reverse conduction blocking diodes or the use of IGBTs. Reverse blocking diodes may be used when several MOSFETs are paralleled, since the rate-of-change of diode forward voltage with temperature does not encourage current sharing of the devices during the diode conduction phase. Also given in (3) is the voltage characteristic during the phase period $\theta = \pi + \theta_d$ to $\pi + \theta_1$ when the opposite switch in the bridge leg is conducting (SW_3 in Fig. 1).

During the period $\theta_1 \rightarrow \theta_2$, the voltage across SW_1 rises to V_t, the "terminal" voltage of the switch. Extensive practical measurements show that this rise can be modeled as being essentially linear. The leg voltage, $V_{\rm to}$, therefore reduces accordingly during this time, as described by (4), shown at the bottom of the next page. The leg voltage during the complementary time, when SW_3 carries current, is also given in (4).

During the period when commutation occurs, $\theta_2 \rightarrow \theta_3$, the current from the resonant load charges the capacitance across the switches. The total capacitance consists of the nonlinear parasitic drain-source capacitance $(C_{\rm oss})$, Fig. 4, of both the transistor that is turning off and its complimentary paring, and any

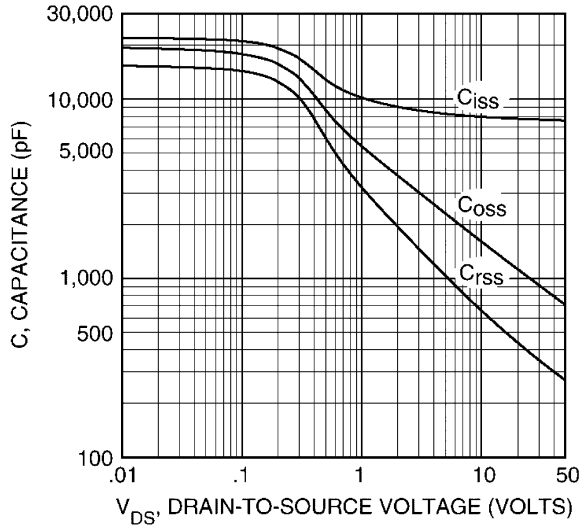

Fig. 4. Voltage dependency of MOSFET parasitic capacitances (reproduced courtesy of Advanced Power Technology: APT5010LVR).

additional component capacitance connected across the transistor. At low voltages, the drain-source capacitance dominates, while the commutation capacitance dominates at high voltages.

Since SW_1 can be considered to be 'off' during this phase, all load current flows into the commutation capacitors and the parasitic drain-source capacitances. As the parasitic capacitors are a nonlinear function of applied voltage, the calculation of the commutation angle can be simplified by assuming SW_1 turns off instantaneously, and the commutation capacitance is charged until it reaches the applied dc-link voltage. The stored charge is the integral of the output current, (5), taken over the commutation period, as given in

$$i_{\mathrm{out}}(t) = I_{\mathrm{out}} \sin(2\pi f_s t + \theta_d) \tag{5}$$

$$q_{\mathrm{com}} = \frac{I_{\mathrm{out}}}{2\pi f_s} \int_{\theta_2}^{\theta_3} \sin(\theta + \theta_d)\, d\theta \tag{6}$$

which can be solved for θ_3

$$\theta_3 = \pi + \theta_d - \cos^{-1}\left(\frac{2\pi f_s q_{\mathrm{com}}}{I_{\mathrm{out}}} - \cos(\theta_2 - \theta_d)\right). \tag{7}$$

By assuming a sinusoidal leg current, and noting the voltage is $\pi/2$ radians out of phase with the current, and of the same frequency, the output voltage can be written as (8), shown at the bottom of the page. Finally, between $\theta = \theta_3$ and $\theta = \pi + \theta_d$, the voltage across SW_1 exhibits a similar characteristic to the switch conduction period, differing only in the polarity of the offset. In particular, if the diode resistance R_d is equal to the switch on-state resistance, R_{tr}, and the conducting voltage drop across the diode, V_{diode}, is equal to the switch on-state voltage drop, V_{tr}, then $v_d(\theta) = v_{\mathrm{cond}}(\theta)$. In the more general case however, the output voltage is described by (9), shown at the bottom of the page. Equations (2)–(9), therefore, provide a generic piecewise description of the steady-state behavior of the inverter under the rather mild assumptions that 1) diode reverse recovery does not significantly influence the behavior of the inverter/load combination, 2) instantaneous output current remains positive during the period $\theta = \theta_1 \rightarrow \pi$, and 3) the switch rather than the diode carries the current in the period $\theta = 0 \rightarrow \theta_1$. The latter two conditions hold for a MOSFET, providing the magnitude of the instantaneous device current is less than that required to create a body-resistance voltage-drop of sufficient value to forward bias the internal anti-parallel diode into its conducting state.

To show the validity of the presented piecewise model of the inverter switching characteristics, a SPICE-based model of the inverter leg employing International Rectifier IRFPS40N50L MOSFET devices is used, Fig. 3(b). A sinusoidal current source is included to represent the effects of the resonant output load.

$$v_{\mathrm{Leg}} = v_{\mathrm{to}}(\theta) = \begin{cases} V_{\mathrm{DC}} - V_{\mathrm{tr}} - R_{\mathrm{on}} I_{\mathrm{out}} \sin(\theta_1 - \theta_d) - \left((\theta - \theta_1)\dfrac{V_t - V_{\mathrm{tr}} - R_{\mathrm{on}} I_{\mathrm{out}} \sin(\theta_1 - \theta_d)}{\theta_2 - \theta_1}\right) & \theta = \theta_1 \ldots \theta_2 \\ V_{\mathrm{tr}} + R_{\mathrm{on}} I_{\mathrm{out}} \sin(\theta_1 - \theta_d) + \left((\theta - \theta_1 - \pi)\dfrac{V_t - V_{\mathrm{tr}} - R_{\mathrm{on}} I_{\mathrm{out}} \sin(\theta_1 - \theta_d)}{\theta_2 - \theta_1}\right) & \theta = \theta_1 + \pi \ldots \theta_2 + \pi \end{cases} \tag{4}$$

$$v_{\mathrm{Leg}} = v_{\mathrm{com}}(\theta) = \begin{cases} V_{\mathrm{DC}} - V_d - \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta_d - \theta_2) + \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta - \theta_d) & \theta = \theta_2 \ldots \theta_3 \\ V_d - \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta_d + \pi - \theta_2) + \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta - \theta_d) & \theta = \theta_2 + \pi \ldots \theta_3 + \pi \end{cases} \tag{8}$$

$$v_{\mathrm{Leg}} = v_d(\theta) = \begin{cases} -V_{\mathrm{diode}} - I_{\mathrm{out}} \sin(\theta - \theta_d) R_d & \theta = \theta_3 \ldots \pi + \theta_d \\ V_{\mathrm{DC}} + V_{\mathrm{diode}} - I_{\mathrm{out}} \sin(\theta - \theta_d) R_d & \theta = \theta_3 + \pi \ldots 2\pi + \theta_d \end{cases} \tag{9}$$

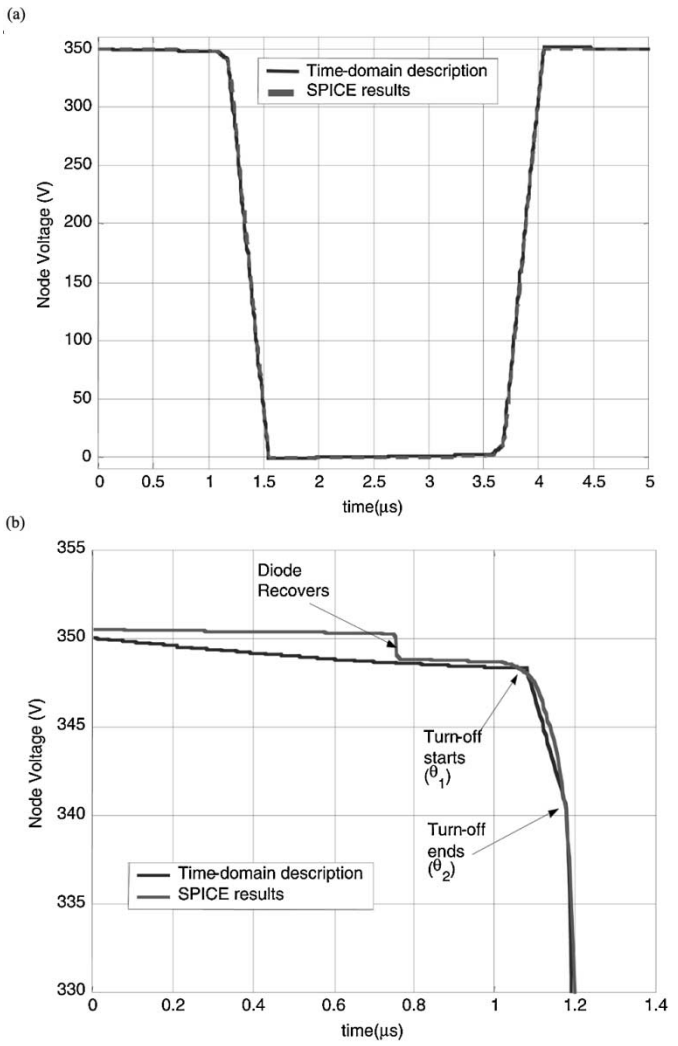

Fig. 5. (a) Switching cycle and (b) detail of diode recovery and transistor turn-off.

A comparison of results from time-domain SPICE simulations, with the predicted behavior of the inverter [from (3)–(9)], is shown in Fig. 5(a), and indicates good correspondence is achievable during the majority of the cycle. Fig. 5(b) shows a magnified view to indicate the typical influence of diode recovery, along with details of the transistor turn-off period. It can be seen that while there is a small difference in the shape of the output voltage waveforms, the times at which the turn-off begins and ends, and the voltages at which these occur, are predicted accurately by the model. {Note: the SPICE results show the diode actually providing energy into the system during recovery. This is not an appropriate characteristic and is therefore not included in the piecewise time-domain model}.

IV. Describing Function of Generic Inverter Leg

To derive the fundamental mode approximation (FMA) describing-function of a generic inverter leg, and investigate the domain of applicability of the proposed model, operation of the circuit [Fig. 3(b)] is considered for various switch turn-off angles, θ_1, between $\theta_1 = \theta_d \rightarrow \pi$. The describing function of the leg is initially obtained by taking the *Re*al and *Im*aginary components of the fundamental from the FFT of the resulting time-domain leg voltage waveform. The resulting voltages from SPICE simulations along with those from the describing function are compared in Fig. 6. To preserve the phase information, results are analyzed by considering both the *Re*al and *Im*aginary components of the leg voltage, individually. The maximum applied pulse-width is limited by the necessity for the commutation capacitors to fully charge to the dc-link rail voltage before the output current changes polarity. This is indicated in Fig. 6 by the "$q_{\rm com}$ limit." Values of θ_2 greater than this give rise to truncated commutation, whereby the capacitor is partly discharged by the opposing transistor turning on. The good correlation between results from the derived model (line) and those from SPICE simulations, Fig. 6, indicate that the dominant characteristics of the inverter leg are captured by the proposed model, particularly for $\theta_2 > \pi/3$ radians (60°) (conduction time of switch ≈0.8 μs); below this value diode reverse recovery dominates the turn-off characteristics. It is also of note that some discrepancy between the results occurs above the $q_{\rm com}$ limit (especially the imaginary component) due to the assumption that a device switches-on at the instant that the current passes through zero ($\theta = 0, \pi, 2\pi$ etc). If the total switch capacitance is not fully charged at the end of half a switching cycle, a result of employing a piecewise model is that it necessarily predicts a step change in the leg voltage. This cannot occur in practice since it implies a finite amount of charge must be transferred to the commutation capacitance in zero time. The domain of applicability of the model is therefore bounded by the assumption that complete charging of the commutation capacitance can occur during half a switching cycle. In reality, circuit operation outside this domain results in large transient current flows through the switching devices, leading to a significant increase in both switching device loss and electromagnetic noise.

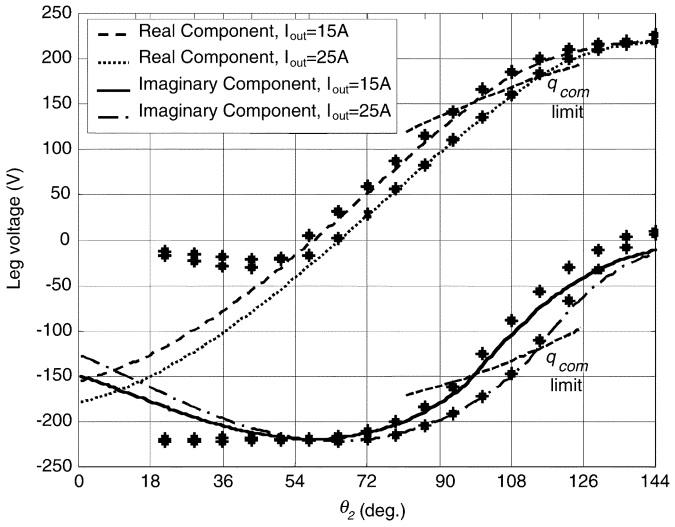

Fig. 6. Leg voltage components.

V. Model Reduction

Although the proposed model incorporates the dominant characteristic of switching behavior, the complexity can be reduced by considering the impact of each parameter $(C_{\rm comm}, V_t, R_{\rm on}, V_d, R_d)$ on the FHA equivalent output voltage of the bridge leg ($V_{\rm Leg}$). Applying a sinusoidal current

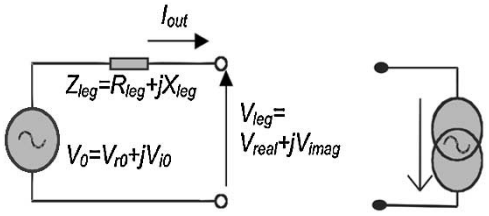

Fig. 7. Thévenin equivalent source.

sink to the output of the piecewise description of the bridge leg, resulting in an output voltage V_{Leg}, allows the impact of variations in the circuit parameters to be determined by considering a Thévenin equivalent circuit representation (Fig. 7).

As the proposed model of the bridge leg is only valid for a defined range of output currents viz. those allowing correct commutation of the bridge leg, two output current levels selected from small perturbations about a nominal operating point, are used to find the Thévenin components, Z_{leg} and V_0, for each perturbation of either $C_{\mathrm{comm}}, V_t, R_{\mathrm{on}}, V_d, R_d$.

Each component is selected individually for analysis, and its value is halved; a "new" Thévenin equivalent circuit then being obtained for each case. Sensitivity to variations in each component is assessed by repeating the process for a range of pulse widths (θ_1), and calculating the RMS variation of the Thévenin model components from those of the original. The results of these analyzes are summarized in Fig. 8, from which it can be seen the components that have the greatest influence on output voltage are C_{comm}, V_t and R_{on}. Consequently, the original piecewise time-domain model [(3)–(9)] can be simplified to (10) by only including the influence of these elements. In particular, the output is assumed to begin at exactly the dc-link voltage while the diode is forward biased $(\theta = 0 \rightarrow \theta_d)$, and then be subject to a voltage drop due to the body resistance of the MOSFET until the end of the MOSFET turn-off period $(\theta = \theta_d \rightarrow \theta_2)$. Although the actual turn-off ramp is not now directly considered, the time period of the ramp is, since the commutation capacitor charging period is very sensitive to the starting time. The commutation capacitor charging profile is also dependent on the starting voltage, so the portion of the leg-voltage due to commutation begins at an angle θ_2, and voltage, $V_{\mathrm{dc}} - V_t$. This implies a discontinuity in the characteristic of $\approx -V_t$ at θ_2. After the commutation event (at θ_3), the voltage is clamped to 0 V. The second half of the operation sequence then commences analogously as (10), shown at the bottom of the page.

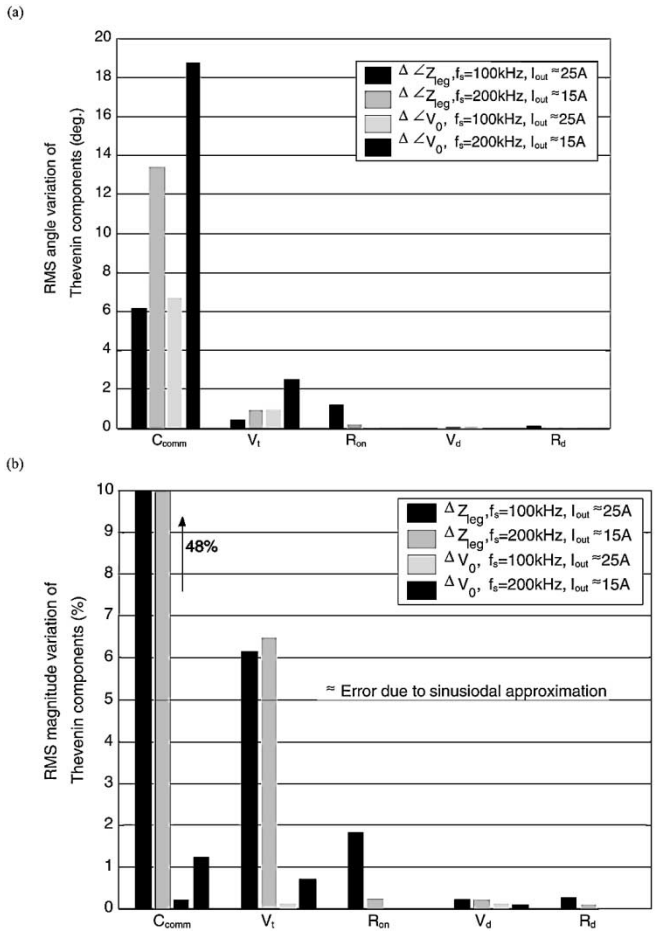

Fig. 8. Effect of different elements of the time-domain description on the Thévenin equivalent circuit (a) angle and (b) magnitude.

VI. Describing Function of Inverter Leg

A describing function to model the inverter leg is obtained from a FHA of (10). This is most conveniently found from the first harmonic of the Fourier series of the leg voltage described in the "angle-domain," Since the relative phase shift of the output voltage is important, the complex form of the output voltage vector is retained $(V_{\mathrm{Leg}}(\mathrm{FMA}) = V_{\mathrm{real}} + jV_{\mathrm{imag}})$, resulting in the describing function being comprised of both *Re*al and *Im*aginary components (11), (12). To simplify notation, i_{out} is also divided into constituent components I_{sin} and I_{cos}, where I_{sin} is in phase with V_{real}, and I_{cos} correspond-

$$v_{\mathrm{Leg}}(\theta) = \begin{cases} V_{\mathrm{dc}}, & \theta = 0 \ldots \theta_d \\ V_{\mathrm{dc}} - I_{\mathrm{out}} R_{\mathrm{on}} \sin(\theta - \theta_d), & \theta = \theta_d \ldots \theta_2 \\ \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta - \theta_d) + V_{\mathrm{dc}} - V_t - \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta_d - \theta_2), & \theta = \theta_2 \ldots \theta_3 \\ 0, & \theta = \theta_3 \ldots \pi + \theta_d \\ -I_{\mathrm{out}} R_{\mathrm{on}} \sin(\theta - \theta_d), & \theta = \pi + \theta_d \ldots \pi + \theta_2 \\ \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta - \theta_d) + V_t - \dfrac{I_{\mathrm{out}}}{2\pi f_s C_{\mathrm{comm}}} \cos(\theta_d - \theta_2 + \pi), & \theta = \pi + \theta_2 \ldots \pi + \theta_3 \\ V_{\mathrm{dc}}, & \theta = \pi + \theta_3 \ldots 2\pi \end{cases} \tag{10}$$

ingly leading by $\pi/2$ radians; thus $I_{\text{out}} = \sqrt{I_{\text{sin}}^2 + I_{\text{cos}}^2}$ and $\tan(\theta_d) = (I_{\text{sin}})/(I_{\text{cos}})$

$$\begin{aligned} V_{\text{real}} = \Bigg\{ & -\frac{2V_{\text{DC}}}{\pi}\cos(\theta_3) + \frac{R_{\text{on}}}{2\pi}((\sin(2\theta_2) - 2\theta_2)I_{\text{sin}} \\ & + (\cos(2\theta_2) - 1)I_{\text{cos}}) \\ & + \frac{2V_t}{\pi}(\cos(\theta_3) - \cos(\theta_2)) \\ & + \frac{I_{\text{sin}}}{4\pi^2 f_s C_{\text{comm}}}(4\cos(\theta_2)\cos(\theta_3) \\ & - \cos(2\theta_3) - \cos(2\theta_2) - 2) \\ & + \frac{I_{\text{cos}}}{4\pi^2 f_s C_{\text{comm}}}(2\theta_2 - 2\theta_3 - 4\sin(\theta_2)\cos(\theta_3) \\ & + \sin(2\theta_2) + \sin(2\theta_3)) \Bigg\} \end{aligned} \tag{11}$$

$$\begin{aligned} V_{\text{imag}} = \Bigg\{ & \frac{2V_{\text{DC}}}{\pi}\sin(\theta_3) + \frac{R_{\text{on}}}{2\pi}((\cos(2\theta_2) - 1)I_{\text{sin}} \\ & + (-\sin(2\theta_2) - 2\theta_2)I_{\text{cos}}) \\ & + \frac{2V_t}{\pi}(\sin(\theta_2) - \sin(\theta_3)) \\ & + \frac{I_{\text{sin}}}{4\pi^2 f_s C_{\text{comm}}}(-2\theta_2 + 2\theta_3 + \sin(2\theta_2) \\ & + \sin(2\theta_3) - 4\cos(\theta_2)\sin(\theta_3)) \\ & + \frac{I_{\text{cos}}}{4\pi^2 f_s C_{\text{comm}}}(4\sin(\theta_2)\sin(\theta_3) \\ & + \cos(2\theta_2) + \cos(2\theta_3) - 2) \Bigg\}. \end{aligned} \tag{12}$$

The switching behavior of a single inverter leg can now be generalized to model both legs of the inverter H-bridge; the output voltage then being between the mid-point node of each leg.

To identify each set of equations with the appropriate leg, $\alpha_{\{1,2,3...\}}, C'_{\text{comm(PWM)}}$ and $\beta_{\{1,2,3...\}}, C'_{\text{comm(LOAD)}}$ are employed, respectively, for describing the characteristics of the "PWM-commutated leg" and the "load commutated leg," where the angles $\alpha_{\{1,2,3...\}}$ replace the general angles $\theta_{\{1,2,3...\}}$ to mark the various switching events in the PWM-commutated leg, and the angles $\beta_{\{1,2,3...\}}$ replace the general angles $\theta_{\{1,2,3...\}}$ to mark the various switching events in the load-commutated leg. The output voltage is found by effectively subtracting the voltage of the "load-commutated leg" from that of the "PWM leg." Now, since the upper switch in the PWM leg is turned on π radians out of phase with the load-commutated leg, and the output current similarly reversed, the voltage at the PWM leg must be derived with a π radians phase-shift. Therefore, the output voltage is actually found by adding the voltage contribution of each leg

$$\begin{aligned} V_{\text{out}} = \Bigg\{ & -\frac{2V_{\text{DC}}}{\pi}(\cos(\alpha_3) + \cos(\beta_3)) \\ & + \frac{R_{\text{on}}}{2\pi}((\sin(2\alpha_2) + \sin(2\beta_2) - 2\alpha_2 - 2\beta_2)I_{\text{sin}} \\ & + (\cos(2\alpha_2) + \cos(2\beta_2) - 2)I_{\text{cos}}) \\ & + \frac{2V_t}{\pi}(\cos(\alpha_3) + \cos(\beta_3) - \cos(\alpha_2) - \cos(\beta_2)) \\ & + \frac{I_{\text{sin}}}{4\pi^2 f_s C'_{\text{comm(PWM)}}}(4\cos(\alpha_2)\cos(\alpha_3) \\ & - \cos(2\alpha_3) - \cos(2\alpha_2) - 2) \\ & + \frac{I_{\text{cos}}}{4\pi^2 f_s C'_{\text{comm(PWM)}}}(2\alpha_2 - 2\alpha_3 \\ & - 4\sin(\alpha_2)\cos(\alpha_3) + \sin(2\alpha_2) + \sin(2\alpha_3)) \\ & + \frac{I_{\text{sin}}}{4\pi^2 f_s C'_{\text{comm(Load)}}}(4\cos(\beta_2)\cos(\beta_3) \\ & - \cos(2\beta_3) - \cos(2\beta_2) - 2) \\ & + \frac{I_{\text{cos}}}{4\pi^2 f_s C'_{\text{comm(Load)}}}(2\beta_2 - 2\beta_3 \\ & - 4\sin(\beta_2)\cos(\beta_3) + \sin(2\beta_2) + \sin(2\beta_3)) \Bigg\} \\ & + j\Bigg\{ \frac{2V_{\text{DC}}}{\pi}(\sin(\alpha_3) + \sin(\beta_3)) \\ & + \frac{R_{\text{on}}}{2\pi}((\cos(2\alpha_2) + \cos(2\beta_2) - 2)I_{\text{sin}} \\ & - (\sin(2\alpha_2) + \sin(2\beta_2) + 2\alpha_2 + 2\beta_2)I_{\text{cos}}) \\ & + \frac{2V_t}{\pi}(\sin(\alpha_2) - \sin(\alpha_3) + \sin(\beta_2) - \sin(\beta_3)) \\ & + \frac{I_{\text{sin}}}{4\pi^2 f_s C'_{\text{comm(PWM)}}}(-2\alpha_2 + 2\alpha_3 + \sin(2\alpha_2) \\ & + \sin(2\alpha_3) - 4\cos(\alpha_2)\sin(\alpha_3)) \\ & + \frac{I_{\text{cos}}}{4\pi^2 f_s C'_{\text{comm(PWM)}}}(4\sin(\alpha_2)\sin(\alpha_3) \\ & + \cos(2\alpha_2) + \cos(2\alpha_3) - 2) \\ & + \frac{I_{\text{sin}}}{4\pi^2 f_s C'_{\text{comm(Load)}}}(-2\beta_2 + 2\beta_3 + \sin(2\beta_2) \\ & + \sin(2\beta_3) - 4\cos(\beta_2)\sin(\beta_3)) \\ & + \frac{I_{\text{cos}}}{4\pi^2 f_s C'_{\text{comm(Load)}}}(4\sin(\beta_2)\sin(\beta_3) \\ & + \cos(2\beta_2) + \cos(2\beta_3) - 2) \Bigg\}. \end{aligned} \tag{13}$$

It should be noted that $C'_{\text{comm(Load)}}, C'_{\text{comm(PWM)}}$ are "equivalent capacitances" that include the nonlinear parasitic output capacitance of the switching device. A degree of verification of the model can be seen from Fig. 9, where, by fixing α_1, V_{DC} and I_{out}, and varying β_1, a good correlation between SPICE and the derived results is evident for values of device on-time, T_{on}, greater than the diode recovery time of 0.8 μs.

A. Output Voltage Range Versus Frequency

As the operating frequency is increased, the required commutation capacitor charge time leads to a relative increase in the switching time of the leg with respect to the switching period. This acts to increase the output voltage for low values of output pulse width, controlled by β_1 (α_1 being fixed), while, conversely, acting to decrease the output voltage for high pulse widths (β_3 approaching π radians). It is therefore apparent that the commutation capacitor charging-time constrains the range of β_1, hence limiting the time that the output voltage can be clamped to the supply.

B. Input Current

The average current drawn by the inverter is the product of the total charge drawn from the source over a switching cycle, and the switching frequency. From Figs. 1 and 10 (which shows one

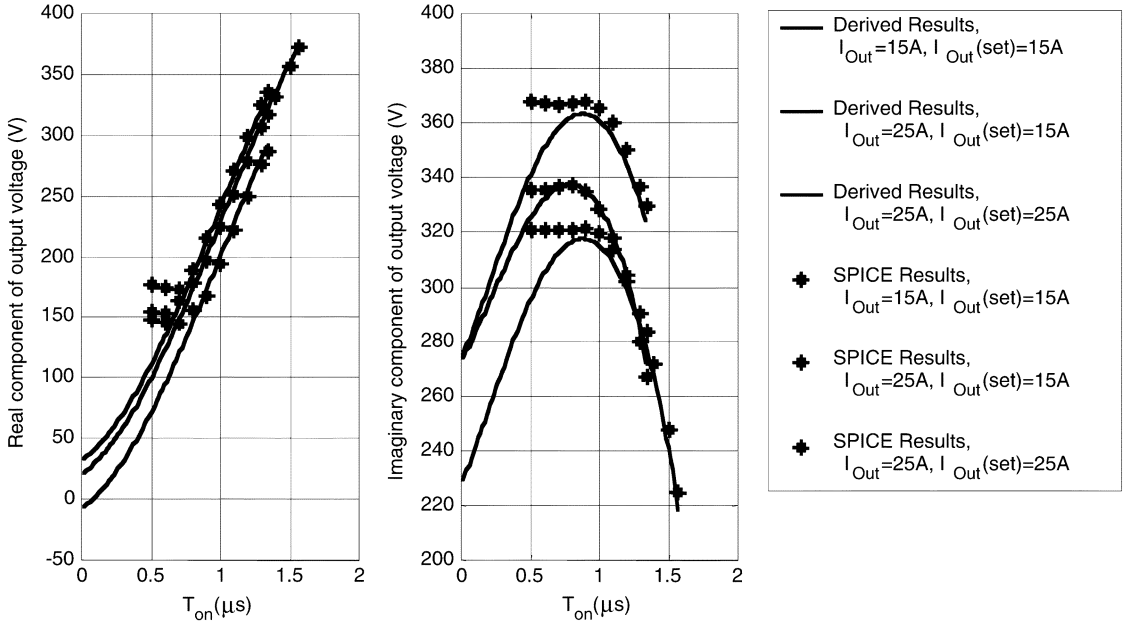

Fig. 9. Total output voltage from the inverter.

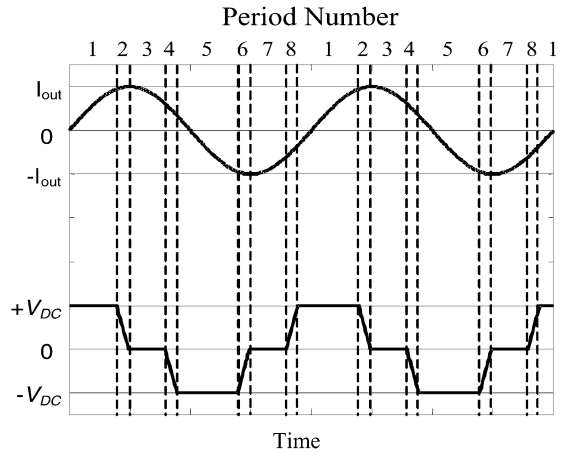

Fig. 10. Definition of Periods 1 to 8.

cycle of the inverter output voltage and current subdivided into time-domain piece-wise components), an analytical function for the averaged supply input current can be obtained by successively considering each of the eight steady-state operating periods.

1) Period 1: $\{(\alpha_3 - \pi)$ to $\beta_2\}$*:* During Period 1 the load is connected across the supply by D_1 and D_4, and subsequently by the operation of SW_1 and SW_4. The charge flowing from the supply for this period can be seen to be a function of the output current. Assuming the output current is sinusoidal with a variable phase-shift such that the diodes do not become reverse biased before their anti-parallel transistors turn on, the charge can be found by integration

$$\begin{aligned} q_1 &= \frac{1}{2\pi f_s} \int_{\alpha_3 - \pi}^{\beta_2} i_{\mathrm{out}}(\theta)\, d\theta \\ &= \frac{I_{\cos}}{2\pi f_s}[\sin(\alpha_3) + \sin(\beta_2)] \\ &\quad - \frac{I_{\sin}}{2\pi f_s}[\cos(\alpha_3) + \cos(\beta_2)]. \end{aligned} \tag{14}$$

Although the solution is dependent on output current (amplitude and phase) and commutation angles, it is not explicitly dependent on supply voltage. However, implicitly, the output current is a function of the (complex) output voltage, which, in turn, is a function of the supply voltage. Moreover, α_3 is a function of the supply voltage and the output current.

2) Period 2: $\{\beta_2$ to $\beta_3\}$*:* Here, the load current is apportioned to discharging C_2 and charging C_4 (from the supply), the magnitude of each being determined by the ratio of capacitances $C_2 : C_4$. Since the parasitic capacitances across the switching devices vary as a function of applied voltage, the instantaneous supply current varies over the commutation period. The charge flowing from the dc link is therefore equal to that required to charge C_4 (plus the parasitic capacitance across the source-drain terminals of SW_4) from 0 V to V_{DC} (15). The function relating the charge stored in the nonlinear parasitic capacitor across the MOSFET, to the dc link voltage, $F_c(V_{\mathrm{dc}})$, is found by integrating the MOSFET output capacitance, C_{oss}, as a function of v_{ds}

$$q_2 = C_4 V_{\mathrm{DC}} + F_c(V_{\mathrm{DC}}). \tag{15}$$

Equation (15) is also approximately correct given the case of truncated commutation, since, if C_2 is not completely discharged at the end of the cycle, SW_2 will turn-on and charge C_4 from the dc link, while rapidly discharging C_2. The energy stored in C_2 will then dissipate in SW_2, increasing switching loss.

3) Period 3: $\{\beta_3$ to $\alpha_2\}$*:* The output current circulates through SW_1 and D_2, and hence, no current is drawn from the supply

$$q_3 = 0. \tag{16}$$

4) Period 4: $\{\alpha_2$ to $\alpha_3\}$*:* The load current is divided into a portion circulating via C_1, and the other from the load, through C_3 and into the supply. The current to the supply is of opposite

polarity to that discussed for Period 2: therefore energy is returned. The charge flowing from the supply to the H-Bridge is therefore that required to discharge C_3 and the parasitic capacitance across SW_3

$$q_4 = -C_3 V_{DC} - F_c(V_{DC}). \tag{17}$$

5) Period 5: $\{\alpha_3 \text{ to } (\pi+\beta_2)\}$*:* Initially, current flows from the load, via D_2 and D_3, to the supply; on reversal it flows from the supply, through SW_2 and SW_3 to the load, (similar to Period 1)

$$q_5 = \frac{1}{2\pi f_s}\int_{\alpha_3}^{\beta_2+\pi} -i_{out}(\theta)\,d\theta. \tag{18}$$

The sign change is due to the voltage across the load being reversed. Considering the sign change as a phase shift of π radians, (18) simplifies to (19), which is equivalent to q_1

$$q_5 = \frac{I_{cos}}{2\pi f_s}[\sin(\alpha_3)+\sin(\beta_2)] - \frac{I_{sin}}{2\pi f_s}[\cos(\alpha_3)+\cos(\beta_2)] = q_1. \tag{19}$$

6) Period 6: $\{(\pi+\beta_2) \text{ to } (\pi+\beta_3)\}$*:* Here, current is drawn from the supply in charging C_2 via the load. If C_2 is equal to C_4, then q_6 is equal to q_2

$$q_6 = C_2 V_{DC} + F_c(V_{DC}). \tag{20}$$

7) Periods 7 & 8: During Period 7, the load current circulates through SW_3 and D_4 (similar to Period 3) and the charge from the supply will be zero

$$q_7 = 0. \tag{21}$$

During Period 8, SW_3 commutates, with some of the output current flowing through C_3 and D_4, the remainder flowing through C_1, D_4 to the supply. Charge flowing into the supply is therefore equal to the requirements to charge C_1 from 0 V to $+V_{DC}$ [see (22)]. If C_1 equals C_3, then q_8 is equal to q_4

$$q_8 = -C_1 V_{DC} - F_c(V_{DC}). \tag{22}$$

a) Average Input Current: The average input current is given by the product of the sum of $q_1 \rightarrow q_8$, and the switching frequency. It is notable that terms relating to the charge stored in the parasitic capacitance of the MOSFETs cancel, leaving

$$I_{dc} = \frac{I_{cos}}{\pi}[\sin(\alpha_3)+\sin(\beta_2)] - \frac{I_{sin}}{\pi}[\cos(\alpha_3)+\cos(\beta_2)] + (C_2 + C_4 - C_1 - C_3)V_{DC} f_s. \tag{23}$$

A comparison of results of I_{dc} from (23), with those from SPICE simulations, is given in Fig. 11 for a variety of β_2 and I_{out}, where a close agreement is apparent for $T_{on} > \sim 0.8\ \mu s$ (corresponding to the reverse recovery time of the SPICE-model diodes). The high degree of correlation remains even when the PWM leg undergoes truncated commutation (i.e., when T_{on} is greater than the q_{com} limit), which is consistent with our analysis, which does not consider the destination of the charge during the commutation period.

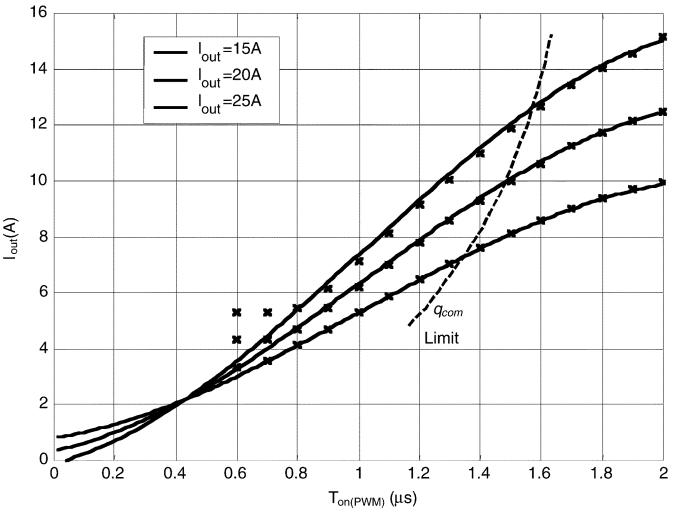

Fig. 11. Average input current as a function of PWM gate pulse-width.

(a)

(b)

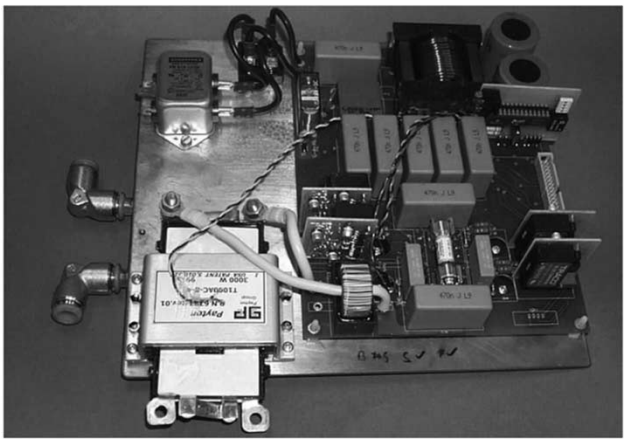

Fig. 12. Prototype induction heating system (a) application heating a bolt to 1000 °C and (b) 2.5-kW inverter circuit.

Experimental measurements from a prototype induction heating system, shown in Fig. 12, (whose parameters have been accurately measured) have also been obtained to verify the predictions. The equivalent circuit of the induction heating work-head, which represents the load on the bridge, is shown in Fig. 13. The load circuit is connected to the inverter, with

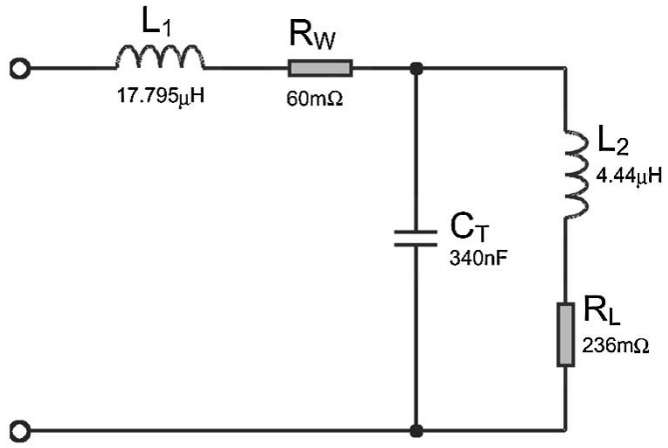

Fig. 13. Equivalent work-head circuit parameters.

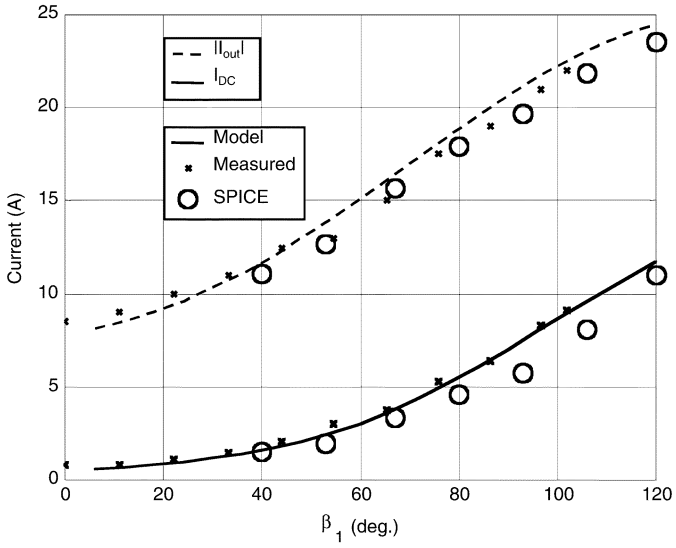

Fig. 14. Output- and input-current as a function of β_1, from the experimental system under test, a full system SPICE model, and the SIMULINK system model incorporating the proposed describing function.

TABLE I
COMPONENT VALUES USED IN THE VERIFICATION OF THE SYSTEM MODEL

Component	Description	Value
$SW_1 \rightarrow SW_4$	Power switching MOSFETs	APT5101LVR
C_1, C_3	Load commutated leg commutation capacitors	4.7nF
C_2, C_4	PWM commutated leg commutation capacitors	10 nF
θ_d	Current phase set-point bias	0^o
α_l	Turn-off signal angle for the load commutated leg	134^o

parameters shown in Table I, via a 2:1 ratio step-down transformer, and the inverter is fed from a 300-V, 9-A supply.

As β_1 increases, the pulse-width, and hence the output voltage from the system, increases. This is reflected in an increase in the output current from the inverter, shown as the peak output current value in Fig. 14. The input current also further increases with β_1 over the range of output current as the relative time available to transfer energy from the dc link to the output increases with output pulse width. However, with β_1 small, the effect of the commutation period is significant, therefore some excitation of the workhead circuit occurs leading to a minimum output current. Furthermore, due to the effect of the commutation capacitors, a minimum input current flows at $\beta_1 = 0$. From Fig. 14, a good correlation between the experimental data and the predicted results for the inverter is apparent [4]–[9].

VII. MODEL LIMITATIONS

The presented time-domain description (10) is valid only when the switch in anti-parallel with the conducting diode at the end of the cycle, is turned-on before the current passes through zero (normal operation, θ_d positive). In other cases, the output current transfers from the diode to the commutation capacitors, and the modeling of an additional period is required between $\theta_d + \pi$ to π. During this period, the voltage at the centre of the

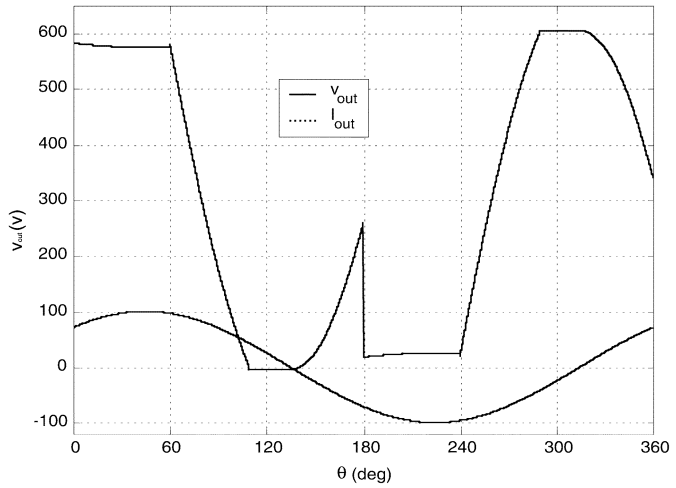

Fig. 15. Terminated commutation.

leg increases (see Fig. 15) until the switching device turns on. At the instant of turn-on, the partially charged commutation capacitor will be shorted, resulting in a large current spike (and incurring high loss). To accommodate this operating condition, (10) is modified to (24), shown at the bottom of the next page. If the output current further advances beyond the point where $\theta_d + \pi = \theta_3$, the leg voltage cannot reach the supply rail before the output current reverses, making the $dv_{\rm out}/dt$ reverse, as shown in Fig. 16. The commutation period then terminates at the turn-on of the transistor, again incurring high loss and high $dv_{\rm out}/dt$. Beyond this point, the calculation of θ_3 from (7) can provide complex results, and is no longer valid. However, θ_3 still depicts the end of the commutation cycle and, for this mode of operation, $\theta_3 = \pi$ radians. The leg voltage is therefore

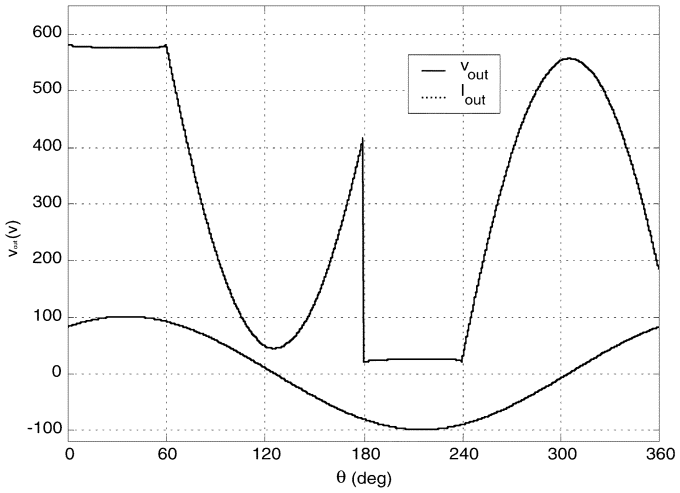

Fig. 16. $dV_{\rm out}/dt$ reversal before leg voltage reaches 0 V.

very similar to the case for terminated commutation (Fig. 15) as (25), shown at the bottom of the page.

If θ_d is advanced still further, the leg voltage, after initially reducing at device turn-off, rises to the supply voltage, whereupon the anti-parallel diode across the switch that has just turned off becomes forward biased and supports the output current. At $\theta = \pi$ radians, the lower switch turns on, and supports the output current. During turn-on, it dissipates all of the energy in the commutation capacitors and has to accommodate the diode reverse recovery; thus incurring high loss. The angle at which the diode begins to conduct, $\theta_4 = 2\pi + 2\theta_d - \theta_2$, is obtained by exploiting symmetry of the charging waveform, see Fig. 17. θ_4 is thus defined as the angle at which the voltage across the capacitors reach $V_{\rm DC} - V_t$. In reality, the voltage will rise to $V_{\rm DC} + V_d$, and, the exploitation of symmetry in this manner introduces an error into the calculation. However, since the resulting $dv_{\rm out}/dt$ at θ_4 is high, and the voltage error $(=V_{\rm diode} + V_t)$ is low, the timing error introduced is small; except in cases when θ_d approaches $-\pi/2$ or $V_{\rm DC}$ is very low. This mode occurs if $\theta_d \leq (\theta_2/2) - (\pi/2)$ (does not account for the effects of V_t and $V_{\rm diode}$) as (26), shown at the very bottom of the page.

$$v_{\rm Leg}(\theta) = \begin{cases} V_{\rm DC} - I_{\rm out}R_{\rm on}\sin(\theta-\theta_d), & \theta = 0\ldots\theta_2 \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_{\rm DC} - V_t - \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta_d-\theta_2), & \theta = \theta_2\ldots\theta_3 \\ 0, & \theta = \theta_3\ldots\pi+\theta_d \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}, & \theta = \pi+\theta_d\ldots\pi \\ -I_{\rm out}R_{\rm on}\sin(\theta-\theta_d), & \theta = \pi\ldots\pi+\theta_2 \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_t - \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta_d-\theta_2+\pi), & \theta = \pi+\theta_2\ldots\pi+\theta_3 \\ V_{\rm DC}, & \theta = \pi+\theta_3\ldots2\pi+\theta_d \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_{\rm DC} - \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}, & \theta = 2\pi+\theta_d\ldots2\pi \end{cases} \tag{24}$$

$$v_{\rm Leg}(\theta) = \begin{cases} V_{\rm DC} - I_{\rm out}R_{\rm on}\sin(\theta-\theta_d), & \theta = 0\ldots\theta_2 \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_{\rm DC} - V_t - \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta_d-\theta_2), & \theta = \theta_2\ldots\pi \\ -I_{\rm out}R_{\rm on}\sin(\theta-\theta_d), & \theta = \pi\ldots\pi+\theta_2 \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_t - \dfrac{I_{\rm out}}{2\pi f_s C_{\rm comm}}\cos(\theta_d-\theta_2+\pi), & \theta = \pi+\theta_2\ldots2\pi \end{cases} \tag{25}$$

$$v_{\rm Leg}(\theta) = \begin{cases} V_{\rm dc} - I_{\rm out}R_{\rm on}\sin(\theta-\theta_d), & \theta = 0\ldots\theta_2 \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_{\rm dc} - V_t - \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta_d-\theta_2), & \theta = \theta_2\ldots\theta_4 \\ V_{\rm dc}, & \theta = \theta_4\ldots\pi \\ -I_{\rm out}R_{\rm on}\sin(\theta-\theta_d), & \theta = \pi\ldots\pi+\theta_2 \\ \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta-\theta_d) + V_t - \dfrac{I_{\rm out}}{2\pi f_s C'_{\rm comm}}\cos(\theta_d-\theta_2+\pi), & \theta = \pi+\theta_2\ldots\pi+\theta_4 \\ 0, & \theta = \pi+\theta_4\ldots2\pi \end{cases} \tag{26}$$

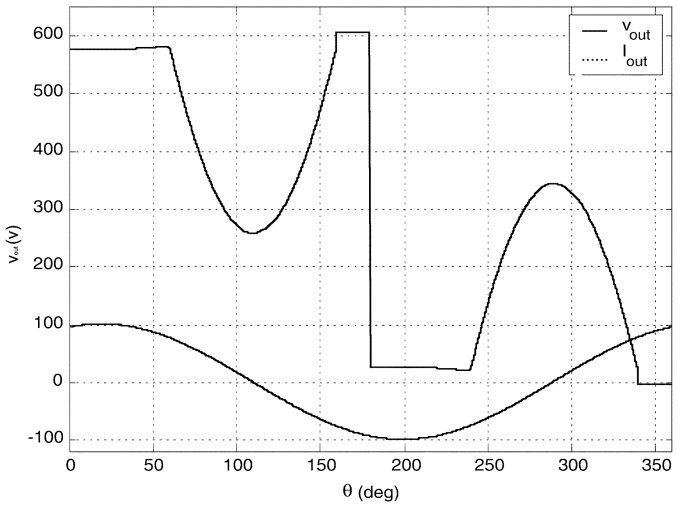

Fig. 17. High loss during incorrect commutation.

During normal operation, the resonant circuit is excited such that it appears predominantly inductive (to reduce commutation losses). However, if the unmodified describing function is coupled to a transient FMA model of a high-order resonant circuit (such as an in-circuit averaged model), the resulting system model can exhibit instability if the current transiently assumes a capacitive characteristic. Use of describing-functions derived from (24)–(26) address this issue. Moreover, if θ_d becomes greater than θ_2 (a highly inductive characteristic), the diode will still be conducting when the switch turns off, implying that the capacitors do not begin to support the current until I_{out} crosses zero (at θ_d), thereby effectively limiting θ_2 to $\geq\theta_d$.[10]

VIII. Conclusion

The paper presents the derivation of a novel describing function to model the output voltage of a H-bridge inverter, and includes a functional description of the relationship between the output- and supply-currents. Accuracy of the resulting model is demonstrated by comparison with SPICE simulation results, and with practical measurements from a prototype induction heating system. The model facilitates system simulation over a number of cycles of the input utility supply, ultimately allowing optimization of control systems without the significant computational overhead normally incurred by having to employ at switching-cycle level simulation. In particular, it is notable that the proposed model executes, typically, some 10 000 times faster than a H-bridge inverter modeled using Spice.

Limitations of model applicability are discussed, with particular emphasis to operation during incorrect commutation of the H-bridge, along with suggested modifications to the proposed model where appropriate.

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