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High Mobility N-Type Field Effect Transistors Enabled By Wse2/ pdse2 Heterojunctions

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HIGH MOBILITY *N*-TYPE FIELD EFFECT TRANSISTORS ENABLED BY $WSE_2/PDSE_2$ HETEROJUNCTIONS

by

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DISSERTATION

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Advisor Date

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DEDICATION

This work is dedicated to my father, Attorney Arthur Bowman, Jr., who passed away from complications due to covid-19 in May 2020. It is one of the great disappointments of my life that he did not survive to witness this. He played an integral role in my decision to study the nanoscale world. I will continue that study in his honor.

ACKNOWLEDGEMENTS

I would like to acknowledge my advisor, Dr. Zhixian Zhou, whose attentiveness to my work and great enthusiasm for research made this all possible. Much appreciation also goes to the members of my dissertation committee: Dr.'s Jian Huang, Zhi Feng Huang, and Ming-Cheng Cheng, and Dr.'s Sean Gavin and Ratna Naik of the Wayne State University Department of Physics and Astronomy for their mentorship and encouragement.

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CHAPTER 1. MOTIVATION

1.1 $PdSe_2$: A Promising Candidate for Post-Silicon Electronics

The continued downscaling of metal-oxide-semiconductor field effect transistor (MOSFET) technology has been the driving force of the digital age. The progress is basically measured by Moore's Law, which predicts that the number of transistors that are densely packed into an integrated circuit doubles every 2 years[1]. The highest count to date was achieved in 2020 by the Chinese technology company Huawei who reported 1.53 x 10^{10} MOSFETs on their HiSilicon Kirin 9000 processor. A schematic of a standard three-terminal MOSFET is shown in **figure 1.1**. Silicon is the most widely used channel material in MOSFETs. However, silicon MOSFETs are approaching a fundamental limit. In standard silicon-on-insulator (SOI) devices this is captured by the transistor characteristic length, λ,

$$\lambda_{SOI} = \sqrt{\frac{\varepsilon_s}{C_g} t_s} \tag{1.1}$$

Where ε_s is the channel dielectric constant, C_g is the gate capacitance per unit area and t_s is the channel thickness. If the channel length is 5 to 10 times larger than λ, the drain electrode will be electrostatically shielded from the source by the combination of the gate and substrate. Around the 7 nm mark, the drain electrode is close enough to the source to participate in the injection of charge carriers into the channel region, which causes the device to turn on prematurely in a phenomenon known as Drain Induced Barrier Lowering (DIBL)[2].

IBM departed from the conventionally used MOSFET and FinFET designs to demonstrate silicon-based FETs with 5 nm channel lengths using nanosheets in a "gate all around" configuration[3]. Yet we could also continue downscaling by simply replacing silicon with a different semiconductor that possesses similar properties, but not does not exhibit DIBL at sub-10

nm channel lengths. Thus, around the dawn of the new millennium, the search began for an alternative.

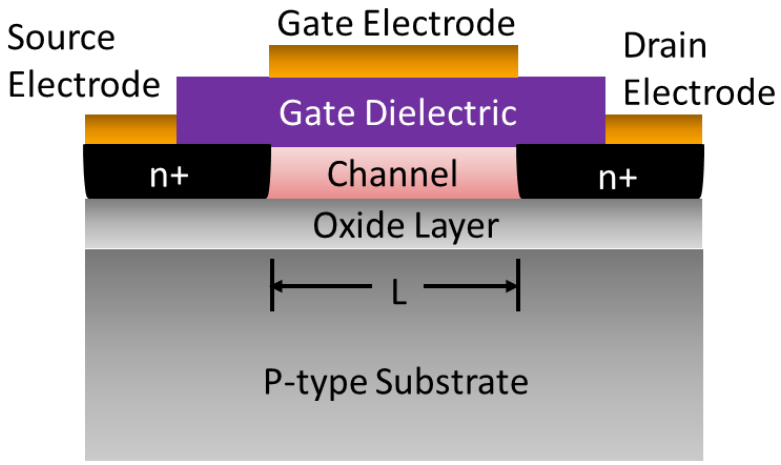


Figure 1.1|: Schematic of a basic 3-terminal MOSFT. This device is '*n*-type', meaning most charge carriers are electrons, rather than holes. *n*-type MOSFETs will be the focus of this work, although the logic is ever the same for *p*-type.

The 2004 discovery of graphene was a seminal moment in this search. Graphene is a monolayer of graphite; an atomically thin sheet of carbon bonded in a hexagonal lattice. Graphene has an extremely high theoretical mobility of ~ 10^4 cm^2 V^{-1} s^{-1}, is chemically and thermally stable, and is mechanically strong enough for applications in flexible electronics[4]. The intraplanar bonds in graphene are covalent, while the interplanar bonds are supplied by a much weaker Van Der Waals (VDW) interaction. This allows for the peeling of graphene layers from graphite using a scotch-tape-based exfoliation technique, and the fabrication of graphene-based heterostructures and devices via a simple dry pick-up and transfer[5]. However, graphene is a semi-metal; its valence and conduction bands meet at the so-called Dirac point (where the carrier mobility can approach that of a Dirac fermion[6]). The absence of an intrinsic bandgap leads to

high leakage currents in graphene-based FETs and attempts to engineer a bandgap in graphene were only marginally successful.[7-9]

Fortunately, graphene is only one member of the large family of layered two-dimensional (2D) materials. The hundreds of such materials that have been found have a wide range of electrical properties from metals and semi-metals to insulators, topological insulators, semiconductors, and superconductors[10-12]. In the last five years, transition metal dichalcogenides (TMDCs) have arisen as a subset of 2D materials with a graphitic structure and widely tunable band gaps.[13-15] TMDCs are so-named because their elemental structures follow the general formula of MX_2, where M is a *d*-block transition metal, (e.g., Mo, W, and Ti) and X is a chalcogen (e.g., S, Se, and Te). The graphitic lattice of TMDCs render the preparation of monolayers and heterostructure devices a relatively simple task[16]. TMDCs such as MoS_2 have shown moderate carrier mobilities of ~ 50 $cm^2\ V^{-1}\ s^{-1}$ and high transistor ON/OFF ratios near ~ 10^6 at room temperatures[17]. Monolayer MoS_2 FETs have also been shown to perform well at single nanometer gate lengths[18].

With the discovery of group 6 TMDC monolayers, the search for a viable alternative to silicon has already come close to achieving its purpose. But there is still significant room to improve the performance of FETs based on 2D material devices. Alongside the TMDCs, phosphorene has also been shown to be a promising body for high performance devices. Phosphorene FETs show more moderate ON/OFF ratios of ~ 10^4, but a mobility nearly 5 times that of MoS_2, owing to a smaller and narrower bandgap and thus a small effective hole mass. The phosphorene bandgap is also more widely tunable than those of the group 6 TMDCs, varying from ~ 300 meV for bulk phosphorene and 2 eV for monolayer crystals.[19] Unlike graphene and TMDCs, the phosphorene lattice is orthorhombic, and the atoms are strongly puckered; that is, they are not ideally planar, but oscillate in-and-out of plane in a regular, corrugated manner. This leads to lower

symmetry in phosphorene than in TMDC layers, giving rise to exotic in-plane anisotropic electronic,[20] optoelectronic,[21] and thermal[22] properties. However, apropos practical device applications, TMDCs are generally preferred to phosphorene, as phosphorene is highly unstable in air.

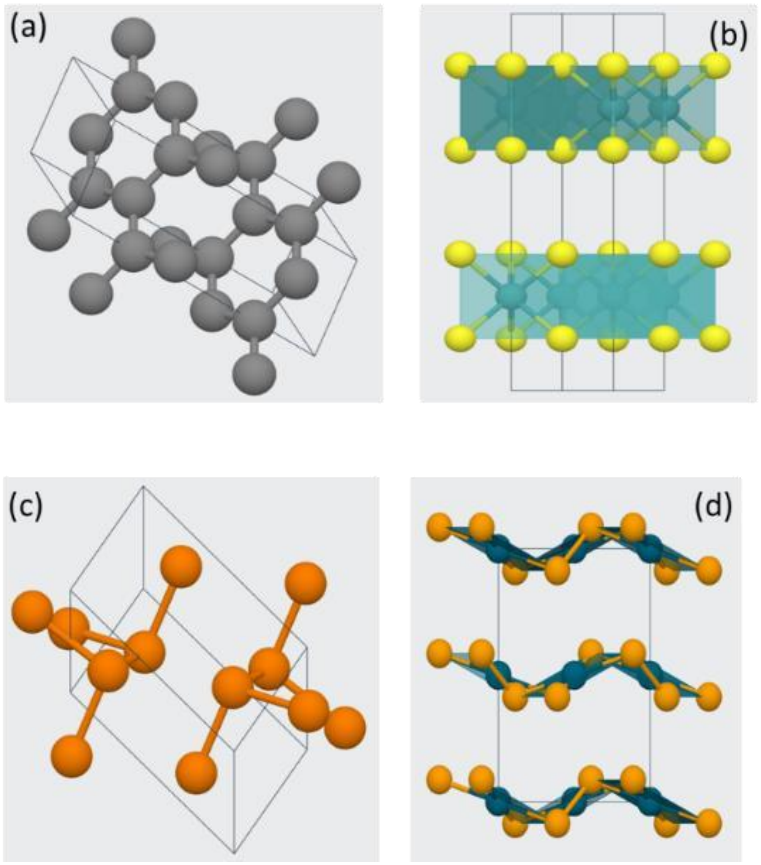


Figure 1.2| Lattice Structure of **a:** graphene, **b:** MoS_2 (to represent traditional 1T and 2H TMDCs), **c:** BP, and **d:** $PdSe_2$. The graphene and BP crystals are side viewed to show the shapes of their respective unit cells. Note that atoms in graphene and MoS_2 lattices are confined to a single plane, while those of BP and $PdSe_2$ are in and out-ofplane but are still within the limit of a 2D system. This is an illustration of 'puckering'. Originally appeared in the Materials Project.[106]

Thus, we desire a 2D material which possesses the high mobility and highly tunable bandgap of phosphorene, high ON/OFF ratio of TMDCs, but is also highly stable. In the last four years, 'noble' TMDCs such as palladium di-selenide ($PdSe_2$) and platinum di-selenide emerged as a class of candidates[23-25]. The noble TMDCs also follow the MX_2 formula, only now M is a noble

metal (e.g., Pd or Pt) bonded to the usual chalcogens. The lattice structures of MoS_2, phosphorene, and $PdSe_2$ are shown in **figure 1.2**.

Both $PtSe_2$ and $PdSe_2$ are stable in air and have high carrier mobilities, but the $PdSe_2$ band structure affords a slightly larger ON/OFF ratio[26], so we shall henceforth focus on the latter. The $PdSe_2$ lattice consists of strongly puckered pentagons, quite unique among 2D materials. Its bandgap has a similar degree of tunability as that of phosphorene, varying from 300 meV for bulk to 1.3 eV for monolayer crystals. Bulk $PdSe_2$ FETs have shown a carrier mobility of ~158 $cm^2V^{-1}s^{-1}$, and few-layer FETs have shown ON/OFF ratios as high as 10^6[27]. Yet, a $PdSe_2$-based FET which simultaneously shows high mobility and ON/OFF ratio has yet to be demonstrated. In this work, we will elucidate a mechanism to overcome current performance limitations on few-layer $PdSe_2$ FETs and study the intrinsic transport properties of this novel 2D material.

1.2 The $PdSe_2$ Lattice and Energy Band Structure

Layered $PdSe_2$ crystallizes in the space group *pbca* with an orthorhombic unit cell of

$$\vec{a} = 5.75\ \text{Å}\ (4), \vec{b} = 5.87\ \text{Å}\ (4),\ \vec{c} = 7.70\ \text{Å}\ (3)\ and\ V = 259.43\ (5)\ ^{28} \quad (1.2)$$

As can be seen from figure 1.2, the chalcogen atoms in MoS_2 (and the other group 6 TMDCs) layers lie along a straight line. But because of strong puckering, the chalcogen atoms in $PdSe_2$ layers lie periodically above and below the *ab* plane. The vertical puckering distance is ~ 1.6 Å. An overhead view of the $PdSe_2$ lattice is shown in **figure 1.3**. It can be seen from this that a single Pd atom is coordinated with four Se atoms in the same layer, compared with six chalcogens coordinated with the transition metal in MoS_2. In other words, $PdSe_2$ has a much larger crystal field than the group 6 TMDCs. This could mean a more disordered electronic field as well.[29]

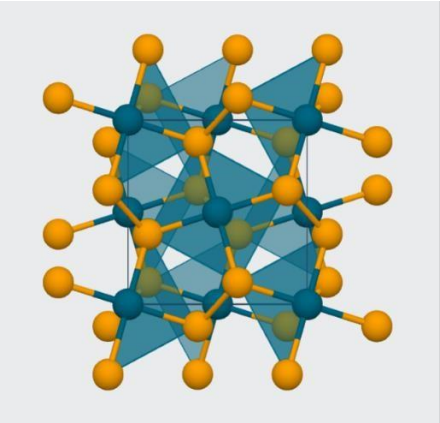


Figure 1.3| Overhead view of the $PdSe_2$ lattice. Originally appeared in the Materials Project.[106]

Due to the atomic scale thickness of 2D materials, intrinsic properties such as band structure and lattice vibrations are highly sensitive to the preparation method of growing the bulk crystal. The same material grown by slightly different methods can produce different layer sizes, thicknesses, doping, defects, vacancies, etc[30].

The intensity, line shapes, peak positions, and full widths at half maxima of the Raman peaks of 2D materials all contain useful information to characterize physical and chemical properties such as electronic states and electron-phonon coupling[31].This combined with the fact that device fabrication can be carried out using the same flakes as those sampled for Raman peaks makes Raman spectroscopy a powerful characterization method. 2D materials exhibit Raman peaks due to both intralayer and interlayer modes. The composition and structural phase can be deduced from the intralayer modes. Much can be learned about the interlayer coupling by treating the layers as wholes and considering the layer-layer vibration between them in the socalled linear-chain model.

Chi et. al reported peaks at 143, 205, 221, and 255 cm^{-1} in the first-order Raman spectrum of few-layer $PdSe_2$[32], originating from intralayer vibrations of the crystal lattice, namely $A_g{}^1$, $A_g{}^2$, B_{1g}, and $A_g{}^3$. They then used the same flakes to fabricate $PdSe_2$-based phototransistors. Defining

the photoresponsivity as the photoresponse current generated per unit power of incident light on a specified area,

$$R = \frac{I_{ph}}{PA_s} \tag{1.3}$$

Bulk (~ 8 nm thick) $PdSe_2$ phototransistors showed R = 500 μA/W, which increased to a 5.35 A/W in devices based on few-layer (~ 3.8 nm thick) crystals. The 6 order of magnitude increase in the photoresponse current was attributed to the large degree of tunability of the $PdSe_2$ bandgap, specifically tuning to a stronger valley convergence in the conduction band in fewlayer $PdSe_2$. However, Javey[33] (who also reported $PdSe_2$ phototransistors) found that the intensity of first-order Raman peaks also increases with decreasing thickness. The locations of their Raman peaks were consistent with those found by Chi, although there is some disparity in the physical explanations for the peaks.

Liu identified the location of the first mode as $A_g{}^1 - B_g{}^1{}_1$. The smaller two peaks that constitute the second mode are defined as those at $A_g{}^2$, and $B_g{}^2{}_1$, respectively. These first three modes are believed to be due to vibration of the Se atoms. The fourth and strongest mode is taken to be a convolution of two modes at $A_g{}^3$, and $B_g{}^3{}_1$, and believed to be due to the relative motion between the Pd and Se atoms.

Liu further found some peaks in the spectrum of few-layer $PdSe_2$ that were absent in bulk which were predicted by ab initio calculations. As the thickness tunes from bulk to few-layer, the space group changes from *Pbca* to $Pca2_1$, resulting in additional peaks.

Unlike the Raman spectra, there is not much experimental data available to elucidate the energy band structure of $PdSe_2$ layers. Photoluminescence (PL) measurements would normally be performed to accomplish this. The PL spectrum of $PdSe_2$ (and PdS_2) quantum dots was investigated[33], but this is a 1D phase of the material. There would likely be more emissions in the

spectrum of 2D $PdSe_2$ due to the additional degrees of freedom. However, Singh did perform calculations of the density of states (DOS) and energy band structure of layered $PdSe_2$ using the linearized augmented plane wave (LAPW) method in the WEIN2K code[34] .

The LAPW is one of the most accurate methods for calculating the electronic structures of crystalline solids. Like most methods in the Density Functional Theory, it is a procedure for solving the Kohn-Sham equations for the ground state density, total energy, and Kohn-Sham eigenvalues which yield the energy band structure of electrons in a crystalline system for a specified basis set. The unit cells are divided into non-overlapping atomic spheres and centered at their lattice sites and interstitial regions. Inside the atomic spheres, the linearized radial eigenfunctions and eigenvalues can be obtained from

$$\varphi_{k_n} = \sum_{lm}[A_{lm}u_l(r, E_l) + B_{lm}\dot{u}_l(r, E_l)]\, Y_{lm}(\hat{r}) \tag{1.4}$$

Where (r, E_l) is the solution of the radial Schrödinger equation corresponding to an energy, E_l, $\dot{}_l(r, E_l)$ is its derivative for the same energy value, and $Y_{lm}(\hat{r})$ are spherical harmonics. (r, E_l) and $\dot{u}\ (r, E_l)$ are generally obtained via numerical integration of a radial mesh. The coefficients A_{lm} and B_{lm} are functions of k_n and are determined by requiring that the basis function inside the sphere matches that at the interstitial regions.

In the interstices, the eigenfunctions are given by a plane wave expansion,

$$\varphi_{k_n} = \frac{1}{\sqrt{\omega}} e^{ik_n r} \tag{1.5}$$

Where k is the wavevector in the first Brillouin zone and $k_n = k + k_n$ are the reciprocal lattice vectors. The solutions to the Khon-Sham equations in each region are then expanded in a combined basis set according to the linear variation method,

$$\psi_{k_n} = \sum_n c_n \varphi_{k_n} \tag{1.6}$$

And the coefficients c_n are determined using the Rayleigh-Ritz variational principle. Cutoff parameters $R_{min}K_{max}$ corresponding to the smallest atomic radius and the magnitude of the largest wave vector are typically introduced to ensure convergence. Singh first performed the LAPW calculations for the experimental bulk structure, using the unit cell in Equation 1.2, atomic radii of R = 2.5 Bohr for Pd and 2.1 Bohr for Se and cutoff parameters $R_{min}K_{max} = 7$.

After bulk structure calculations, the modified Beck-Johnson potential (mBJ) was used to relax the internal coordinates for both bulk and monolayer. Spin-orbit coupling was considered in all calculations.

Figure 1.4 shows the calculated DOS of bulk $PdSe_2$. The Fermi energy is set to zero. As was previously noted, both the bulk and the monolayer phases exhibit well defined band gaps of 300 meV for bulk and 1.43 eV for monolayer. Interestingly, the binding energy of 190 meV/atom is well above that of graphite[35] (~ 35 meV/atom), BP[36] (~ 40 meV/atom), and MoS_2[37] (130 meV/atom) which is a testament to the strong interaction between layers that arises due to puckering. This also suggests it may be difficult to prepare monolayer $PdSe_2$ via mechanical exfoliation, a challenge we will revisit in the "Fabrication Methods".

It is clear from the DOS that in both monolayer and bulk crystals most states at the band edges are contributions from the *d*-orbitals of the Pd atoms and the *p*-orbitals of Se. There is also some visible hybridization of the 4*d* states of Pd and the 4*p* states of Se that arises due to the intraplanar (covalent) bonds.

Figure 1.4 also shows the calculated band structure of the bulk $PdSe_2$ phase along high symmetry *k* points. The band gap is indirect. Incidentally, the transition to a direct band gap in the monolayer phase that occurs in many group 6 TMDs does not occur in $PdSe_2$. Special attention should be paid to the concavity of the valence and conduction bands near the Γ point.

The valence band is extremely flat, while the conduction band is quite narrow. Although $PdSe_2$ FETs are ambipolar (as we shall see in the coming sections) the band structure behooves us to focus on demonstrating high performance *n*-type devices. The large effective mass would be a limiting factor on the hole mobility.

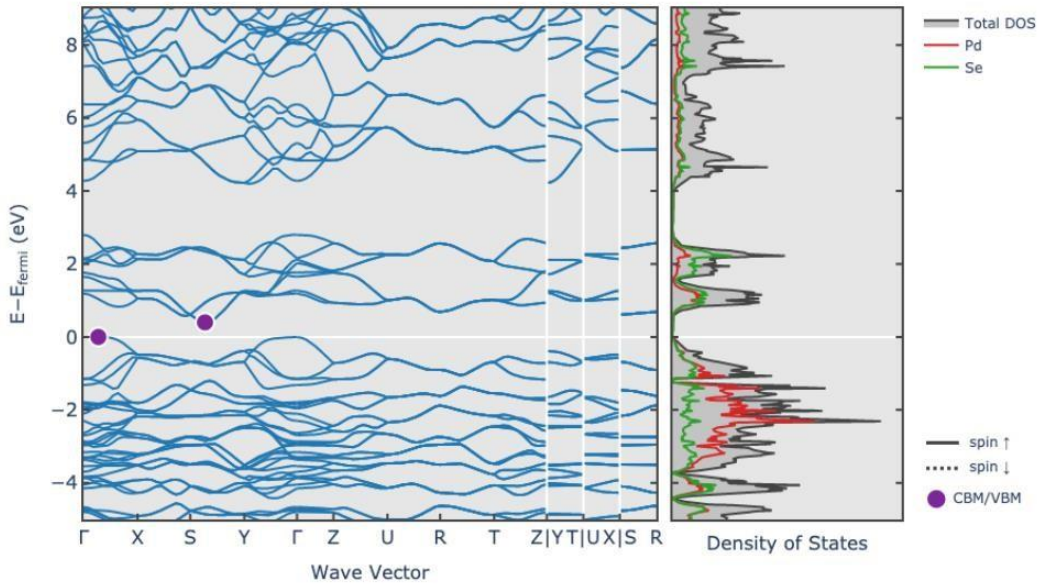


Figure 1.4 | Calculated DOS and energy band structure for bulk $PdSe_2$. Originally appeared in the Materials Project.[107]

1.3 Performance Limitations on $PdSe_2$ FETs

As is the case with all 2D semiconductors, the main performance limitation in $PdSe_2$based MOSFETs is a substantial Schottky barrier which tends to form at the drain source contacts[38]. The barrier is a result of an energy mismatch between the electron affinity of the $PdSe_2$ channel, χ_s, and the work-functions of conventionally used metal electrodes, Φ_M. In most cases, $\Phi_M > \chi_s$.

At equilibrium, electrons flow from the semiconductor to the metal and leave a positive space charge region in the semiconductor. Under forward bias, electrons easily flow from semiconductor to metal. But under reverse bias, the flow of electrons from the metal is limited to only those with enough energy to pass over the built-in potential barrier. For this reason, Schottky-

type contacts are sometimes also referred to as rectifying contacts because the current can be large or small depending on the direction of an applied bias. Ideally, the Schottky Barrier Height (SBH), Φ_B, can be predicted by the Schottky-Mott rule,

$$\Phi_B = \Phi_M - \chi_s \tag{1.7}$$

However, experimental reports of Schottky Barrier heights are usually far greater than those predicted by the rule, even in the case of the Si and GaAs FETs that are used in digital electronics today[39]. Instead, the Fermi level tends to pin to a fixed point in the semiconductor bandgap and this Fermi Level Pinning (FLP) effect tends to be dominant regardless of the choice of metal workfunction[40-42].

The sources of the Fermi Level Pinning (FLP) effect in 2D semiconductor devices are many. Firstly, the Schottky-Mott model presumes an atomically sharp discontinuity between electrode and channel, which is rarely the case due to chemical bonds that take place spontaneously and modify the original energy levels.[43] Secondly the decaying metallic wavefunction can penetrate the channel region by several nanometers, leading to metal-induced gap states. Third and most determinately, the VDW assembly and metallization processes introduce chemical disorder and defect states. This is especially true when the metal contacts are formed via aggressive processes like thermal evaporation, which deposits metal into lithographs via cluster bombardment and heating of the contact region. Such a process can easily damage the semiconductor lattice near the interface[44].

There hasn't been much investigation into the sensitivity of $PdSe_2$ FETs to metal work function, so it is difficult to postulate exactly where the Fermi level pins. However, the slight oscillation of $PdSe_2$ atoms in and out of the crystal plane implies the *d*-orbitals of the Pd atoms and the *p*-orbitals of Se which lie along the band edges could have an even stronger interaction

with metal electrodes than orbitals lying along the band edges of the group 6 TMDCs. This may be reflected in the reported SBH of ~ 250 meV for $PdSe_2$ FETs formed using Ti electrodes[45]. The contact resistance of 2 MΩμm is also much larger than that reported for any group 6 TMDC.

Figure 1.5 shows an energy band diagram of a metal source contact in a $PdSe_2$ MOSFET at the Schottky-Mott limit.

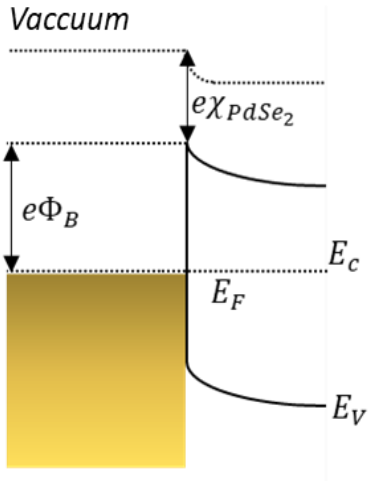


Figure 1.5 | Metal source contact of a $PdSe_2$ FET at the Schottky-Mott limit

1.3.1: Transfer Characteristics:

Generally, a MOSFET is said to be 'high performing' based on two plots: the transfer characteristics (current as a function of gate voltage, V_g, at a specified drain-source bias, V_{ds}) and the output characteristics (current as a function of the drain-source bias, V_{ds}, at a specified V_g). Usually, the transfer characteristics are plotted for a series of drain-source biases and the output characteristics are plotted for a series of gate voltages. Every other figure of merit that we will discuss (carrier mobility, SBH, etc.) is extracted from these two curves, either at room temperature or from their temperature dependence. We will flesh this out more fully in the "Results" section.

In the presence of a large Schottky barrier, the transfer characteristics will generally show a 'bowing' region at low gate voltages (specifically where $V_g \cong V_{th}$). In this region, the current is

small and primarily due to thermally assisted tunneling. There isn't enough energy for thermionic emission, and the tunneling resistance is high due to large depletion layer widths, which can be on the order of nanometers[46]. At higher gate voltages, most carriers can emit over the barrier, and the 'bowing' region gives way to a linear current-voltage relationship.

The 2D conductivity and carrier mobility are both extracted from the transfer characteristics. In an ideal MOSFET, the carrier mobility is limited only by the quantum mechanical scattering of charge carries by acoustic phonons, which emanate from the crystal lattice of the channel. This is conventionally referred to as the 'phonon-limited mobility' or 'channel limited mobility'. As the device is cooled to cryogenic temperatures, thermal excitations of these acoustic phonons are suppressed- hence the mobility increases, usually by a factor of two or three. Due to lattice defects and other unavoidable traps, it is nearly impossible for any material to reach its theoretical mobility. $PdSe_2$ FETs have shown a cryogenic mobility as high as 520 cm^2/Vs[47], although its theoretical value is believed to be 9,800 cm^2/Vs.

As we will see, there are different ways of discussing mobility, but they are all extracted from the transfer characteristics. A Schottky barrier can have two possible effects on the temperature dependence. It *may* cause the mobility to appear to decrease, an artifact which results from barrier heights that are so large they cannot be overcome even at high gate voltages. But even if the mobility appears to increase upon cooling, there will be a substantial positive shift in the threshold voltage (causing the 'bowing' region to grow larger). This latter effect is often neglected in reports of high performance 2D MOSFETs, even though its presence is a clear indication that the device is barrier limited.

To see how, let us briefly dig into the thermionic emission and diffusion theory of Bethe and the diffusion theory of Schottky[98]. The current voltage characteristics of an *n* or *p*-type (in the

latter case, the barrier is modeled as a series of *forward* biased Schottky diodes) FET are described by the Shockley Diode Equation:

$$I = A^{**}T^2 e^{\frac{-q\phi_B}{K_B T}} \left[e^{\frac{-qV}{K_B T}} - 1 \right] \tag{1.8}$$

Where T is the temperature and A^{**} is the effective Richardson constant. To first approximation, the probability of electrons emitting over the potential maximum is Maxwell distributed over the mean free path, λ,

$$f_p = e^{-x_m/\lambda} \tag{1.9}$$

But the electronic energy distribution tends to be distorted from this Maxwellian form by quantum mechanical tunneling of some electrons through the barrier as well as reflection of other electrons off it. The impacts of these quantum effects are accounted for in the reduced effective Richardson constant, A^{**}, which reduces up to 50% from A* according to the relation

$$A^{**} = \frac{f_p f_Q A^*}{1+\left(\frac{f_p f_Q v_R}{v_D}\right)} \tag{1.10}$$

The ratio of the total current flow, f_Q, in which these effects are considered to current flow f_p in which they are neglected is strongly dependent on the applied gate voltage and the position of the quasi-Fermi level relative to the SBH.

As was previously noted, at room temperature, there is enough thermal energy for a substantial amount of charge carriers to thermionically emit over the barrier, while a smaller portion can tunnel through, and the current will be predominately given by **Equation 1.8**. But as cryogenic temperatures are approached that thermal energy can no longer be supplied, hence the current will be due entirely to tunneling. The tunneling current is given by

$$J = e v_R n \Theta \tag{1.11}$$

Where e is the electron charge, v_R is the Richardson velocity, n is the carrier density, and Θ is the tunneling probability. v_R has the form,

$$v_R = \sqrt{\frac{K_B T}{2\pi m^*}} \tag{1.12}$$

The average velocity with which electrons approach the interfaces of the barrier. The tunneling probability is derived from the Time Independent Schrodinger Equation, treating the Schottky barrier as a triangular potential in the WKB approximation to obtain

$$\Theta = exp\left(-\frac{4}{3}\left(\frac{\sqrt{2qm^*}}{\hbar}\right)\frac{{\phi_B}^{3/2}}{\mathcal{E}}\right) \tag{1.13}$$

Where Ɛ is the applied electric field. The fact that $\Theta \propto e^{-(\phi_B)^{\frac{3}{2}}/\mathcal{E}}$ indicates that the tunneling current can be severely limited by a large contact barrier, and successively greater voltages must be applied to turn on a FET at cryogenic temperatures. Thus, we have explained why the positive shift in the threshold voltage is evidence that a FETs is contact limited.

Now that we understand the reason for this phenomenon, how do we quantify it? One way is to calculate the subthreshold swing, SS. The SS is the inverse of the subthreshold slope; the amount of gate voltage needed to produce one decade of drain current.

$$SS = \frac{dV_{GS}}{dlog(I_D)} \tag{1.14}$$

The drain current behaves similarly to a forward biased diode in the subthreshold region, so the SS can also be written as

$$SS = \frac{dV_{GS}}{dlog(I_D)} = mu_T \ln(10) \tag{1.15}$$

Where u_T is the thermal voltage and m is the diode ideality factor[48]. In most FET designs at room temperature, the diffusion of charge carriers sets the minimum possible SS- known as the thermionic limit- to 60 mV/dec. At this limit, the ideality factor is close to unity, and the thermal

voltage is ≈ 30 mV. Yet, sub-thermionic field effect transistors have been demonstrated via band-to-band tunneling[49].

Obviously, a large 'bowing' region implies a large SS. The transfer characteristics will not rise 'sharply' upon reaching the threshold voltage. Instead, the slope of the current vs gate voltage (not to be confused with the subthreshold slope, since contact effects can be seen well after turn-on) will be smaller than ideal, and vary by region, according to whether the current is due to thermally assisted tunneling or thermionic emission. Cooling to cryogenic temperatures will only exacerbate the problem.

If the drain/source contacts are Ohmic, the transfer characteristics will rise with near infinite slope and the SS will be close to the thermionic limit. The fact that we cannot reduce the SS all the way to zero does mean that there is always going to be some 'bowing' in the transfer characteristics and therefore the Schottky barrier will always have some non-zero height. But so long as the SBH is smaller than the thermal energy of charge carriers, (25 meV at room temperature) its effects can be said to negligible.

1.3.2: Output Characteristics:

The effects of the barrier on the output characteristics are often much less noticeable. Ohmic contacts will simply show output characteristics that obey Ohm's law; so long as the gate voltage is above threshold, the current will rise linearly with the applied bias, until the bias is large enough to cause the channel resistance to decrease, at which point the current saturates. The total resistance can be readily obtained from the inverse slope of the I-V curves in the linear region.

A substantial barrier will lead to non-linear output characteristics, especially at lower applied biases and gate voltages. Sometimes, the non-linearity is symmetric, suggesting that the SBH is roughly the same at both the drain/source contacts. Yet, most of the time there is some asymmetry. As we elucidated earlier, there are many factors that can contribute to Fermi level

pinning and each contact can suffer from a different combination of these factors. To reiterate further, a large enough gate voltage will enable thermionic emission over the barrier. I-V curves can become linear in this gate voltage range.

Sometimes, at higher temperatures the output characteristics can show a deceiving linearity that belies the presence of a contact barrier. This is generally not an intrinsic effect. It has been shown that annealing can create hybridized contacts to the channel and modify the band alignment[50], and this is just one possible reason for such deceiving linearity. Therefore the output and transfer characteristics have to be considered together in order to make any reliable proclamations on the nature of the contacts.

Javey fabricated a 6.8 nm thick $PdSe_2$ FET fabricated on a commercial SiO_2/Si substrate[51]. The room temperature electron mobility was decently high at ~ 130 cm^2/Vs, with a moderate ON current of ~ 10 µA/ µm. The transfer and output characteristics were nearly linear at room temperature- even at lower gate voltages. Yet upon examining the temperature dependence of the transfer characteristics, we see a ~ 15 V shift in the threshold voltage as the device is cooled to 77 K. The SBH was not calculated in this work, but it is likely several times the thermal energy of charge carriers.

1.4 Strategies for High Performance FETs

The tendency of large Schottky barriers to form at the interface between the semiconducting channel and metal drain/source contacts is not only a performance limitation for TMDC-based MOSFETs. Even the Si-based FETs used in commercial technologies have substantial contact barriers. The difference is that barriers in Si devices can be virtually eliminated at the contact regions using a process known as selective ion implantation[52].

In this method, a high-powered plasma is generated via RF or microwave radiation to ionize donor (or acceptor) atoms under ultra-high vacuum. The vacuum suppresses collisions with

ambient gas molecules, causing the ions to form a linearized beam. The ion beam is then accelerated via electromagnetic fields and directed at a target substrate. The substrate surface is bombarded with ion energies ranging from a few hundred to a few million meV; enough to penetrate the substrate lattice and knock out atoms from their sites. Annealing is then implored to "activate" the dopant by substituting dopant ions into the vacancies.

This can have one of two cumulative effects; either a lowly doped layer will form near the silicon surface, or an interfacial dipole will form. In both cases, the silicon conduction (or valence, in the case of *p* contacts) band bends downwards relative to the Fermi level of the metal, reducing the SBH. The reduction can be controlled simply by modulating the ion dose.

Unfortunately, local doping of the contact regions via selective ion implantation is not possible for 2D materials. The technique is too destructive; the penetration depth of implanted ions is usually anywhere from 10 nm-1 μm, which is thicker than a monolayer of any 2D material.

Thus, the search began for a different method of locally doping the contact regions in 2d TMDCs, or otherwise reducing the Schottky barrier height. One method that has drawn a lot of attention is phase engineering. Chhowalla showed that the metallic 1T phase of MoS_2 can be locally induced on the (typical) semiconducting 2H phase, dropping the contact resistance by an order of magnitude[52]. Yang performed a similar study in which the contact resistance to $MoTe_2$ was reduced via a locally induced transition of $MoTe_2$ from its hexagonal layer structure into an octahedral metallic phase. However, such transitions are usually unstable above critical temperatures, (100° C in the latter case) limiting their practical device applications.

There has also been great success in engineering low resistance Ohmic contacts via surface and substitutional doping. Javey demonstrated a high performance FET based on monolayer WSe_2 by chemically doping the surface of the contact regions with NO_2. The channel region was

encapsulated with Pd, both to ensure local doping of the contact regions as well as to exploit the fact that Pd is a high-κ dielectric and therefore a good candidate for a top-gate with excellent electrostatics[54]. The same group also saw success with surface charge transfer doping of MoS_2 using potassium[55] and benzyl viologen[56].

Ye had some success with surface doping of few-layer MoS_2 and WS_2 using a chlorination technique[57]. However, the doping was not localized in this case, but instead diffused throughout the channel region. Although Ye's devices happened to not suffer from this effect, non-localized dopants can lead to a significant amount of charge-impurity scattering, somewhat degrading the mobility compared to typically reported values.

MOSFETs based on MoS_2 tend to show naturally *n*-type behavior, whereas WSe_2 FETs tend to be more naturally *p*-type. As such, it is generally easier to *n*-dope the contacts in MoS_2 FETs and *p*-dope WSe_2 contacts to improve the device performance. However, Suh managed to show degenerate hole doping of MoS_2 by substitution of Mo cations with Nb atoms[57].

Effective though they may be at significantly reducing the Schottky barrier height and contact resistance, most surface doping techniques suffer from poor air or thermal stability.[58] It would also be challenging to scale them up for commercial applications. Substitutional doping presented a great alternative in this sense. The Nb atoms are secured via covalent bonding during the growth process, and do not degrade the chemical or thermal stability of MoS_2 in any way.

In 2016, our group (lead by Chuang) devised a completely dry method of degenerately doping the contact region of WSe_2 FETs that exploits the pristine nature of the VDW bonds between 2D materials[59]. They transferred two distinct pieces of Nb-doped WSe_2 onto a WSe_2 channel via VDW assembly. This was advantageous over attempting to form locally doped contact regions in the same crystal due to the difficulty associated with creating a doping profile that is sharply demarcated from the channel region. Each contact was ~20 nm thick to ensure degenerate

doping, and the channel region was passivated with ~10 nm h-BN to ensure a welldefined channel and locally doped contacts.

The result was WSe_2 FETs which showed excellent behavior at room temperature and a temperature dependence (the mobility reached ~10^3 at 5 K) which facilitated the study of several intrinsic properties of WSe_2 due to the absence of any noticeable contact effects. The mechanism of this '2D/2D contact' strategy is remarkably like selective ion implantation in Si devices. A larger carrier density in the degenerately doped contact as compared to the intrinsically doped channel leads to a work function difference between the two, and therefore a band offset. The offset is generally small owing to the weak interaction between VDW materials and can thus be readily tuned by a back-gate voltage. An energy band diagram explaining this phenomenon is shown in **Figure 1.6**.

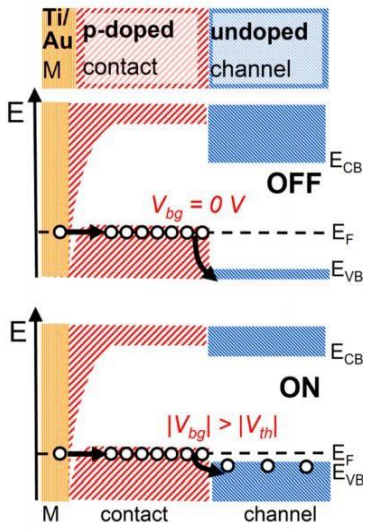


Figure 1.6 | Band diagram explaining the operation of a WSe_2 FET with degenerately *p*-doped 2D/2D contacts. Originally appeared in ref. 59.

Clearly, 2D/2D contacts are the superior strategy to try out on demonstrating low resistance Ohmic contacts to $PdSe_2$. However, if we take another look at the (calculated) $PdSe_2$ band structure in **figure 1.4** as we said before, along the Γ point, the valence band is quite wide, leading to a low

hole mobility- a problem that cannot be solved by doping. In principle, this would cause us to look for a substitutional *n* dopant like Re, which has also been shown to enhance the carrier concentration in WSe_2[60]. However, our group also demonstrated that while 0.5% Nb doped WSe_2 showed degenerate doping and a nearly temperature-independent carrier density, 0.5% Re doped WSe_2 showed- in contrast- a thermally activated behavior, owing to the trapping of electrons in localized states below the mobility edge[61]. It would seem $PdSe_2$ differs too much from the group VI TMDs for 2D/2D contacts to result in high performance FETs.

So, if we've ruled out the most effective strategies in both industry and research for engineering low resistance contacts in FET, how will we achieve the high performance $PdSe_2$ FETs we desire? In this work, we will discuss the results from another strategy developed by our group that is every bit as stable and scalable as 2D/2D contacts, but suitable for improving the the performance of ultrathin $PdSe_2$ FETs: using TMDCs as semiconducting *interlayers*.

As is the case with all things in the field, the use of 2D materials as a contact interlayer began with graphene. When Park inserted it at the interface of Ti and bulk Si[62], the contact resistivity, , was reduced to 1.4 nΩ cm^2, which is very close to the theoretical value of 1.3 nΩ cm^2. Interestingly, that study showed the exact same reduction occurs when monolayer h-BN is inserted as the interlayer, despite the fact that h-BN is an insulator. Clearly, something happens to modify the band alignment when a monolayer of a 2D material is inserted at the metal/semiconductor interface.

Our first guess may be that the interlayers de-couple the metal/semiconductor interface to de-pin the Fermi level and eliminate the effects of MIGS. Insulating thin films such as SiN, TiO_2, and ZnO have been inserted at the Si/metal interface before, and all served to reduce the ρ_c. They had to be thin enough (< 1 nm) to avoid incurring a large tunneling resistance, which explains

why monolayers of graphene and h-BN were used. But Park's calculation of the pinning factor complicated the picture. The pinning factor is one if the FL is de-pinned (Schottky limit) and zero if it is fully pinned (Bardeen limit). Park showed that the pinning factor between conventionally used metal contacts, graphene interlayers, and monolayer h-BN interlayers are all near the Bardeen limit.

The Fermi level is still quite pinned, but as Park elucidated, the metal/2D interlayer contact acts as a fully metalized contact with a reduced metal work function and pinning point near the conduction band edge of the channel. Furthermore, a dipole forms at the interface of the metal and 2D interlayer, buttressing the barrier height reduction. Park stipulates that the surface roughness of Si and the presence of dangling bonds may be the reason we still observe strong FLP. It stands to reason that the pinning factor would approach the Schottky limit if a 2D semiconductor was used as an interlayer to contact a 2D TMDC channel.

Pop et al employed this method to improve the performance of $MoTe_2$-based FETs[77]. They chose to use Sc contacts to $MoTe_2$ due to the low Sc work function but had to insert an hBN monolayer to mitigate performance losses since Sc is also highly reactive. The result was a nearly threefold reduction in the barrier height compared to that of conventionally used metals. But the reduction was not a complete one; the measured barriers were consistently in the 80-100 meV range, which is comparable to the barrier height of few-layer MoS_2 FETs with Ti/Au contacts. This can be explained by the *partial* de-pinning of the Fermi level. With the insertion of an h-BN interlayer, their $MoTe_2$ devices went from showing a significant amount of reverse biased leakage (hole) current to completely *n*-type behavior. However, the substantial electron barrier suggests the de-pinning effect is not complete. They stipulate this is due to local metaltelluride compounds still playing some role in the transport. $MoTe_2$ is not very chemically stable itself. Perhaps with

more stable metals and channel materials we can use an h-BN monolayer to realize a high performance device TMDC-based FET with a pinning factor that is close to the Schottky limit.

Our group (lead by Andrews and myself) accomplished this[79]. We used monolayer h-BN as an interlayer in air-stable MoS_2-based FETs with Ti/Au contacts. The result was again a significant reduction in the barrier height to around ~ 50 meV. However, we found that large bandgap of h-BN leads to a series tunneling resistance, even if the Fermi level is de-pinned.

Hence, we decided to move in a different direction altogether. We used WSe_2 and $MoSe_2$ as interlayers to an MoS_2 channel. We found that the barrier height of devices with WSe_2 interlayer was comparable to that when h-BN is used, but the lowest height was observed using $MoSe_2$. Our results showed that we can not only use 2D semimetals and insulators as interlayers, but 2D semiconductors as well, with the best device performance yielded by the latter.

The mechanism of 2D semiconductor interlayers differs completely from that of 2D semimetals or insulators. Our goal is no longer to de-pin the Fermi level; the pinning factor of our MoS_2 FETs is nearly zero. Rather, we seek to take advantage of favorable energy band alignment across the metal/TMDC interlayer/TMDC channel interface to engineer a small effective contact barrier. On the one hand, the Fermi level of the metal will pin close to the conduction band edge of the interlayer. One the other hand, there will be an offset between the band edges of the channel and interlayer, which will be small since both materials are group 6

TMDCs. Thus, the effective barrier height will follow the relation,

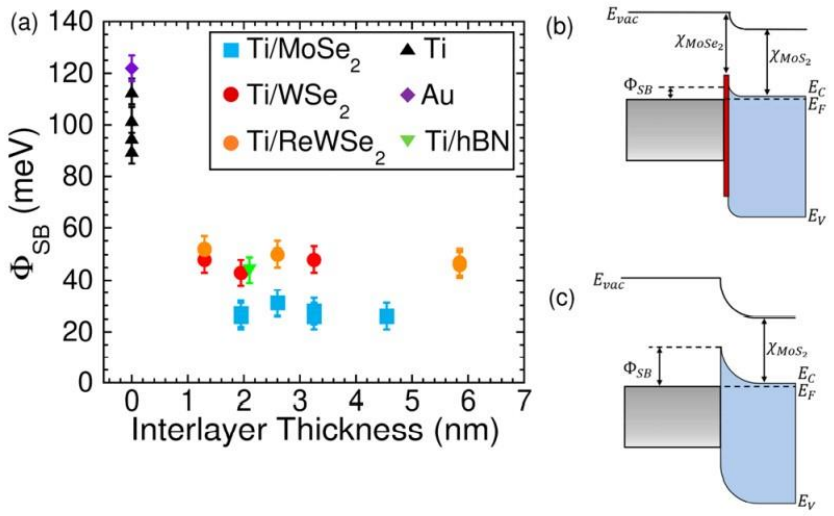
$$\Phi_{B,} = (E_F - \chi_{IL}) - (\chi_{channel} - \chi_{IL}) = E_F - \chi_{channel} \quad (1.16)$$

Where E_F is the energy at which FLP occurs at the metal/TMDC interlayer interface.

In the case of $MoSe_2$ interlayers in MoS_2 FETs, the band offset between the two materials is relatively small- hence the barrier height follows suit. This was further confirmed by the fact

that the height was slightly larger in WSe_2 interlayer FETs than in $MoSe_2$ interlayer FETs, since the band offset between WSe_2 and MoS_2 is slightly larger than that between MoS_2 and $MoSe_2$. The barrier height was also similar using lightly *n*-doped $Re_{0.005}W_{0.995}Se_2$ as an interlayer, suggesting the reduction is principally due to the small band offset; interfacial dipoles do not play a major role. A summary of the calculated SBH of MoS_2 FETs with 2D material interlayers is shown in **Figure 1.7a**.

Figure 1.7d shows a proposed energy band diagram for high performance $PdSe_2$ devices using this contact strategy. We do not know as much about the experimental band structure of $PdSe_2$, (particularly the position of the conduction band edge) hence it is harder to predict exactly which of the group 6 TMDCs will work best as a contact interlayer to a $PdSe_2$ channel. The small band gap of $PdSe_2$ could lead to a large band offset regardless of which material we select. But it's also possible we will find that the small bandgap facilitates a large ON current due to an ultralow tunneling resistance.



(d)

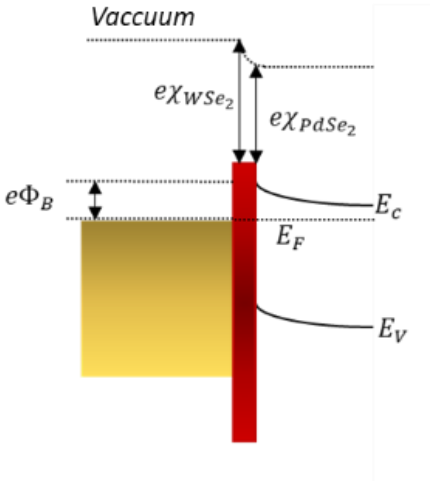


Figure 1.7| a. SBH of MoS_2 FETs with 2D material interlayers as a function of interlayer thickness. **b-c.** Energy band diagrams of an MoS_2 FETs with and without $MoSe_2$ as a semiconductor interlayer, showing the mechanism by which the SBH is reduced when $MoSe_2$ is reduced at the metal/semiconductor interface. (**a-c** originally appeared in ref 64) **d.** Proposed energy band diagram of $PdSe_2$ FETs with semiconductor interlayer. The interlayer can be any (stable) group 6 or group 10 TMDC.

CHAPTER 2: DEVICE FABRICATION AND CHARACTERIZATION

2.1 Mechanical Exfoliation

Most groups that study devices based on 2D materials find it easier to use chemical vapor deposition (CVD) to grow ultrathin samples. But CVD is an expensive and time consuming process, and the defects[65,66] and grain boundaries[67] that tend to form during growth can introduce challenges in subsequent steps of device fabrication. Hence, as we mentioned in the introduction, mechanical exfoliation from a bulk CVD grown crystal is the ideal method to prepare few-layer, bilayer, and monolayer TMDCs as well as graphene and h-BN.

Our bulk $PdSe_2$ crystals were grown by Mandrus' group at the University of Tennessee. The synthesis was performed via chemical vapor transport with iodine as the agent. Polycrystalline $PdSe_2$ was made from a mixture of Pd, (Alfa-Aesar, 99.999%) and Se (AlfaAesar, 99.999%) powders, and then used as a starting material to grow single crystals, resulting in a ~ 2.5 mm^3 flake. The flake was confirmed to be phase pure via X ray diffraction. Bulk crystals of group

6 TMDCs, graphite, and h-BN were all purchased from various nanotechnology companies (HQ Graphene, SPI Supplies, and 2D Semiconductor Supplies, respectively).

To exfoliate, a smaller flake of the bulk material is placed on a piece of scotch tape. A top scotch tape is then pressed onto the flake and bottom scotch tape, and then peeled back. The (weak) interlayer interaction implies the top scotch tape can easily peel off a much thinner layer from the bulk crystal. The process is then repeated until both tapes hold a checkerboard of exfoliated crystals with randomly distributed thicknesses, as shown in **figure 2.1c**.

In practice, obtaining ultrathin layers by mechanical exfoliation requires 3-5 pieces of top scotch tape, wasting both tape and crystals. Huang developed a repeatable method for exfoliating high-quality, large area samples of graphene and the bismuth, strontium, calcium, copper oxide superconductor $Bi_2Sr_2CaCu_2O_2$[68]. In the conventional exfoliation method, substrates comprised of SiO_2 on heavily doped Si are sonicated in acetone and isopropyl alcohol (DI water and piranha solution are also used), and then exposed to oxygen plasma to destroy any ambient adsorbates. Immediately after the plasma clean, the substrate is placed face down on the top scotch tape. The tape is then slowly removed and some percentage of the samples on tape are transferred to the substrate. The thicknesses of transferred crystals can be readily determined by their optical contrast; a bright white color indicates a thickness > 20 nm. Monolayers and bilayers are a translucent pink.

Huang's procedure for cleaning the substrate is conventional. But after cleaning, the substrate and attached tape are heated around 100˚C for ~ 5 minutes, and then cooled to room temperature. The tape is then slowly peeled back, as usual. Heating anneals the top layer (or layers) of bulk crystals to the substrate, greatly increasing the adhesion between the two. This improved adhesion also leads to increased sample size and yield (the total area covered by samples on the substrate, per exfoliation). The resultant graphene flakes obtained by Huang had areas between

60,000-85,200 μm^2, four orders of magnitude higher than the typical size of a 2D material. Heating also had no effect on the FET performance of the exfoliated graphene. Chemically gated four-terminal devices exhibited a room temperature mobility of 4,000 cm^2/Vs and the usual near-absent ON/OFF ratio.

However, Huang says little of the practicality of the new method for exfoliating monolayer and few-layer TMDs or h-BN. As we quickly found, this is because applying the method directly to TMDs yields large-area flakes, but the lowest attainable thickness is about 3 nm (~ 4 layers). Moreover, we postulated earlier that ultrathin $PdSe_2$ is likely harder to exfoliate than ultrathin samples of the group 6 TMDs, so it became important to devise a method that works across a wider range of 2D materials.

We have achieved this by making a couple modifications to Huang's method. First, we hold the top scotch tape at a small (0-45°) angle relative to the bottom tape. It was recently postulated that this assists in cleaving[69]. Holding the top and bottom tapes parallel to each other is akin to ripping off the entire surface area of ultrathin layers from the bulk crystal, while performing the exfoliation at a small angle ensures the ultrathin layer will be peeled back from the corner. Second, before the substrate cleaning, we search the checkerboards of exfoliated samples via optical microscope for ultrathin samples. On tape, thicker samples will shine bright, few-layers appear in a shale gray color, and bilayers and monolayers can only be identified by their silhouettes. After plasma treatment, the substrate is placed exactly where those samples have been found.

Huang claims to obtain large area graphene on substrate by annealing the top layer of a much thicker flake on tape. In our experience, ultrathin flakes are already on tape. Heating treatment simply ensures that the desired flake is transferred. Also, we perform the transfer of exfoliated crystals from tape to substrate *at* 100° C. We believe this ensures the sample surfaces

will be free of any tape residue. Some of the large-area flakes obtained using our method are also depicted in **figure 2.1 e-f**. As will be seen in the coming sections, FETs fabricated using our samples also exhibit good device performance.

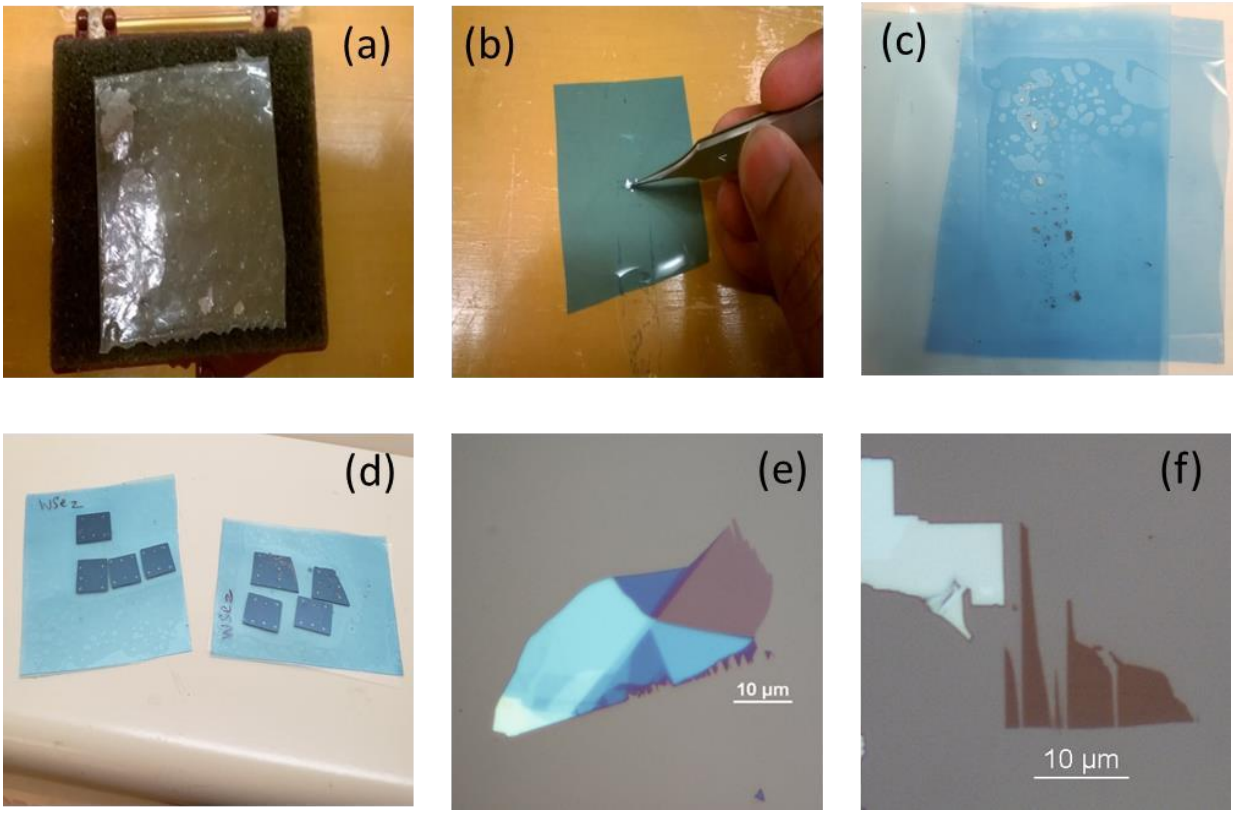


Figure 2.1| a-c: Mechanical exfoliation of MoS_2. **d:** Clean SiO_2 on Si substrates after being placed on exfoliated WSe_2 (before heating step) **e-f:** Optical micrographs of large area monolayer WSe_2 (left) and few-layer $PdSe_2$ (right). Both samples were exfoliated to SiO_2 using our modified version of the method developed by Huang.

2.2 Van Der Waals Assembly

2.2.1: PDMS Transfer

As we also briefly mentioned in the introduction, 2D materials can be stacked atop one another in a process formally known as VDW assembly, a powerful tool that enables us to engineer a wide variety of device structures. Realizing novel devices is often a simple matter of stacking the same materials in a different arrangement. However, it is critical that all interfaces between

materials be of the highest quality, as any residue or bubbles in the junctions between materials can introduce non-intrinsic effects in the ultimate device performance.

One widely used method of producing high quality material interfaces is polydimethylsiloxane (PDMS) transfer. PDMS is a transparent, highly flexible, and quite sticky polymer, upon which 2D materials can also be exfoliated. To make it, a 10:1 ratio of silicone base and curing agent is mixed, bubbles form and the mixture is then placed under vacuum to remove for 30 minutes to remove them. The mixture is then spin coated onto a polished Si wafer, baked for 30 minutes at 80˚ C, and finally cooled for another 30 min. Once cooling is done, it is cut into approximately one hundred stamps.

Stamps are then laid atop exfoliated crystals, and then removed. The strong adhesion will cause some crystals to transfer from the tape to PDMS, where they can be searched via optical microscope. In this case, the optical contrast doesn't change. Once an ideal sample is found, a blade is used to cut a smaller stamp around the sample. It is separated from the large stamp and placed on a glass slide.

The glass slide is the link between the sample and the micromanipulator, as can be seen in **figure 2.2**. The micromanipulator enables us to move the slide and thus align the sample on PDMS with another sample which has been exfoliated onto SiO_2. Once the desired alignment is achieved, the slide is lowered to bring the two samples into contact. The PDMS is then slowly removed, leaving a VDW heterostructure (provided the VDW forces hold the stack together).

The adhesion between materials can be improved by light annealing, typically for 30 minutes at 250 ˚C in 10% Hydrogen and 90% Argon (known as forming gas).

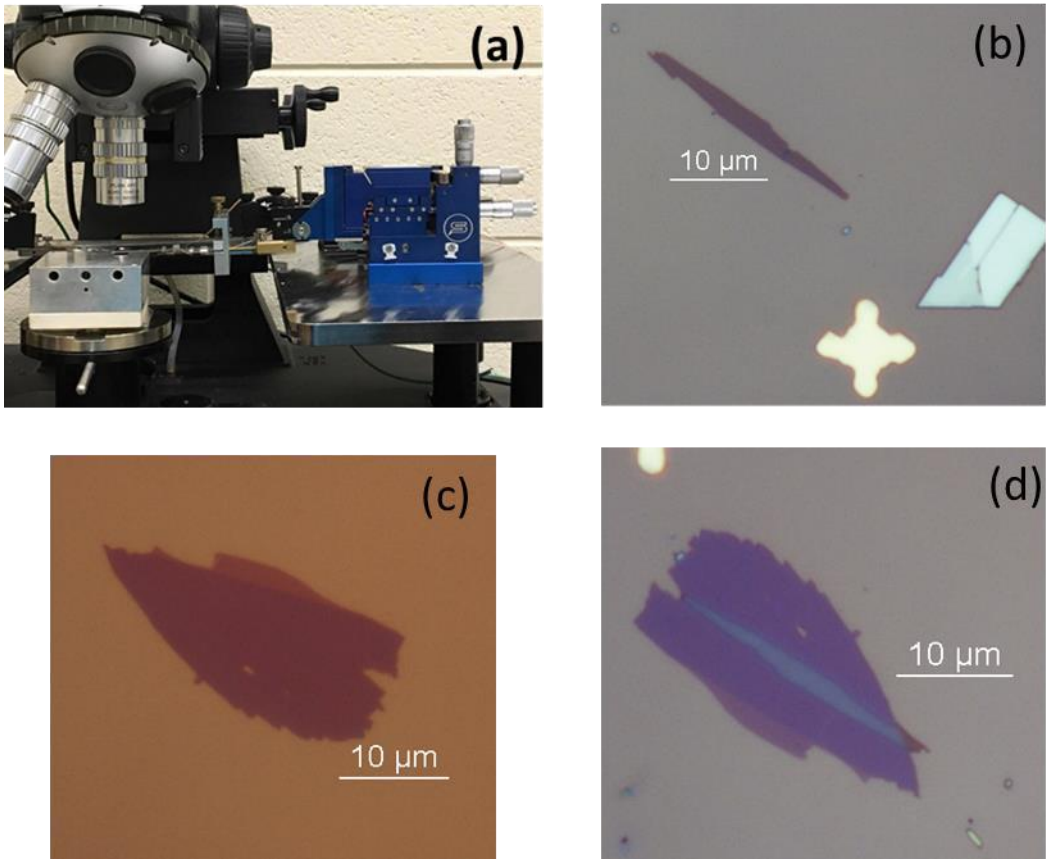


Figure 2.2| a: Set-up for VDW assembly: optical microscope, (for viewing the transfer) sample stage, and micromanipulator (with mounted glass side). **B:** Few-layer $PdSe_2$ on SiO_2, **c**: Few-layer WSe_2 on SiO_2, **d:** VDW consisting of few-layer WSe_2 stacked atop few-layer $PdSe_2$

2.2.2: Polycarbonate (PC) Pick-Up Method

The PDMS transfer mechanism does suffer from a fundamental drawback. The adhesion between exfoliated materials and PDMS is not that strong. Consequently, the minimum attainable thickness of samples on PDMS is approximately three layers. Perera did report a monolayer of MoS_2, but such samples are in general few and far between.

The PC pick-up method has proved quite useful in transferring ultrathin materials (or heterostructures involving them). 'PC' in this case refers to a 6 to 1 ratio mixture of chloroform and polycarbonate resin. The resin is added in cube form to chloroform, and then placed on a plate shaker for around 30 minutes to dissolve.

To transfer the sample, the substrate is first mounted on a glass slide and secured using double-sided tape. Two droplets of PC are administered onto the substrate via micro-pipette. Weighing paper is laid atop the droplets, spreading them out into a thin film that completely covers the entire substrate. The 2D material to be transferred is located on the substrate, and a stamp of PDMS is placed atop the now PC-coated material. A blade is used to cut the PC around the PDMS stamp, and excess PC is carefully removed. At this point, all that remains on the substrate is the 2D material, PC film, and PDMS stamp.

Deionized water is then pipetted under the PC. The water attracts to the SiO_2 substrate, and seeps between it and the (hydrophobic) PC film, separating the two. The sticky PC takes the 2D material with it. The PDMS stamp allows us to mount the 2D material-on-PC to a glass slide, which is then loaded onto the micromanipulator, as it is in PDMS transfer.

The procedure for transferring 2D materials on PC and on PDMS are quite similar, with a few notable differences. The 2D material on PC is aligned and brought into contact with another material on SiO_2. For PDMS transfer, the PDMS touches the substrate only enough so that the 2D material to be transferred makes intimate contact with the material it is being transferred to. For the PC pick up method, once the alignment is complete, the entire stamp is touched down onto the substrate at 110° C. We transfer at this temperature for two reasons: first, to improve the VDW adhesion between materials, and second to eliminate any ambient moisture that may get trapped in the interface. The transfer stage is heated to 130˚ C, at which point the PC melts and sticks to the substrate. The glass slide is lifted using the micromanipulator, taking the PDMS stamp with it.

A huge advantage of PC over PDMS is that PC allows for sequential (or ‘batch’) transfers to be performed. **Figure 2.3** depicts this portion of the process. After removing the PDMS stamp, the PC is cooled to ~50° C (at which point it solidifies) and tweezers are used to remove it from the SiO_2 substrate. The VDW attraction between the initial material on PC and the target material

on SiO_2 will hold the two together, picking up the target off the substrate. Now we have a VDW heterostructure on the PC film, which we can add more layers to simply by repeating the process.

Sequential pick-ups yield high quality material interfaces since the target materials are picked up using the VDW interaction alone. The only possible contaminant is the water that was used to pick up the initial material- generally not a problem so long as it is quickly blown off with an inert gas after the sample-on-PC is mounted on the PDMS stamp. Once the final transfer is complete, the substrate is bathed in chloroform, dissolving the PC film, and leaving the VDW heterostructure. It is generally unnecessary to anneal this structure in forming gas, as it was already somewhat annealed in air.

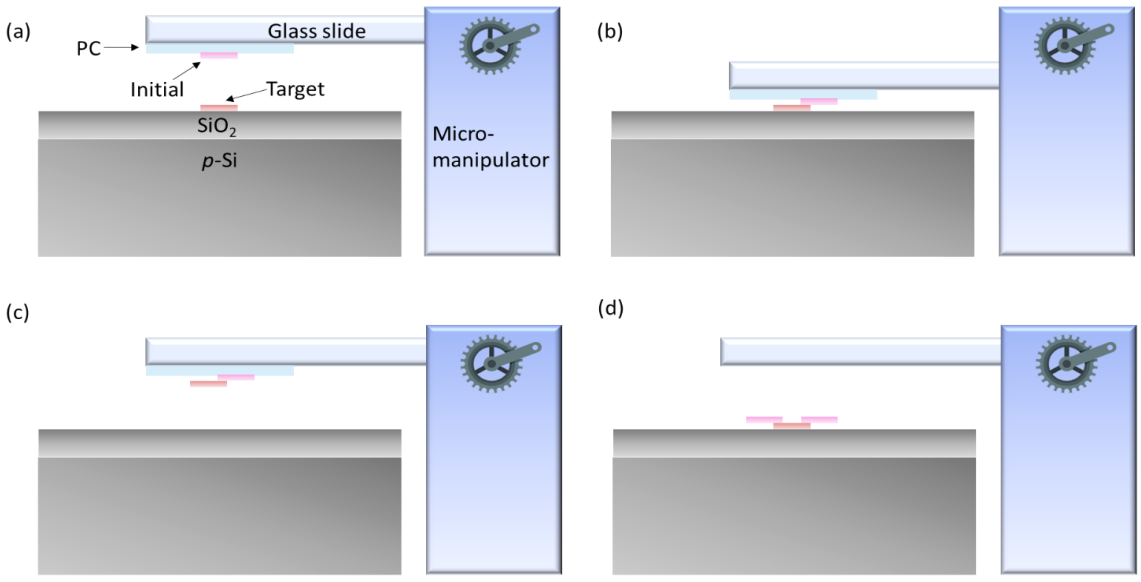


Figure 2.3| a: sample on PDMS aligned with another on SiO_2 via the micromanipulator. **b:** Touchdown of the PC film to bring the initial and target materials into intimate contact. **c**: Pick up of the target material by the initial material **d:** Completed VDW heterostructure on SiO_2 (after dissolving PC).

2.2.3: Polypropylene carbonate (PPC) Pick-Up Method

There is yet a third method of stacking 2D materials. Polypropylene carbonate (PPC) is a transparent, polymerous film very similar to PC. It is mixed in a similar fashion to PC (cubes of PPC resin are dropped in chloroform and placed on a mechanical shaker to dissolve). The thickness

of the resultant film is about 1 μm; much thicker than PC, and hence much easier to handle with tweezers.

The most attractive feature of PPC is the ability to use it in an 'inverted' pick-up method that takes advantage of h-BN as the ideal initial material. Booth noticed that this method was highly effective in achieving atomically clean interfaces in a heterostructure consisting of graphene sandwiched between h-BN layers[70]. We also noticed that the inverted pick-up method showed improved interface quality over the PC pick up method for reasons we will postulate below.

The PPC film exhibits strong adhesion to 2D materials at 40° C. As shown in **figure 2.4a**, our first step is to drop cast the PPC solution onto a PDMS stamp and let it dry to form a hockeypuck-shaped film. The PPC/PDMS stack is used to pick-up h-BN at 40° C (**figure 2.4b-c**)**.** Subsequent pick-ups of other 2D materials are then performed at 110° C, as we would using the PC pick up method. Once the final transfer is performed, the heterostructure-on-PPC stack is flipped so that the PPC contacts SiO_2 and the heterostructure sits on top (**figure 2.4d**)**,** hence why this is commonly referred to as the 'inverted' pick-up method. The whole stack is then annealed in forming gas, eliminating the PPC and leaving only the VDW heterostructure. (**figure 2.4e**)**.** h-BN forms a very high quality interface with nearly any 2D material, as Booth showed with graphene. Another group used it to form atomically clean interfaces between monolayers of h-BN and WSe_2[84]. We noticed that the interface quality between $PdSe_2$ and other 2D materials is more variable. As is evident in **figure 2.4f**, few-layer $PdSe_2$ adheres quite well to h-BN, but the interface between $PdSe_2$ and group 6 TMDCs can be riddled with bubbles.

This may be another consequence of the puckered layer structure of $PdSe_2$. The interlayer interaction between $PdSe_2$ and group 6 TMDCs is likely weaker than that between $PdSe_2$ and hBN. Bubbles tend to form between the former since are unable to be squeezed out by the VDW

attraction. A strong interlayer interaction can easily squeeze out the adsorbates, hence the Wse_2/hBN and graphene/hBN interfaces are relatively bubble-free.

To form VDW heterostructures that involve $PdSe_2$ with atomically clean interfaces, we implored the use of PPC instead of PC. As shown in **figure 2.4b,** we first picked up h-BN, then a very narrow strip of $PdSe_2$, and finally a much wider layer of graphene or group 6 TMDC. When we perform the VDW assembly this way, most of the surface area of the top layer interacts strongly with h-BN, strengthening the interaction between $PdSe_2$ and the top layer as well. The result is a much lower bubble density using PPC than PC. It's necessary to use the inverted method, since we would have to pick up the graphene or group 6 TMDC first to fabricate the same structure using PC.

Of course, *some* bubbles will always form. An 'atomically clean interface' is really one in which there are so few bubbles we can avoid them in fabricating electrodes and ensure they have no effect on the performance of devices made from these structures.

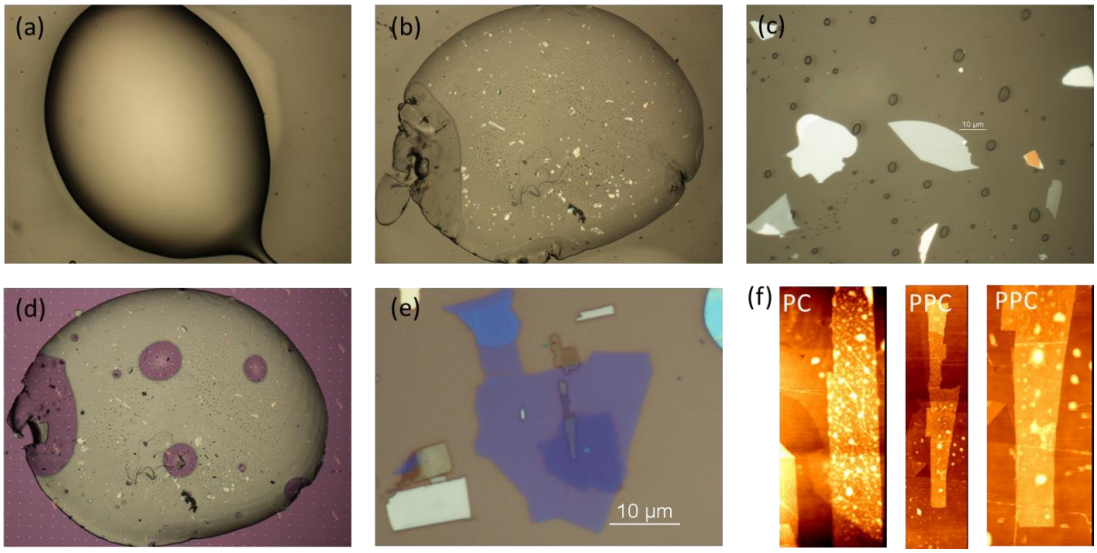


Figure 2.4| a: drop-casted PPC film on PDMS **b-c**: PPC film after picking up h-BN at 40° C. **d**: PPC film after being flipped onto SiO_2. **E:** Completed VDW heterostructure on SiO_2 after annealing away PPC. **F:** comparison of atomic force micrographs of the structure fabricated in part **e** to a similar structure fabricated using PC. Notice the near-absence of bubbles in the overlap region between materials when PPC is used instead of PC.

2.3 Characterization of Surface Morphology and Film Thickness

There are several methods of microscopy to characterize the interface quality, including transmission electron microscopy (TEM), atomic force microscopy (AFM), and optical microscopy[46]. In this work, we implore the latter two techniques to ensure junctions that are as close to the ideal configuration as possible.

2.3.1: Optical Microscopy

The optical microscope employed in this work is the Nikon Eclipse LV150. The complete set-up is shown in **figure 2.5**. It has 5X, 10X, 20X, 50X, and 100X magnification settings. The image is fed back to the Nikon Instruments Elements software, which enables us to measure the dimensions of samples and heterostructures, as well as to subtract stray light from the image to obtain an accurate optical contrast. A rough estimate of the cleanliness of the samples and heterostructures can be made by imaging them in the dark field setting. A Differential Image High Contrast (DIHC) add-on enables a rough characterization of the smoothness and uniformity of samples. Bubbles can be seen in both dark field and DIC images. These capabilities prove very useful in selecting the best samples to transfer on PDMS, as well as roughly checking the quality of transfers.

2.3.2: Atomic Force Microscopy

Once a VDW heterostructure has been built, one hopes to see a smooth overlap of materials in optical micrographs. If the first test of optical microscopy is passed, then an AFM scan is performed. The resolution limit of AFM is angstroms, several orders below the optical diffraction limit, thus the absence of residue and bubbles in an AFM scan is more definitive proof of high quality interfaces.

All AFM images in this work were taken using a Park XE15 AFM, some which can be seen in **figure 2.4**. Another is pictured in **figure 2.5**. The cantilever is configured to scan in

"tapping mode", as opposed to the far more invasive "contact mode"[71]. The cantilever oscillates a small distance above the sample and the surface morphology and thickness are measured by a laser shone on the tip and fed back to the Park AFM software. AFM is also used to confirm the thicknesses of each material in a heterostructure and match them to the optical contrast.

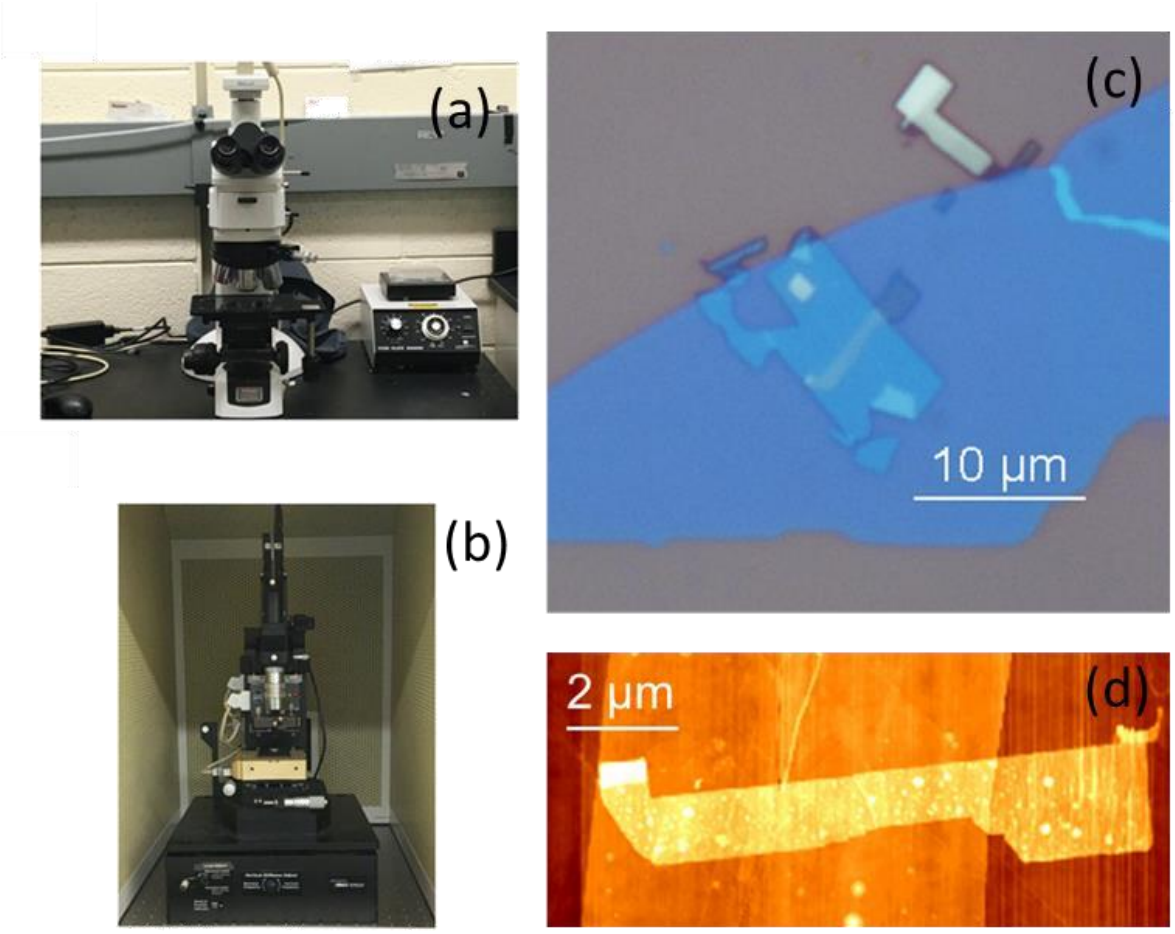


Figure 2.5| a: Nikon Eclipse LV150 Optical Microscope and optical micrograph of VdWH **b:** Park XE15 AFM and AFM scan of the same sample, confirming the sample has a smooth and atomically clean surface.

2.4 Metallization Process

Once the sample or heterostructure has been fully imaged, metal electrodes are fabricated to form a MOSFET. The sample itself is contacted by "inner" electrodes that are designed according to the transport mechanism under study. The inner electrodes are connected to much larger "outer" contact pads, which act as a liaison between the device and electrical

characterization instruments. Occasionally, modifications must be made to the 'outer' patterns, such as the large contact pad for ionic liquid gating. In most cases the outer electrode design does not change.

The electrode fabrication process has three steps. First electrodes are designed, directly from an optical microscope image of the sample. Then, electron beam lithography (EBL) is performed to pattern them. Finally, metal is deposited into the pattern, and the completed device can be electrically characterized.

2.4.1: Electrode Design

Designing of EBL patterns is performed using the computer-aided design (CAD) feature of the Nano Pattern Generation System (NPGS) software. First, an optical micrograph of the sample or heterostructure shot at 100X magnification is imported into CAD. Then, an outline of the sample is drawn. Then the optical micrograph is deleted, and inner electrodes are drawn over this outline. There are also CAD designs for the connecting wires and contact pads that are written at 300X, and 100X that can be modified for such things as a side gate.

2.4.2: Electron Beam Lithography

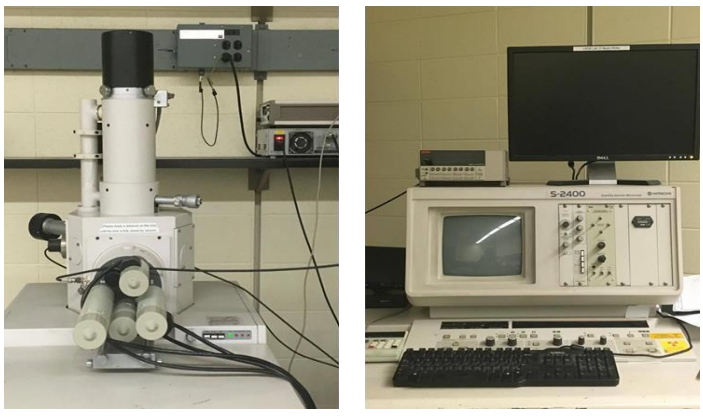
Once the design is completed the preparation for EBL begins. The sample or heterostructure is coated with a polymer known as polymethyl methacrylate (PMMA). In this work, 2 layers of PMMA 495 A4 are spun onto the substrate at 3000 revolutions per minute for 45 seconds, followed by 1 layer of PMMA 950 A2. Each layer of PMMA is coated on and then baked at 180˚ C for 5 minutes. In total, the PMMA should have a thickness of ~ 330 nm. A micromanipulator is used to place a bit of silver paint a a few hundred microns away from the sample.

Electron beam lithography is performed by a Scanning Electron Microscope (SEM). In this project, the Hitachi S2400 is utilized (**figure 2.6**). After the substrate is loaded and sufficiently

high vacuum has been achieved, the beam is optimized by saturating the current, and using a stripe of gold nanoparticles to roughly focus the beam and minimize astigmatism and wobbling. Then, the beam is moved to the substrate, the height is changed to cohere the beam, and metal alignment marks assist in aligning it to the correct angular position and locating the sample. Once near the sample, the silver paint mentioned is used to finely focus the beam; a good focus is implied by clearly identifiable features of silver particles at 300,000X magnification. The CAD design is loaded into a 'run file' and processed. The PMMA is exposed to electron beam in the areas mandated by the design.

After the pattern has been written, it is developed in a solution of methyl isobutyl ketone (MIBK) and methyl ethyl ketone (MEK). Trenches form in the areas where the PMMA has been exposed to the electron beam. If the 'dose' is sufficiently high, (typical doses for areas are 300350 nC/cm^2 and 15-17 nC/cm for lines) the trenches reach all the way through the PMMA to the areas of the sample we intended to expose in the design. MIBK is the main developer. MEK enhances the development process. Development is performed simply by placing the substrate in solution on an orbital shaker for 70 seconds. 495A4 and 950A2 have different molecular weights. This has the effect of producing some 'undercut' of the trenches upon development, which is beneficial for making high quality electrical contacts. Some developed patterns are also shown in **figure 2.6**.

(a)



(b)

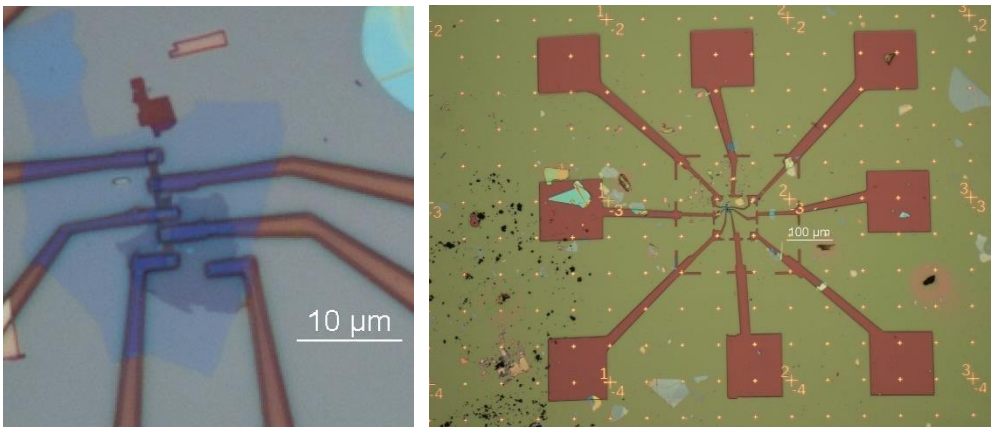


Figure 2.6| a: Hitachi S2400 SEM (left) and control system (right). **b:** Optical micrograph of a fully developed pattern at 100X (left) and 10X (right) magnification. The pattern was generated on the heterostructure

2.4.3: Metal Deposition

The final step of device fabrication is depositing metal into the pattern generated by EBL. The deposition was performed on the Enerjet Evaporator at the Lurie Nanofabrication Facility. The Enerjet is a typical e-beam evaporator, which functions by evaporating source metals under an ultra-high vacuum, (10^{-8}- 10^{-7} torr) that prevents diffusion of the source molecules and restricts them to a beam. It utilizes point sources and long throw distances to minimize heat transfer.

A quartz crystal sensor monitors the rate at which the source metal is deposited. We use a deposition rate of 10 Å/s. During deposition the Enerjet varies the e-beam power to maintain a steady deposition rate for highly uniform surfaces. Approximately 10 nm of titanium is deposited, along with 40 nm of gold. After the deposition is completed, excess metal is lifted off by placing the substrate in acetone for 5-10 minutes. The same device which was patterned in **figure 2.5** is shown after liftoff in **2.7**.

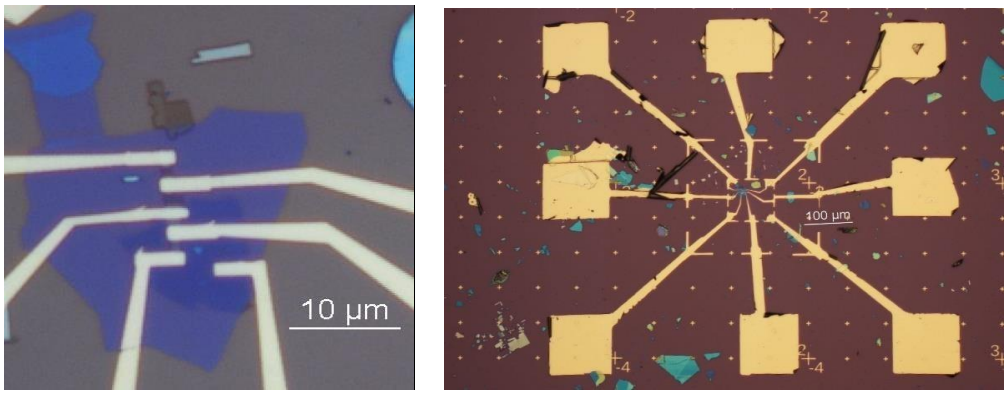


Figure 2.7| Optical micrographs of a few-layer $PdSe_2$ FET after liftoff, the final step of the metallization process.

2.5 Electrical Characterization

To characterize the transfer characteristics and current-voltage characteristics of FETs with 2D material channels, bias and gate voltages are supplied by the Keithley 4200 Semiconductor Characterization System. The Keithley 4200 can perform a wide variety of electrical measurements.

All measurements are performed in the sample chamber of the Lakeshore TTPX (**figure 2.8a**), a typical vacuum probe station. The ultra-high vacuum (10^{-7}-10^{-6} torr) eliminates the effects of ambient adsorbates. The probes are more sensitive to small current fluctuations, ($10^{-15}10^{-12}$ A) than a typic digital multimeter, providing a much more accurate description of device performance. Most of our measurements are 2-point probe, but 4-point probe measurements can also be performed to eliminate parasitic resistances. Liquid nitrogen is used to explore the temperature dependence of FET behavior. The system can cool to as low as ~77 K.

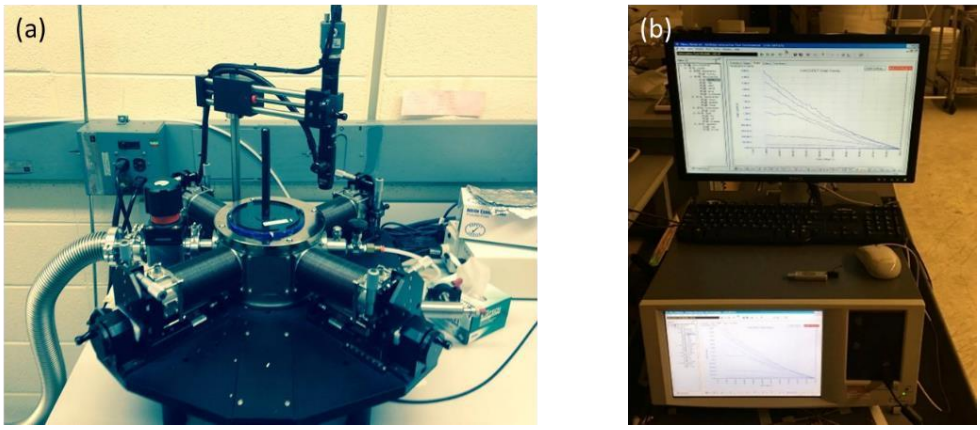


Figure 2.8| a: Lakeshore TTPX Vacuum Probe Station **b:** Keithley 4200 Semiconductor Characterization System

CHAPTER 3: RESULTS AND DISCUSSION

3.1 WSe_2/$PdSe_2$ FETs

To recap, atomically thin and uniform 2D semiconductors with excellent mechanical strength and flexibility are promising channel materials for next generation flexible electronics and optoelectronics beyond the scaling limit of Si-based metal-oxidesemiconductor FETs (MOSFETs). [71-85] While group-6 TMDCs such as MoS_2, $MoSe_2$ and WSe_2 are among the most studied 2D semiconductors, the relatively low electron mobility of group-6 TMDCs at room temperature limits their electronic applications.[108,109] In addition, group-6 TMDCs tend to form a substantial energy barrier with most metals used for making electrical contacts, further limiting their electronics and optoelectronics applications.[76-90]

Recently, group-10 TMDs such as $PtSe_2$ and $PdSe_2$ have emerged as high mobility 2D electronic materials with a theoretically predicted high electron mobility exceeding 1000 $cm^2V^1s^{-1}$ at room temperature[110], which is significantly higher than that of group-6 TMDs such as MoS_2 and WSe_2. Similar to group-6 TMDCs, group-10 TMDCs are also air-stable. In addition, their electronic properties are predicted to change qualitatively with the layer-number, evolving from semi-metallic in bulk to semiconducting with a bandgap over 1 eV in a monolayer. Unlike back

phosphorus, these materials are also chemically stable. However, the experimentally observed field-effect mobility of group-10 TMDs is much lower their theoretically predicted mobility especially for thinner samples, which is likely to be limited by the presence of a non-negligible Schottky barrier (SB) at the contacts.[25, 27] In this article, we demonstrate superior performance of $PdSe_2/WSe_2$ van der Waals heterostructures than $PdSe_2$ or WSe_2 as a channel material of field-effect transistors, where WSe_2 acts as a buffer between $PdSe_2$ and contact metal to alleviate the Fermi-level pinning effect and therefore significantly lower the Schottky barrier. In this article, we demonstrate superior performance of $PdSe_2/WSe_2$ van der Waals heterostructure than $PdSe_2$ or WSe_2 alone as a channel material for field-effect transistors (FETs), where WSe_2 acts as a buffer between $PdSe_2$ and Ti metal at the drain/source contacts to alleviate the Fermi-level pinning effect and therefore significantly lower the SB between Ti metal and $PdSe_2$. As a result, our FETs based on $PdSe_2/WSe_2$ heterostructures exhibit a two-terminal effective mobility exceeding 200 $cm^2 V^{-1} s^{-1}$ at room temperature and approaching 700 $cm^2 V^{-1} s^{-1}$ at 77 K, indicating phonon-limited electron transport. By contrast, the two-terminal effective mobility of FETs based on few-layer $PdSe_2$ alone (without WSe_2) is substantially lower, especially at low temperatures suggesting that the electron transport is limited by the $Ti/PdSe_2$ contacts. In addition, the electron mobility of $PdSe_2/WSe_2$ heterostructures also significantly exceeds that of WSe_2. Furthermore, the increase of bandgap with decreasing $PdSe_2$ thickness leads to higher ON/OFF ratio in FETs consisting of $PdSe_2/WSe_2$ heterostructures with thinner $PdSe_2$. Our $PdSe_2/WSe_2$ heterostructure-based FET consisting of a trilayer $PdSe_2$ and a bilayer WSe_2 concurrently exhibits a high ON/OFF ratio of ~ 10^7 and significantly higher two-terminal electron mobility compared to FETs based on a trilayer $PdSe_2$ or a bilayer WSe_2 alone.

3.1.1 Comparison of $WSe_2/PdSe_2$ FET and $PdSe_2$ FET Performance at Room Temperature

Figure 3.1a shows an optical micrograph **(panels i and ii)** and schematic **(panel iii)** of two FET devices consisting of a $PdSe_2$ nanosheet and $WSe_2/PdSe_2$ heterostructure as the channel material, respectively. The $PdSe_2$ in both devices is ~ 4 nm thick, and the WSe_2 in the $WSe_2/PdSe_2$ heterostructure is ~ 2 nm (3 Layers). To fabricate the FET devices, 10 – 30 nm thick hBN flakes exfoliated on degenerately doped Si with 280 nm of thermal oxide were used as ultra-flat and ultra-smooth substrates to minimize dangling bonds and charge traps. Next, mechanically exfoliated few-layer $PdSe_2$ nanosheets were placed on the hBN substrates by a dry transfer method.[77, 91-92] Subsequently, ultrathin WSe_2 flakes were stacked on top of the $PdSe_2$ nanosheets also by the dry transfer method to form the $WSe_2/PdSe_2$ heterostructure. Finally, metal electrodes, consisting of 10 nm Ti and 40 nm Au, were fabricated on top of the drain/source regions of the $PdSe_2$ or $WSe_2/PdSe_2$ channel by electron beam lithography and electron beam assisted metal deposition.

To measure the electrical properties of the FET devices, back-gate biases were applied through the SiO_2/hBN dielectric stack to tune the carrier density in the channel. **Figure 3.1b, c** displays the output characteristics of the two devices shown in **Figure 3.1a**. While the $WSe_2/PdSe_2$ device exhibits highly symmetric and linear *I*-*V* characteristics (**Figure 3.1c**), the *I*-*V* curves of the $PdSe_2$ device with nominally identical Ti/Au contacts (**Figure 3.1b**) is substantially more non-linear and asymmetric than the $WSe_2/PdSe_2$ device, indicating a more significant SB in the $PdSe_2$ device than in the $WSe_2/PdSe_2$ device.

Figure 3.1d shows the semi-log plots of room-temperature transfer characteristics of the two FETs at a drain/source voltage of V_{ds} = 1 V. Both the ON/OFF ratio and on-current of the $WSe_2/PdSe_2$ device are significantly higher than those of the $PdSe_2$ device, which can be partially

attributed to the enhancement of on-current enabled by lower contact resistance. In addition, the subthreshold swing of the $WSe_2/PdSe_2$ device is also much smaller (sharper) than that of the $PdSe_2$ device. The reduced switching steepness of the $PdSe_2$ device cannot be attributed to charge traps at the channel/dielectric interface because both devices have nominally identical $hBN/PdSe_2$ interface. Therefore, it is likely a contact effect due to thermally assisted tunneling through a SB at the $Ti/PdSe_2$ contacts.[93] By contrast, the near absence of such a thermally assisted tunneling region in the $WSe_2/PdSe_2$ device strongly suggests a significantly reduced SB height (SBH) because higher thermionic current can be reached before the thermally assisted tunneling current becomes dominant in the case of a negligibly small SBH.

Figure 3.1e shows the linear plots of the 2D conductivity (defined as ($\sigma_{2D} = \frac{L}{W}\frac{I_{ds}}{V_{ds}}$, where L and W are the channel length and width, respectively) *versus* gate voltage to quantitatively compare the transfer characteristics of the two devices. While both devices display *n*-type behavior, the threshold voltage of the $PdSe_2$ device is shifted by ~ 50 V to the right (positive direction), suggesting that the current in the $PdSe_2$ is strongly suppressed by a substantial SB in the low gate voltage region ($-20 < V_{gs} < 30$ V) in comparison with the $WSe_2/PdSe_2$ device. This region of suppressed drain current on the linear plot coincides with the thermally assisted tunneling region on the semi-log plot shown in **Figure 3.1d**, providing further evidence of a significant SBH at the $Ti/PdSe_2$ contacts and the WSe_2 layer between Ti metal and $PdSe_2$ significantly reduces the SBH.

Interestingly, while the on-current of the $WSe_2/PdSe_2$ device is ~ 4.6 larger than that of the $PdSe_2$ device measured at the back-gate voltage of 80 V, the field-effect mobility of the former (130 $cm^2\,V^{-1}\,s^{-1}$) is only slightly larger than the latter (117 $cm^2\,V^{-1}\,s^{-1}$). Here the field-effect mobility is defined as

$$\mu_{FE} = \frac{1}{C_{gs}}\frac{d\sigma_{2D}}{dV_{gs}} \tag{3.1}$$

Where C_{gs} is gate capacitance (equivalent series capacitance of SiO_2 and hBN substrate) and σ_{2D} is the 2D conductivity. The strong discrepancy between the differences in on-current and field-effect mobility of the two devices indicates that the field-effect mobility of the $PdSe_2$ device is likely overestimated due to the presence of a notable SB at the contacts that strongly depends on the gate voltage. The drain current in the $PdSe_2$ device is suppressed by a large SBH at low gate voltages (carrier densities) but the current rapidly increases at higher V_{GS} as the SB width is reduced by the gate voltage, leading to an artificially enhanced slope of its transfer characteristic and consequently overestimation of the field-effect mobility.[94] Another possible artifact in the extraction of field-effect mobility is the carrier density dependence of the mobility. In the case of mobility increasing (increasing) with carrier density, the extracted field-effect mobility includes an additional positive (negative) term that is proportional to the first derivative of the mobility over gate voltage (carrier density).[95] However, this is unlikely a major cause of field-effect mobility overestimation in our $PdSe_2$ devices because their actual mobility (Drude mobility) slightly decreases with increasing carrier density in the high gate voltage region (as discussed below in detail), giving rise to a small additional negative term in the extracted field-effect mobility at high gate voltages.

Besides field-effect mobility, we also extracted effective mobility of the two devices. In accordance with the Drude model, the effective mobility is defined by the 2D conductivity over the carrier density.

$$\mu_{\mathrm{eff}} = \frac{\sigma_{2\mathrm{D}}}{n} \tag{3.2}$$

Here the carrier density is defined as

$$n = C_{gs}\left(V_{gs} - V_{th}\right) \tag{3.3}$$

where V_{th} is the threshold voltage. In order to correctly derive the effective mobility, it is important to accurately determine the threshold voltage (V_{th}) corresponding to zero carrier density.

In ideal transistors with low-resistance ohmic contacts, the effective mobility should be consistent with the actual mobility. However, the presence of a significant SB not only shifts the threshold voltage but also reduce the 2D conductivity. As a result, the effective mobility could also deviate significantly from the actual mobility. Therefore, it is important to extract both the field-effect and effective mobilities. They should be consistent with each other in the case of FETs with low-resistance ohmic (or nearly ohmic) contacts and gate independent channel mobility. A discrepancy between the field-effect and effective mobility values extracted from the same device indicates the presence of a significant SB and or carrier density dependent channel mobility.

Because a much large SBH is likely present in the $PdSe_2$ device than in the $WSe_2/PdSe_2$ device as indicated by the large positive threshold voltage shift in the former, we used the threshold voltage of the $WSe_2/PdSe_2$ device to determine the electron density for both devices to avoid underestimation of electron density in the $PdSe_2$ device caused by the threshold shift. As shown in **Figure 3.1f**, the effective mobility of the $WSe_2/PdSe_2$ device is similar to its field-effect mobility, suggesting that the device performance is dominated by the channel rather than by the contact effects. By contrast, the effective mobility of the $PdSe_2$ device is 2-3 times smaller than its field-effect mobility. The substantially smaller effective mobility than field-effect mobility in the $PdSe_2$ device indicates overestimation of field-effect mobility due to the presence of a gate-dependent non-negligible SB: the rapid increase of the drain current as the SB thickness is reduced by the gate voltage leads to an artificially enhanced slope of the transfer characteristics. The effective mobilities of $PdSe_2$ and $WSe_2/PdSe_2$ devices also exhibit qualitatively different gate dependence. While the effective mobility of the $PdSe_2$ device monotonously increases with gate

voltage to ~ 42 $cm^2 V^{-1} s^{-1}$ at ~ 80 V, that of the $WSe_2/PdSe_2$ device initially increases with the gate voltage at low gate voltages and then starts to decrease after it reaches a maximum value of ~126 $cm^2 V^{-1} s^{-1}$ at ~ 34 V. The monotonous increase of two-terminal effective mobility in the $PdSe_2$ device can be attributed to thinning of SB by an increasingly positive gate voltage.

On the other hand, the decrease of effective mobility with gate voltage in the $WSe_2/PdSe_2$ device cannot be explained by gate tuning of the SB. We attribute it to increased channel/dielectric interfacial scattering as the electrons are pulled closer to the channel/dielectric interface by an increasingly positive gate voltage. The interface scattering is likely caused by the impurities introduced in the fabrication process because our devices were fabricated in ambient environment. We expect a much cleaner channel/dielectric interface and reduced interface scattering if the devices are fabricated in inert environment inside a glove box, which will be part of our future research.

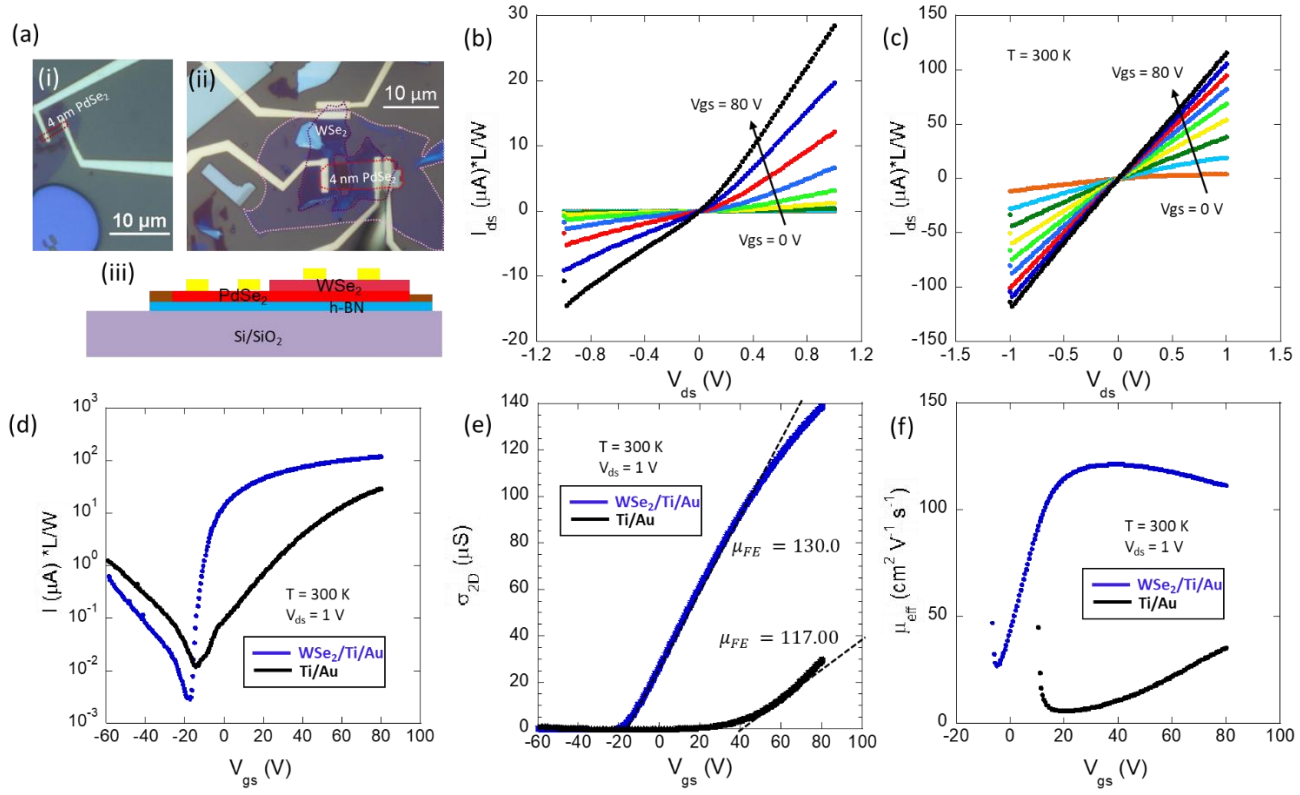


Figure 3.1| **a:** Device structure of WSe_2 and $WSe_2/PdSe_2$ FETs. Optical micrograph of FETs consisting of **(i)** a ~ 4nm thick $PdSe_2$ channel, **(ii)** a heterostructure channel of ~4 nm thick $PdSe_2$ and a ~ 2 nm thick WSe_2, and **(iii)** the side-view schematics of the $PdSe_2$ and $WSe_2/PdSe_2$ devices. (**b-c)** Output characteristics of (**b)** the $PdSe_2$ and **(c)** the $WSe_2/PdSe_2$ FETs. (**d)** Transfer characteristics of the $PdSe_2$ and$WSe_2/PdSe_2$ FETs plotted on semilog scale. (**e)** Two-terminal 2D conductivity of the $PdSe_2$ and $WSe_2/PdSe_2$ FET as a function of gate voltage plotted on linear scale. (**f**) Effective-mobility of the $PdSe_2$ and $WSe_2/PdSe_2$ FETs as a function of gate voltage. All the date are taken at room temperature.

It is worth pointing out that the WSe_2 does not completely cover the channel region of the device in **Figure 3.1**. As a result, the drain-source current only flows in the $PdSe_2$ layer in the $WSe_2/PdSe_2$ device shown in **Figure 3.1a**. Qualitatively and quantitatively similar behavior is observed in $WSe_2/PdSe_2$ devices where WSe_2 completely covers the channel as well as the drain/source regions (see **Figure 3.2**) suggesting that $PdSe_2$ is the active current carrying layer in the $WSe_2/PdSe_2$ device. To further verify that the current through the WSe_2 layer is negligible in the $WSe_2/PdSe_2$ devices, we also measured the transfer characteristics of a WSe_2 FET fabricated from the same piece of WSe_2 forming the $WSe_2/PdSe_2$ heterostructure. The electron current

through the WSe_2 device is over 3 orders of magnitude smaller that in similar $PdSe_2$ and $WSe_2/PdSe_2$ devices (see **3.2 d**). This finding provides strong initial evidence that the performance of $PdSe_2$ devices is largely limited by the Schottky contacts, and replacing $PdSe_2$ with $WSe_2/PdSe_2$ heterostructure as the channel material significantly reduces the SBH at the drain/source contacts and thus improve the devices performance. In $WSe_2/PdSe_2$ devices, the primary role of the WSe_2 layer is to reduce the SBH and contact resistance.

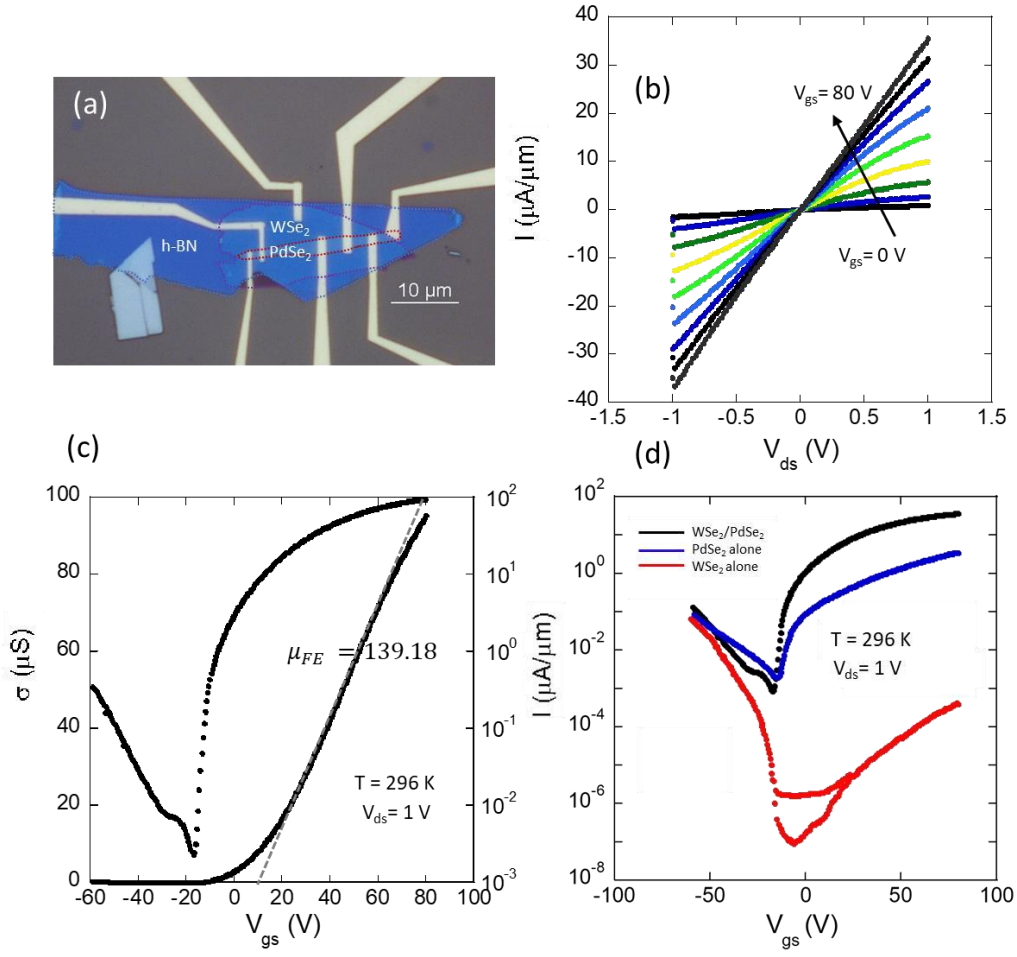


Figure 3.2| **a:** Optical micrograph of a $WSe_2/PdSe_2$ FET consisting of a trilayer (~2.1 nm thick) WSe_2 over a ~ 4 nm thick $PdSe_2$ in the channel. (**b**) Output and **(c)** transfer characteristics of the $WSe_2/PdSe_2$ FET at room temperature. (**d)** Comparison of the drain current *versus* gate voltage of FETs consisting of $WSe_2/PdSe_2$, $PdSe_2$, and WSe_2 channels. The over 4 orders of magnitude lower on-current through the WSe_2 channel than through the $WSe_2/PdSe_2$ channel indicates that the current in the $WSe_2/PdSe_2$ device primarily passes through the $PdSe_2$ layer in the channel region.

3.1.2 Comparison of Temperature Dependence of $WSe_2/PdSe_2$ FET and $PdSe_2$ FETs

To further elucidate the effects of WSe_2 layer on the device characteristics of $WSe_2/PdSe_2$ FETs with $PdSe_2$ as the active channel material, we have measured the transfer characteristics of two otherwise nearly identical FETs except that Ti metal is in direct contact with $PdSe_2$ in one device while Ti metal is in contact with a $WSe_2/PdSe_2$ heterostructure in the drain and source regions of the other device. To fabricate the devices, a trilayer WSe_2 with a gap in-between was dry-transferred on top of a few-layer $PdSe_2$ so the drain and source regions of the device consist of a $WSe_2/PdSe_2$ heterostructure while the channel consists of $PdSe_2$ only (**Figure 3.3a inset**). After all measurement were completed, a second device with $PdSe_2$ in the drain and source regions was made by extending the metal electrodes into the channel region (**Figure 3.3d inset**). **Figures 3.3a** and **3.3d** show transfer characteristics of the two devices measured at different temperatures down to 77 K and 100 K, respectively. Since these devices consist of essentially the same PdS_2 channel, any variations in doping or gating effects in the channel material can be neglected. The primary difference between them is that drain and source contacts are formed to a $WSe_2/PdSe_2$ heterostructure in the device shown in **Figure 3.3a** while Ti metal is directly contacting a $PdSe_2$ in **Figure 3.3d**. With increasing electron concentration, the device with $Ti/PdSe_2$ drain and source contacts displays a crossover from an insulting regime, where the current increases with increasing temperature, to a metallic regime, where the current decreases with increasing temperature.[96]

On the other hand, the current of the device with $Ti/WSe_2/PdSe_2$ drain and source contacts monotonously decreases with increasing temperature without a noticeable crossover from an insulating regime to a metallic regime. Because the two devices contain the same $PdSe_2$ nanosheet in the channel region, the observed differences in the temperature-dependent transfer characteristics can be chiefly attributed to the stronger suppression of drain current by a larger SBH at the $Ti/ PdSe_2$ contacts, especially at lower carrier concentrations. As the temperature

decreases, the thermionic and thermally assisted current over the SB are increasingly suppressed, especially at relatively low carrier concentrations (gate voltages). A higher gate voltage is required to turn on the device at lower temperature in the presence of a larger SBH at the drain and source contacts, leading to an increasingly more positive threshold voltage. Therefore, the observed crossover from an insulating regime at low gate voltages to a metallic regime at high gate voltages in the device shown in **Figure 3.3d** is likely a contact effect instead of the metal-insulator-transition of the channel. In comparison, the threshold voltage of the device with a $WSe_2/PdSe_2$ heterostructure in the drain and source regions is nearly temperature independent suggesting a negligibly small SBH which does not limit current flow in the on-state of the device (**Figure 3.3a**). A smaller SBH also leads to higher 2D conductivity with larger temperature dependence.

Next, we compare the mobility of the two devices at different temperatures as shown in **Figure 3.3b, e**. Because a strong suppression of the current at low gate voltages and subsequent rapid increase in I_{ds} at higher gate voltages may result in overestimation of field-effect mobility, we compare the effective mobility of the two devices as a function of gate voltage at different temperatures. In order for the two-terminal effective mobility to accurately represent the true mobility of the channel, not only the contact resistance needs to be significantly lower than the channel resistance, which is validated by the monotonous decrease of the two-terminal 2D conductivity as the device is cooled to 100 K with $Ti/WSe_2/PdS_2$ drain/source contacts shown in **Figure 3.3a**, but also the threshold voltage should correspond to zero carrier concentration. On the other hand, the presence of a substantial SBH of the device with $Ti/ PdSe_2$ contacts shifts the threshold voltage in the positive gate voltage direction. Therefore, the threshold voltage V_{th} extracted from the device in **Figure 3.3a** at room temperature is also used for the device in **Figure**

3.3d to avoid the underestimation of carrier density and thus possible over estimation of mobility caused by SB induced threshold voltage shift.

Figure 3.3b shows that the effective mobility of the device with Ti/WSe_2/$PdSe_2$ drain/source contacts first rapidly increases to a maximum value and then gradually decreases as the gate voltage further increases. On the other hand, μ_{eff} in the device with Ti/$PdSe_2$ contacts keeps increasing with gate voltage until V_{gs} = 80 V as shown in **Figure 3.3e**. This qualitative difference suggests that the true channel mobility may slightly decrease at higher gate voltages and that the monotonous increase of the effective mobility in **Figure 3.3e** is an artifact caused by a substantial SB at the contacts. Another significant difference between the two devices is that the effective mobility of the device with Ti/$PdSe_2$ contacts increases (decreases) with temperature at gate voltages below (above) ~ 60 V, while the effective mobility of the device with Ti/WSe_2/$PdSe_2$ contacts monotonously decreases with increasing temperature in the entire gate voltage region for the on-state. The increase of effective mobility with temperature in the lower gate voltage region of the device with Ti/$PdSe_2$ contacts indicate that the two-terminal mobility of the device is limited by the SB which is nearly negligible in the device with Ti/WSe_2/$PdSe_2$ contacts. Moreover, the effective mobility of the device with Ti/WSe_2/$PdSe_2$ contacts at 100 K (~520 $cm^2V^{-1}s^{-1}$) is about 5 times larger than that of the device with Ti/$PdSe_2$ contacts even at the highest gate voltage (V_{gs} = 80 V), which is likely due to the lower SBH in the former.

The temperature dependence of the peak (maximum) effective mobility of the two devices are shown in **Figure 3.3c** and **3.3f**, respectively. The effective mobility of the device with Ti/WSe_2/$PdSe_2$ contacts increases from ~220 $cm^2V^{-1}s^{-1}$ at room temperature to ~520 $cm^2V^{-1}s^{-1}$ at 100 K following a $\mu \sim T^{-\gamma-1.1}$ dependence in the temperature range between 160 K and room temperature. On the other hand, the effective mobility of the device with Ti/$PdSe_2$ contacts is much

smaller following a much weaker temperature dependence of $\mu \sim T^{-0.4}$. The lower effective mobility and weaker temperature dependence of effective mobility in the latter can also be attributed to a large SBH which increasingly limits the current flow with decreasing temperature. This discrepancy indicates that the contact resistance in the device with Ti/$PdSe_2$ contacts contributes significantly to the total resistance of the device and the channel resistance of the device with Ti/WSe_2/ $PdSe_2$ contacts dominates. In addition, the larger SBH in the former also leads to faster increase of contact resistance with decreasing temperature.

To shed additional light on the role of SBH in contributing to the differences between the two devices, the filed-effect mobility in two different linear regions of the transfer characteristics (shown as region I and region II in **Figures 3.3a and 3.3d**) are also plotted as a function of temperature in **Figure 3.3c, f**. While the field-effect mobility extracted from the lower gate-voltage linear region (region I) of the device with Ti/WSe_2/$PdSe_2$ contacts is only slightly larger than its effective mobility, the field-effect mobility extracted from the higher gate-voltage region (region II) of the device is lower than its effective mobility. The field-effect mobilities extracted from both gate-voltage regions also follow similar power-law temperature dependence. By sharp contrast, the field-effect mobilities of the device with Ti/$PdSe_2$ contacts extracted from both gate-voltage regions are larger than its effective mobility and also follow a stronger temperature dependence.

The discrepancy between the effective mobility and field-effect mobility can be attributed to channel and/or contact effects. The field-effect mobility is expected to be consistent with the actual channel mobility (Drude mobility) in ideal field-effect transistors with low-resistance ohmic contacts and if the mobility is carrier-density independent. In this case, the 2D conductivity *vs*. gate voltage should also be linear. However, in realistic devices which have a substantial SB present at the metal/semiconductor interface, the derived field-effect mobility is likely to deviate

from actual channel mobility, leading to underestimate or overestimate of the mobility. Overestimate of the mobility is possible when the drain/source current is suppressed by the SB in the low carrier density (gate voltage) region. As the carrier density increases, the thinning of the SB can give rise to rapid increase of tunneling and thermally assisted tunneling current. Consequently the slope of 2D conductivity *vs*. gate-voltage can be enhanced leading to overestimation of mobility. We believe this is the case for the device with Ti/$PdSe_2$ contacts. Another possible artifact in the extraction of field-effect mobility is the carrier density dependence of the mobility. In the case of mobility increasing (decreasing) with carrier density, the extracted field-effect mobility includes an additional positive (negative) term that is proportional to the first derivative of the mobility over gate voltage (carrier density). The lower field-effect mobility than effective mobility of the device with Ti/WSe_2/$PdSe_2$ contacts in the high gate-voltage region can be attributed to decreasing channel mobility with carrier density due to increased interfacial scattering. This scenario is in agreement with the gate-voltage dependence of the effective mobility, which also decreases with gate voltage in the high-gate voltage region (**Figure 3.3b**). This finding provides further evidence that a substantial SBH is present in the device with Ti/$PdSe_2$ contacts and the SBH can be significantly reduced by replacing $PdSe_2$ with WSe_2/$PdSe_2$ as a channel material.

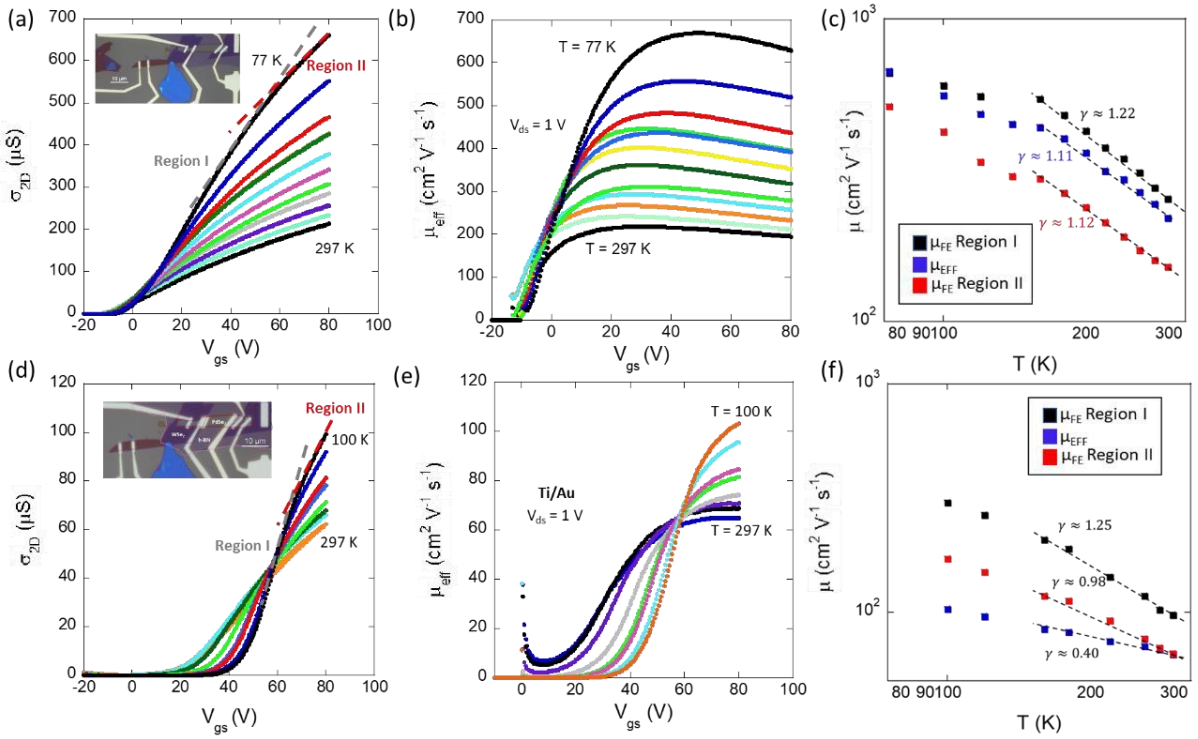


Figure 3.3| **a:** Temperature-dependent transfer characteristics and mobility comparison for two FETs with Ti/WSe_2/$PdSe_2$ (**a,b, c**) and Ti/$PdSe_2$ contacts (**d,e,f**). Both devices consist of a 6.7 nm thick $PdSe_2$ in the channel; and the WSe_2 at the contacts is ~ 2.1 nm. (**a,d**) The 2D conductivity measured down to 77 K at V_{ds} = 1 V. Red dashed lines indicate different slopes in the low and high gate-voltage regions labeled as region I and region II, respectably). (**b,e**) Effective mobility defined as $\mu_{eff} = \sigma_{2D}/C_{gs}$ (V_{gs}–V_{th}). (**c,f**) Comparison of temperature-dependent peak (maximum) effective mobility (μ_{eff}) and field-effect mobility (μ_{FE}) extracted from regions **I** and **II** in (**a, d**).

3.1.3 Schottky Barrier Height of WSe_2/$PdSe_2$ FET and $PdSe_2$ FETs

Next, we quantitatively compare the SBH of FETs devices consisting of $PdSe_2$ and WSe_2/$PdSe_2$. The FETs are modeled as two back-to-back Schottky diodes connected by a $PdSe_2$ or WSe_2/$PdSe_2$ channel. Our SBH extraction method is based on the thermionic emission current through a reverse-bias Schottky diode at the flat-band voltage.[97] The thermionic emission current density is given by[98].

$$I_{ds} = A_{2D}^{*} T^{3/2} e^{\left(-\frac{q\Phi_B}{k_B T}\right)} \left[1 - e^{\left(-\frac{qV}{k_B T}\right)}\right] \tag{3.4}$$

Where A_{2D}^{*} is the 2D equivalent of Richardson's constant, T is the temperature, q is the electron charge, V is the applied voltage at the junction, and Φ_B is the effective barrier height. To

extract the SBH, the drain voltage is biased such that $|qV| \gg k_B T$, which makes the term in brackets in **equation 3.4** ≈ 1 for the reverse-bias Schottky contact. Rearranging **equation 3.4** and taking the natural log of $I_{ds}/T^{3/2}$ yields:

$$\ln\left(\frac{I_{ds}}{T^{3/2}}\right) = \ln(A_{2D}^{*}) - \Phi_B\left(\frac{q}{k_B T}\right) \tag{3.5}$$

From **equation 3.5**, the slope of $\ln\left(\frac{I_{ds}}{T^{3/2}}\right)$ is proportional to the extracted Φ_B for a given gate voltage. Since the gate voltage is effectively tuning the charge doping in the junction, thermally assisted tunneling and tunneling current through the SB may become significant at high positive gate voltages (carrier densities) for an electron SB. In this case, the extracted Φ_B based on the themionic emission model is expected to be smaller than the actural SBH. On the other hand, an increasingly negative gate voltage increases the channel barrier height, which consequently leads to a higher extracted Φ_B. The extracted Φ_B becomes the true SBH at the flat-band voltage, above which the extracted Φ_B as a function of gate voltage deviates from its linearity (at lower gate voltage).

Figure 3.4 a,b shows the Arrhenius plots of two representative FETs with $PdSe_2$ and $WSe_2/PdSe_2$ at the contacts, respectively. While the Arrhenius plots from the device with $PdSe_2$ at the contacts display negative slopes for the entire temperature region (**Figure 3.4 a**), the slopes of the Arrhenius plots from the device with $WSe_2/PdSe_2$ at the contacts are positive above 220 K and become negative at lower temperatures (**Figure 3.4 b)**. The observed positive slopes in **Figure 3.4 b** cannot be explained by thermionic emission or thermally assisted tunneling over a SB and is likely limited by the channel, which is consistent with the larger 2D conductivity and higher two-terminal mobility observed in devices consisting of $WSe_2/PdSe_2$. When the total resistance of an FET device is dominated by the channel, its current decreases with temperature due to increased phonon scattering at higher temperatures giving rise to a positive slope of the Arrhenius plots. As

the temperature decreases, the contact resistance becomes dominant over the channel resistance, leading an activation behavior corresponding to negative slopes. Therefore, we extracted the Φ_B of the $WSe_2/PdSe_2$ device from the temperature region below 220 K. By contrast, the current of the $PdSe_2$ device is contact limited as signified by negative slopes of the Arrhenius plots in the entire temperature region (**Figure 3.4a)**. The absolute values of the slopes of the $PdSe_2$ device decreases below 180 K, which corresponds to a transition from thermionic emission at higher temperatures to thermally assisted tunnel at lower temperatures. Therefore, we extracted the Φ_B of the $WSe_2/PdSe_2$ device from the temperature region above 180 K.

Figure 3.4c, 3.4d shows the extracted Φ_B as a function of gate voltage for the $PdSe_2$ and $WSe_2/PdSe_2$ devices, respectively. The SBH is determined as the effective barrier height at the flat band voltage, the point above which the effective barrier height starts to deviate from the linear dependence of the gate voltage. Above (more positive than) the flat band voltage, thermally assisted tunneling current across the SB can no longer be ignored, leading to a weaker dependence of the extracted Φ_B on the gate voltage. Using this technique, SBHs of 158 meV and 22 meV are determined for $PdSe_2$ and $WSe_2/PdSe_2$ devices, respectively. The drain/source contacts of our $WSe_2/PdSe_2$ devices can be modeled as metal-semiconductor-semiconductor (MSS) or metal-insulator-semiconductor (MIS) contacts. Several different mechanisms have been proposed to explain the reduction of SBH in MIS contacts including attenuation of MIGS, formation of electronic dipole at the insulator-semiconductor interface, passivation of interfacial defects, and interfacial doping.[99-103] Alternatively, the drastic reduction of SBH in our $WSe_2/PdSe_2$ devices can be attributed to the synergy of Fermi-level pinning to WSe_2 and favorable conduction-band offset between the WSe_2 and $PdSe_2$ layers.[64]

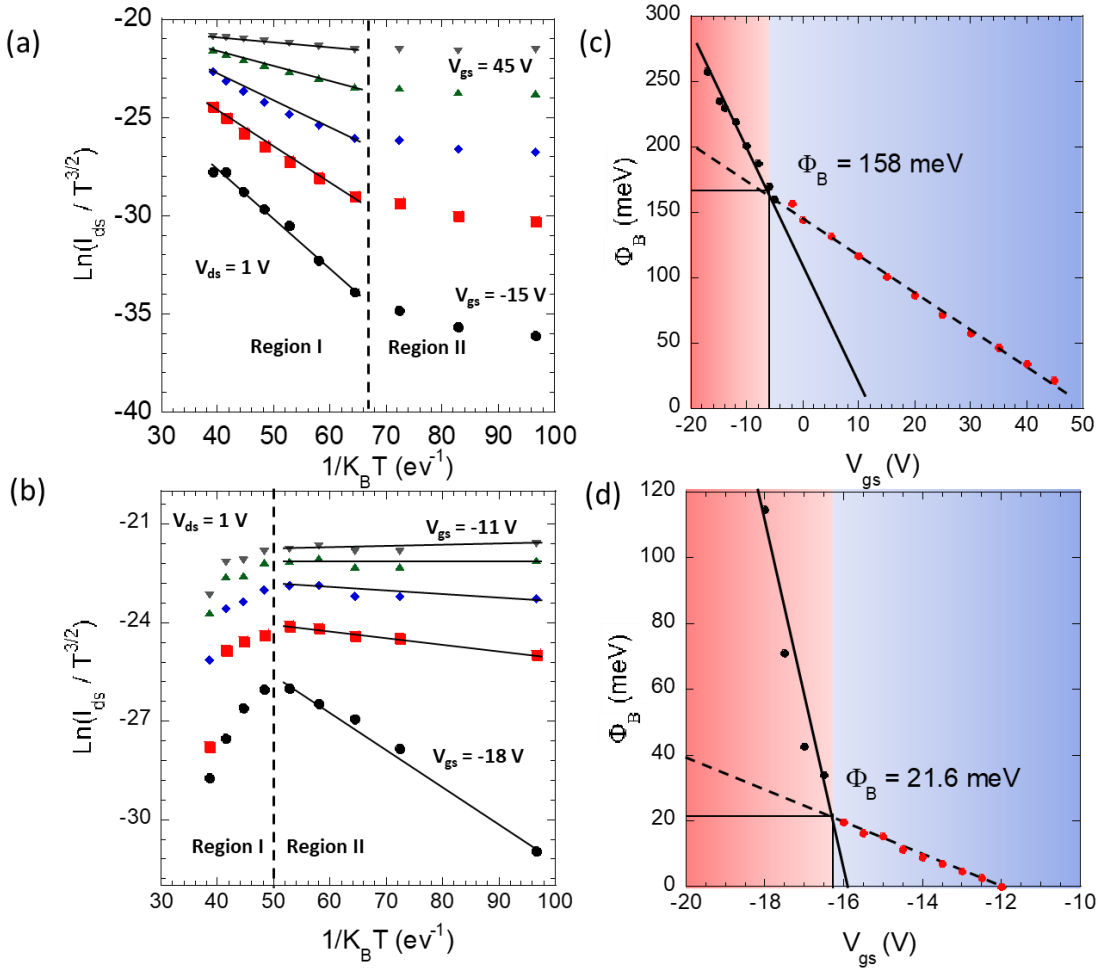


Figure 3.4| **a:** Flat-band Schottky barrier height extraction. **(a,b)** Arrhenius plots of **(a)** $PdSe_2$ and **(b)** $WSe_2/PdSe_2$ FETs contacted by Ti metal for various gate voltages. **(c,d)** The extracted *n*-type effective barrier height at various gate voltage, where the flat-band SBH is measured to be **(c)** 158 meV and **(d)** 21.6 meV in $PdSe_2$ and $WSe_2/PdSe_2$ FETs, respectively. The $PdSe_2$ FET consists of a ~ 9 nm $PdSe_2$ channel. The $WSe_2/PdSe_2$ FET consists of a ~ 4 nm $PdSe_2$ and ~ 2 nm WSe_2 in the heterostructure channel.

3.1.4 Comparison of Contact Resistance of $WSe_2/PdSe_2$ FET and $PdSe_2$ FETs

To quantitatively understand the impact of reduced SBH on the contact resistance, transfer length method (TLM) was used to extract the contact resistance of FETs devices consisting of $PdSe_2$ and $WSe_2/PdSe_2$ channels. **Figure 3.5 a, b** shows the output characteristics of the $WSe_2/PdSe_2$ and $PdSe_2$ devices with different channel lengths at V_{gs} = 80 V, respectively. Optical micrographs of the devices for TLM measurement are shown in the **inset of Figure 3.5 a, b**. The

slight super linear behavior exhibited in the output characteristics of the $PdSe_2$ device can be attributed to the substantial SBH at the Ti/ $PdSe_2$ contacts. **Figure 3.5 c, d** shows the total resistance normalized by width (R_{Total}) for the $PdSe_2$ and $WSe_2/PdSe_2$ devices, which was obtained from the slope of the *I-V* characteristics and plotted as a function of channel length at different gate voltages. The reasonably good linear fit to the data at different gate voltages indicates relatively low variability among the contacts and channels. The *y*-intercept of the linear fit yields the total contact resistance $2R_{\mathrm{C}}$. It is worth pointing out that care must be taken to ensure that the total resistance of the shortest channel device is not significantly larger than $2R_{\mathrm{C}}$ in order to avoid large errors in contact resistance.[104-105] The TLM measurements at V_{gs} = 80 V yield a contact resistance of 11.4 kΩ μm for the Ti/$PdSe_2$ contacts and 2.7 kΩ μm for the Ti/ $WSe_2/PdSe_2$ contacts, which is qualitatively consistent with their respective SBH disparities. The difference in the contact resistance between Ti/$PdSe_2$ and Ti/ $WSe_2/PdSe_2$ contacts increases as the carrier concentration (gate bias voltage) decreases as illustrated in **Figure 3.5 e**, which is expected given their SBH difference because the larger SBH at Ti/$PdSe_2$ contact leads to higher contact resistance especially at lower carrier densities. On the other hand, the contact resistance of the small SBH at Ti/ $WSe_2/PdSe_2$ contact is relatively insensitive to the carrier density. In addition, the relatively small SBH at Ti/ $WSe_2/PdSe_2$ contact also leads to relatively weak temperature dependence of the contact resistance as shown in **Figure 3.5 f.**

To further demonstrate the advantage of $WSe_2/PdSe_2$ heterostructure over $PdSe_2$ as a channel material in the FET performance, we have systematically studied multiple $PdSe_2$ and $WSe_2/PdSe_2$ devices with varying $PdSe_2$ thicknesses. Either bilayer or trilayer WSe_2 nanosheets were used to form the $WSe_2/PdSe_2$ heterostructures in these devices. **Figure 3.6** summaries the two-terminal effective mobility and on/off ratio as a function of $PdSe_2$ thickness in these devices.

The two-terminal effective mobility of $WSe_2/PdSe_2$ devices is consistently higher than that of $PdSe_2$ devices at all $PdSe_2$ thicknesses as shown in **Figure 3.6 a**. While the on/off ratios of both $PdSe_2$ and $WSe_2/PdSe_2$ devices increase as the $PdSe_2$ thickness decreases, which is expected because the bandgap of $PdSe_2$ increases with decreasing thickness[25, 27, 33], the on/off ratio is consistently higher and increases faster with decreasing $PdSe_2$ thickness in $WSe_2/PdSe_2$ devices than in $PdSe_2$ devices. As the thickness of $PdSe_2$ decreases to ~ 2 nm (3 layers), an high on-off ratio of ~ 10^7 is achieved in the $WSe_2/PdSe_2$ device, which is about 2 orders of magnitude higher than that in the $PdSe_2$ device fabricated from the same piece of the ~ 2nm thick $PdSe_2$. In addition, the two-terminal effective mobility of the $WSe_2/PdSe_2$ device is over 2 orders of magnitude larger than that in the $PdSe_2$ device and also orders of magnitude larger than the two-terminal effective mobility of a bilayer or trilayer WSe_2 FET. These results are consistent with the lower SBH and consequently smaller contact resistance in the in the $WSe_2/PdSe_2$ devices.

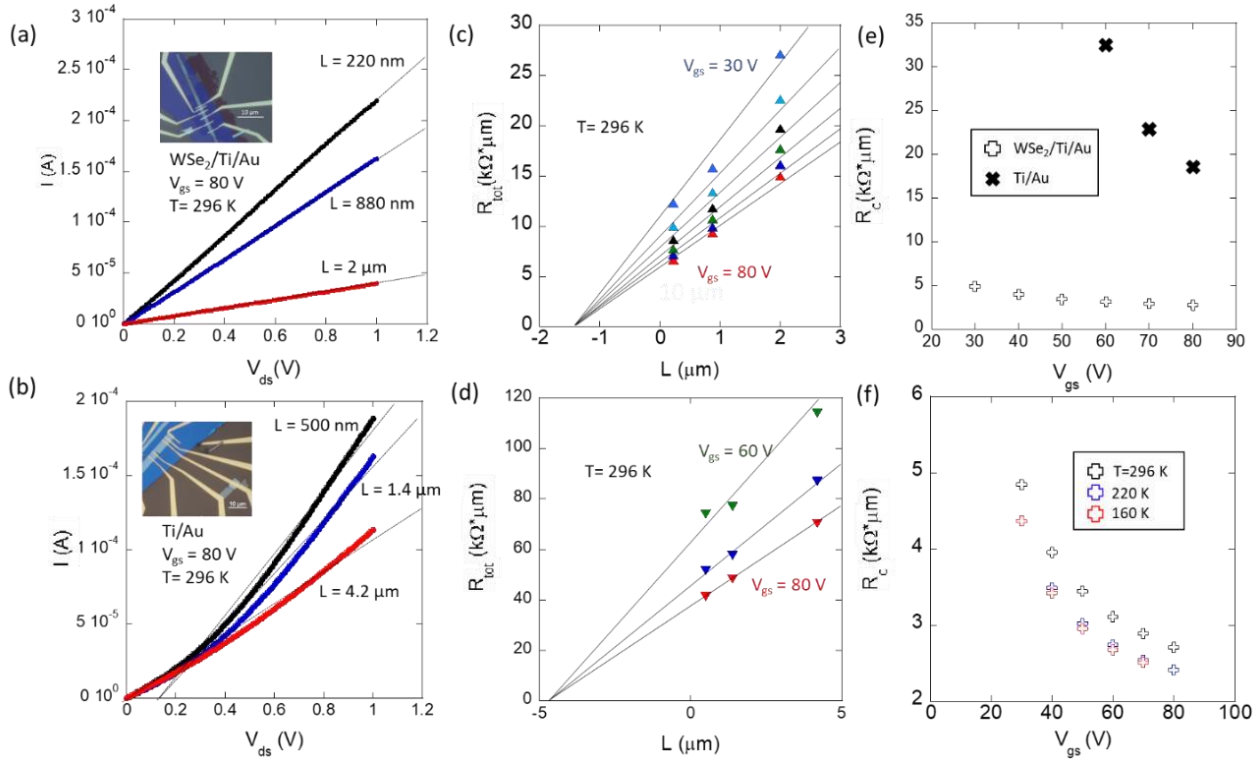


Figure 3.5| **a:** Contact resistance of $WSe_2/PdSe_2$ and $PdSe_2$ FETs with Ti metal contacts. (**a**–**b**) Room-temperature I_{ds}–V_{gs} output curves for different channel length at V_{gs} = 80 V for (**a**) $WSe_2/PdSe_2$ and (**b**) $PdSe_2$ FETs. Both the $WSe_2/PdSe_2$ and $PdSe_2$ devices contain a ~ 9 nm thick $PdSe_2$ in the channel. (**c-d**) The total resistance normalized by width (R_{Total}) as a function of channel length for each type determined by the slopes from (**a-b**) at different gate voltages for the (**c**) $WSe_2/PdSe_2$ and (**d**) $PdSe_2$ FETs. The y-intercept yields twice the contact resistance ($2R_C$). (**e**) Comparison of extracted contact resistance for the $WSe_2/PdSe_2$ and $PdSe_2$ devices as a function of carrier density (gate voltage bias**). (f)** Contact resistance of the $WSe_2/PdSe_2$ devices as a function of carrier density measured at different temperatures.

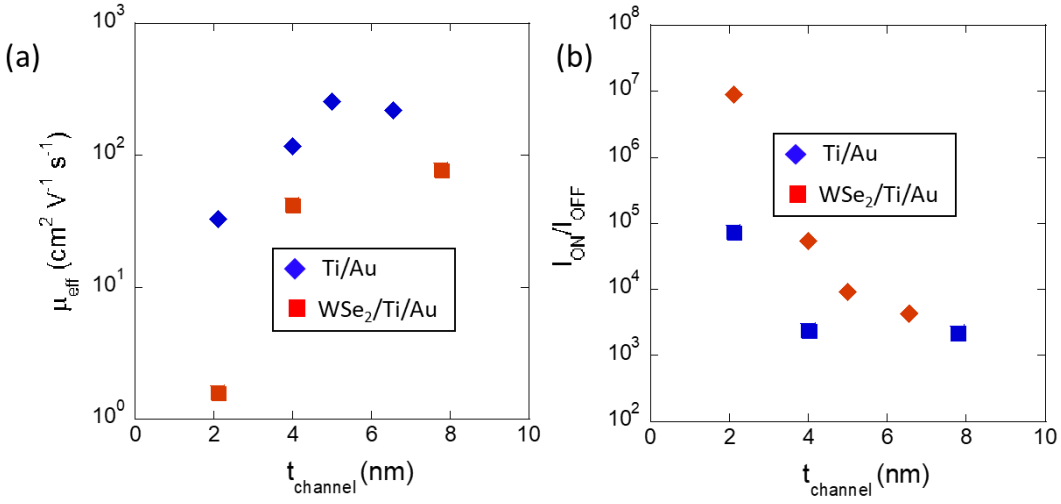


Figure 3.6| **a:** Effective mobility of several $PdSe_2/WSe_2$ FETs and $PdSe_2$ FETs with varying $PdSe_2$ thicknesses. (**b)** ON/OFF ratios of the $PdSe_2/WSe_2$ and $PdSe_2$ FETs fabricated as a function of $PdSe_2$ thickness.

Figure 3.7 shows the device performance at room temperature of a 6.7 nm $WSe_2/PdSe_2$ FET (whose temperature dependence is reported in **Figure 3.7**) measured over ~2 years apart. The device was stored in a desiccator environment. From April 2019 to August 2021, we observed an increase in the OFF current increases by ~50% and a ~10% reduction in the ON current (**Figure 3.7b**) and 2-terminal conductivity (**Figure 3.7c**). There is also a ~ 4.4 V shift in the threshold voltage. These phenomena can be readily attributed to local oxidation of the Ti layer at the sidewalls of the metal electrodes, which are not protected by gold.

Astonishingly, there is no change in the effective mobility over the same period. We can only conclude that the device remains channel limited, despite some slight degradation of the contacts.

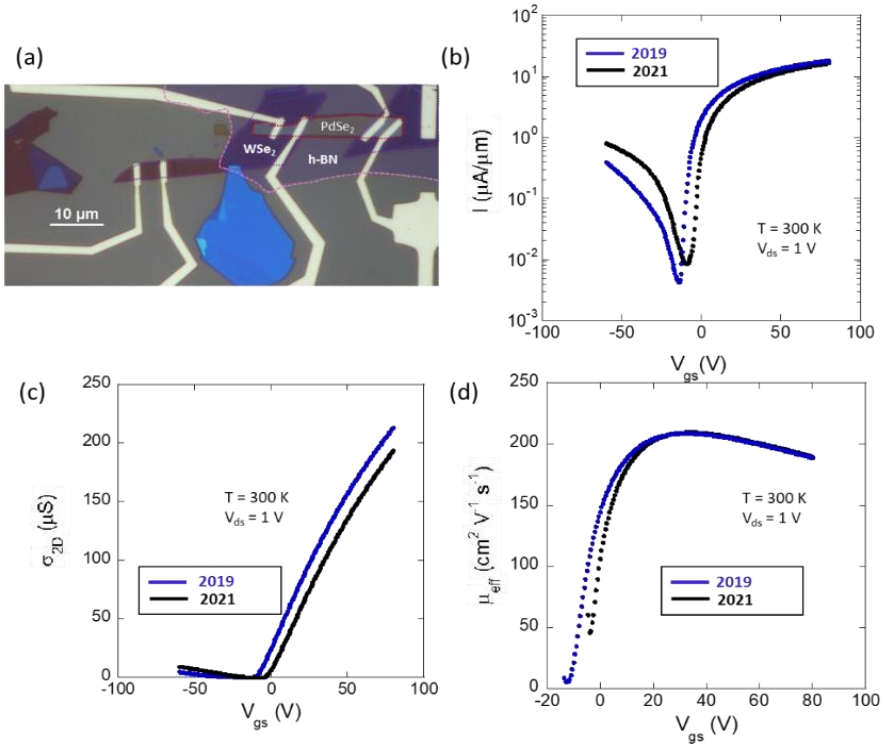


Figure 3.7| **a:** 6.7 nm $WSe_2/PdSe_2$ FET when it was first fabricated in 2019. **b:** Semilog plot of transfer characteristics of 6.7 nm $WSe_2/PdSe_2$ FET in 2019 and 2021, showing the increase in the OFF current. **c:** 2-terminal conductivity of 6.7 nm $WSe_2/PdSe_2$ FET in 2019 and 2021, showing a slight decrease and positive shift of the threshold voltage. **d:** Effective mobility of 6.7 nm $WSe_2/PdSe_2$ FET in 2019 and 2021, showing little change over time.

CHAPTER 4: CONCLUSION AND FUTURE WORK

In conclusion, we report the fabrication of high performance $WSe_2/PdSe_2$ FETs by using $WSe_2/PdSe_2$ heterostructure as a channel material to overcome the high SBH at the metal/ $PdSe_2$ contacts and the relatively low intrinsic mobility of WSe_2. The addition of a bilayer or trilayer WSe_2 significantly lower the SBH at the contacts and contact resistance in our $WSe_2/PdSe_2$ device. The improvement in drain/source contacts leads to enhanced device performance including higher on-current, high on-off ratio and higher two-terminal mobility. This contact engineering strategy of using $WSe_2/PdSe_2$ heterostructure in place of individual $PdSe_2$ is air and thermally stable, and compatible with conventional semiconductor processes. It may be implemented in the production of flexible electronics by incorporating large scale $WSe_2/PdSe_2$.

Our future work should focus on rigorously explaining the mechanism. One way to do do this is to compare the performance of $WSe_2/PdSe_2$ FETs with the performance of $PdSe_2$ FETs which utilize other 2D TMDCs, (primarily MoS_2 and $MoSe_2$) as interlayers. The conduction band minimum of, say, MoS_2 is slightly lower than that of WSe_2. Thus, if the good performance of $WSe_2/PdSe_2$ FETs is based on a small offset between the conduction bands of the two materials, then the performance of $MoS_2/PdSe_2$ FETs should be even better. Meanwhile, the conduction band minimum of $MoSe_2$ lies in between those of WSe_2 and MoS_2, so we would expect the SBH of $MoSe_2/PdSe_2$ FETs to lie somewhere in between that of $WSe_2/PdSe_2$ FETs and $MoS_2/PdSe_2$ FETs, and so on. It is easy to see how a systematic study could elucidate the the dependence (or lack thereof) of the SBH on conduction band minimum of the contact interlayer.

A similar study could be performed by forming electrodes from other metals such as Ni, or Al. According to **Equation 1.16**, the SBH of $WSe_2/PdSe_2$ FETs should be relatively the consistent across a range of metals, since E_F is invariant with the metal work function. If we could show that the SBH of heterolayer FETs involving a 2D semiconductor stacked atop $PdSe_2$ is far more

sensitive to variations in the top layer as opposed to the metal electrodes, it would serve as definitive proof that the top layer indeed functions as a contact interlayer.

On the other hand, if the success of $WSe_2/PdSe_2$ junctions is due to de-pinning of the Fermi level, then in principle hBN/$PdSe_2$ FETs should be slightly worse than that of heterolayer FETs using 2D semiconductor interlayers due to its larger band gap, and thus tunneling resistance. Furthermore, since a range of 2D and 3D insulators have been used as contact interlayers, we could also systematically study the dependence of the SBH on the tunneling resistance.

Even more fundamentally, though, is the fact that the $PdSe_2$ band structure is simply not that well characterized. PL measurements on 2D $PdSe_2$ would help immensely in this regard. So, too, would X Ray Photoelectron Spectroscopy measurements to determine the exact position of band edges. Finally, all of our devices (even those with direct metal contacts) can be used as phototransistors as well, as has been done with other TMDC heterostructure devices.[92] The photocurrent data would provide additional useful information on $PdSe_2$ and its properties.

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ABSTRACT

HIGH MOBILITY *N*-TYPE FIELD EFFECT TRANSISTORS ENABLED BY $WSE_2/PDSE_2$ HETEROJUNCTIONS

by

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Two-dimensional (2D) semiconductors such as transition metal dichalcogenides (TMDs) have emerged as a promising candidate for post-silicon electronics. Few-layer tungsten diselenide (WSe_2), a well-studied TMD, has shown high hole mobility and ON/OFF ratio in field effect transistor (FET) devices. But the *n*-type performance of WSe_2 is still quite limited by the presence of a substantial Schottky Barrier. Palladium diselenide, ($PdSe_2$) is a newly discovered TMD that is of interest because of its high electron mobility, and moderate ON/OFF ratios. However, despite its relatively small bandgap, the *n*-type performance of few-layer $PdSe_2$ FETs has also been limited by a Schottky barrier, which is likely due to Fermi-level pinning. In this work, we report high performance *n*-type FETs enabled by a few-layer $WSe_2/PdSe_2$ heterojunction, which is significantly better than FETs consisting of a WSe_2 or $PdSe_2$ channel.

We observe a high ON/OFF ratio of 10^5, with a two-terminal electron mobility of ~139 $cm^2\ V^1\ s^{-1}$ in a ~ $WSe_2/PdSe_2$ FET consisting of a trilayer WSe_2 and a ~ 4 nm $PdSe_2$.The mobility of the device continues to rise as the temperature decreases down to cryogenic temperatures, indicating that the device performance remains to be channel limited due to a relatively low Schottky Barrier height. A heterojunction consisting of bilayer $PdSe_2$ and bilayer WSe_2 showed

an ON/OFF ratio approaching 10^7, while still maintaining a moderate mobility of ~ 57 $cm^2 V^{-1} s^{-1}$. We believe the significantly improved device performance enabled by our contact-engineering technique will facilitate real-world electronic applications of 2D semiconductors and enable further study of the intrinsic properties of layered 2D materials

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