Combination of Interleaved Single-input Multiple-output DC-DC Converters

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***Abstract*—This paper analyses, simulates and verifies an experimental prototype of a four-phase interleaved DC-DC converter. It is based on a SEPIC-Ćuk combination. The developed prototype has been used in single-input multiple-output (SIMO) applications. This combined converter allows obtaining dual output voltages of the same value, from a single input DC voltage and with only a power switch. Multiphase interleaved DC-DC converters achieve a better dynamic response and low ripple, maintaining their efficiency. Each converter is connected in parallel, thereby managing their losses by distributing them between more components, which facilitates the thermal management of the multiphase converter and allows handling high power values in small sizes with respect to solutions for a single phase. Two control strategies were applied: synchronous operation mode (SOM) and interleaved operation mode (IOM). The simulation results allow the comparison of both operational modes, verifying that the IOM presents advantages with respect to the ripple at the input and output currents. The experimental prototype was designed for a distributed power architecture and bipolar DC microgrid (MG).**

***Index Terms*—Bipolar DC, DC-DC converter, interleaved.**

I. Introduction

THE electronic power systems integration, together with energy management, are currently more and more in demand. More concepts for electric systems consider high efficiency, high power density, faster load transient response, small size, weight reduction, maintenance and low cost as important elements. This is primarily due to the need for miniaturization driven by applications with severe restrictions on space [1]. In these applications, the integration of single or multiple power systems are used to interconnect all subsystems, which distribute energy to different loads, with converters operating in power ranges from few a few watts to hundreds of kilowatts. This also requires the incorporation of technologies and solutions that aim for very high power densities.

The multiport power converters (MPCs) contribute to electronic power system integration since they allow for the connection of different sources, storage systems and loads, with different voltage levels. In multiport power converters, the different sources, load and storage systems are connected to the ports, which allows for the harvesting and processing of the power, in the same way as signal processing, a power processing system processes the available power at the inputs to be usable at the outputs, in terms of the output voltage or current, and where that power flow can be controlled and adjusted to the different loads [2], [3]. MPCs are classified depending on the number of inputs and outputs, which include configurations for multiple-input, multiple-output (MIMO) [4], [5]; multiple-input single-output (MISO) [6]–[9]; and SIMO [10]–[12] converters. Multiport converters can be found in applications that cover many different power levels, from traditional applications, such as power supplies (switch-mode and linear) discrete and integrated in a package, to applications with higher power, such as the integration of renewable energy sources (RES) into the grid, distributed generation (DG), as well as for hybrid/electric vehicles (HEV/EV) and micro-grids (μG).

In the same way, SIMO DC-DC converters are potentially useful for a wide range of power applications. They are widely used in applications for typical distributed power architectures (DPA) that produce typical DC output voltages, such as 5 V, 12 V, 24 V, or 48 V used in intermediate bus architecture (IBA), central control architecture (CCA) and dynamic bus architecture (DBA) for medical, telecom, datacom, and light-emitting diodes (LEDs). Power architecture (Fig. 1) produces DC output intermediate voltage from nominal input voltage; furthermore an intermediate DC link is used for supply point-of-load regulators (POLs) or low-dropout linear regulators (LDOs), that will power CPUs, ASICs, FPGAs, I/O, USB power delivery, and other low-voltage devices, with an output power level from several hundred watts to several kilowatts. Non-isolated DPA produce DC output intermediate voltage from 5 V to 12 V/20 A, with a nominal input voltage of 36 V or 72 V. Single-input multiple-output converters integrated in a single package contain combinations of DC-DC converters and LDOs.

Electrical isolation by means of a transformer increases the size and cost, while also reducing the efficiency. However, non-isolated converters are the most appropriate for many applications.

Higher power applications also follow similar trends. Currently, distributed generation systems are becoming increasingly important in the electric grid [13], [14]. Their integration requires new system configurations that allow them to be

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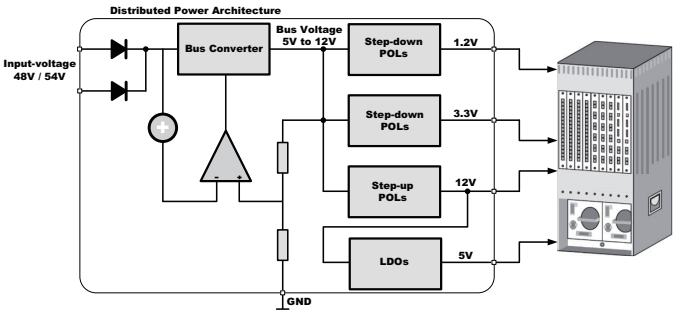


Fig. 1. Distributed power architecture.

controlled more efficiently and reliably. In this sense, some of the proposed solutions are based on the use of microgrids. The microgrids of type AC (alternating current) or DC (direct current) allow for a better and simpler management of systems with high penetration of distributed generation [15]–[17]. On the other hand, most distributed generators supply DC power and most loads are fed in this current form. This has led to the proposal of using DC microgrids instead of AC microgrids, since they have the following advantages: higher efficiency, require less wires, no stability problem, null line reactance, not necessary to control the frequency, zero rating, and line resistance is lower and presents lower electromagnetic interference. In the same way, there are also some drawbacks in the implementation of microgrids. Among those that stand out: there are no installed networks of this type, protection is more complex since there is no zero crossing in the voltage so that the cut in fault conditions is more complicated and charges are required to adopt to this type of network. These drawbacks do not exclude DC microgrids as a viable alternative for systems with a high presence of distributed generation.

There are different topologies of DC microgrids: monopolar, bipolar and homopolar. Among these, the bipolar is the most versatile, as shown in Fig. 2 [18]. It is characterized as a configuration of three conductors, which are designated: positive ($+V_{\mathrm{DC}}$), negative ($-V_{\mathrm{DC}}$) and neutral (Ground). Depending on which conductors the loads are connected to, it is possible to have two voltage levels, V_{DC} and $2V_{\mathrm{DC}}$. These networks are more complex but have the advantage of having lower losses and therefore greater power transport capacity, the current through the neutral is null when the system is balanced and each output can operate independently, thus, in the case of a fault in one of them, the other can continue working.

The distributed generation source is usually connected to the DC network through a DC-DC converter. The converter is a key element in the operation of the system since among the other functions, it must adopt voltage levels between source and microgrid [19]–[24].

In its origin, the parallel connection of converters was used to overcome the limitations that high power had in the classic conversion techniques and power devices. The interleaving of converters has been proposed in recent years in different applications [25]–[29], as an additional improvement to the parallel connection of converters, as shown in Fig. 3 for N-phases interleaved step-down (Buck), step-up (Boost) and step-down/step-up (Buck-Boost) converters. The interleaved operation of multiphase converters is obtained when several converters are connected in parallel and their control signals are shifted in time, which allows for the displacement of both the demand and the energy delivery in time. A distribution of power between phases improves the dynamic performance and the cancellation of ripple at the input and the output. In addition, it increases the effective frequency of the ripple and thus significantly reduces the requirements of the output filter capacitor and the input inductors. By connecting several parallel converters to manage the distribution of losses between more components, thiw will help facilitate the thermal management of the multiphase converter, allowing for the handling of high power values in small sizes with respect

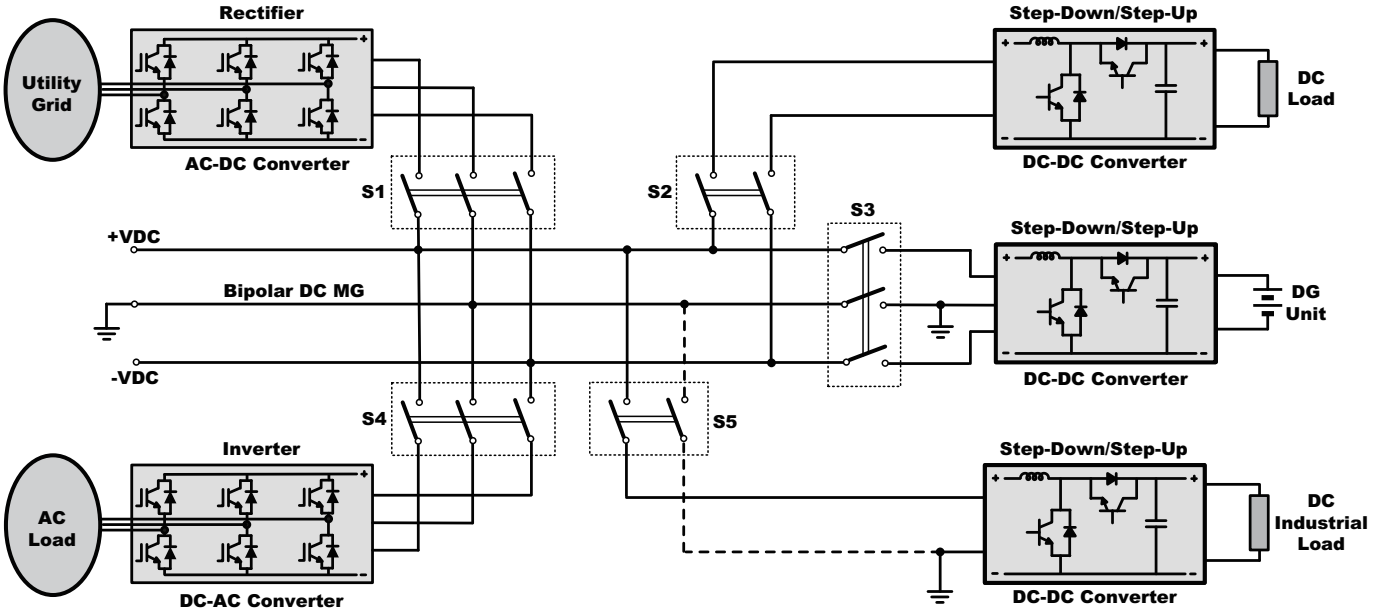
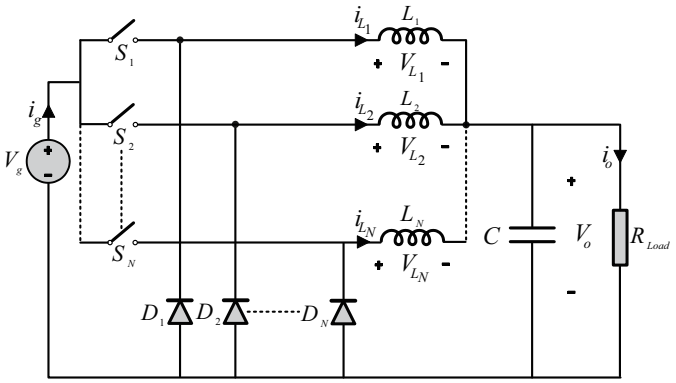
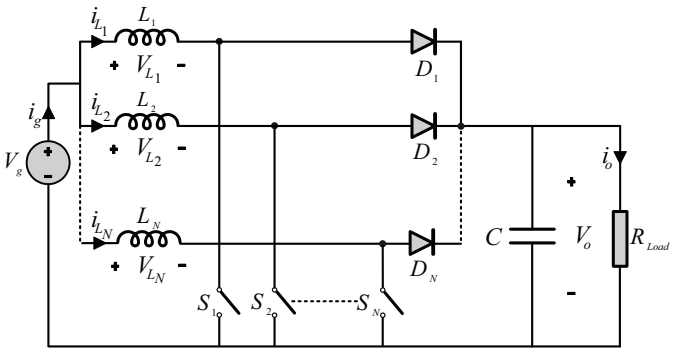


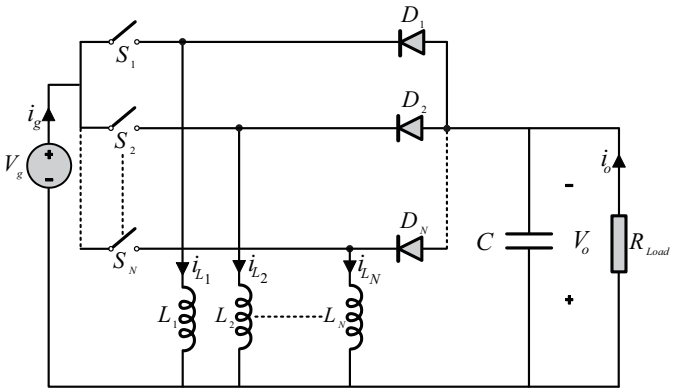
Fig. 2. Typical structure of a bipolar DC power network.



(a) N-phases interleaved Buck converter.



(b) N-phases interleaved Boost converter.



(c) N-phases interleaved Buck-Boost converter.

Fig. 3. N-phases interleaved single inductor converters.

to single phase solutions. The interleaving of converters is oriented to many of the present demands related to high currents and low voltage. Many power architectures must satisfy supplies up to 100 A at very low voltages and provide fast transient responses. The importance of the interleaved technique and its applications has caused all manufacturers to currently develop an application specific integrated circuit (multiphase controller) capable of generating this type of signal. This technique is widely used by regulated DC-DC converters.

On the other hand, the combination of basic converters is described in [30]. A SEPIC-Ćuk combination converter is presented as a suitable configuration for the connection of DG to a bipolar DC microgrid [31], [32]. Its main advantage is that it only uses one switching device for a rail-to-rail outputs or balanced dual-output voltage, ±V volts. This topology is a good solution for low power. However, large power systems would require higher power rated components. It is usual to use several converters working in parallel, reducing the power of each one. Typically, each converter operates in a synchronous manner. That is, a trigger pulse of the same frequency is applied to each switching device at the same instant in time.

In this paper, an interleaved converter based on a SEPIC-Ćuk combination converter for the connection of distributed generation to bipolar DC microgrids and power architecture is proposed. The interleaved operation of multiphase converters is interesting in high power/current applications because it has the advantage of reducing the current ripple. This allows the use of smaller capacitors, without reducing efficiency, and a faster transient response in comparison with a single-phase converter and smaller inductor size.

II. Proposed Interleaved Converter Description

A multiphase interleaved DC-DC converter basically consists of connecting several converters in parallel, operating out of phase over time, achieving a better dynamic response, low ripple and maintaining the efficiency. Traditionally the technique of interleaving has been applied to single-inductor synchronous converters such as Buck, Boost and Buck-Boost (Fig. 3). However, it can also be applied to configurations of two inductors, such as: Zeta, SEPIC and Cuk; configurations of several switches, such as: half-bridge, push-pull and full-bridge (h-bridge); and configurations with a transformer single-switch, such as: forward and flyback.

Figure 4 shows the electrical circuit of N-phases interleaved SEPIC and Ćuk converters. All phases demand current at the input and deliver current at the output displacing both the demand and the energy delivery during that time.

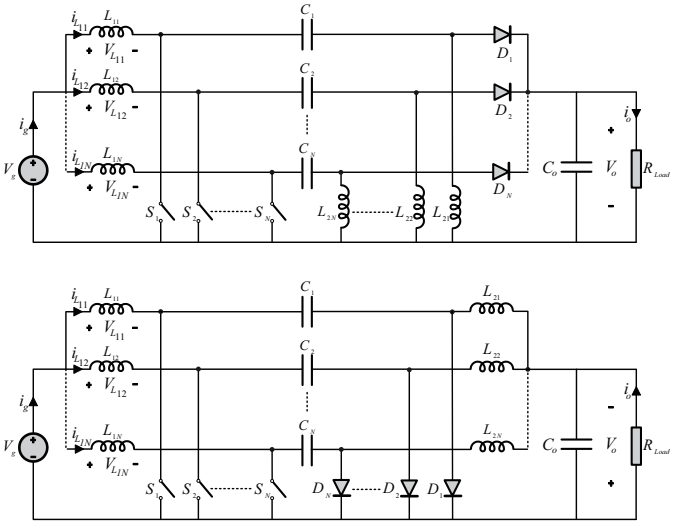


Fig. 4. N-phases interleaved SEPIC and Ćuk converters.

One of the advantages of interleaving is the possibility to cancel the current ripple in each phase, so that, the output capacitor has to filter less current ripple. Fig. 5(a) shows an example for four phases of how current ripple is canceled.

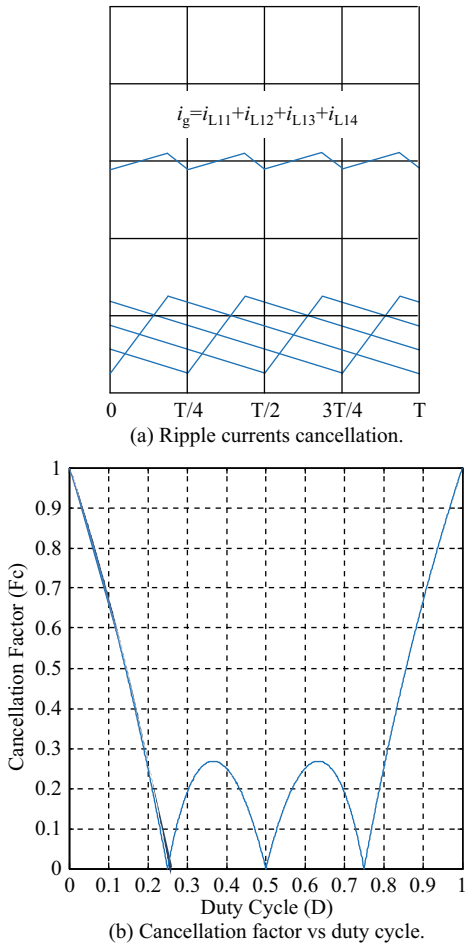
The cancellation factor (F_c), which varies between 0 and 1, represents the relationship between the input current ripple (ΔI_g) and the current ripple of each phase (ΔI_L) as it is indicated in (1).

$$\Delta I_g = F_C \cdot \Delta I_L$$

where

$$F_C = \frac{\Delta I_g}{\Delta I_L} = N \prod_{i=1}^{N-1} \left(1 - \frac{1}{|i - ND| + 1}\right)$$
$$\text{for} \quad N = 2, 3, 4 \ldots. \quad \text{Triangular waveform} \tag{1}$$
$$F_C = \frac{\Delta I_g}{\Delta I_L} = \frac{|\sin(\pi N D)|}{N \sin(\pi D)}$$
$$\text{for} \quad N = 1, 2, 3, 4 \ldots. \quad \text{Sinusoidal waveform}$$

For a triangular waveform ripple, (1) shows how the ratio of the input current ripple and cancelation factor varies with changes in D (duty cycle). To obtain a small ripple at the input current, the cancellation factor should be close to zero. The ripple cancellation depends on the number of phases and duty cycle in which the converter operates (Fig. 5(a)). The variation in D causes the cancelation of the input ripple which will not be 100% throughout the range. In Fig. 5(b), it can be observed that for four phases, a high ripple cancellation is obtained with a duty cycle between 20% and 80%. Beyond these D values, the ripple cancellation decreases as it comes closer to the extremes.



(a) Ripple currents cancellation.

(b) Cancellation factor vs duty cycle.

Fig. 5. Ripple cancellation for 4-phase interleaved converters.

An interleaved SEPIC-Ćuk combination converter is based on integration of a SEPIC and a Ćuk converter (as the Fig. 6 shows). They share the power controlled switch and the input inductor. This allows for obtaining two DC bipolar output voltages with a step-up/step-down relationship (A Cuk converter provides an output voltage inverted while the SEPIC output voltage polarity remains the same), and simplifies the use of a gate drive circuit because only one switch needs to be controlled. By shifting the operation in the time of a four SEPIC-Ćuk combination converter, its interleaved operation mode (IOM) is achieved, as shown in Fig. 6. This reflects some of the advantages of the interleaved mode, in terms of low ripple and higher power capacity.

Consider a four parallel SEPIC-Ćuk combination converter connected to a power source (V_g), as shown in Fig. 6; the input current (i_g) is the sum of the four currents for the SEPIC-Ćuk combination converters i_1, i_2, i_3 and i_4. If all SEPIC-Ćuk combination converters are clocked synchronously (SOM), then the system behaves exactly as a single large converter. In this equivalent converter, the input current ripple is roughly the sum of the current ripple of each parallel-connected converter. However if the converters are working in IOM, the input current ripple of the equivalent converter can be less than the sum of the current ripple of each parallel connected converter.

The operation of an interleaved SEPIC-Ćuk combination converter can be explained based on Fig. 6, both in the step-up and step-down mode, and for each of the phases. For phase 1, when the switch S_1 is on, the inductance L_{11} stores energy, which is supplied by the source (V_g). Furthermore, the stored energy in C_{11} and C_{21} capacitors are transferred to the L_{21} and L_{31} inductors. In this situation, the output capacitors (C) supply energy to the loads, since the freewheeling diodes (D_{11} and D_{21}) are off. D_{11} and D_{21} diodes are turned on when the switch S_1 is off (Fig. 6). In this case, the inductance L_{11} transfers its energy to the C_{11} and C_{21} capacitors, and at the same time supplies power to the loads. The same happens for the other three converters, but at different time instants: $DT_S + T_S/4$, $DT_S + T_S/2$ and $DT_S + 3T_S/4$ respectively.

Table I summarizes the expressions of voltages and currents at the converter elements of the SEPIC-Ćuk combination converter for each of the phases, assuming that the converter operates in a continuous conduction mode (CCM).

III. Experimental Prototype

To test its characteristics, an experimental prototype of a four-phase interleaved SEPIC-Ćuk combination converter is first simulated and later developed (Fig. 7). The system model was implemented with Simulink blocks. The converter was designed to a power rating of 25 kW, an input voltage of 100 V (from a renewable energy source) and a bipolar output of +/−200 V DC. There is no standard that establishes the voltage value in a bipolar DC network, nor with respect to the output voltage of the DG systems. In the tests presented, 100 V of input voltage have been used as it is approximately

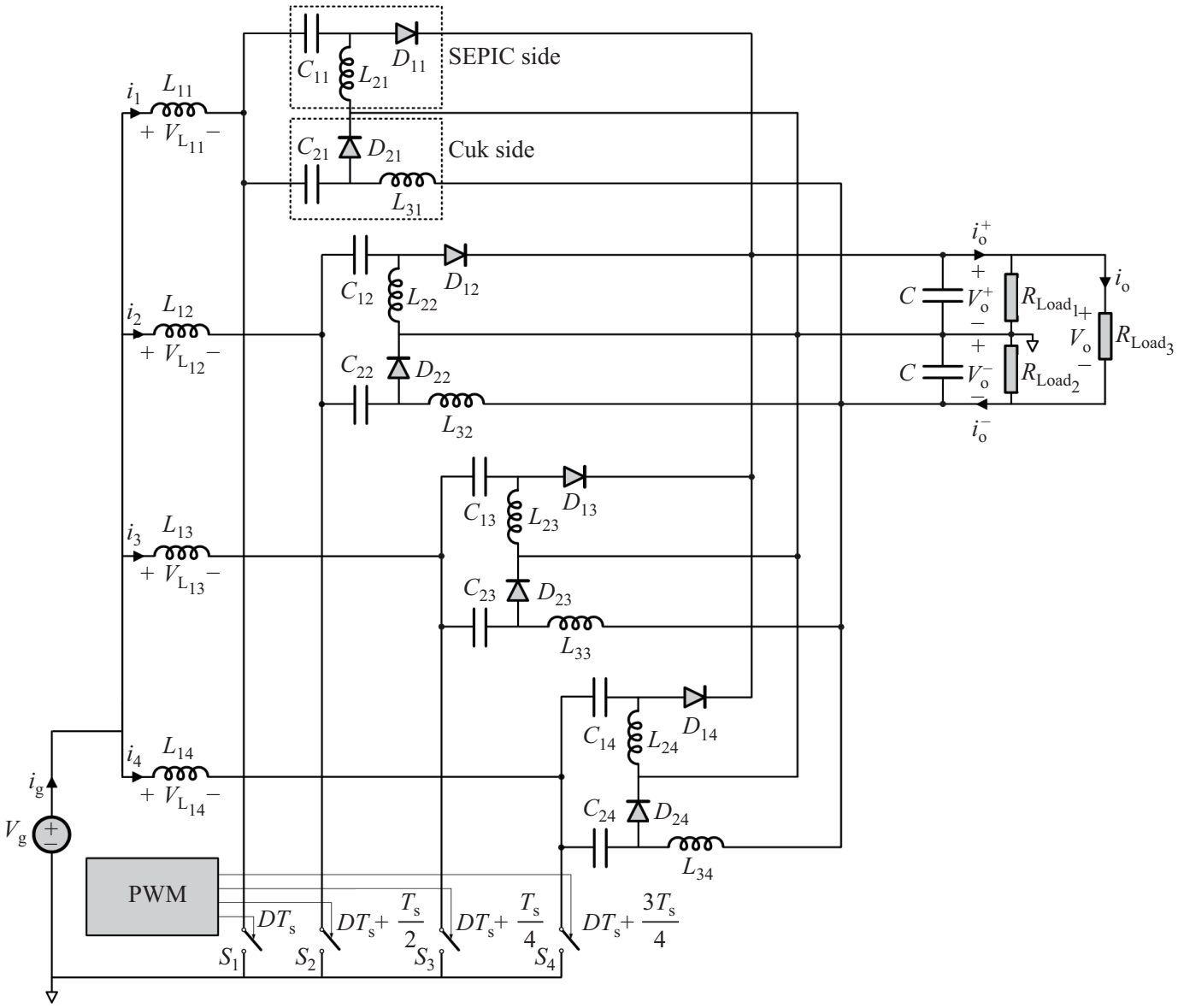


Fig. 6. Four-phase interleaved SEPIC-Ćuk combination converter.

TABLE I
PERFORMANCE OF A SEPIC-ĆUK COMBINATION CONVERTER

	Switch (S_N)	D_{1N}	D_{2N}
Semiconductor voltages	$V_g + V_o^+$	$V_g + V_o^+$	$V_g + V_o^-$
Semiconductor average currents	$\frac{V_g D^2}{4 \cdot R_o \cdot (1-D)^2}$	$\frac{V_g D}{4 \cdot R_o^+ \cdot (1-D)^2}$	$\frac{V_g D}{4 \cdot R_o^- \cdot (1-D)^2}$
	V_{C1N}	V_{C2N}	
Capacitor average voltages	V_g	$V_g + V_o^-$	
	$I_{L1N,\,AVG}$	$I_{L2N,\,AVG}$	$I_{L3N,\,AVG}$
Inductor average currents	$\frac{V_g D^2}{4 \cdot R_o \cdot (1-D)^2}$	$\frac{V_g D}{4 \cdot R_o^+ \cdot (1-D)^2}$	$\frac{V_g D}{4 \cdot R_o^- \cdot (1-D)^2}$

the voltage of a DG system with energy storage composed of 8 batteries of 12 V each. Regarding the value of the output voltage, +/−200 V has been chosen because there are examples of bipolar DC networks with this voltage level.

The current supplied by the DC source (Fig. 6), under conditions of maximum power is $I_g = 250$ A, therefore the input current for each converter will be:

$$I_1 = I_2 = I_3 = I_4 = \frac{250}{4} = 62.5 \text{ A} \tag{2}$$

A. Design Specifications

The selection of the input inductors (L_{11}, L_{12}, L_{13} and L_{14}) of each combined converter that form the interleaved structure is done by establishing a tolerable ripple for each input inductor. Its peak-to-peak value, for phase 1, is given by:

$$\Delta i_1 = \frac{V_g}{L_{11}} D T_S \tag{3}$$

where T_S is the switching period. Establish for Δi_1 a 4% of the average input current for L_{11}, $T_S = 40$ μs ($f_S = 25$ kHz)

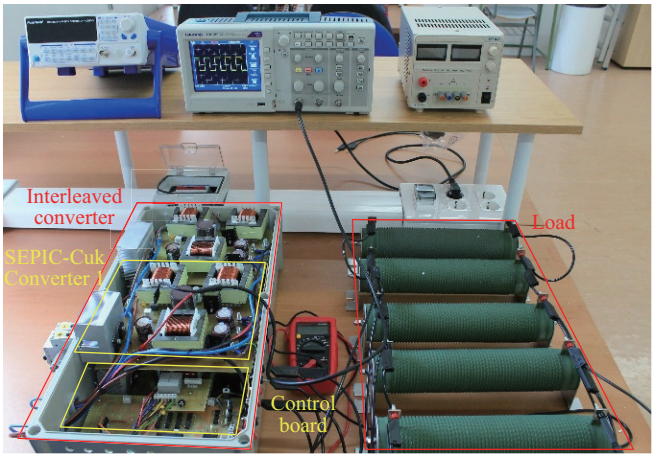


Fig. 7. Experimental prototype.

and a nominal duty cycle (D) of 2/3. According to (3), the L_{11} inductor must be of 1.06 mH. Here, a value of $L_{11} = L_{12} = L_{13} = L_{14} = 1$ mH was chosen.

For chosing the inductors L_{21}, L_{22}, L_{23}, L_{24} and L_{31}, L_{32}, L_{33}, L_{34}, it is assumed that the converters work in CCM in a power range. In this case, an interval between 1 kW and 20 kW has been considered. For the lowest power, the input current in each SEPIC-Ćuk combination converter is 2.5 A. According to Table I, for phase 1:

$$I_1 = \frac{V_g D^2}{4 \cdot R_o \cdot (1-D)^2} \tag{4}$$

This allows the maximum resistance to be obtained, $R_o = 40\ \Omega$.

On the other hand, a SEPIC-Ćuk combination converter works in CCM when the next expression is satisfied:

$$\frac{L_{eq}}{2R_o T_S} \geqslant (1-D)^2 \tag{5}$$

where $\frac{1}{L_{eq}} = \frac{1}{L_{11}} + \frac{1}{L_{21}} + \frac{1}{L_{31}}$.

With $R_o = 40\ \Omega$, the inductance L_{eq} must be 0.356 mH. Furthermore, considering $L_{21} = L_{31}$, an inductance value of 1.10 mH is obtained, whereby for the inductances $L_{2N} = L_{3N}$ a value of 1 mH is chosen.

Assuming that the voltage in the link capacitors C_{12} and C_{21} must be constant, their values can be determined by imposing the resonant frequencies (ω_r) which must be lower than the switching frequency (ω_S) in order to ensure constant voltage. In the same way, the resonance frequency for ensuring that the converter does not operate in DQRM (discontinuous quasi-resonant mode) or DCVM (discontinuous-capacitor-voltage mode) is:

$$\begin{aligned} &\omega_S > \omega_r; \text{with} \\ &\omega_{r_2}^2 = \frac{1}{C_{21}(L_{11}+L_{31})} \quad \text{for Ćuk side,} \\ &\omega_{r_1}^2 = \frac{1}{C_{11}(L_{11}+L_{21})} \quad \text{for SEPIC side} \\ &\text{furthermore: } C_{11} > \frac{D^2 T_S}{8R_o} \text{and} C_{21} > \frac{D^2 T_S}{8R_o} \end{aligned} \tag{6}$$

For a switching period (T_S) of 40 µs and $f_S = 100\ f_r$ the previous inequalities are satisfied for a minimum capacity value of 202 µF (for C_{11} and C_{21}). So, a commercial value of 470 µF is chosen.

In the same way, the voltage ripple in C_{11} and C_{21}, for phase 1, is given by:

$$\begin{aligned} \Delta v_{C_{21}} &= \frac{V_g \cdot D^2}{(1-D) \cdot 4R_o \cdot C_{21} \cdot f_S} \\ &\Rightarrow \frac{\Delta v_{C_{21}}}{V_o^-} = \frac{D}{4R_o \cdot C_{21} \cdot f_S}, \quad \text{Ćuk} \\ \Delta v_{C_{11}} &= \frac{V_g \cdot D^2}{(1-D) \cdot 4R_o \cdot C_{11} \cdot f_S} \\ &\Rightarrow \frac{\Delta v_{C_{11}}}{V_o^+} = \frac{D}{4R_o \cdot C_{11} \cdot f_S}, \quad \text{SEPIC} \end{aligned} \tag{7}$$

For $C_{11} = C_{21} = 470$ µF the voltage ripple is 0.71%, when the converter supplies the maximal power according to (4).

The selection of the output capacitors C is also made to obtain the desired voltage ripple value. In this case, the frequency of the ripple is four times the switching frequency. Its peak-to-peak value, for rail-to-rail outputs, is given by:

$$\begin{aligned} \frac{\Delta v_o^-}{V_o^-} &= \frac{(1-D)}{8 \cdot L_{21} \cdot C \cdot (4f_S)^2}, \quad \text{for Ćuk side} \\ \frac{\Delta v_o^+}{V_o^+} &= \frac{D}{R_o^+ \cdot C \cdot 4f_S}, \quad \text{for SEPIC side} \end{aligned} \tag{8}$$

A capacitor (C) of $C = 470$ and µF have been considered for low voltage ripple.

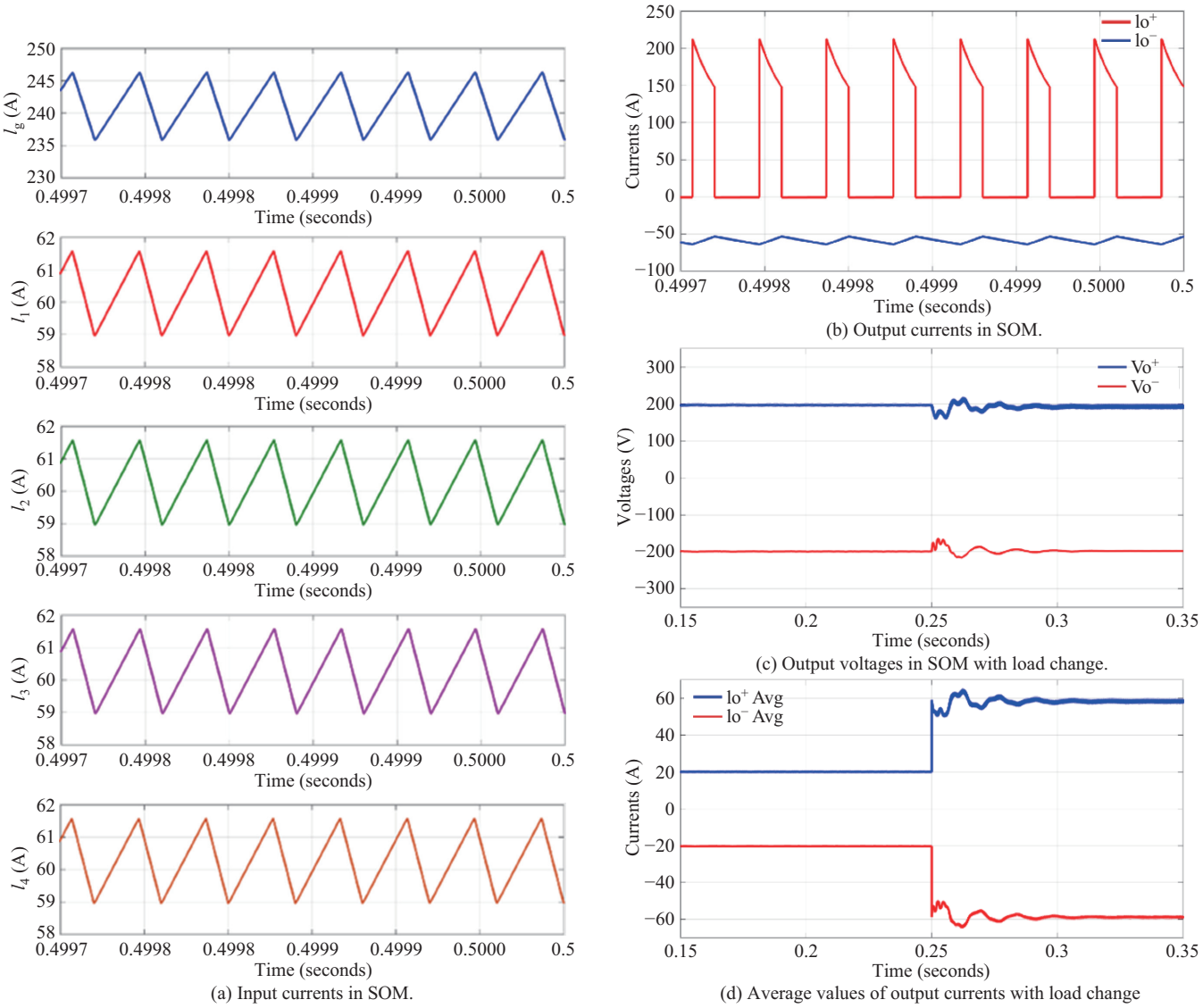
Table II shows the component list.

TABLE II
PASSIVE ELEMENT VALUES

L_{1N}	1 mH
L_{2N}, L_{3N}	1 mH
C_{1N}	470 µF

B. Simulation Results

For the simulation, first the four converters are controlled in SOM. Figure 8 shows the most significant waveforms when this mode of operation is applied. In the following test, the interleaving technique is used. For this test, the PWM signal applied to each converter is shifted a quarter of a period. In this case, since the switching period is 40 µs, the phase shift is 10 µs. Figure 9 shows the waveforms obtained for a input voltage of 100 V, a duty cycle of 2/3 and with loads of $R_{Load1} = R_{Load2} = R_{Load3} = 10\ \Omega$. As it can be seen for the two operating modes, SOM and IOM, the input current (I_g) and the output current at Ćuk side (I_o^-) are triangular waveforms. However, the output current at the SEPIC side (I_o^+) is discontinuous and a trapezoid waveform. Under these conditions, the average current for each interleaved converter is 60 A, and the total current supplied by the DC source is 240 A. In the case of SOM, this current has a peak to peak ripple of 10 A, while in IOM this ripple is reduced to 1 A. Regarding the output current, its average value is 60 A in both modes. However, its ripple is much higher in SOM (Fig. 8(a)) than in



(a) Input currents in SOM.

(b) Output currents in SOM.

(c) Output voltages in SOM with load change.

(d) Average values of output currents with load change

Fig. 8. Simulation results in SOM.

IOM (Fig. 9(a)) with current peaks of 210 A in the first case. So, the interleaved technique significantly reduces the output current ripple. This implies a better quality of the power in its output and therefore a reduction in the characteristics of the output filter.

To verify the dynamic behavior of the converter, the simulation has been performed when a change in load occurs. Thus, initially, the load is made up of resistance values $R_{\text{Load1}} = R_{\text{Load2}} = 10\ \Omega$ and $R_{\text{Load3}} = \infty$. After a time of 0.25 ms, the resistance R_{Load3} takes a value of 10 Ω. Figures 8(d) and 9(d) show the change in the load currents. Regarding the output voltages, Figures 8(c) and 9(c) show their transient response. When the SOM technique is applied, an oscillation appears in the output voltages. So, at the positive side, the voltage ranges from 165 V to 220 V with a damping time of approximately 15 ms. On the other hand, when the IOM technique is applied, the oscillation is between 175 V and 211 V with a damping time of approximately 15 ms. Therefore, with the IOM technique, the overvoltage is much less than that produced with the SOM technique. A similar analysis can be done for the voltage at the negative output side with the same results.

C. Experimental Results

Experimental results were obtained with four interleaved SEPIC-Ćuk combination converters. The input voltage was 100 V and the output voltage was regulated to 200 V by means of a cost effective PWM controller. The switching frequency was set at 25 kHz. At the bipolar output of the converter, a resistance of 80 Ω was connected to the positive output (R_{Load1}) and the negative output (R_{Load2}). To reproduce the phases displaced, four octal D-Type flip-flops were used, which contained eight flip-flops, with a total of thirty-two outputs, all of them connected in a chain. The PWM signal of 25 kHz generated by the controller was used together with a synchronization signal of 1 MHz for the latches. The PWM signal is delayed 1 μs for each flip-flop. The Q outputs with delay 0 μs, 10 μs, 20 μs and 30 μs are used to drive each

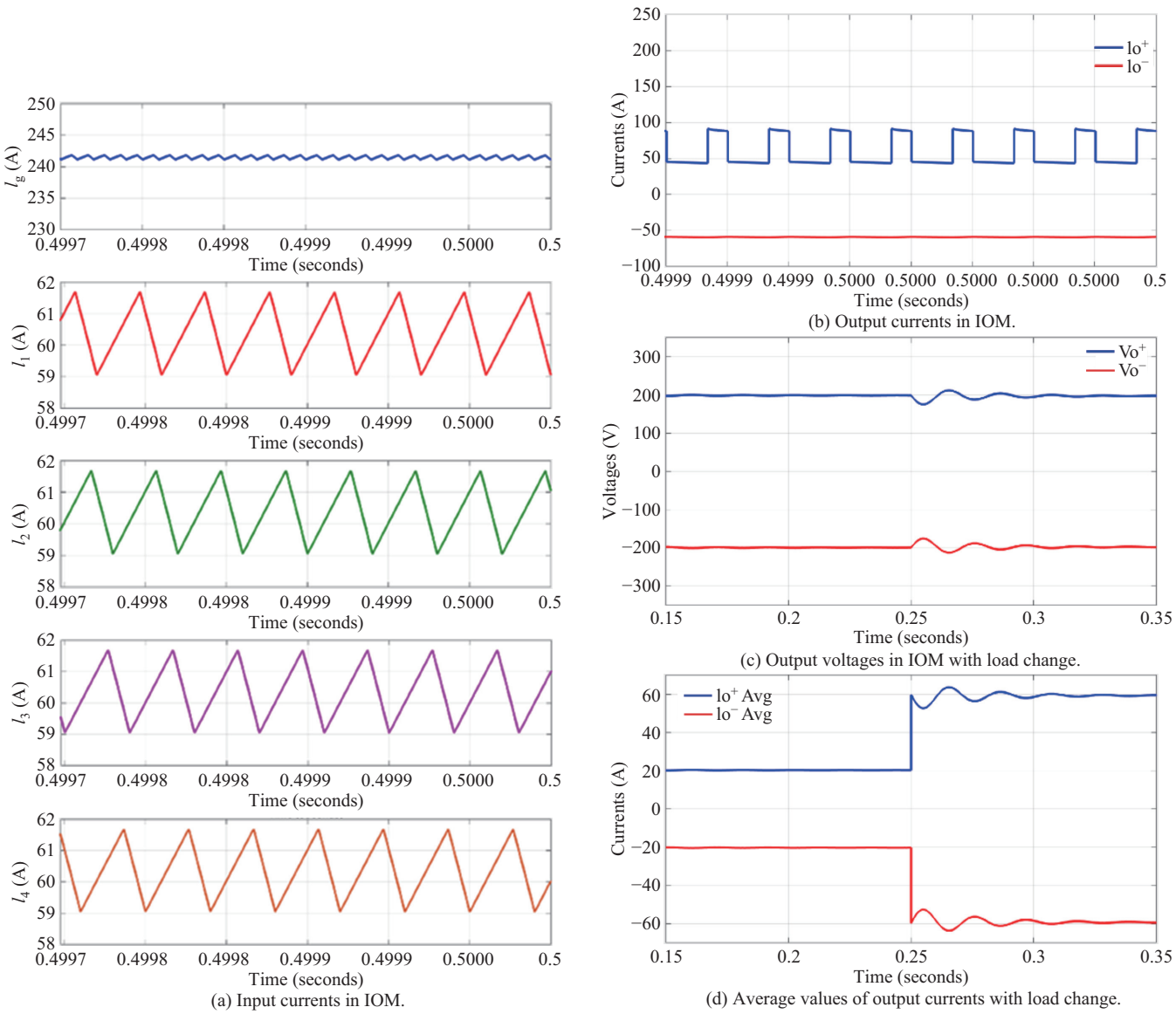


Fig. 9. Simulation results in IOM.

of the four SEPIC-Ćuk combination converters using a gate-driver circuit.

When the SOM technique was applied, the waveforms of the input currents for each converter (according to Fig. 6, it is I_1, I_2, I_3 and I_4) are shown in Fig. 10a. Each current has an average value of 2.4 A and they present a ripple of 3 A. The DC source current (I_g in Fig. 6) has an average value of 9.7 A and a ripple of 9 A. Output currents (I_o^+, I_o^-) have an average value of 2.2 A. Fig. 10b shows the source current and output currents. The measured output voltages are 199.2 V and -199.8 V at the positive and negative outputs, respectively.

When the converters are controlled using the IOM technique, the average value of the input current (I_1, I_2, I_3 and I_4) for each converter is 2.4 A and its ripple is 3.1 A. Figure 11(a) shows the waveforms of the input currents. Otherwise, Figure 11(b) shows the DC source current (I_g). Its average value is 9.6 A with a ripple of 1.1 A. Figure 11(b) also shows the output currents through the positive and negative terminals (I_o^+ and I_o^-). Both currents have an average value of 2.3 A. The experimental results emphasize that the source current has a much lower ripple when the IOM technique is applied. The average values of the output voltages are 199.2 V and -200.0 V.

On the other hand, Fig. 12 shows the output voltages and the load current for the positive output when a change in the load occurs and the IOM technique is applied. In this case, the change is due to the connection of a resistance of 80 Ω between the positive and negative outputs (R_{Load3}). Thus, the output current changes its value from 2.3 to 7.4 A. Here, a small oscillation can be seen in the output voltages at the moment of the change, settling at average values of 199.8 V and -200.5 V.

Before the load change, the power delivered by the converter is 920 W and when the change occurs, the power delivered is 2,960 W. On the other hand, the power supplied by the DC source is 970 W, in these conditions the average input current

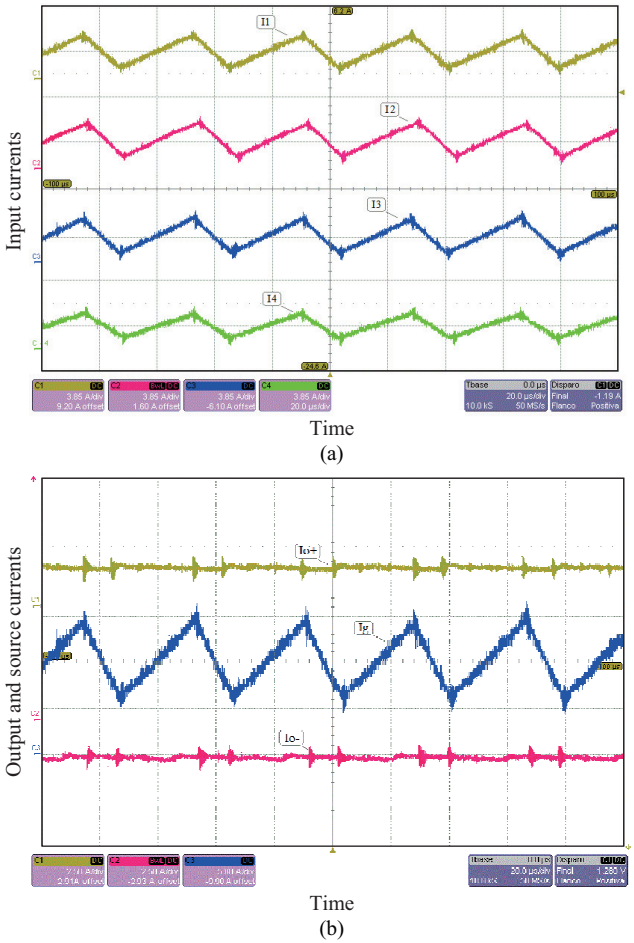


Fig. 10. Experimental result of the interleaved converters when SOM technique is applied: (a) input currents, I_1 (C1: 3.85 A/div, 9.2 A offset), I_2 (C2: 3.85 A/div, 1.6 A offset), I_3 (C3: 3.85 A/div, -6.1 A offset), I_4 (C4: 3.85 A/div, -13.5 A offset) (b) Io+ (C1: 2.5 A/div, 2.91 A offset), I_o^- (C2: 2.5 A/div, -2.93 A offset), I_g (C3: 5 A/div, -9.9 A offset).

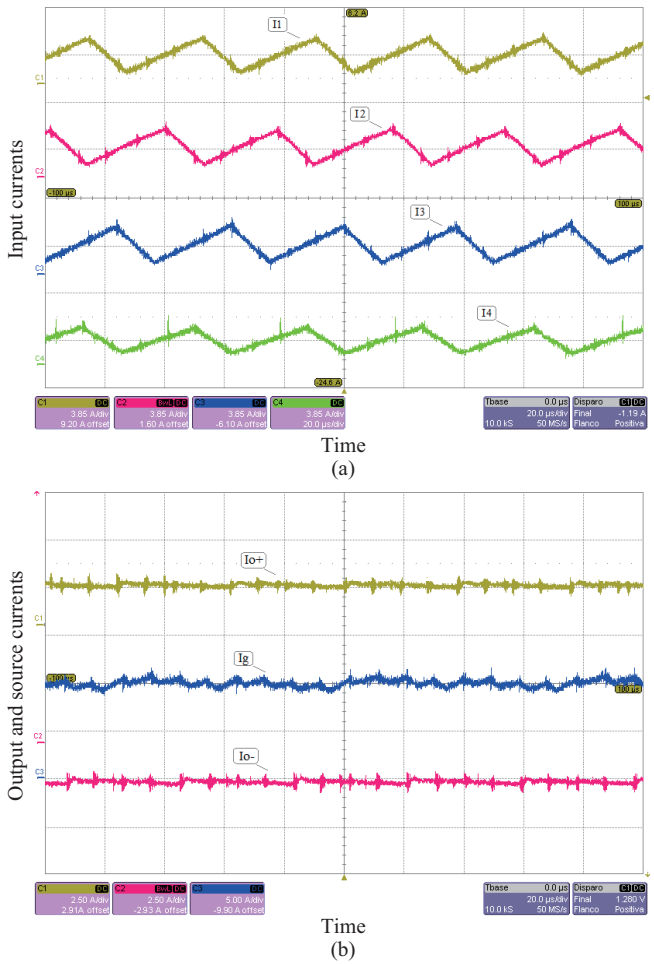


Fig. 11. Experimental results of the interleaved converters when the IOM technique is applied: (a) input currents, I_1 (C1: 3.85 A/div, 9.2 A offset), I_2 (C2: 3.85 A/div, 1.6 A offset), I_3 (C3: 3.85 A/div, -6.1 A offset), I_4 (C4: 3.85 A/div, -13.5 A offset) (b) I_o^+ (C1: 2.5 A/div, 2.91 A offset), I_o^- (C2: 2.5 A/div, -2.93 A offset), I_g (C3: 5 A/div, -9.9 A offset).

is 9.7 A and the voltage is 100 V. After the load change, the average input voltage is 94.2 V and the average input current is 35.7 A, so the input power is 3,363 W. The efficiencies obtained are above 88%.

IV. Conclusion

Single-input multiple-output DC-DC converters have become fundamental structures in many applications, due to their miniaturization and integration tendencies. This paper analyzes an experimental prototype of a four-phase interleaved DC-DC converter based on a SEPIC-Ćuk combination for single-input multiple-output (SIMO) applications. This converter combination obtains dual output voltages of the same value, from a single input DC voltage. The main advantage of the SEPIC-Ćuk combination converter is that it only requires a switch to be controlled and its control terminal is grounded. Multiphase interleaved DC-DC converters achieve a better dynamic response and low ripple, maintaining their efficiency. Each converter is connected in parallel, therefore they manage the losses by distributing them between more components, which facilitates the thermal management of the multiphase converter, allowing it to handle high power values in a smaller

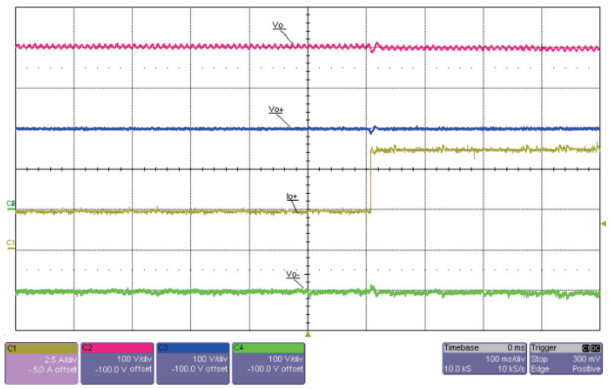


Fig. 12. Experimental result of the interleaved converters when IOM technique is applied and a load change occurs. Channel C1: 2.5 A/div, -5 A offset; Channel C2, C3 and C4: 100 V/div, -100 V offset.

size with respect to the solutions of a single phase.

Two control strategies have been applied: synchronous operation mode (SOM) and interleaved operation mode (IOM).

The simulation and experimental tests allowed for the comparison of both operational modes, verifying that the IOM

presents advantages with respect to the ripple of the input and output currents. The experimental prototype was designed for a distributed power architecture and bipolar DC microgrid (MG). This has allowed the behavior of the interleaved structure to be verified.

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