Analysis of balancing algorithms for Quasi-Two/Three-Level Single Phase Operation of a Flying Capacitor Converter

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Keywords

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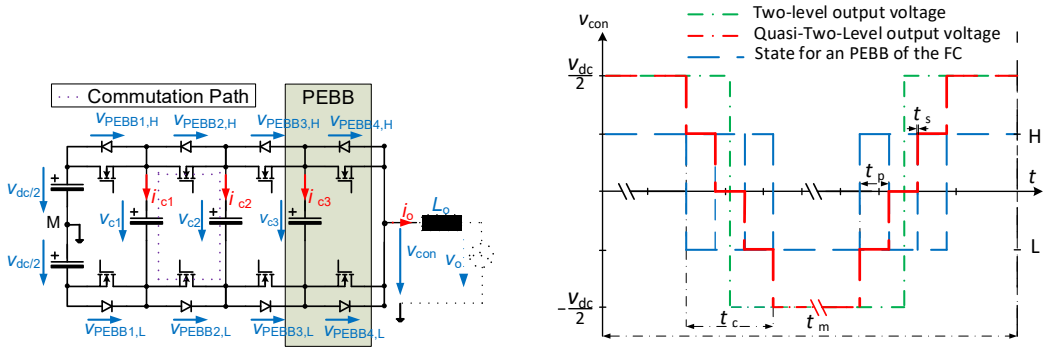
Abstract

Today's standard medium voltage converters are operated with low switching frequencies and contain bulky passive components. One concept to change this is the Quasi-Two-Level operation (Q2O) of multilevel converters with fast switching semiconductors to minimize passive components. The Flying Capacitor Converter (FCC) with SiC semiconductors and operated with Q2O is thus a converter with minimized passive components. In this paper, a comparison of balancing algorithms for Quasi-Two-Level operation of a FCC is presented. The differences between the various methods are demonstrated by simulation and measurement results. Furthermore, a modulation principle with balancing for Quasi-Three-Level operation of a FCC is introduced. With the FCC, it is easy to upgrade from the Q2O to Quasi-Three-Level operation (Q3O) to take full advantage of a three-level output voltage.

Introduction

The generation of electrical energy is currently in a state of transition and will be massively expanded in the next few years due to global climate protection targets. The power of inverter-based generation plants for renewable energies is increasing and these can no longer be integrated exclusively into the low-voltage grids due to the increasing system power ratings. Thus, the grid applications for medium voltage converters will increase in relevance. Today's standard medium voltage converters are either based on the Modular Multilevel Converter (MMC) technology requiring a considerable amount of DC link capacitors or on various 3/5-level converter topologies which are operated at low switching frequencies and contain bulky line filters. Both concepts still lead to relatively high costs due to the high amount of passive components, which are major reasons for the slow spread of medium voltage power converters in grid applications. One promising concept is the Quasi-Two-Level operation (Q2O) of multilevel converters with fast switching semiconductors to minimize the passive components. The Flying Capacitor Converter with Quasi-Two-Level represents a promising variant of such a medium-voltage converter with a greatly reduced expenditure for the DC capacitors. The Quasi-Three-Level offers the possibility to further improve the quality of the output voltage. Compared to the Q2O, the capacitance of one DC capacitor per phase must be increased, but at the same time the filter elements on the AC side can be further reduced.



(a) 5-level FCC, single phase design

(b) Quasi-Two-Level output voltage principle

Fig. 1: 5-level flying capacitor converter, diagram of Quasi-Two-Level switching sequence

Fundamentals of the Flying Capacitor Converter

The concept of the Flying Capacitor Converter (FCC) was first introduced [1]. The multilevel voltage is generated by switching capacitors into the active current path. A n-level FCC ($n \in \mathbb{N}$) is made of $2 \cdot (n-1)$ power semiconductor switches and $(n-2)$ flying capacitors in addition to the DC link capacitor, an exemplary 5-level FCC is shown in fig. 1 (a). The commutation cells of the FCC consist of one high side and one low side semiconductor and the corresponding capacitor. To avoid a short circuit between the capacitors of two adjacent cells, only one transistor of each cell is switched on at the same time.

Each flying capacitor C_i has a different nominal voltage $v_{\mathrm{c,nom},i}$.

$$v_{\mathrm{c,nom},i} = v_{\mathrm{dc}} \cdot \frac{n-1-i}{n-1} \quad i \in [1 \ldots (n-2)] \tag{1}$$

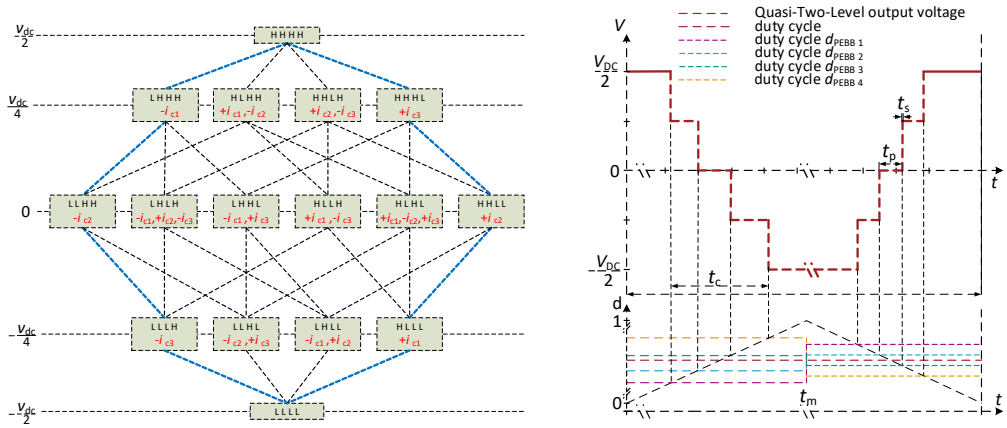
To simplify the construction of an FCC, the converter is built by using modular components i.e. Power Electronic Building Blocks (PEBB). Since the commutation cell is the repeating circuit element, the PEBB consists of one commuctation cell without the second capacitor, as can be seen in fig. 1 (a). An n-level converter requires $(n-1)$ PEBBs. The required average forward blocking voltage of the semiconductors in a PEBB can be calculated with eq. (2).

$$v_{\mathrm{PEBB,nom}} = \frac{v_{\mathrm{dc}}}{n-1} \quad n \in \mathbb{N} \tag{2}$$

During operation, the blocking voltage across the semiconductors always deviates from the average blocking voltage in eq. (2), because the capacitor voltages are free floating and not clamped by external voltages sources. Hence, the voltage across the capacitors varies if the capacitors are switched into the output current path. This is the case for all output voltage levels except $+\frac{v_{\mathrm{dc}}}{2}$ and $-\frac{v_{\mathrm{dc}}}{2}$. In order to keep the blocking voltage of the semiconductors within a reasonable range , it is necessary to balance the capacitor voltages to keep their difference voltage within acceptable limits.

Depending on the operation mode, there are different ways to achieve this: Conventional multilevel operation with Alternative Phase Opposition Disposition (APOD) modulation or Phase Disposition (PD) works by exchanging carrier signals symmetrically for the corresponding semiconductor or with an active balancing algorithm [2].

For Q2O there are two types of balancing: passive or active. For the active method an additional voltage measurement is required. A method with passive balancing for a stationary operating point is presented in [3]. Furthermore, several active balancing algorithms are presented in literature [3, 4, 5]. For active balancing, there are essentially two degrees of freedom available in the modulation. In addition to the time period for which a capacitor is switched into the output current path, the current direction in the



(a) Switching state chart for a 5-level flying capacitor

(b) Quasi-Two-Level modulation principle

Fig. 2: Quasi-Two-Level operation balancing and modulation

capacitor can also be varied due to the redundant switching states.

Quasi-Two-Level Operation

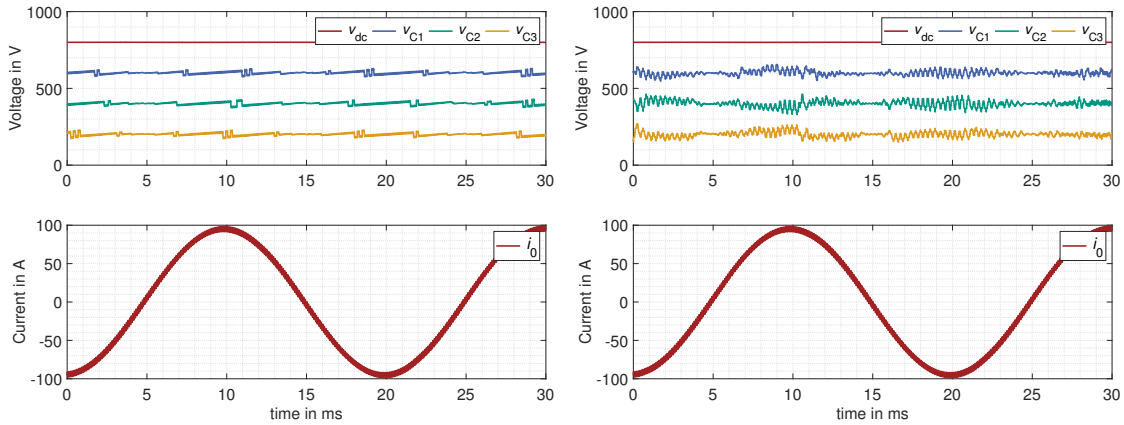
The basic idea of the Quasi-Two-Level modulation is to use the higher level multilevel topology in combination with a two-level modulation scheme. Hence, the applied control and modulation strategies are very similar to the simple ones used for a standard two-level converters. In addition, the advantages of multilevel converters in terms of output voltage waveform (reduced $\mathrm{d}v/\mathrm{d}t$, lower overvoltages) can be used even at high output voltages. The frequency spectrum of the AC output voltage is comparable to that of a 2-level converter. Figure 1 (b) shows a simplified output voltage (red line) of the Quasi-Two-Level modulation and for comparison the output voltage of a two-level converter (dashed green line). Each time a PEBB state (dashed blue line) is changed, a different multilevel voltage is generated. The quasi-two-level switching time t_C is typical below than 5% of the modulation time t_m and in the range of usual interlocking times. For better representation t_C was increased in Figure 1 (b) and Figure 2 (b). The time t_C is the sum of t_p of a switch event.

The Q2O of the FCC with an balancing algorithm was presented independently in [3, 4, 5]. The problem of balancing was fundamentally solved with two different methods. This principle of the modulation of the Quasi-Two-Level algorithm is illustrated in fig. 2 (b) by using the method described in [4]. A carrier-based modulation with an carrier for each PEBB is used to generate the gate signals. Each PEBB has different levels of duty cycle to switch with time delay so that the the Quasi-Two-Level output voltage is generated. The publications [3, 5] showed no significant differences by generation the gate-signals.

Algorithms of Balancing the Capacitor Voltages by Quasi-Two-Level Operation

The balancing methods published so far can be divided into two methods: The first methods [3, 5] has a fixed switching sequence and varies t_p, i.e. the time an intermediate voltage is active. The second methods, formulated and investigated in our earlier work in [4], varies the switching sequence while t_p fixed.

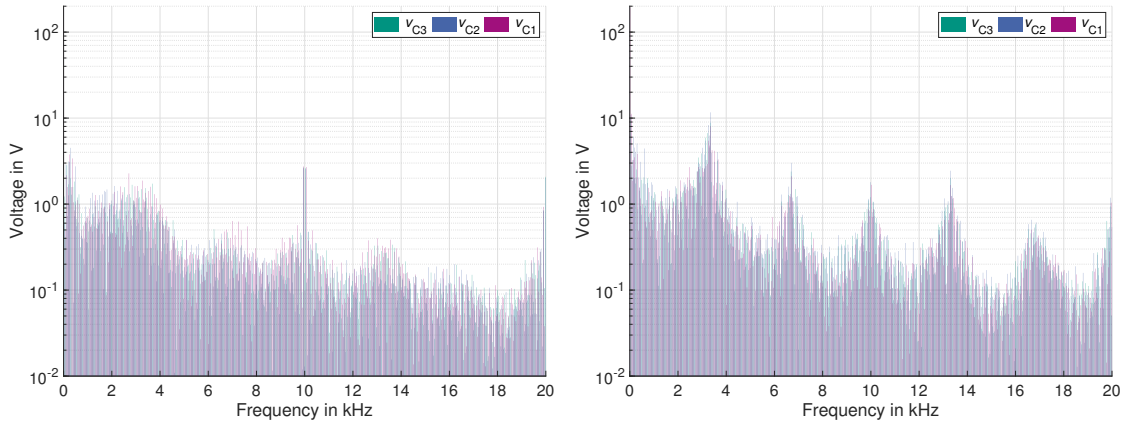
The algorithms of [5] only use the switching sequences marked in thick blue in fig. 2 (a). Depending on the capacitor voltage deviations, the time t_p is selected to be either minimal or maximal. The maximum of t_p depends on the capacitor capacitance and its permissible voltage range in operation. The minimum of t_p depends on the locking time of the used semiconductors, which is dependent on the switching times of the semiconductors ($t_p > t_s$). If at the next switching state the deviation of the actual capacitor voltage and the calculated mean value of the capacitor voltage $v_{c,\mathrm{nom},i}$ decreases, then this switching state is set with the maximum t_p, otherwise the switching state is set only for the minimum t_p.



(a) Simulation results of the first methods [5] balancing algorithm - fixed switching sequences and different time t_p

(b) Simulation results of the second methods [4] balancing algorithm - variable switching sequences and fixed time t_p

Fig. 3: Comparison of capacitor voltage waveforms with the same simulation configuration



(a) Frequency spectrum of the first methods [5] balancing algorithm - fixed switching sequences and different time t_p

(b) Frequency spectrum of the second methods [4] balancing algorithm - variable switching sequences and fixed time t_p

Fig. 4: Comparison of the frequency spectrum of capacitor voltage waveforms

For the algorithms in the second methods, all possible switching sequences in fig. 2 (a) are used. An optimal path is selected depending on the deviation of the actual capacitor voltage and the calculated mean value of the capacitor voltage $v_{c,nom,i}$. Here, the allowable range of t_p is also limited by the above mentioned parameters, but a fixed value is used for this algorithm.

Comparison of the Balancing Algorithm for Quasi-Two-Level Operation with simulation Results

To compare the balancing principles, one algorithm from each methods was implemented in the same simulation environment. The setup is a 5-level FCC with capacitance of 1000nF, a switching frequency of 10 kHz and an inductance L_o of 1 mH in the output. At the output, a single-phase voltage source is connected to the center point M of the split DC link. The split DC link is clamped to $+\frac{v_{dc}}{2}$ with a voltage source directly in the simulation. The hardware parameters of the components as well as the control and carrier-based modulation are identical. Therefore, the differences of the capacitor voltages are caused by the different algorithms. Figure 3 shows the various curves of the capacitor voltages and the output current. It can be seen that both algorithms keep the capacitor voltages stable within a tolerance band around their nominal set-point. The algorithm from the second methods [4] always has larger deviations in capacitor voltages than the algorithm from the first methods [5]. The algorithm

from second methods produces a larger mean capacitor voltage deviation than the algorithm from first methods. In this comparison, the frequency spectrum of the capacitor voltages were also considered, whose absolute values are lower with algorithm from first methods than with algorithm from second methods. The frequency spectrum of the capacitor voltages of the respective algorithms are plotted in fig. 4. The high-frequency voltage deviation with algorithms of first methods are existing exclusively by the switching frequency. The variable switching sequence, on the other hand, does not show such a significant conetration at the switching frequency.

In summary, the results for the algorithm of the first methods are better than for the second methods. Moreover, the coding effort for the algorithm of the first methods is lower than for the one of the second methods. Thus, the first algorithm has significant advantages over the second in stationary operation. For dynamic changes and error cases, the second method has more degrees of freedom.

Quasi-Three-Level Operation

The basic idea of the Quasi-Three-Level modulation is to use the multilevel topology in combination with a three-level modulation scheme. The approach is very similar to that of the Quasi-Two-Level. For the passive components in the output filter, the Q3O makes a significant difference since the voltage deviations to a sine wave with the Q3O is significantly smaller. The Common Mode Voltage is just as smaller and thus a lower stress on the insulation. The modulation is comparable to a three-level modulation and the superimposed control is equal to a standard three-level control, only the balancing is fundamentally different. The Quasi-Three-Level Operation (Q3O) of FCC was introduced in [6].

The basic difference to the Q2O is that one capacitor C_i needs a larger capacitance. This capacitor is required for the zero-voltage output level of the Quasi-Three-Level operation and thus it is not only switched into the current path transiently for a short time t_p and should be able to carry the output current for a full modulation period t_m, depending on the modulation duty cycle. Considering fig. 2 (a) for the 5-level FCC, the possible zero-voltage switching combinations where only one capacitor carries the output current are the combinations with capacitor C_2. The corresponding capacitance of C_2 is calculated according to eq. (3). The design is equivalent to the dimensioning explained in [4] for Quasi-Two-Levels capacitors. In addition to the modulation period t_m, the capacitance depends on the maximum output current $\hat{i}_\mathrm{o}$ and the acceptable capacitor voltage variation $\Delta v_\mathrm{c,max}$ during operation. Usually $\Delta v_\mathrm{c,max}$ is selected in the range of 10...15 % of $v_\mathrm{PEBB,nom}$.

$$C_\mathrm{C2} = \frac{t_\mathrm{m} \cdot \hat{i}_\mathrm{o}}{\Delta v_\mathrm{c,max}} \tag{3}$$

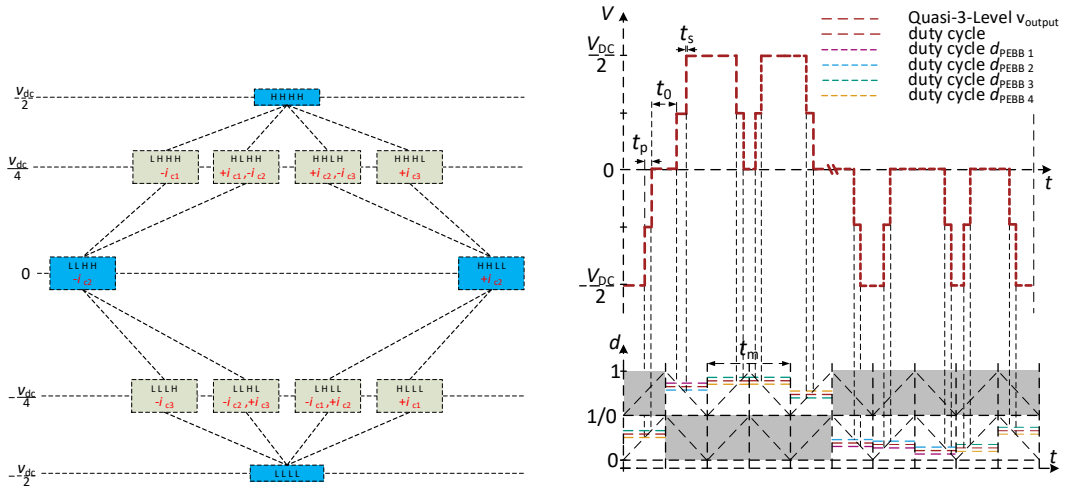
A novel approach of Modulation and Balancing Principle of the Quasi-Three-Level Operation is described below.

Novel Modulation and Balancing Principle of the Quasi-Three-Level Operation

In fig. 5 (b), the principle of the Quasi-Three-Level modulation is illustrated. A multi-carrier method is used. Regarding the modulation, there are four states which are switched on for a longer time than t_p. These are the blue colored states in fig. 5 (a). The other states are used, as for the Quasi-Two-Level, only for a short time t_p.

For Quasi-Three-Level operation, the balancing of the capacitor voltages takes place in two stages. First, the capacitor C_2 is balanced. Thus, depending on the deviation of the current capacitor voltage from the calculated mean value, one of the states LLHH or HHLL is selected. This is done depending on the difference between the actual capacitor voltage and its nominal value. The state which reduces the deviation is chosen once per modulation period.

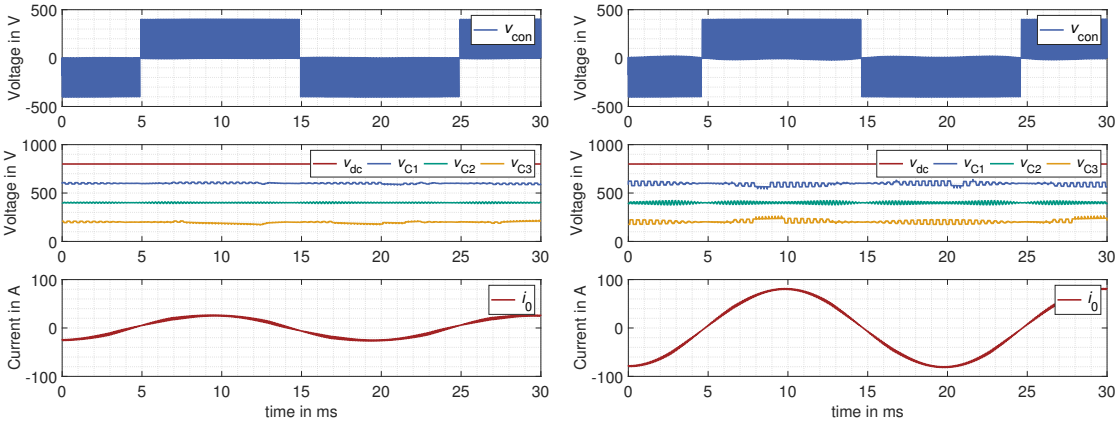
The second step is to balance the other capacitors. For this purpose, the states required for the next switching event are determined according to the balancing principle of [4]. In this principle, fixed time



(a) Switching state chart for a 5-level flying capacitor for Quasi-Three-Level Operation

(b) Quasi-Three-Level modulation principle

Fig. 5: Quasi-Three-Level operation balancing and modulation



(a) Simulation results of the balancing algorithms for Quasi-Three-Level with an output current of 25 A

(b) Simulation results of the balancing algorithms for Quasi-Three-Level with an output current of 80 A

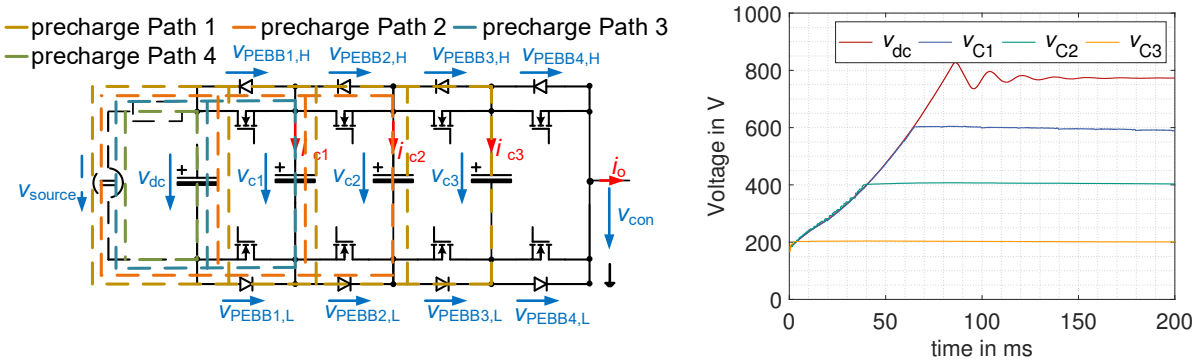
Fig. 6: Simulation results for Quasi-Three-Level with the balancing algorithms by various current value

periods t_p are used and balancing is done by choosing different states to reduce the deviation of capacitor voltages from their mean values. This is performed two times per modulation period.

The principle of the other methods of Quasi-Two-Level balancing would not be suitable here, because balancing is not possible with a fixed switching sequence and variable t_p. There is no charging and discharging of the capacitors realizable by shorter or longer t_p in the possible paths. This would require negative t_p, which it is not possible to realize.

Simulation Results of the Quasi-Three-Level Operation

The simulation setup is a 5-level FCC with capacitance of 1000nF for C_1 and C_3 - the capacitor C_2 with 0.08mF , a switching frequency of 10 kHz and an inductance L_o of 1 mH in the output. At the output, a single-phase voltage source is connected to the center point M of the split DC link. The split DC link is clamped to $+\frac{v_{dc}}{2}$ with a voltage source directly in the simulation. The simulation results of the Quasi-Three-Level are shown in fig. 6. To demonstrate the Quasi-Three-Level operation, the output voltage of the converter was plotted in addition to the capacitor voltage waveforms and the grid current. The balancing algorithm keeps the capacitor voltage within the permissible deviations and works stable. The algorithm including its implementation has not yet reached the same quality of the capacitor voltage



(a) Sketch of the Flying Capacitor with precharge paths of the capacitors

(b) Measurement of the precharging of the FCC with low voltage

Fig. 7: Start up for Operation by a single phase Flying Capacitor Converter

curve as the algoithms of the Quasi-Two-Level. The principle of selecting the path with the minimum deviation of the capacitor voltages leads to the result that a continuous deviation of the capacitor voltage is achieved in some operating ranges of a capacitor. These continuous deviations will be found in the capacitor voltages with always similar values of the output current. In the future, this effect should be examined in more detail.

Start up for Operation by a single Phase Flying Capacitor Converter

In order to operate the converter, the capacitors must be precharged so that the distribution of the DC link voltage results in the semiconductors after eq. (2). The precharging of the FCC with the flying capacitors and DC link capacitor is realized from the DC side.

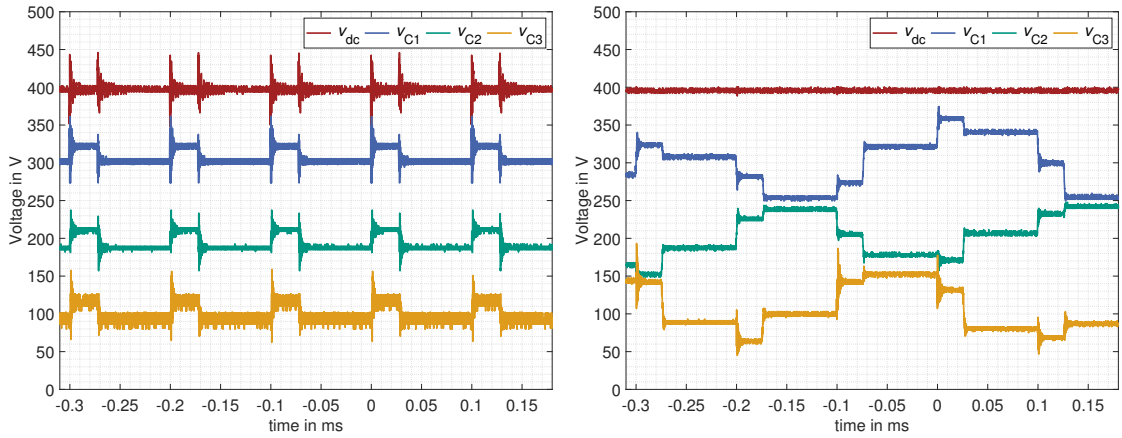
Precharging works in such a way that in the first step all necessary semiconductors are switched on, so that all capacitors are connected in parallel. The current flow path is drawn in fig. 7 (a) as precharge path 1. Then, the voltage of the DC source is ramped up and the capacitors are charged with a constant current. When the voltage of the capacitors has reached the nominal value of capacitor C_3, the according semiconductors are switched off and the other capacitors are charged. The corresponding current flow is labeled as precharde path 2 in fig. 7 (a). The algorithm always switches off the respective semiconductors when the capacitor voltage has reached the setpoint of the respective capacitor. In the example of a 5-level FCC, the semiconductor is switched off a total of 3 times until the DC link capacitor is charged. In fig. 7 the precharge process is plotted from a measurement of the capacitor voltages. The overshooting of the DC link voltage is a result of the dynamics of the current and voltage regulation of the DC power supply. After the capacitors are charged, the balancing of the capacitor voltages and modulation of the output voltage as well as the regulation of the output side can start directly.

Measurements with using a single Phase Flying Capacitor Converter

In [7] the hardware of a Power Electronic Building Block for a FCC for Q2O was presented. The measurement results were generated with two PEBB's connected in series. The setup is a 5-level FCC with capacitance of 1000 nF, a switching frequency of 10 kHz and an inductance L_o of 1 mH in the output.

In the following, measurement results for the operating of the FCC with buck converter mode are presented. The buck converter operation was implemented with an LC filter and DC power supply at the output and a DC power supply to supply the DC link. In single-phase operation, buck converter mode is easier to implement than a single-phase voltage source in combination with a split DC link capacitor.

For the measurements, the voltage of each PEBB ($v_{PEBB,nom}$) was chosen to be 100 V. The voltage was selected low to increase the visibility of the voltage changes by the measurement. Therefore, the duty cycle in operation is in the range of 25 %, because the DC power supply at the output limits the output voltages up to 100 V and output current up to 100 A. .



(a) The measured capacitor voltage of the first methods balancing algorithm - fixed switching sequences and different time t_p

(b) The measured capacitor voltage of the second methods balancing algorithm - variable switching sequences and fixed time t_p

Fig. 8: Measurement results by a single phase FCC for Q2O with buck converter operation

Comparison of the Balancing Algorithm for Quasi-Two-Level Operation with Measurements Results

In fig. 8 the capacitor voltage curves of the different balancing algorithms are shown. The measurement was executed with 75 A in each case, so that the capacitor voltage changes are similar. In fig. 8 (a) , t_p was varied in the range of 500 ns to 1000 ns. The switching sequence has been fixed as described in [5]. In fig. 8 (b) , t_p was fixed at 500 ns. The switching sequence has been selected according to [4].

It can be seen that the curve of the capacitor voltages of the measurement is similar to the simulation results. The difference is that in the measurement, a constant operating point with the same output current and duty cycle was used in comparison to the AC current in the simulation.

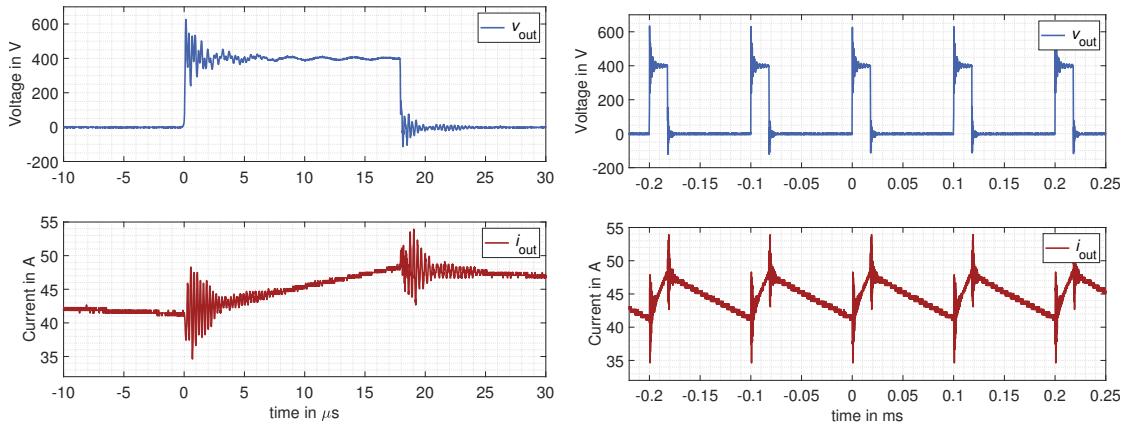
The different balancing algorithms result in different voltage deviations over time. The average voltage deviation for fig. 8 (a) is smaller than for fig. 8(b). The fixed switching sequence always charges each capacitor and discharges each in the same way. The magnitude of the voltage deviation depends on t_p and i_o.

In fig. 8 (b) the different switching sequences lead to voltage deviations, which need to be compensable by the algorithm. During the dimensioning of the capacitors and semiconductors of the prototype, a maximum permissible deviation of 80 V of the capacitor voltage was specified, which both of them fulfill.

What is noticeable in the measurement in fig. 8 (a) is that an oscillation is formed on the capacitor voltages due to the fixed switching sequence. This is not as noticeable with different switching sequences in fig. 8 (b). This is a disadvantageous characteristic, which has not been shown in the simulation results so far. Not all passive effects of the real structure are modeled in the simulation. The distributed leakage inductance in the commutation cells is implemented as a central element and the modeling of the semiconductors does not include a voltage-dependent output capacitance of the mosfets. Since in [5] the adjacent PEBBs are always switched one after the other, a resonance is formed in the structure. Therefore, an oscillation is formed between the Mosfet output capacitances and the distributed leakage inductance, which is transferred to the neighboring PEBBs when they also switch with a delay. The impact of this behavior is also visible in the overvoltages in the following chapter.

Comparison of the output voltage with different operation

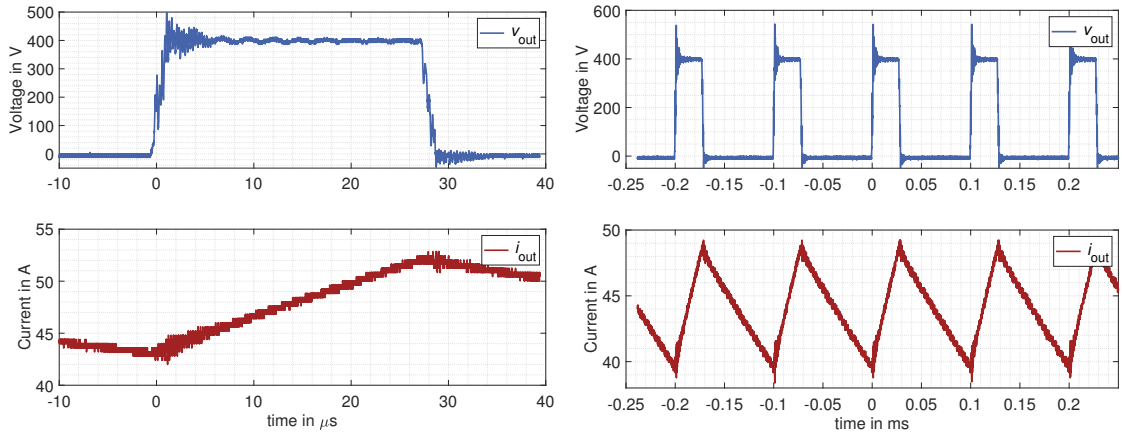
The output voltage waveforms of the Quasi-Two-level and Two-level operation are illustrated in fig. 9,fig. 10 and fig. 11.



(a) The Two-Level Output voltage by buck converter operation with $t_p = 0$

(b) An Overview of Two-Level Output voltage by buck converter operation with $t_p = 0$

Fig. 9: Measurement results by a single phase Flying Capacitor Converter for Two-Level Operation



(a) The Quasi-Two-Level Output voltage by buck converter operation

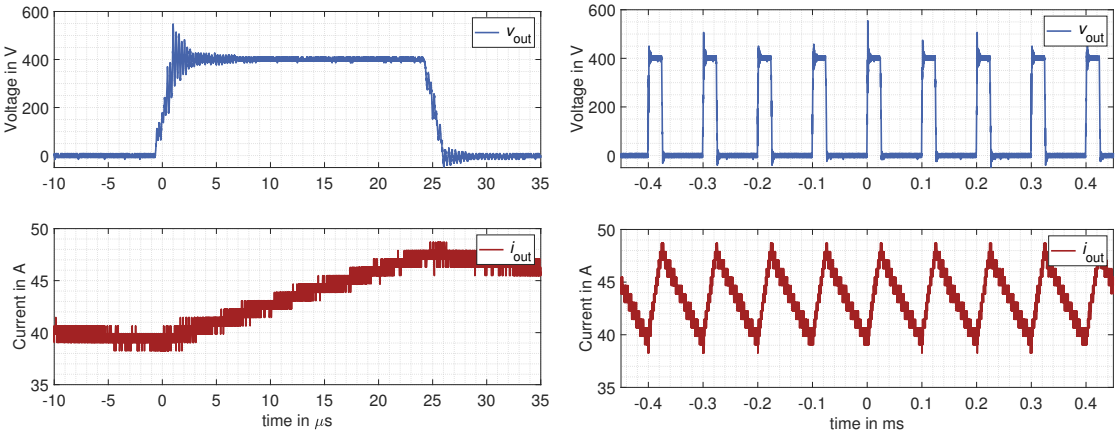
(b) An Overview of Quasi-Two-Level Output voltage by buck converter operation

Fig. 10: Measurement results by a single phase FCC for Q2O with balancing the capacitor voltage with the first methods [5] balancing algorithm - fixed switching sequences and different time t_p

With the prototype, it is possible to switch all semiconductors synchronously ($t_p = 0$) or with a time delay ($t_p > 0$). In the graphs, the output voltage v_{con} is always measured against $-\frac{v_{dc}}{2}$. There is always a plot with the switching events shown magnified and many events in a sequence.

In fig. 10 (a) and fig. 11 (a) the Quasi-Two-Level output voltage is shown and the three short-time switched multilevel voltage stages can be seen. In fig. 9 (a) the two-level output voltage is shown, which is generated by synchronously switching all semiconductors on the high or low side.

Depending on the choice of t_p and the balancing algorithm, the overvoltage at the output-voltage varies. In the setup, the overvoltage is the largest for the two-level operation. With the quasi-two level, the overvoltage is always smaller. However, it can be seen in fig. 11 (b), that depending on the individual switching frequencies, the overvoltage becomes smaller and larger. The overvoltage with the used switching sequences according to [5] are the switching sequences with the largest overvoltage. Considering the reduction of the overvoltage, the balancing principle with variable switching sequence with its greater complexity can outperform the principle with fixed switching sequence with a different weighting of the selection of successive switching states.



(a) The Quasi-Two-Level Output voltage by buck converter operation

(b) An Overview of Quasi-Two-Level Output voltage by buck converter operation

Fig. 11: Measurement results by a single phase FCC for Q2O with balancing the capacitor voltage with second methods [4] balancing algorithm - variable switching sequences and fixed time t_p

Conclusion

This paper presents a comparison and analysis of balancing principles for Q2O of the FCC. The algorithms with fixed switching sequence are easier to implement and generate smaller deviations of the capacitor voltage. Futhermore Simulation results and measurement results of Q2O were presented. The capacitor voltage deviations in simulation and measurements are comparable and thereby validate the function of the algorithms. With a fixed switching sequence, the measurements of the capacitor voltages have shown that an oscillation in the capacitor voltages is pronounced. The effects of the different balancing algorithms on the output voltage were analyzed with the measurement results of the Q2O. The overvoltage of the Quasi-Two-Level operation is always smaller than by Two-Level Operation, however, with the choice of the switching sequence this overvoltage can be additionally positively influenced. In addition, a Quasi-Three-Level operation of the FCC with a modulation principle and novel balancing algorithm is presented. For this purpose, simulation results of the balancing algorithm in Quasi-Three-Level operation are presented with a brief analysis of the resulting present. The Quasi-Three-Level operation can be achieved with only the increase the capacitance of one capacitor per phase. Pre-charge operation of capacitor voltages was explained and and verified experimentally by measurement results.

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