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Electrothermal Ruggedness of High Voltage SiC Merged-PiN-Schottky Diodes Under Inductive Avalanche & Surge Current Stress

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***Abstract*—A comprehensive range of surge current measurements and UIS tests have been conducted for Silicon PiN diodes, SiC JBS diodes and SiC MPS diodes with temperatures ranging to up to 175°C. The results show that the SiC devices outperform the Silicon devices in terms of the avalanche ruggedness, while the SiC MPS diode can compete with the Silicon PiN diode in terms of the surge current performance. These results are validated by the experimental measurements and their subsequent calculated avalanche energy.**

***Index Terms*—Silicon Carbide (SiC), Junction Barrier Schottky, Merged PiN Schottky, Avalanche, Surge Current**

I. INTRODUCTION

Power diodes are key components in power electronics converters in automotive and renewable energy sectors [1]. Experimental [2] and simulation-based [3] of these devices have been at the center of power electronics research. Devices are either Unipolar, i.e. MOSFETs transistors and Schottky diodes, or Bipolar, i.e BJT transistors or PiN diodes [4]. Merged-PiN-Schottky (MPS) diode structure can be the compromise to exhibit the best attributes of both PiN and Schottky diode. This is because the additional implanted P+ well located just below the Schottky contact, as can be seen in Fig. 1, can reduce the electric field at Schottky contact and suppress the leakage current [5], while carriers from the P+ regions can be injected into the drift to trigger the conductivity modulation to reduce the on-state voltage drop. A further reduction of leakage current is expected in SiC MPS diode [6]. Surge Current ruggedness and Avalanche ruggedness of SiC MPS diode have been experimentally characterized in [7]–[12], but with the lack of comparison with other similar rated power rectifiers.

This paper explores the surge current ruggedness of commercially available 4H-SiC MPS diodes in contrast to Closely Rated Silicon PiN and 4H-SiC Junction Barrier Schottky (JBS) diode, the single event avalanche performance of these three devices is also evaluated by means of experimental measurements. Section II explains the mechanism of UIS tests and provides insights based on the experimental results while Section III provides the surge current performance analysis on three devices. Conclusions are provided in Section IV.

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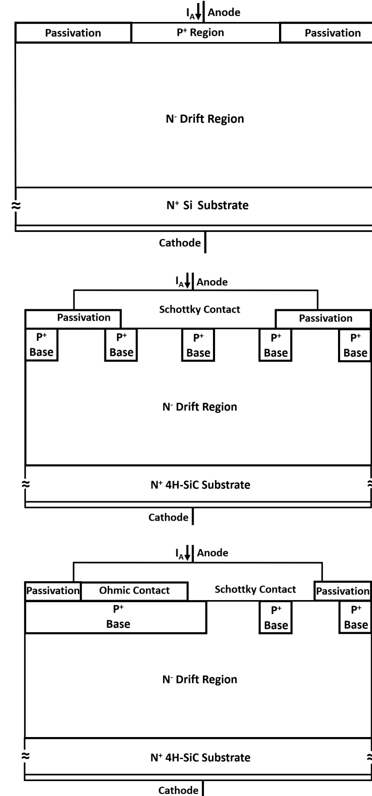

Fig. 1. The cross-sectional schematic of the Silicon PiN, SiC JBS diode and SiC MPS diode, respectively.

II. Unclamped Inductive Switchings test

A. Experimental Set-Up

The single event avalanche ruggedness of Silicon PiN, SiC JBS and SiC MPS diodes have been investigated through a wide scale of UIS measurements [13]. Table. I includes the key parameters of three diodes. All the devices are TO-220 packaged. The UIS testing board is shown in Fig. 2 with a high voltage IGBT (IXBX55N300) acting as the power switch. The initial temperature of diodes before each UIS event is controlled from 25°C to 175°C via ITC-100RL PID Temperature Controller. A load inductor of 1.25 mH is charged to the peak avalanche current that is proportional to the length of the gate pulse L_P, with pulse length of 80 μs & 160 μs, and proportional to the DC link voltage V_{DC} increased from 90 V to 360 V. When the IGBT switches off, the current flowing through the inductor starts to decrease while a counter Electromagnetic Force (EMF) will be induced to resist the abrupt change. The diode voltage rises to the breakdown voltage [12], [14], triggering the avalanche current to flow through the diode. The resulting power dissipation cause the surge of junction temperature, degrades the diode breakdown ruggedness or destroys the device as the hotspot at junction termination with potential for melting of the anode metallization [11]. Typical current and voltage waveforms in a single UIS event is shown in Fig. 2. Unlike the power diodes which will suffer high electrothermal stress, the IGBT will stay safe due to the much higher voltage ratings (3 kV at 110°C). The DC link voltage is initially set to an low value to ensure an initial avalanche energy lower than their failure limit. Such wide range of experimental measurements mimic the actual application.

TABLE I
THE KEY ELECTRICAL PARAMETERS OF THE THREE DIODES USED IN UIS TEST.

Structure	Silicon PiN	4H-SiC JBS	4H-SiC MPS
Model	DSI30-12A	C4D20120A	GC20MPS12-220
Manufacturer	IXYS	CREE	GeneSiC
Blocking Voltage	1200 V	1200 V	1200 V
Forward Current	30 A at 130°C	26 A at 135°C	30 A at 135°C
Leakage Current	40 μA	200 μA	10 μA

B. Result Analysis

Fig. 3 and Fig. 4 show the UIS waveforms at different DC-link voltages until failure, which is also known as the destruction of devices. When the device failure occurs, the diode conducts in the reverse conduction with increasing current levels because of the discharging of the DC link capacitor as the diode lost its blocking capability. In all cases, the Silicon PiN diode fails faster and at lower voltages compared with the SiC JBS & SiC MPS diode. The recovery process of Silicon PiN diode, as in Fig. 3, has been skipped as the device cannot handle such high induced avalanche current. Fig. 5 emphasize the difference in avalanche ruggedness among three

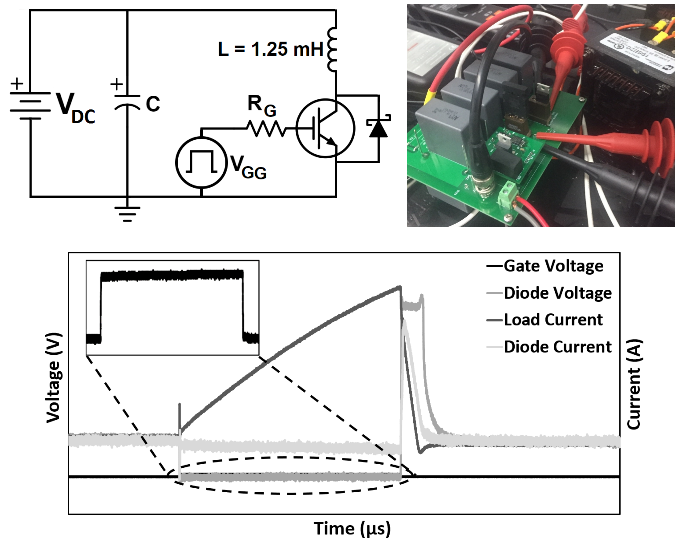

Fig. 2. The UIS test circuit schematic, the UIS test board and the typical waveforms under UIS test.

different diodes at failure mode. In contrast with the diode current of Silicon devices which reach the level of load current immediately after the failure, the rate of current increase is found to be much smaller. This is because of the much smaller impact ionization coefficients in SiC devices which enables a slower generation process of electron-hole pairs [15]. Fig. 6 shows the similar comparison at elevated temperature, all devices is found to be failed at lower voltages with shorter recovery period. This can be explained by the fact that there is less headroom to dissipate power during the recovery process when the temperature is increased.

The avalanche energy is an important parameter since the avalanche breakdown mechanism of power rectifiers is avalanche energy breakdown as a high induced power increase the junction temperature to destroy the devices. The critical avalanche energy is determined as the maximum value before failure of the device during the progressive single UIS tests as highlighted in Fig. 7, can be derived as:

$$E_{ava} = \int_0^{t_{ava}} V_{diode}(t) \cdot I_{diode}(t) \cdot \mathrm{d}t \qquad (1)$$

where t_{ava} is the time duration of device avalanche.

When comparing Fig. 7 for the different devices, the impact of environment temperature on avalanche energy for SiC devices is negligible compared with that of pulse length and DC-link voltage, while a surge of avalanche energy is found at higher temperatures for Silicon PiN diode. For UIS test at 175°C, the critical avalanche energy of Silicon PiN, SiC Schottky and SiC MPS diode is 223.15 mJ, 137.12 and 176.50 mJ. In-line with the physical expectation [16], the maximum allowable avalanche energy of SiC MPS is larger than that of SiC JBS diode since the wide p+ region in MPS structure has a positive effect to promote the avalanche ruggedness. Despite the higher critical avalanche energy of PiN diode, it is always failed at lower DC-link voltage in the progressive UIS test.

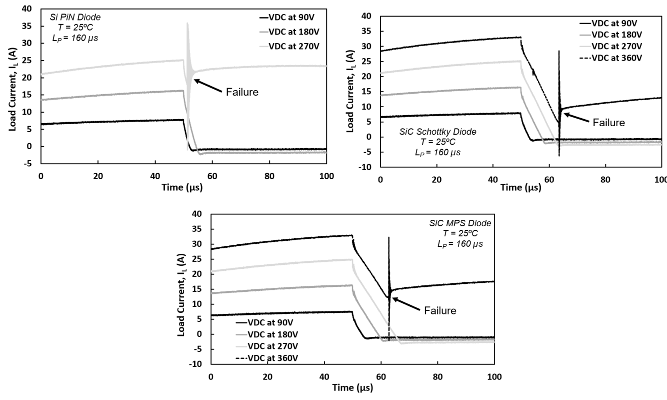

Fig. 3. Avalanche load current for different DC-link voltage until the device failure for Silicon PiN diode, SiC JBS diode and SiC MPS diode.

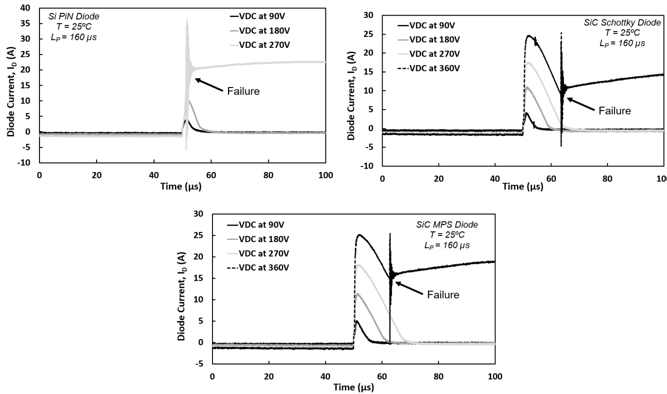

Fig. 4. Avalanche diode current for different DC-link voltage until the device failure for Silicon PiN diode, SiC JBS diode and SiC MPS diode.

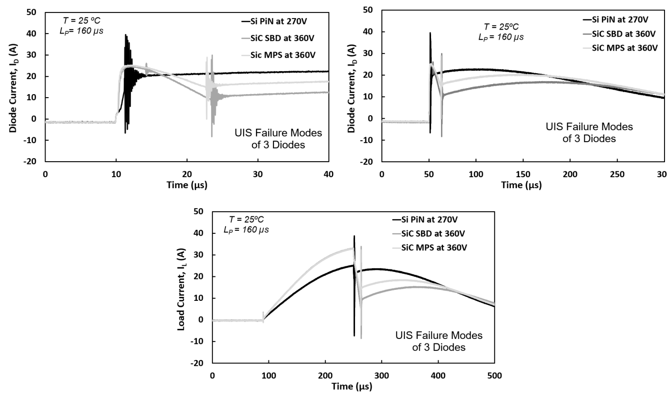

Fig. 5. The (top left) zoomed-in and (top right) overall waveforms of diode current at failure and the (bottom) overall waveform of load current when failure occurs.

III. Surge Current Test

A. Experimental Set-Up

For Surge Current measurements [17]–[19], the C4D20120A SiC JBS diode is replaced by a 1200V/26A SiC JBS diode with reference C4D20120H while the DSI30-12A Silicon PiN diode is replaced by a 1200V/30A Silicon PiN diode with reference DSEP30-12B. The Surge current testing

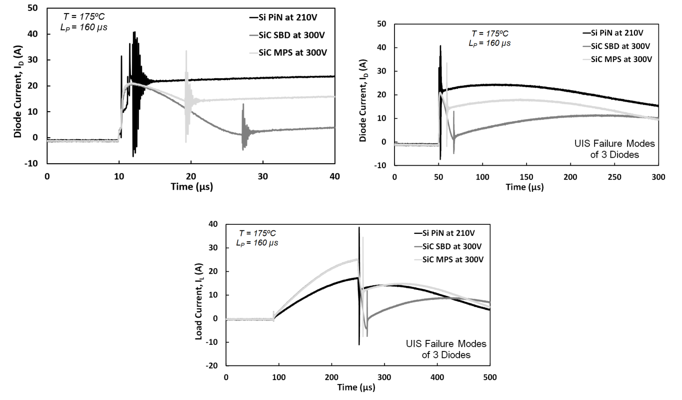

Fig. 6. The new avalanche limit for the 3 diodes when tested at 175°C.

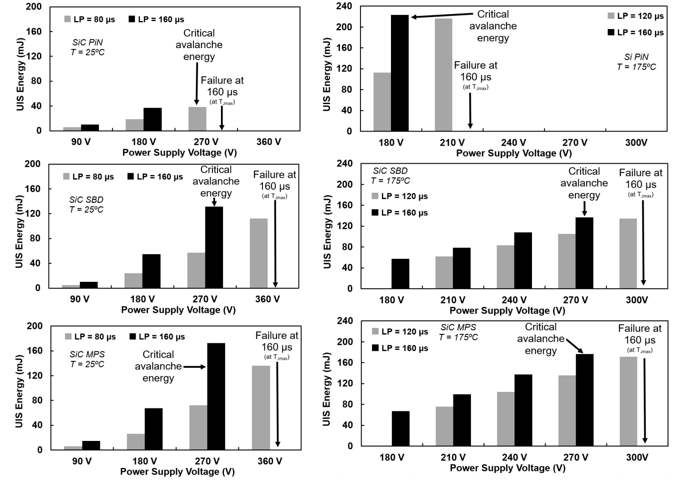

Fig. 7. Determination of critical avalanche energy from the UIS test at 25°C and at 175°C.

board and the typical current and voltage waveforms in a single surge current event [20] is shown in Fig. 8. Four parallel connected Silicon power IGBTs IXGK400N30A3 are used to accurately set the current conduction time of 100 μs through the diode [14], [21]. A 2052 μF capacitor bank was used to ensure that the most of the charge stored inside the capacitors can be released during the surge current event to avoid the diode voltage overshoot in the IGBT. The initial temperature before the circuit turn-on is controlled from 25°C to 175°C via the same temperature controller used for UIS measurements. The charge stored in the capacitors is proportional to the DC link voltage V_{DC} increased from 40 V to 160 V. When the IGBTs switch on, the charge stored in capacitors will be released to induce the surge current I_{Surge}.

The resulting power dissipation cause the surge of junction temperature, degrades the diode blocking capability or destroys the device as the hotspot at junction termination with potential for melting of the aluminum anode metallization [7], [22], [23]. Unlike the power diodes which will suffer high electrothermal stress, the IGBTs will stay safe because of the increased current rating from the parallel connection.

Unlike the UIS measurements where the failure of devices can be directly observed from the waveforms, a B2901A Source/Measure Unit is used to capture both the Forward I-V characteristic and reverse leakage current of all three diodes to trace degradation and detect failure during the surge current measurements.

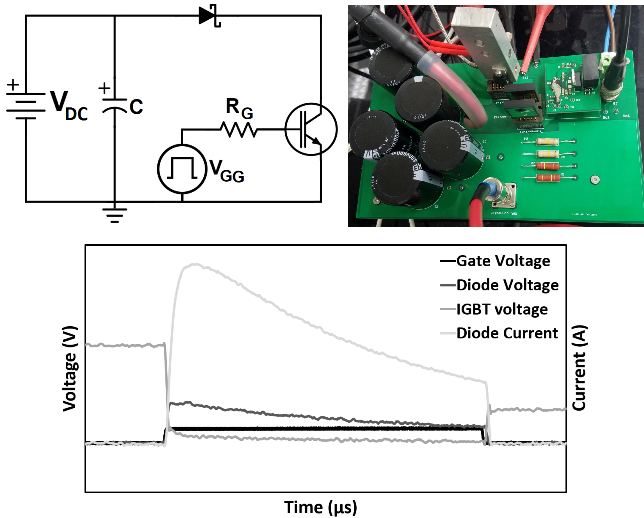

Fig. 8. The Surge Current test circuit schematic, the surge current test board and the typical waveforms under surge current.

B. Result Analysis

Fig. 9-11 show the forward voltage drop and the forward surge current of three diode rectifiers under non-repetitive surge testing. It is observed that the forward surge current increases with DC link voltage, as expected, while the on-state voltage across diodes is increasing with increased surge current. For Silicon PiN diode, the less voltage increment is observed at high currents as a indicator of conductivity modulation, which also hold true at elevated temperatures. However, the conductivity modulation, which is not in line with the physical expectation, is less evident in the case of SiC devices at both low and high temperatures. This is mainly because of the low carrier lifetime in SiC impeding adequate conductivity modulation in the drift region in on-state, contributing to additional on-resistance. This problem becomes aggravated if the current imbalance between Schottky junction and pn junction within the device occurs after the injection of hole from P+ region, leading to the smaller effective area for carrying the surge current and dissipating the surge energy [24]–[26]. The minor conductivity modulation for SiC JBS diode is expected [23] as it favours the unipolar conduction through the JBS structure which is designed to block high voltage while secure its unipolar conduction mode [5]. However, this is a crucial disadvantage of MPS diodes which is expected to have high level injection.

Fig. 12 emphasizes the difference in forward voltage and surge current among three different diodes at surge current mode. It can be seen that the surge current for Si PiN diode is the largest, followed by that of SiC JBS and that of MPS. The on-state voltage of SiC JBS diode is the highest followed by that of SiC MPS diode and Silicon PiN diode while the minor conductivity modulation provided by the wide p+ region of MPS diode provides a lower voltage compared to that of JBS diode. These are true at both low and high temperatures.

Fig. 13 and Fig. 14 provide a comparative illustration of the failure limit of the three devices under surge testing at 25°C and 175°C, respectively. The occurrence of device failure during the surge testing is identified by means of monitoring

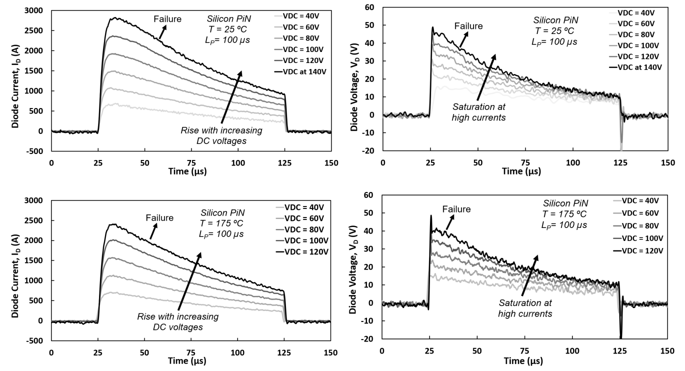

Fig. 9. Forward voltage and current during the non-repetitive surge testing for Silicon PiN diode at 25°C & 175°C.

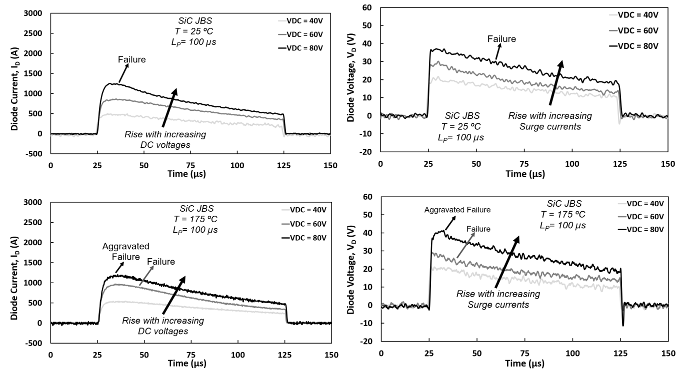

Fig. 10. Forward diode voltage and current during the non-repetitive surge testing for SiC JBS diode at 25°C & 175°C.

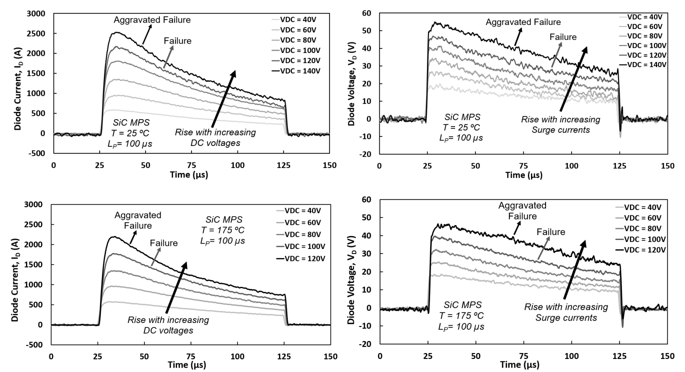

Fig. 11. Forward diode voltage and current during the non-repetitive surge testing for SiC MPS diode at 25°C & 175°C.

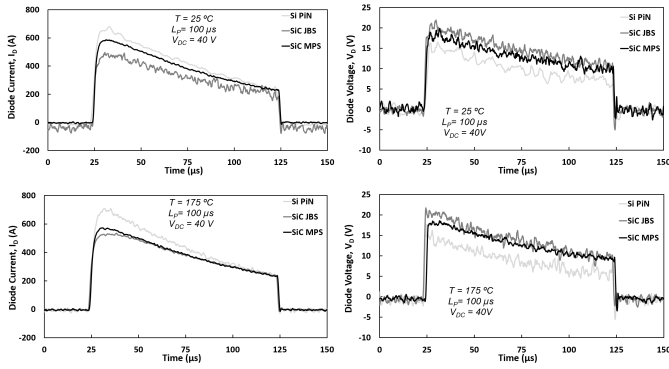

Fig. 12. Forward diode voltage and current during the non-repetitive surge testing for three devices at 25°C & 175°C.

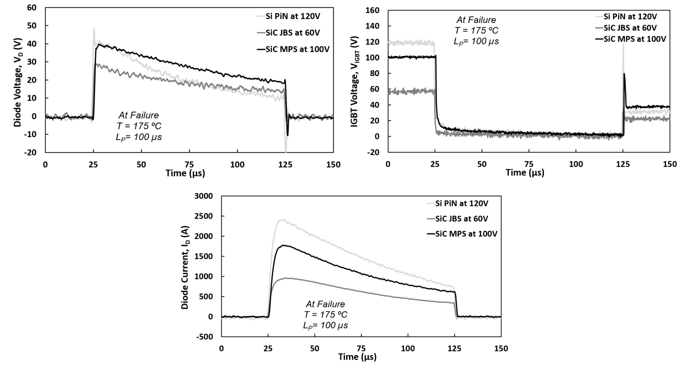

Fig. 14. Forward diode voltage, IGBT voltage and diode current when failure occurs for three devices at 175°C.

the I-V characteristic and leakage current as shown in Fig. 15-17. When the electrothermal stress is increased, the threshold voltage is found to decrease while the decrease of slope($\frac{dv}{di}$) indicate the decrease of on-state resistance. In terms of leakage current, significant degradation is observed where the leakage current starts to rise at low blocking voltages while that during normal operation remain constant. The faulty reverse mode performance is found to be aggravated when the surge current is further increased, as shown in Fig. 16 and Fig. 17, where the breakdown voltage is reduced to almost zero and the leakage current increases akin to that in a conductor. In contrast, Fig. 15-17 shows that minor degradation is observed in I-V characteristic when the surge testing is repeated at higher DC-link voltages after the failure is observed from the leakage current, especially for the case of SiC JBS diode where the convergence between the normal condition I-V characteristic and faulty I-V characteristic is observed. Fig. 9-11 and Fig. 13-14 also illustrate that the diode can still conduct surge current during measurements even though the failure is already caused inside the device. In all cases, the SiC JBS diode failed at the lowest surge current, followed by SiC MPS and Silicon PiN diode. When the temperature is increased, all devices is found to be failed at lower voltages. This can be explained by the fact that there is less headroom to dissipate power during the recovery process when the temperature is increased.

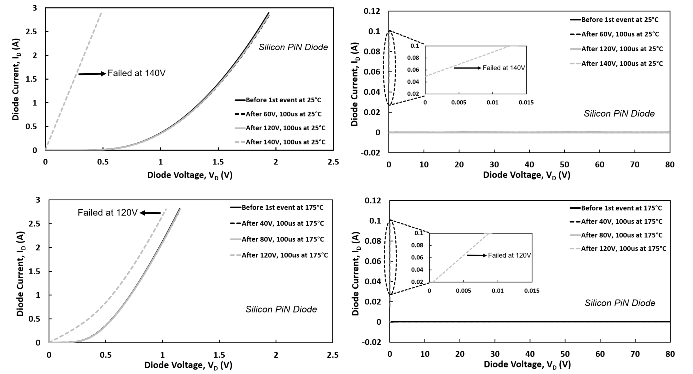

Fig. 15. Forward I-V characteristics and reverse leakage current captured during the non-repetitive surge testing for Silicon PiN diode at 25°C & 175°C.

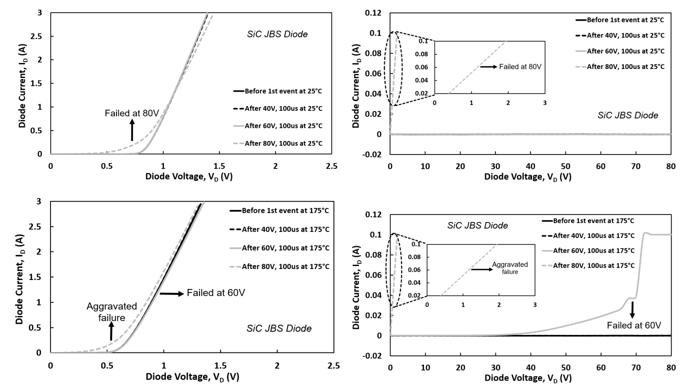

Fig. 16. Forward I-V characteristics and reverse leakage current captured during the non-repetitive surge testing for SiC JBS diode at 25°C & 175°C.

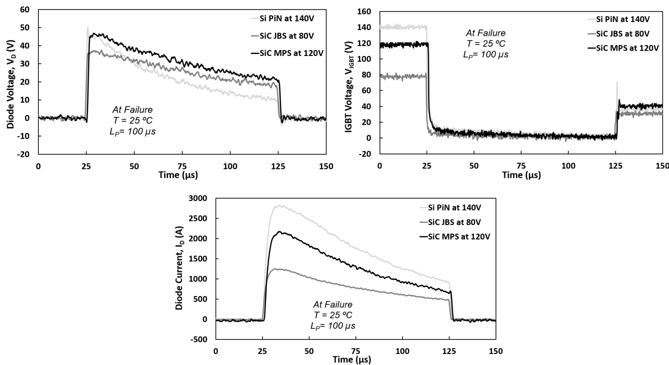

Fig. 13. Forward diode voltage, IGBT voltage and diode current when failure occurs for three devices at 25°C.

Since the degradation or destruction of devices under the surge testing can be linked to high dissipated energy leading to molten metallization [7], [28], the dissipated surge energy is also calculated akin to that in UIS measurements. The critical surge energy is determined as the maximum value before failure of the device during the progressive surge tests as highlighted in Fig. 18-20, can be derived as:

$$E_{Surge} = \int_0^{t_{ava}} V_{diode}(t) \cdot I_{diode}(t) \cdot \mathrm{d}t \tag{2}$$

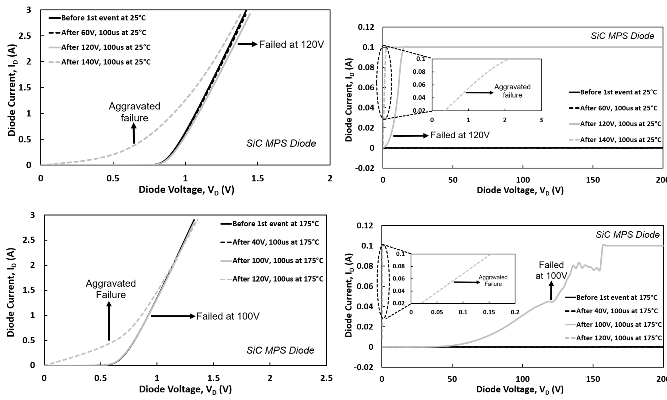

Fig. 17. Forward I-V characteristics and reverse leakage current during the non-repetitive surge testing for SiC MPS diode at 25°C & 175°C.

where t_{Surge} is the time duration of surge current conduction. At low temperature, the critical Surge energy of Silicon PiN is the highest, followed by that of SiC MPS, and then that of SiC JBS diode. This is also expected from Fig. 9-11 as the induced surge current of Silicon PiN diode is higher than that of SiC devices. The larger die size of Silicon PiN diode also causes a lower current density and energy dissipation per area [27], which increase the reliability. The critical energy is found to be lower at higher temperatures. This is because of the shorter recovery period available at high temperatures, primarily due to the smaller difference between the junction temperature and the preset temperature making the energy dissipation more difficult. The critical energy of Silicon PiN diode is found to be lower than that of SiC MPS at elevated temperature. This is because the thermal conductivity of SiC, which is two times higher than that of Silicon, become dominant to have a more effective heat dissipation. Despite the SiC MPS diode able to sustain a larger surge energy compared to Silicon PiN diode before the actual failure takes place, this device always failed at lower surge currents during the progressive surge tests.

For power system applications with long steady-state operation, the lack of conductivity modulation is prone to destructive consequences as the increased power dissipation can create extra heat while the negative temperature dependence of on-state resistance can lead to thermal runaway. But the minor modulation is suitable for high frequency application as the low stored charge and thus the fast-switching transient is secured. To optimise the conductivity modulation effect of the MPS diode, it is necessary to increase the minority carrier lifetime to reduce the voltage and current required to enter the high-level injection mode [5]. A positive feedback loop between current and temperature is generated since the hotter diode with lower voltage can conduct more current that will continue to increase until failure.

IV. Conclusion

In this paper, the surge current performance and avalanche ruggedness of Silicon PiN diode, SiC JBS diode, and SiC MPS diode have been investigated by means of wide-scale experimental measurements in a range of temperatures to up

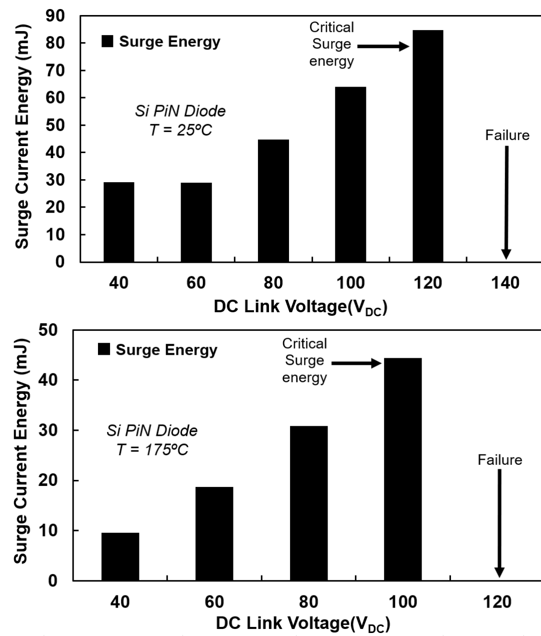

Fig. 18. Determination of critical surge energy for Silicon PiN diode from the surge testing at 25°C and at 175°C.

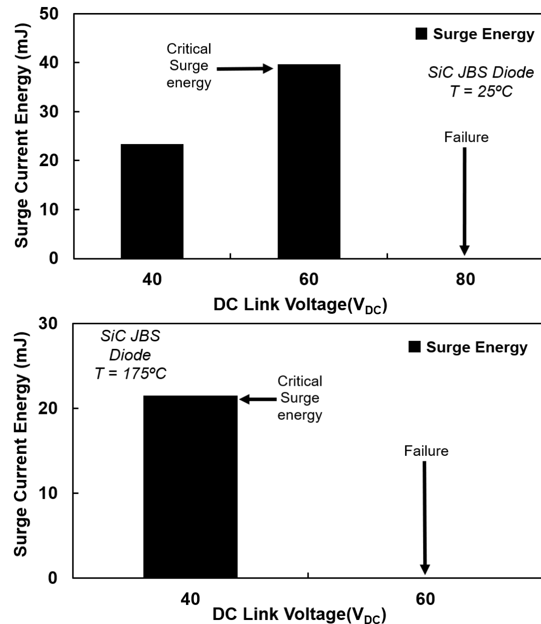

Fig. 19. Determination of critical surge energy for SiC JBS diode from the surge testing at 25°C and at 175°C.

to 175°C. Although the Silicon PiN diode have the highest avalanche energy, SiC MPS diode is the most electrothermally rugged devices as it can withstand higher load currents, followed by that of the SiC JBS diode, and then the Silicon PiN diode, as is reflected by the measurement results. In terms of the surge testing, Forward I-V characteristic and reverse leakage current are also captured to monitor degradation inside devices. All the devices can still conductor current at the on-state akin to a pure conductor even though the failure is

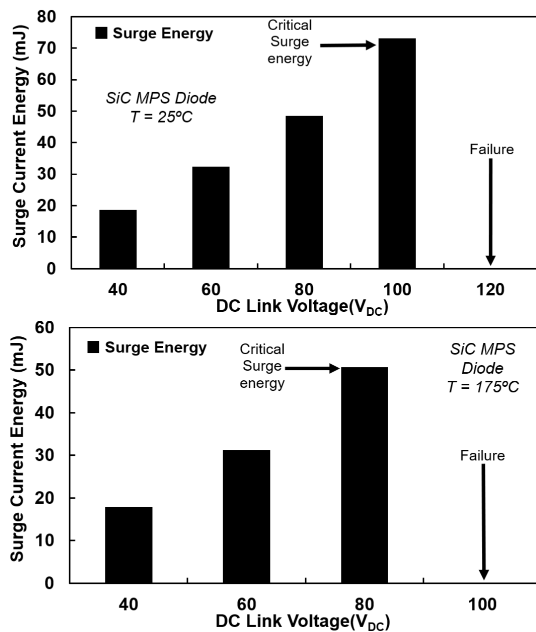

Fig. 20. Determination of critical surge energy for SiC MPS diode from the surge testing at 25°C and at 175°C.

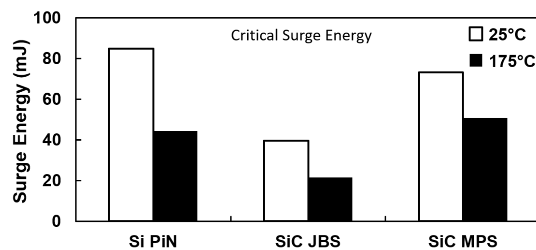

Fig. 21. Comparison of critical surge energy for Silicon PiN, SiC JBS & SiC MPS diode at different temperatures.

identified in their reverse characteristic. However, the reverse blocking capability is lost as the breakdown voltage has been abruptly reduced after the failure is spotted. Thanks to the conductivity modulation observed in the Silicon PiN diode during the surge testing and the larger die size, Silicon PiN diode has the highest surge ruggedness at room temperature while the SiC MPS diode is the most electrothermally rugged devices at high temperatures because of the high thermal conductivity. These are reflected by the measurement results and the calculated surge energy.

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