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Positive and Negative Bias Temperature Instability on Crosstalk-Stressed Symmetrical & Asymmetrical Double-Trench SiC MOSFETs

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***Abstract*—The bias temperature instability (BTI) has been an issue for SiC MOSFET. The device performance would vary with the induced threshold drift. In this paper, the peak shoot-through current during crosstalk under the impact BTI is investigated in regard to increase of stressing time and recovery time for SiC symmetrical and asymmetrical double-trench MOSFET as well as planar MOSFET for comparison purpose. The change of threshold voltage under BTI is measured and are compared with the shoot-through. The measurement of threshold drift under accelerated gate stressing is also conducted and the impact of temperature is investigated.**

***Index Terms*—Silicon Carbide, MOSFET, BTI, Crosstalk, Double-Trench**

I. Introduction

Threshold voltage drift has been a reliability issue for SiC MOSFETs used in power electronics converters fore renewables applications [1], especially after stressing applied on the gate. Thus is a reliability issue in MOS-gated transistors, i.e. MOSFETs [2]–[4] & IGBTs [5], [6], as oppose to current-driven devices, i.e. BJTs [7] & Thyristors [8]. It is also important in high voltage GaN HEMTs [9]. This is a consequence of charge trapping or de-trapping on the oxide layer depending on the polarity of stress. Unlike Silicon MOSFET, SiC MOSFET is more sensitive to gate stressing because there is Carbon presented at the oxide-channel interface which are potential origins for the traps as well as its wide band-gap property accommodating more traps in trapping/de-trapping of charges [10]. The threshold voltage drift significantly impact the circuit operation in terms of on-state loss and turn-ON/turn-OFF delay. In recent studies of bias temperature instability (BTI) characteristics mainly focuses on SiC planar MOSFET. With the introduction of double-trench structured SiC MOSFET, it has became a popular candidate for industrial applications since it allows high cell-density implemented on the design so that on-state conduction loss and parasitics are reduced [11]. In this paper, the impact of BTI on crosstalk shoot-through current has been studied on symmetrical and asymmetrical double-trench MOSFETs in comparison with the planar MOSFET. These devices have also been previously subjected to UIS [12] and short-circuit [13] tests. The cross-sectional structure of these devices are shown in Fig. 1.

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II. Impact of BTI on Crosstalk Shoot-through

In this section, the selected DUTs are subject to positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI). The experimental procedure along with the circuit is demonstrated in Fig. 2. The gate resistance (R_{G_Bot}) at bottom side where DUTs sit is selected to be 330 Ω so that the shoot-through could be exaggerated. The impact of stressing time and recovery time is investigated.

A. Impact of Recovery Time

Fig. 3 and Fig. 4 shows the peak shoot-through current measured for the three DUTs being subject to a fixed +20V/10s at a increase of recovery time under 25°C and 175°C, respectively. The dashed line in the graphs represents unstressed case. At positive gate stressing, electrons are captured by oxide traps so that threshold voltage is increased and this parasitic turn-ON

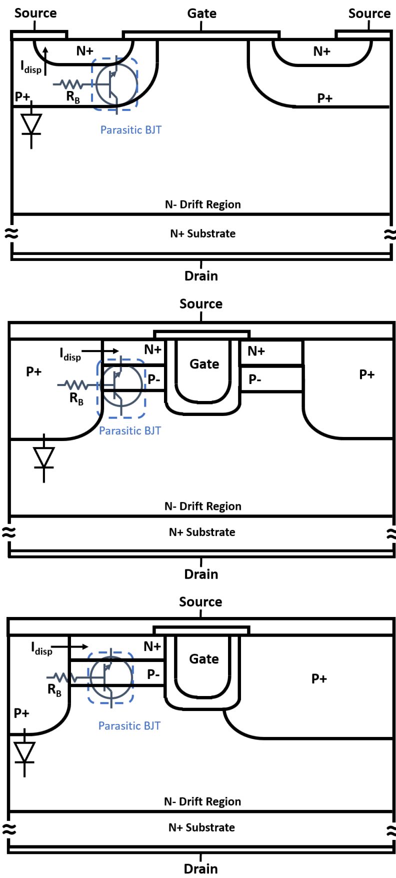

Fig. 1. Cross-sectional schematics of SiC planar MOSFET, SiC symmetrical double-trench MOSFET and SiC asymmetrical double-trench MOSFETs, respectively.

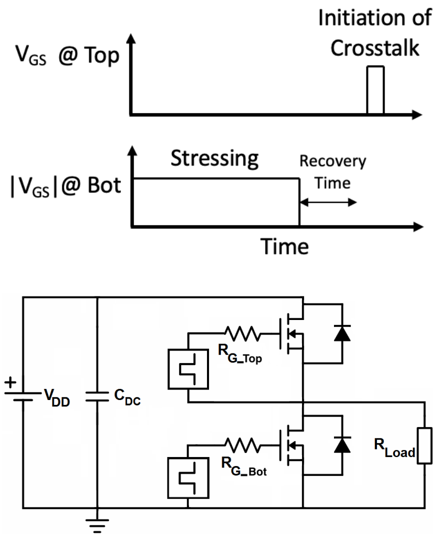

Fig. 2. Experiment procedure and test circuit to investigate the impact of BTI on crosstalk shoot-through.

at crosstalk is damped. With the increase of recovery time, threshold voltage restores so that the measured peak shoot-through gradually approaches the unstressed case. it can be observed that at 25°C, 1s is enough for the peak shoot-through current to nearly fully recover. This feature is retained when temperature rises to 175°C except for symmetrical double-trench MOSFET with significant residual shoot-through drift at 1s recovery time, this indicates that there is more permanent damage induced during the stressing at high temperature.

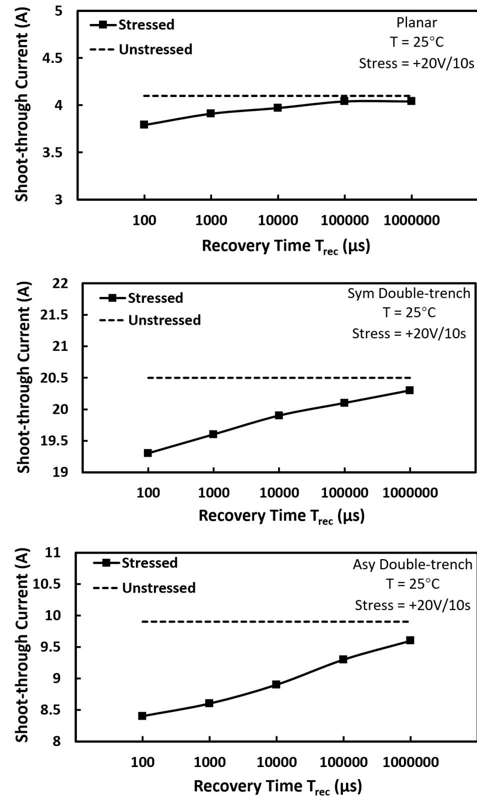

Fig. 3. Peak shoot-through current for three DUTs under PBTI at increase of recovery time under 25°C.

Fig. 5 and Fig. 6 shows the peak shoot-through current measured for the three DUTs being subject to a fixed -20V/10sec at a increase of recovery time under 25°C and 175°C, respectively. The dashed line represents the unstressed case. At negative gate stressing, electrons are released from the oxide traps so that threshold voltage is decreased and shoot-through at crosstalk is enhanced. In this NBTI case, it is noticed that, unlike the PBTI case, at the maximum recovery time of 1s, there is still shoot-through drift remained which suggests that the negative voltage causes more long-term degradation on device. It should be mentioned that gate stressing not only impact shoot-through by means of threshold drift but also mobility degradation [14]. Hence, the actual threshold drift occurred behind the shoot-through measurement would be more significant in the NBTI case and less in the PBTI case.

B. Impact of Stressing Time

Both threshold drift and peak shoot-through variation has been measured in regard to a stressing time increase with a fixed recovery time of 0.5 sec. The threshold drift is defined as

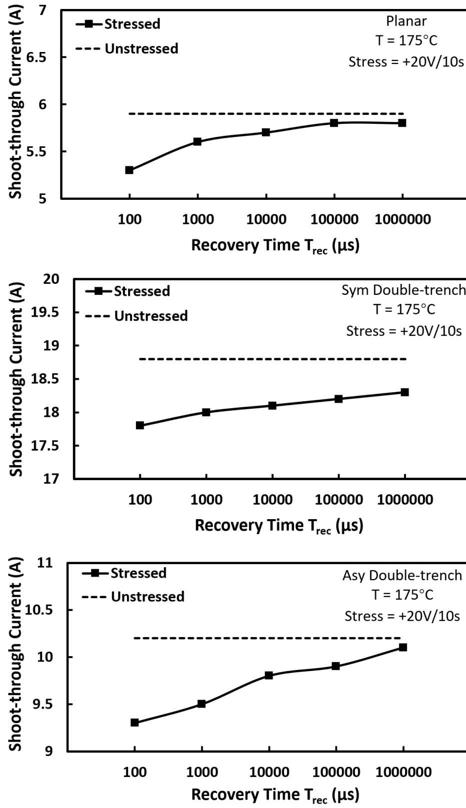

Fig. 4. Peak shoot-through current for three DUTs under PBTI at increase of recovery time under 175°C.

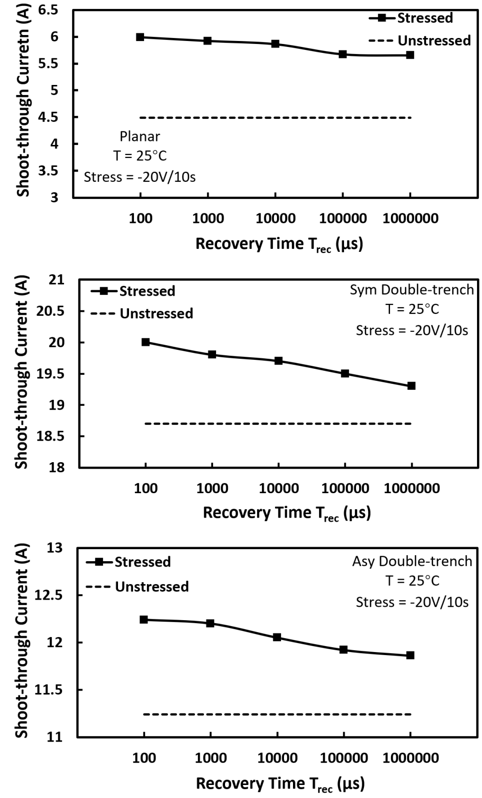

Fig. 5. Peak shoot-through current for three DUTs under NBTI at increase of recovery time under 25°C.

1mA at drain-source voltage (V_{DS}) of 0.5 V measured using source measure unit (SMU) B2902A. Since these two parameter measurement are performed on two different individual devices, they are normalized to make a fair comparison as shown in Fig. 7 and Fig. 8 for PBTI and NBTI respectively.

As the stressing time increases, it is expected to have more pronounced effect on the threshold drift since traps deep inside the oxide layer will be involved. In the PBTI case, although clear threshold drift has been recorded for three devices with stressing time increase, planar shows a significant corresponding change in peak shoot-through while it is milder for asymmetric double-trench and nearly no change for symmetrical double-trench MOSFET. During the shoot-through, the device is operating in saturation region, so the current can be represented in equation

$$I_{Sat} = \frac{Z_{CH}\mu_n C_{OX}}{L_{CH}}(V_{GS} - V_{TH})^2 \tag{1}$$

Where Z_{CH} and L_{CH} are channel width and length respectively, μ_n is channel carrier mobility and C_{OX} is specific capacitance of gate oxide.

From the equation, higher induced gate voltage (V_{GS}) would make the term $(V_{GS} - V_{TH})^2$ less sensitive to the change of threshold (V_{TH}) and thus the shoot-through current. From comparison for three DUTs in terms of transient induced gate voltage, symmetrical and asymmetrical double-trench MOSFET show higher induced gate voltage than planar, as plotted in Fig. 9. This explains why shoot-through is nearly unchanged at increasing time of PBTI for symmetrical double-trench MOSFET, and the slightly lowered peak shoot-through could be attributed to mobility degradation. In the NBTI case, planar MOSFET shows different feature in threshold drift from the other two double-trench MOSFET. The planar MOSFET has a more steady change in threshold at increase of stressing time but the other two double-trench MOSFET has a much mild slope despite the huge drift at the 0.01 sec stressing time. This indicates that the most of traps in the two double-trench DUTs have low emission time constant. As for the shoot-through current, the planar MOSFET still shows the corresponding change to threshold drift but the other two double-trench DUTs maintains constant. However, compared with PBTI case, the planar in NBTI has less percentage change of shoot-through with more severe threshold drift, which could be a consequence of mobility degradation.

III. Experiment on Accelerated DC Stressing

In this section, the three DUTs are placed under high gate voltage above recommended rating for accelerated stressing both positively and negatively. The experiment procedure is demonstrated in Fig. 10. It follows a measure-stress-measure sequence [15]. Threshold voltage is defined at the 1 mA of drain current from sweeping gate voltage on ohmic region.

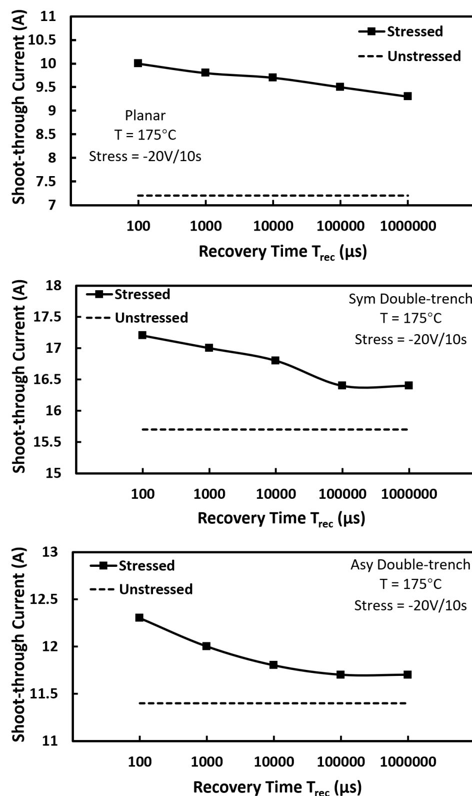

Fig. 6. Peak shoot-through current for three DUTs under NBTI at increase of recovery time under 175°C.

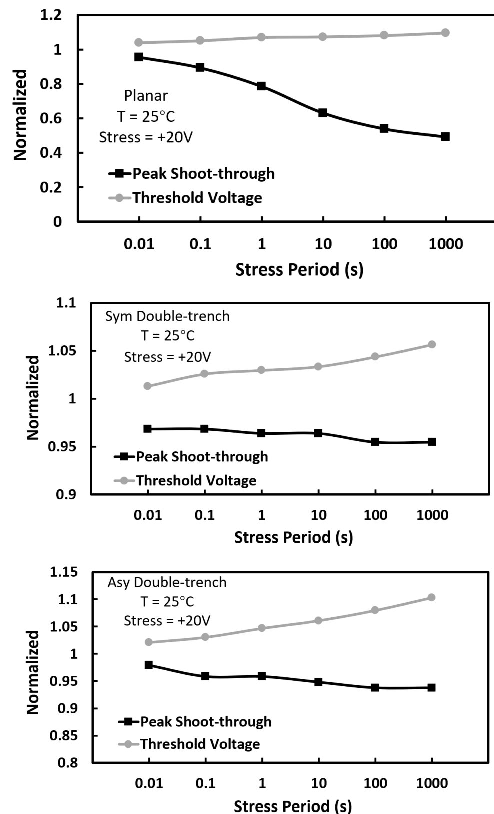

Fig. 7. Normalized threshold and peak shoot-through current for three DUTs under PBTI at increase of stressing time under 25°C.

Fig. 11 shows the how I-V curve changes with stressing time at 25°C and 175°C under +36 V gate stress. Fig. 12 shows the DUTs' threshold voltage under +36 V gate stressing at temperature from 25°C to 175°C. It can be seen that there is an increasing trend of threshold voltage drift with temperature rise which is in line with the theory that more traps generation incurs more drift [16]. Another observation is the turn-around effect on the planar MOSFET when the temperature is 25°C. The sweeping curve exhibiting the turn-around effect is shown in Fig. 13 The turn-around effect has been reported in literature due to positive trapped charges in the oxide when there is high gate voltage applied, inducing high electric field [17]. To capture more details of this phenomenon, the stressing time for the planar MOSFET is extended to 5000 sec. The commonly observed turn-around effect occurs at the beginning of stress, which is different in this case. It can also be seen that as the temperature rises, the turn-around effect no longer appears on the planar MOSFET. One feature that makes difference between the planar device and the other two double-trench devices is the gradient of the curve. The two double-trench devices show consistent linearity while planar has more gentle sloping at early stressing phase and much sharper at long stressing time. This indicates that electron capture time constant is uniformly distributed in the two double-trench MOSFETs but more concentrated on high values in planar MOSFET, which could be due to more traps are located deep inside the oxide. With the rise of temperature, such characteristic of curve gradient still retained which means that the temperature change does not alter the electron capture time constant distribution.

Fig. 14 shows the how I-V curve changes with stressing time at 25°C and 175°C under −36 V gate stress. Fig. 15 shows the DUTs' threshold voltage under −36 V gate stressing at temperature from 25°C to 175°C. The magnitude of drift increases steadily with the stressing time. In the planar MOSFET, the curve of threshold drift does not extend to the maximum 1000 sec stressing time because before that, the threshold drops to negative and the device performs as normally-on, as shown in Fig. 16. With the temperature rise, the stressing time required for the planar device to enter normally-on state becomes less as a consequence of both threshold voltage lowering and more trap generation for more threshold drift at high temperature. The symmetrical double-trench MOSFET shows milder variation of threshold drift with respect to stressing time followed by more intense change, which demonstrates that the more traps have high hole capture time constant. The knee point of threshold drift appears at shorter stressing time as the temperature increase, indicating that higher temperature brings down the traps' hole capture time constant. In the asymmetrical double-trench MOSFET, the threshold drift happens at the shortest stressing time applied and barely varies at further increase of stressing time, also, the induced

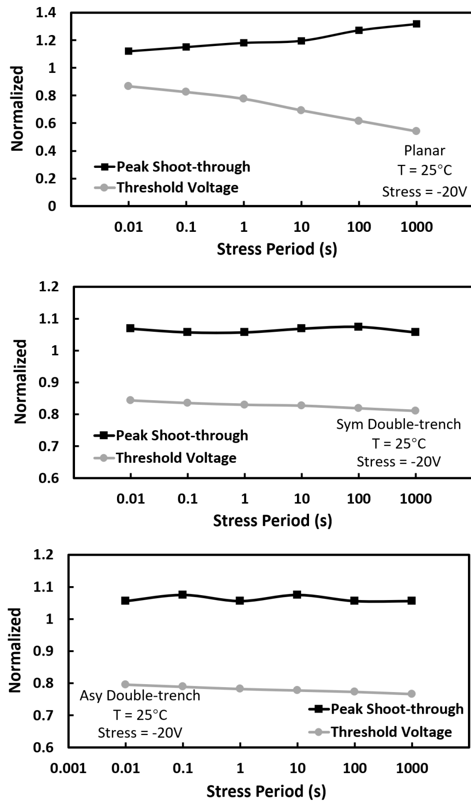

Fig. 8. Normalized threshold and peak shoot-through current for three DUTs under NBTI at increase of stressing time under 25°C.

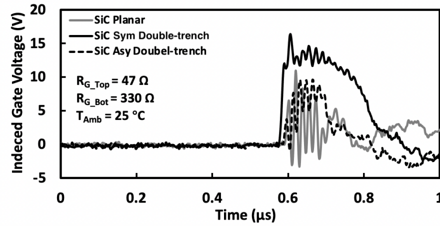

Fig. 9. Comparison of induced gate voltage transient waveforms at crosstalk.

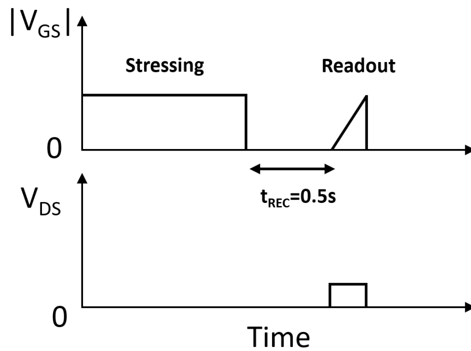

Fig. 10. Experiment procedure of DC gate stressing.

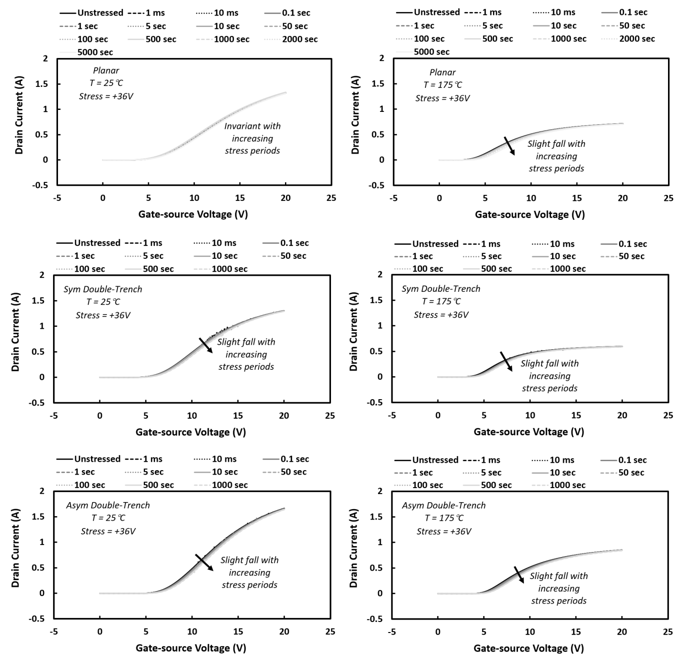

Fig. 11. Sweeping IV curve of the Planar, Symmetrical Double-trench, and Asymmetrical Double-trench SiC MOSFETs under +36V DC gate stressing at 25°C and 175°C.

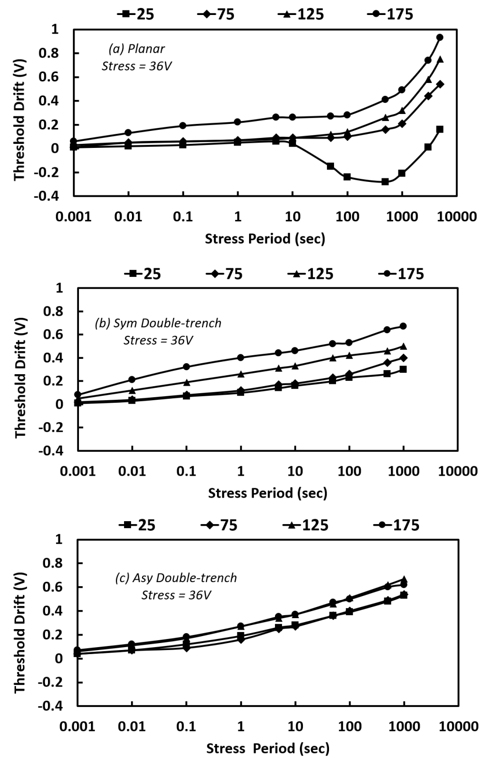

Fig. 12. Threshold voltage drift of DUTs under 36V DC gate stressing from 25°C to 175°C.

threshold drift is much less than the other two DUTs. The unchanged threshold drift in regard to the increasing stressing time suggests that the traps have low hole capture time constant. The temperature dependency is opposite to the planar and symmetrical double-trench MOSFET with lower threshold

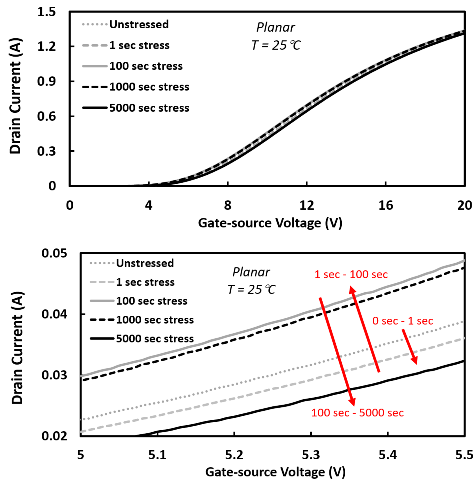

Fig. 13. Zoomed-out and zoomed-in view of the turn-around effect on SiC planar MOSFET.

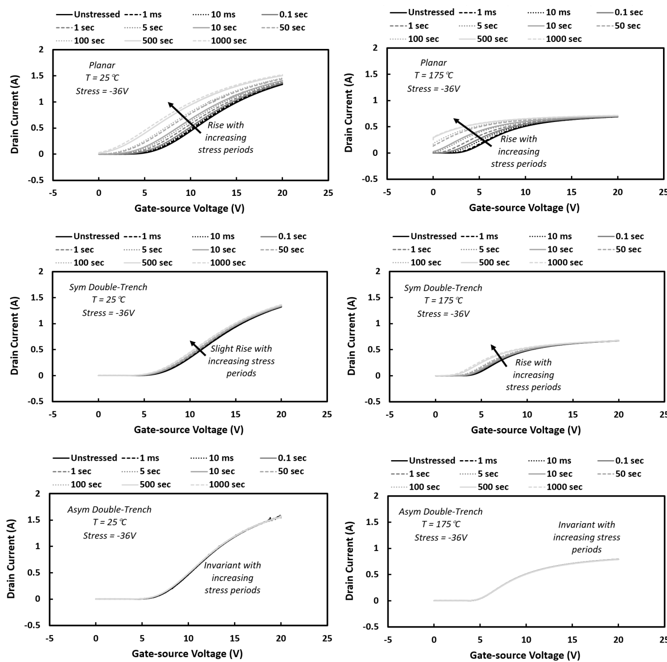

Fig. 14. Sweeping IV curve of the Planar, Symmetrical Double-trench, and Asymmetrical Double-trench SiC MOSFETs under −36 V DC gate stressing at 25°C and 175°C.

drift measured at high temperature. This has been explained by the thermally accelerated recovery happened on the delay between the stress and threshold voltage extraction. This is the reason that threshold drift at different extraction speed after stressing would yield opposite temperature dependency [18].

As the negative stressing voltage is pushed further to −42 V, IV curve trace is shown in Fig. 17 and threshold drift is plotted in Fig. 18. It can be seen that higher stressing voltage magnitude induces more threshold drift on planar and symmetrical double-trench MOSFET. The threshold drift curve of these two DUTs terminates before stressing time reaches 1000 sec as they already turned into normally-on

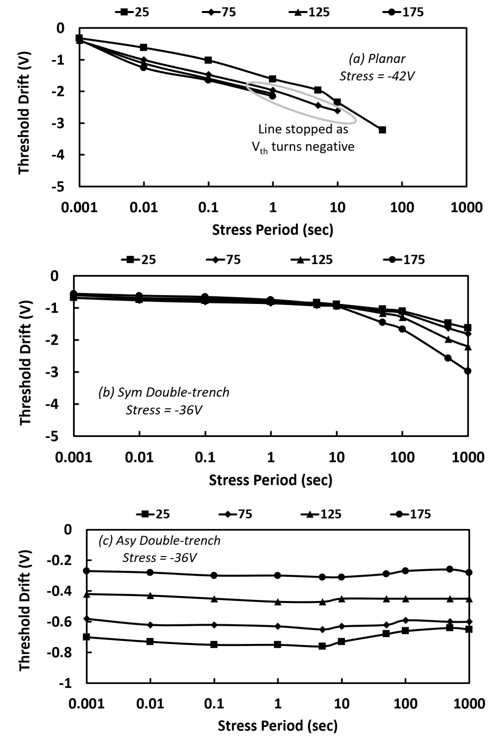

Fig. 15. Threshold voltage drift of DUTs under −36 V DC gate stressing from 25°C to 175°C.

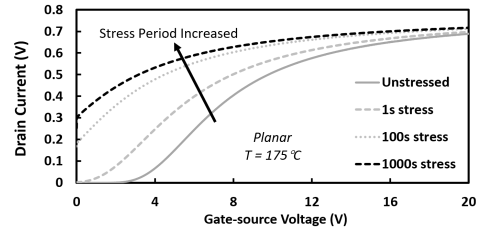

Fig. 16. Sweeping curve of threshold extraction of the Planar DUT under 175°C.

state. The impact of higher stressing voltage magnitude comes from the more significant energy band bending formed at the semiconductor-oxide interface, so traps at higher energy level is involved. However, the threshold drift measured on asymmetrical double-trench MOSFET shows little distinction from that under −36 V stressing which could indicate that few traps are located at higher energy level. The temperature dependency is preserved at the raise of stressing voltage magnitude, but the knee point on symmetrical double-trench MOSFET appears earlier that under −36 V stress, suggesting that there are more traps of low hole capture time constant under the influence of −42 V.

IV. Conclusion

In this paper, the crosstalk characteristic of SiC symmetrical and asymmetrical double-trench MOSFETs have been investigated and compared with SiC planar MOSFETs under positive and negative bias temperature instability test at a range of temperatures. It is shown that all three device structures

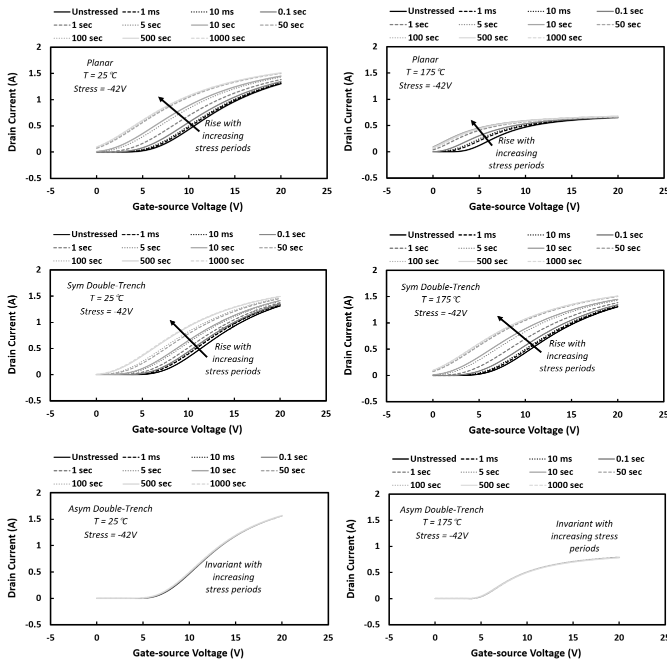

Fig. 17. Sweeping IV curve of the Planar, Symmetrical Double-trench, and Asymmetrical Double-trench SiC MOSFETs under −42 V DC gate stressing at 25°C and 175°C.

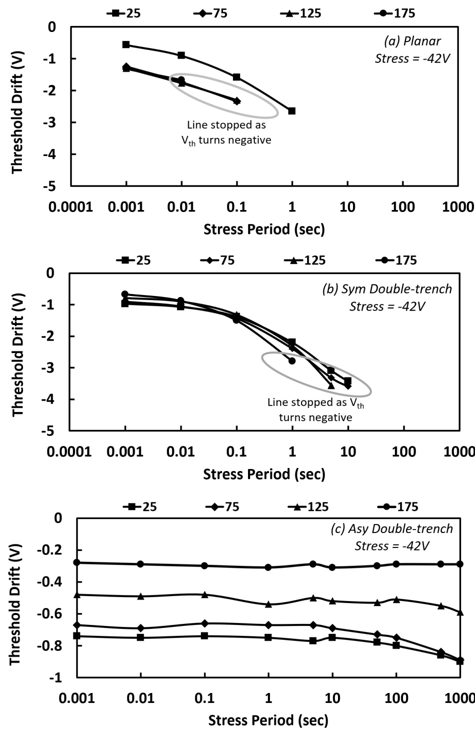

Fig. 18. Threshold voltage drift of DUTs under −42 V DC gate stressing from 25°C to 175°C.

have faster recovery in PBTI compared with NBTI for the same stressing period and magnitude. It also shows that as a result of the higher induced gate voltage in crosstalk on symmetrical and asymmetrical double-trench MOSFETs, the gate threshold voltage drift at increasing stressing time cannot be reflected on shoot-through current, while there is strong correlation between the gate threshold drift and peak shoot-through current in the planar SiC MOSFET structure. In the accelerated DC gate stressing experiment, under positive gate stressing, the rise of temperature promotes more threshold drift and turn-around effect can be seen in the selected planar MOSFET; under negative gate stressing, the planar and symmetrical double-trench MOSFET has more threshold drift with increase of temperature but the trend is opposite on asymmetrical double-trench MOSFET.

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