Unipolar and Bipolar Pulsed Gate Stresses and Threshold Voltage Shifts in GaN e-HEMTs

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***Abstract*— In GaN e-HEMTs, Threshold Voltage (V_{TH}) shift from gate voltage (V_{GS}) stress depends on the V_{GS} magnitude, stress time, recovery time (time between stress removal and V_{TH} measurement), temperature and pulse polarity (0 to + V_{GS} or - V_{GS} to + V_{GS}). In this paper, unipolar (0 to V_{GS}) and bipolar (-V_{GS} to + V_{GS}) pulsed gate stresses have been performed on GaN e-HEMTs with different V_{GS} magnitudes. The pulse frequency ranges from 25 Hz to 200 kHz. The results show negative V_{TH} shifts for unipolar V_{GS} pulses (between 5V and 8V) at long recovery times (above 500 seconds). The V_{TH} shift is proportional to the V_{GS} pulse magnitude. When the recovery time is increased from 50 milliseconds to 500 seconds, the measured V_{TH} shift becomes more negative, indicating a faster release of trapped electrons than holes. In bipolar stresses, results show both positive and negative V_{TH} shifts with no clear magnitude or frequency dependencies.**

Keywords—GaN HEMTs, Gate Stress, Threshold Voltage Stability

I. INTRODUCTION

Threshold voltage (V_{TH}) shift in GaN HEMTs is more complicated than that in traditional silicon and SiC devices with traditional MOS interfaces. This is due to the fact that devices with MOS gates do not have hetero-junctions, hence, threshold voltage shift is due to charge trapping in the gate dielectric and in the semiconductor-to-dielectric interface [1-4]. Hence, positive gate voltage (V_{GS}) stress in MOS gates results in negative charge trapping and positive V_{TH} shifting. Likewise, negative V_{GS} stress leads to positive charge trapping in the dielectric interface thereby leading to a negative V_{TH} shift. However, commercially available normally-OFF Schottky-Gated GaN HEMTs comprise of metal, p-GaN layer, AlGaN layer, GaN buffer layer all on a multi-layer substrate on silicon as shown below in Fig. 1. This figure shows that when the gate of the device is subjected to a positive voltage, electron injection into the p-GaN layer and hole injection into the AlGaN layer can occur with opposing effects on threshold voltage shifting. This means both positive and negative charge trapping can occur at the different interfaces of the complicated multi-layer GaN structure [5-11].

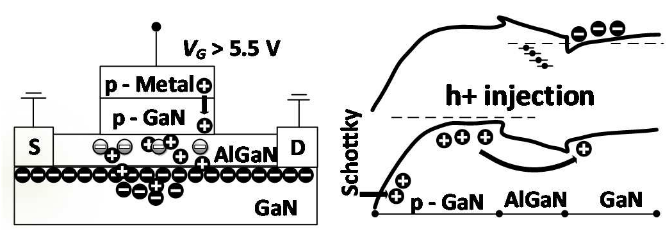

Fig. 1. Schematic picture of GaN HEMT and band diagram of the gate system

In [12], positive V_{GS} stress resulted in positive V_{TH} shift when the V_{TH} measurement was performed 50 µs after stress removal. The reason for the positive V_{TH} shift was stated to be electron injection from the AlGaN/GaN 2DEG channel and subsequent trapping in the p-GaN layer. However, in [13], measurements showed that negative V_{TH} shift resulted from positive V_{GS} stress (V_{GS} =5V) at low temperatures with the V_{TH} shift becoming positive as the temperature increased. At low V_{GS} stress (2V), the shift was positive. The positive V_{TH} shift was attributed to the electron trapping at the AlGaN/GaN interface while the negative V_{TH} shift was attributed to hole trapping at the p-GaN/AlGaN

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interface. Gate voltage stress measurements were performed on 650 V p-GaN HEMTs in [14] and subsequent gate transfer characteristic measurements showed a positive V_{TH} shift due to electron trapping in the p-GaN layer. The time constant for the electron trapping and de-trapping was estimated to be 0.1ms and 100 ms respectively, with negative V_{TH} shift occurring at higher V_{GS} stress. However, in [15], a negative V_{TH} shift was reported from positive V_{GS} stress due to hole injection from the metal into the p-GaN gate. The recovery time was not mentioned. In [16], Ohmic and Schottky p-GaN gated GaN HEMTs were tested and simulated under positive and negative V_{GS} stress and V_{TH} was measured using double-pulse measurements. The results showed that the polarity of the V_{TH} shift depended on the leakage currents of the Schottky contact. Measurements of V_{TH} instability using the third quadrant forward voltage as a technique were introduced in [17, 18]. The measurement results showed an initial positive V_{TH} shift for positive V_{GS} stress at high voltages however as the recovery time was increased, the V_{TH} shift became negative. Hence, it is clear that the V_{TH} shift in GaN is more complicated since it depends on V_{GS} stress time, magnitude, temperature and recovery time.

In this paper, the impact of the V_{GS} stress voltage magnitude, V_{GS} pulse frequency, polarity of V_{GS} turn-OFF value and the role of preconditioning on the measured V_{TH} in GaN HEMTs is experimentally evaluated. Section II describes the experimental setup, section III discusses the results and section IV concludes the paper.

II. Experimental Setup

In this paper, V_{GS} stress and V_{TH} measurement is performed using a Source-Measurement-Unit (SMU) from Keithley model 2602B. By using a relay and programming the SMU using Labview, the configuration of the circuit can change from stress mode to measurement mode. Fig. 2(a). shows a circuit schematic of the measurement system in stress mode while Fig. 2(b). shows the schematic in measurement mode. In stress mode, the gate driver applies the stress voltage onto the DUT with the drain-source terminals of the DUT shorted. The V_{TH} is measured by shorting the gate and drain terminals and measuring the voltage drop across the drain-source while a current of 1mA is forced through the device. The picture of the set-up is shown in Fig. 2(c). where the gate driver board is shown alongside the DUT, the national instrument controller and the relays used to switch between V_{GS} stress mode and V_{TH} measurement mode. The recovery time (time between V_{GS} stress and V_{TH} measurement) is set by the SMU. Fig. 2(d). shows the entire test set-up including the SMU, the test PCB, gate driver, electric heater (for setting junction temperature) etc.

The device under test (DUT) is a 650 V enhancement mode GaN HEMT from GaN Systems with datasheet reference GS66508T. The device was mounted and soldered onto a custom designed interface board for interfacing with the SMU.

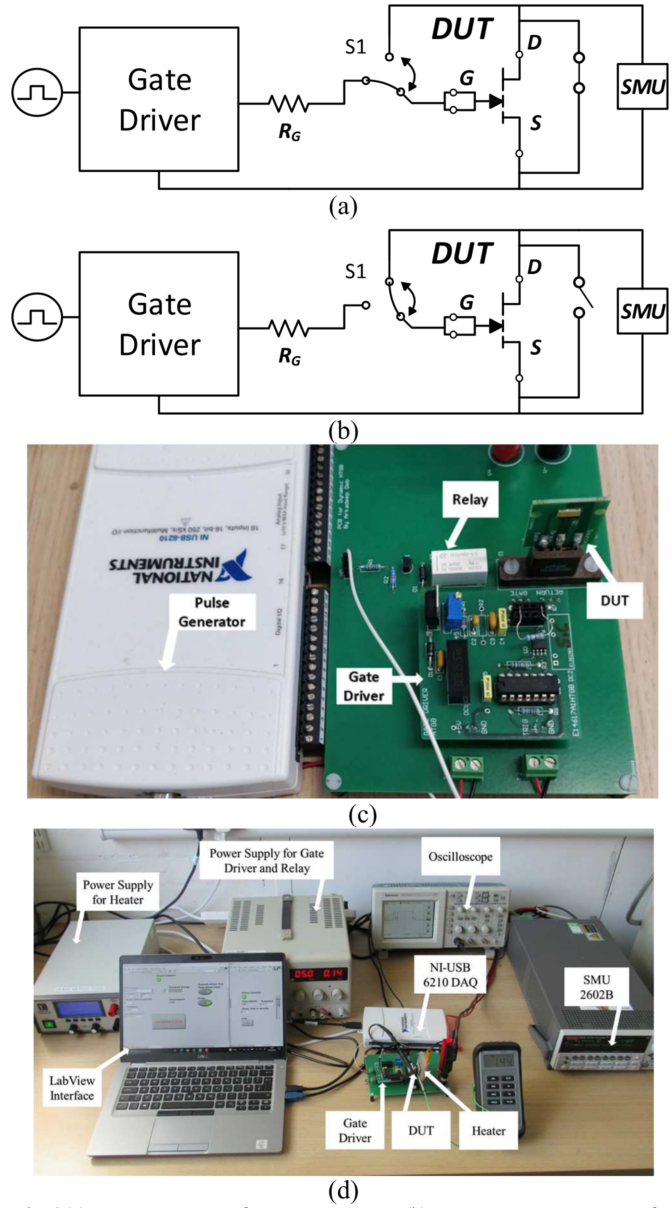


Fig. 2(a). V_{GS} stress set-up for GaN e-HEMTs (b). V_{TH} measurement set-up for GaN e-HEMTs (c). Gate driver board and Controller for HTGB Test of GaN e-HEMTs (d). Test set-up for HTGB test on GaN e-HEMTs

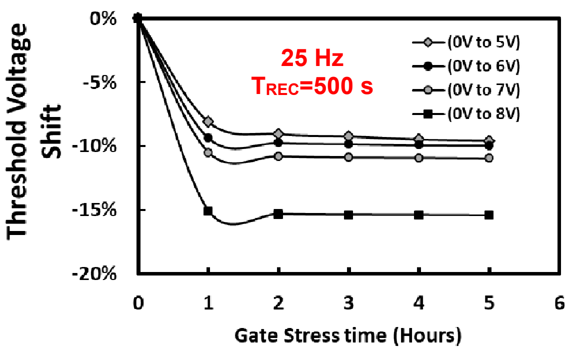
III. Experimental Results

A. Impact of Stress Voltage (Low Frequency Pulses)

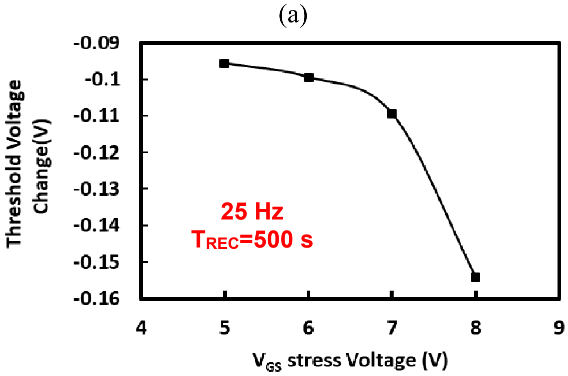
Fig. 3(a). shows results of the measured V_{TH} shift against V_{GS} stress pulse measurements. The pulses are deployed with a frequency of 25 Hz. Fig. 3(a) shows the results of V_{TH} measurements for unipolar stresses at different V_{GS} ranging from 5 V to 8 V. It should be noted that these measurements were performed with long recovery times (over 600 seconds). Negative V_{TH} shift has been attributed to electron trapping in the p-GaN buffer layer from the 2-dimensional electron gas (2DEG) formed between the AlGaN layer and the GaN buffer layer. The relationship between the absolute value of the V_{TH} shift and V_{GS} stress magnitude (for the stated recovery time and voltage range) follows the relation shown in Fig. 2(b) and given by Equation (1) below.

$$V_{TH} = 0.0823V_{GS}^2 - 0.477V_{GS} + 0.826 \quad (1)$$

Fig. 4. shows results of V_{TH} shift measurements from bipolar V_{GS} stress pulses. The results show a positive V_{TH} shift for bipolar V_{GS} pulses with amplitudes of 5 V and 6 V while showing a negative V_{TH} shift for V_{GS} pulses with amplitudes of 7 V and 8 V. Similar to the previous measurements, the recovery time was long (over 500 seconds). The positive V_{TH} shift for 5 V and 6 V bipolar stresses indicates that electron trapping in the p-GaN gate buffer from the 2-DEG dominates the hole injection in the AlGaN layer from the p+ GaN gate. As the amplitude of the bipolar V_{GS} pulse is increased to 7 V and 8 V, the negative V_{TH} shift indicates vice versa.



(a)



(b)

Fig. 3(a). V_{TH} change vs time for unipolar V_{GS} pulsed stress with T_{REC} = 500 s (b). Threshold voltage change vs V_{GS} stress voltage

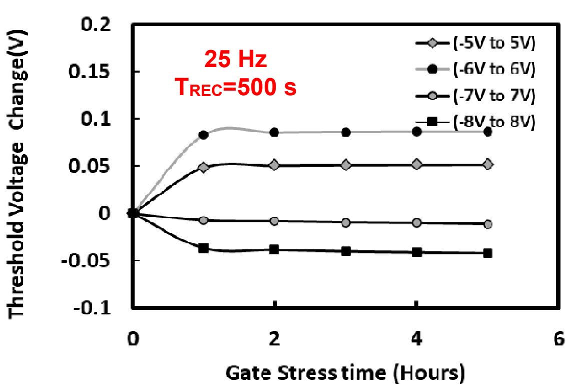


Fig. 4. Threshold voltage change vs pulse number for bipolar V_{GS} pulsed stress T_{REC} = 500 seconds

The measurements in Fig. 4. can also mean that at lower bipolar V_{GS} pulses (5 V and 6 V) trapped holes are more readily released than trapped electrons over long recovery times leading to a net positive shift in V_{TH}. As the magnitude of the bipolar V_{GS} pulse is increased (7 V and 8 V), the reverse is the case.

B. *Impact of Stress Voltage (High Frequency Pulses)*

The impact of the stress voltage on V_{TH} shifting in GaN e-HEMTs has been investigated by applying a 50 kHz V_{GS} pulse with the V_{GS} magnitude varied from 5.5 V to 8 V. The V_{TH} has been measured 50 milliseconds and 500 seconds after stress removal. Fig. 5. shows the pulse sequence, which includes a preconditioning pulse, a pre-test measurement of V_{TH}, a V_{GS} pulse train of defined magnitude, frequency and duty cycle followed by a post-test measurement of V_{TH}.

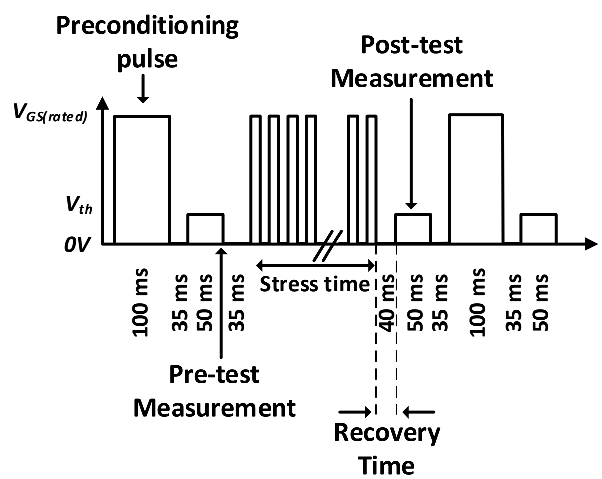
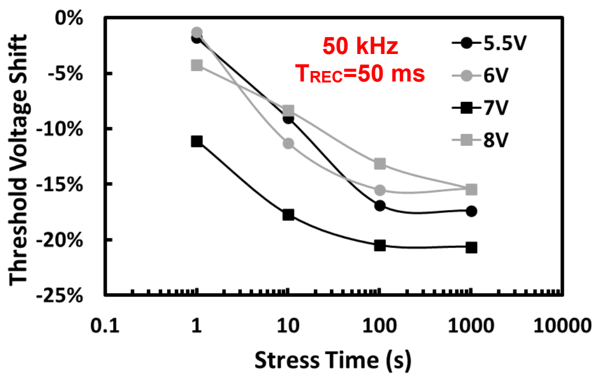


Fig. 5. Pulse sequence for Gate stressing testing at high switching frequencies.

Fig. 6(a). shows the measured V_{TH} with a recovery time of 50 milliseconds while Fig. 6(b). shows that for 500 seconds. The results show a negative V_{TH} shift for pulsed V_{GS} stress at both short (50 milliseconds) and long (500 seconds) recovery times. The measurements in Fig. 6(a). and Fig. 6(b). shows a more negative shift in V_{TH} after a longer recovery time. This agrees with measurements in [17] which show that V_{TH} shift in GaN e-HEMTs subjected to positive V_{GS} stress are initially positive at short recovery times and subsequently become more negative as the recovery time increases. Additionally, [17] also showed the impact of the stress time on the measured peak shift when the device was stressed using a gate voltage of 5.5 V, positive for short stress times and becoming negative as the stress time was increased.



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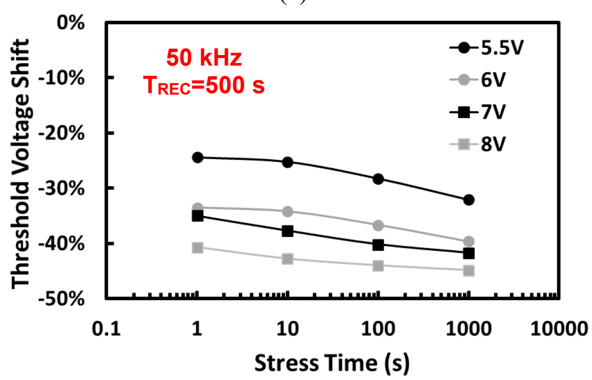

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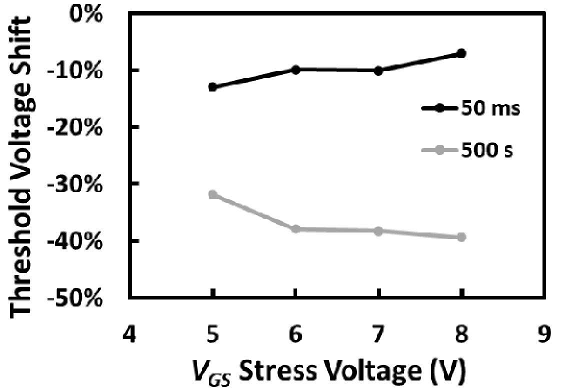


(c)

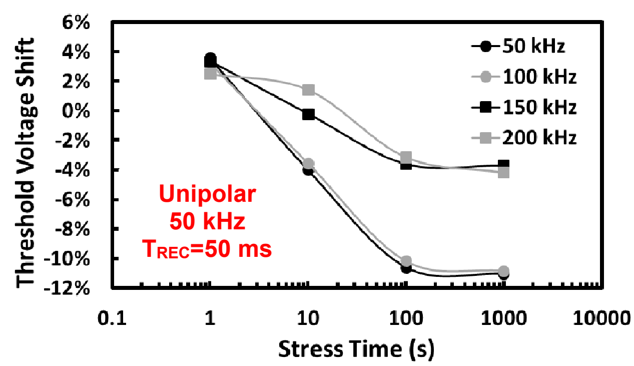
Fig. 6. V_{TH} shift vs time for 50 kHz unipolar V_{GS} pulsed stress (a) Recovery time 50 milliseconds, (b) Recovery time 500 seconds (c) V_{TH} shift as function of stress voltage (1000 seconds pulsed V_{GS} stress – Recovery time 50 millisecond 500 seconds)

Unlike SiC MOSFETs where a positive V_{GS} stress causes V_{TH} to increase because of negative charge trapping, in GaN e-HEMTs, the V_{TH} shift can be positive or negative depending on the V_{GS} stress magnitude and recovery time. The explanation for this is that a positive V_{GS} stress simultaneously causes electron injection into the p-GaN buffer layer (which causes V_{TH} increase) and hole injection into the AlGaN/GaN interface (which causes V_{TH} decrease). Since both these negative and positive charges are released over time, the net movement of V_{TH} will be negative if the electrons are released faster than the holes and positive if holes are released faster than electrons. Also observable in Fig. 6(a). and 6(b). is that fact that the magnitude of the V_{TH} negative shift is directly proportional to the V_{GS} stress at 500 seconds recovery time. However, at 50 milliseconds recovery time, there is no clear trend. This is because there is very significant charge dynamics and the V_{TH} is in transition at this time, hence, the measured V_{TH} is highly unstable.

Fig. 6(c). shows the V_{TH} shift as a function of V_{GS} stress after 1000 seconds for both 50 milliseconds and 500 seconds recovery time. It is clear from Fig. 6(c)., that the magnitude of the measured V_{TH} shifts increases with the recovery time. Also, the magnitude of the V_{TH} shifts decreases with the V_{GS} stress voltage at short recovery times and increases with stress voltage at long recovery times.

C. *Impact of Pulsed Stress Frequency*

Experimental measurements were performed with high frequency V_{GS} stress pulses ranging from 50 kHz to 200 kHz. These pulses were applied with a custom-made gate driver and were done for unipolar stress pulses (0 V to 5.5 V) and bipolar stress pulses (-3 V to 5.5 V). In these measurements, preconditioning was performed on the devices before each pulse sequence. Fig. 7(a). shows test results for a pulsed unipolar V_{GS} stresses in the GaN e-HEMT.



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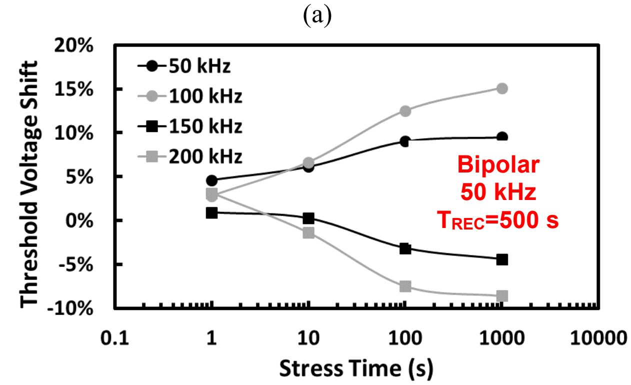


(b)

Fig. 7(a). Threshold voltage change vs stress time for unipolar V_{GS} pulsed stress T_{REC} = 50 milliseconds (b). Threshold voltage change vs stress time for bipolar V_{GS} pulsed stress T_{REC} = 50 milliseconds

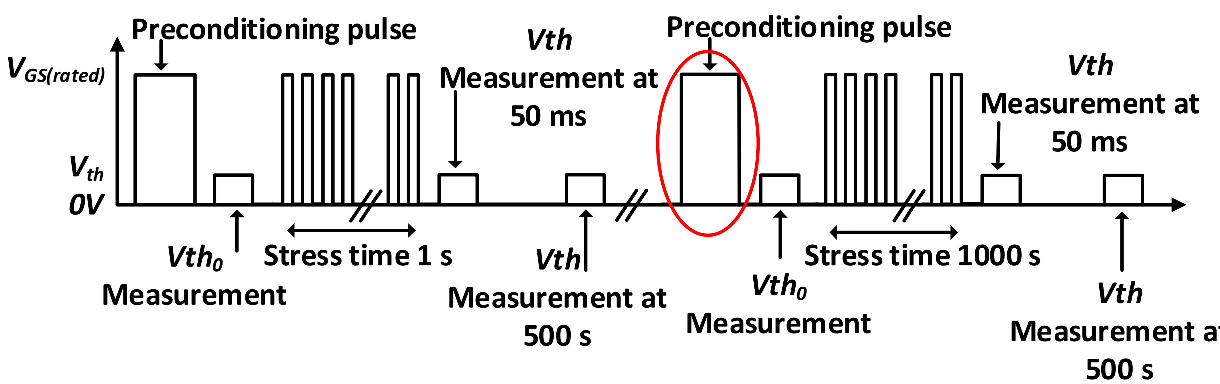
In these measurements, the recovery time (time between V_{GS} stress removal and V_{TH} measurement) was between 30 and 50 milliseconds. The results show a negative V_{TH} shift that is inversely proportional to frequency with the shifts going from 12% at 50 kHz to 4% at 200 kHz. The measurement was repeated on two additional devices and the trends were shown to be repeatable. Fig. 7(b). shows the measured V_{TH} shift for bipolar V_{GS} stress pulses. There is no clear correlation between the V_{GS} pulse frequency at the polarity and magnitude of the measured V_{TH} shift. Further measurements did not produce repeatable results. The explanation here is that the measured V_{TH} from bipolar V_{GS} pulses is highly unstable since both electron and hole injection and release is occurring, hence, for short recovery times, the highly unstable nature of the V_{TH} gives random non-repeatable results.

D. *Impact of Preconditioning*

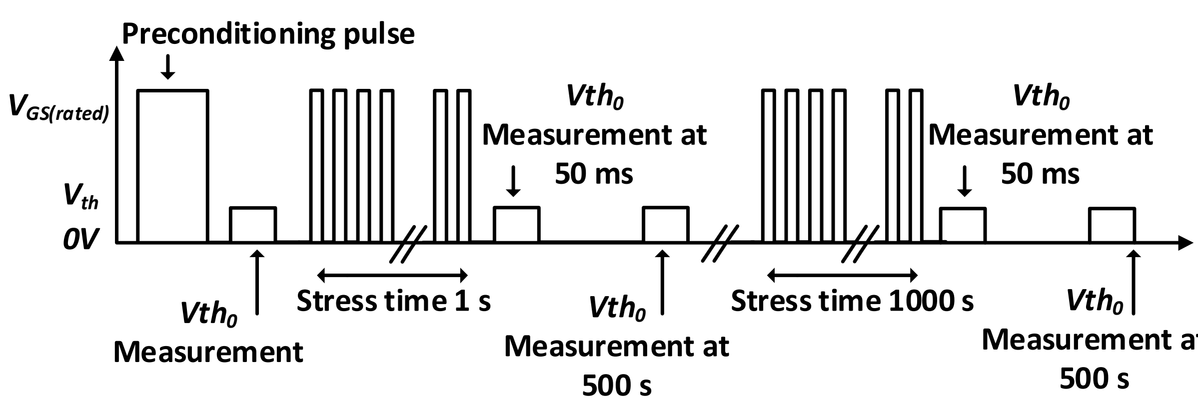
Preconditioning is a pulse applied to the gate of the DUT prior to the pre-test V_{TH} measurement. The purpose of this pulse is to define a known state of charge in the gate system of the DUT so that subsequent V_{TH} measurements performed on the DUT have a reference point i.e., it acts as a charge reset button in the gate. V_{TH} shift from V_{GS} stress comprises of both a temporary component as well as a permanent one. Preconditioning is used to remove the temporary component so that the permanent component is characterized. In this part of the paper, V_{TH} shift as a function of time for different V_{GS} stresses (5.5 V, 6 V, 7 V and 8 V) is assessed. V_{TH} is measured at different time intervals (1, 10, 100 and 1000 seconds) for the same device. In one set of measurements, preconditioning is implemented between the time intervals and in the other set of measurements, there is no preconditioning except for the first measurement. Fig. 8(a) shows the gate pulse sequence when there is preconditioning while Fig. 8(b) shows the gate pulse sequence without preconditioning. The purpose of these measurements is to determine the impact of preconditioning on the measured V_{TH} shift and to see how well preconditioning resets the V_{TH} between measurements.

Fig. 9(a). shows the pre-stress measured V_{TH} for the same device measured at different time intervals with a 5.5 V unipolar V_{GS} pulse applied at 50 kHz. Fig. 9(b). shows the same measurements however with a V_{GS} pulse magnitude of 8 V. In both measurements, the recovery time is 500 seconds, so that the temporary shifts of the V_{TH} have elapsed. In both Fig. 9(a). and Fig. 9(b)., the results show the pre-stress V_{GS} decreases when there is no preconditioning compared to when there is preconditioning. This means that preconditioning restores the pre-test V_{TH} to its original value. The result is that the measured V_{TH} shift is higher (i.e. more negative V_{TH}) when preconditioning is removed.

Fig. 10(a) shows the measured V_{TH} shift for different V_{GS} stress durations for a 50 kHz unipolar V_{GS} pulse (magnitude is 5.5 V) with and without preconditioning. Fig. 10(b) shows similar measurements for another device with a V_{GS} magnitude of 8 V.

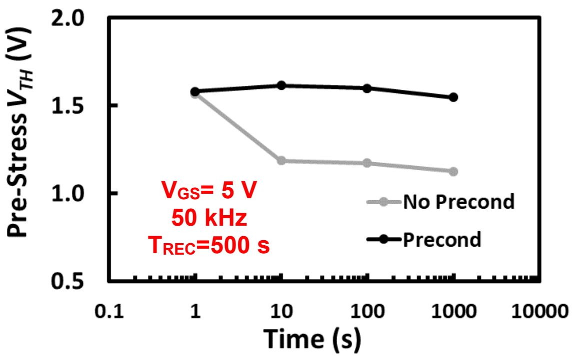


(a)



(b)

Fig. 8. V_{GS} Pulse train for gate stressing of GaN e-HEMT (a) with preconditioning and (b) without preconditioning



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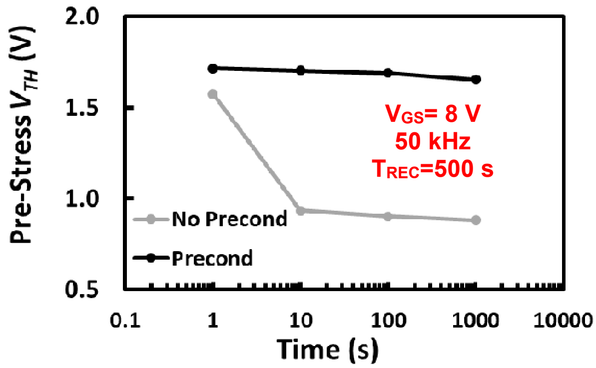
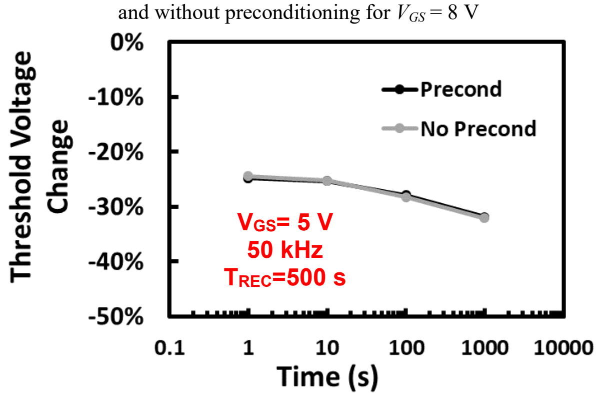
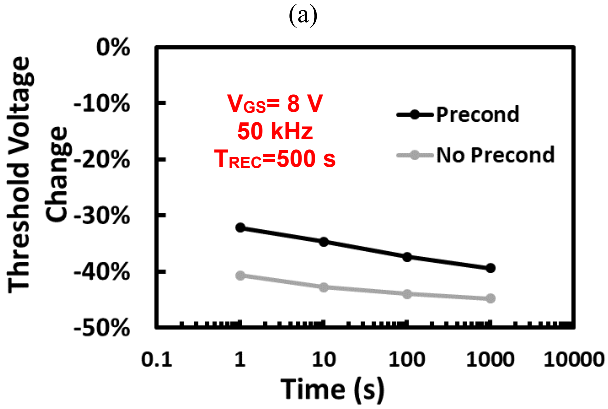


(b)

Fig. 9(a). Measured pre-stress V_{TH} comparison with and without preconditioning for V_{GS} = 5.5 V (b). Measured pre-stress V_{TH} comparison with and without preconditioning for V_{GS} = 8 V



(a)



(b)

Fig. 10(a). Measured V_{TH} change vs time for 50 kHz V_{GS} pulse with V_{GS} = 5.5 V (b). Measured V_{TH} change vs time for 50 kHz V_{GS} pulse with V_{GS} = 8 V

Comparing Fig. 10(a) and 10(b), it is clear that preconditioning does not impact the measured V_{TH} for a 5.5 V V_{GS} stress, whereas for an 8 V V_{GS} stress, preconditioning reduces the magnitude of the measured V_{TH} shift. This is because preconditioning injects electrons into the p-GaN gate buffer and causes the V_{TH} to rise to the pre-test level. Hence, when there is preconditioning, the pre-test V_{TH} is reset to the original V_{TH} at the start of the measurement sequence.

IV. Conclusions

The results in this paper show that unipolar pulsed positive V_{GS} stress results in negative V_{TH} shift in GaN e-HEMTs. When a positive V_{GS} stress voltage is applied on a GaN e-HEMT, electrons are injected into the p-GaN gate while holes are injected into the AlGaN layer. The net result of the V_{TH} shift will depend on which effect is dominant, however, positive V_{GS} stress has been shown to result in negative V_{TH} shift for unipolar V_{GS} stresses. The magnitude of the V_{TH} shift is proportional to the V_{GS} stress. As the recovery time is increased, the magnitude of the negative shift increases. This is because the release of captured electrons occurs at a faster rate compared to the release of trapped holes, thereby leading to an increasing net negative charge as time increases. The V_{TH} shift has been shown to increase with a reduction in pulse frequency for frequencies between the range of 50 kHz and 200 kHz. The measured V_{TH} shifts from bipolar V_{GS} stress pulses showed no discernible pattern with stress voltage and frequency since both positive and negative V_{TH} shift resulted for stress magnitudes between 5 V and 8 V. Measured V_{TH} shift has been shown to be higher without preconditioning compared to with preconditioning. This is because preconditioning resets the V_{TH} (increases it to the pre-test level) by injecting electrons into the p-GaN gate buffer. Assessing V_{TH} shift in GaN e-HEMTs is more complicated that SiC MOSFETs because magnitude and polarity of the V_{TH} shift depends on the magnitude of the V_{GS} stress, the polarity of the V_{GS} stress, the pulse frequency, and the recovery time.

References

[1] J. O. Gonzalez, O. Alatise, and P. Mawby, "Characterization of BTI in SiC MOSFETs Using Third Quadrant Characteristics," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 19-23 May 2019 2019, pp. 207-210, doi: 10.1109/ISPSD.2019.8757624.

[2] J. O. Gonzalez, O. Alatise, and P. Mawby, "Non-Intrusive Methodologies for Characterization of Bias Temperature Instability in SiC Power MOSFETs," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 28 April-30 May 2020 2020, pp. 1-10, doi: 10.1109/IRPS45951.2020.9129637.

[3] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability,* vol. 80, pp. 68-78, 2018/01/01/ 2018, doi: https://doi.org/10.1016/j.microrel.2017.11.020.

[4] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability," *IEEE Transactions on Electron Devices,* vol. 66, no. 11, pp. 4604-4616, 2019, doi: 10.1109/TED.2019.2938262.

[5] J. He, G. Tang, and K. J. Chen, "V_{TH} Instability of p-GaN Gate HEMTs Under Static and Dynamic Gate Stress," *IEEE Electron Device Letters,* vol. 39, no. 10, pp. 1576-1579, 2018, doi: 10.1109/LED.2018.2867938.

[6] M. Ruzzarin *et al.*, "Degradation Mechanisms of GaN HEMTs With p-Type Gate Under Forward Gate Bias Overstress," *IEEE Transactions on Electron Devices,* vol. 65, no. 7, pp. 2778-2783, 2018, doi: 10.1109/TED.2018.2836460.

[7] Y. Shi *et al.*, "Bidirectional threshold voltage shift and gate leakage in 650 V p-GaN AlGaN/GaN HEMTs: The role of electron-trapping and hole-injection," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-17 May 2018 2018, pp. 96-99, doi: 10.1109/ISPSD.2018.8393611.

[8] K. Murukesan, L. Efthymiou, and F. Udrea, "Gate stress induced threshold voltage instability and its significance for reliable threshold voltage measurement in p-GaN HEMT," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 29-31 Oct. 2019 2019, pp. 177-180, doi: 10.1109/WiPDA46397.2019.8998859.

[9] J. Wei *et al.*, "Dynamic Threshold Voltage in p-GaN Gate HEMT," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 19-23 May 2019 2019, pp. 291-294, doi: 10.1109/ISPSD.2019.8757602.

[10] K. Murukesan, L. Efthymiou, and F. Udrea, "On the Challenges of Reliable Threshold Voltage Measurement in Ohmic and Schottky Gate p-GaN HEMTs," *IEEE Journal of the Electron Devices Society,* vol. 9, pp. 831-838, 2021, doi: 10.1109/JEDS.2021.3111809.

[11] T. Oeder and M. Pfost, "Gate-Induced Threshold Voltage Instabilities in p-Gate GaN HEMTs," *IEEE Transactions on Electron Devices,* vol. 68, no. 9, pp. 4322-4328, 2021, doi: 10.1109/TED.2021.3098254.

[12] X. Tang *et al.*, "Demonstration of Electron/Hole Injections in the Gate of p-GaN/AlGaN/GaN Power Transistors and Their Effect on Device Dynamic Performance," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 19-23 May 2019 2019, pp. 415-418, doi: 10.1109/ISPSD.2019.8757614.

[13] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, "Threshold Voltage Instability Mechanisms in p-GaN Gate AlGaN/GaN HEMTs," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 19-23 May 2019 2019, pp. 287-290, doi: 10.1109/ISPSD.2019.8757667.

[14] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Mechanism of Threshold Voltage Shift in p-GaN Gate AlGaN/GaN Transistors," *IEEE Electron Device Letters,* vol. 39, no. 8, pp. 1145-1148, 2018, doi: 10.1109/LED.2018.2847669.

[15] M. Meneghini, O. Hilt, J. Wuerfl, and G. Meneghesso, "Technology and Reliability of Normally-Off GaN HEMTs with p-Type Gate," *Energies,* vol. 10, no. 2, p. 153, 2017. [Online]. Available: https://www.mdpi.com/1996-1073/10/2/153.

[16] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold Voltage Instability in p-GaN Gate AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices,* vol. 65, no. 6, pp. 2454-2460, 2018, doi: 10.1109/TED.2018.2828702.

[17] J. O. Gonzalez, B. Etoz, and O. Alatise, "Characterizing Threshold Voltage Shifts and Recovery in Schottky Gate and Ohmic Gate GaN HEMTs," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 11-15 Oct. 2020 2020, pp. 217-224, doi: 10.1109/ECCE44975.2020.9235650.

[18] J. O. Gonzalez, B. Etoz, and O. Alatise, "Gate stresses and threshold voltage instability in normally-OFF GaN HEMTs," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 7-11 Sept. 2020 2020, pp. P.1-P.10, doi: 10.23919/EPE20ECCEEurope43536.2020.9215865.