Investigation of Repetitive Short Circuit Stress as a Degradation Metric in Symmetrical and Asymmetrical Double-Trench SiC Power MOSFETs

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***Abstract*—In this paper, the reliability of planar, symmetrical, and asymmetrical SiC MOSFET is compared under repetitive short circuit shocks. Both static and dynamic parameters are tested after certain cycles to investigate the degradation pattern of the devices. It has been found out that the planar device has the highest reliability and is barely degraded for almost all parameters after 5000 cycles. The symmetrical device has the lowest reliability, which shows degradation after 50 cycles and ultimately fails after 141 cycles. The asymmetrical device shows significant degradation after 100 cycles and fails to turn-on/off after 1000 cycles. For both symmetrical and asymmetrical devices, the degradation is directly linked to the damage of the gate oxide.**

***Keywords*—Parameter Degradation, SiC MOSFET, Short Circuit Reliability Comparison**

I. Introduction

Silicon carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices have received intense attention these years and are being further exploited through the optimization of device structure. However, the improvement of the performance is in compromise with the device reliability due to more concentrated heat, especially in extreme conditions such as short circuit (SC). Typical short circuit withstand time (SCWT) is 10 μs for Silicon (Si) Insulated Gate Bipolar Transistor (IGBT), but it can be harsh for SiC MOSFET in some cases, leading to the failure or degradation of the device [1], [2].

Recent studies have provided valuable information on the SC reliability comparison of SiC MOSFET devices. For instance, the SCWT and the critical energy of SiC MOSFET with different technology and from different manufacture were compared in [3], [4]. In [5], the SC reliability of 650 V SiC planar and trench MOSFET was compared. According to the results, the trench device failed much earlier than the planar device due to higher heat density. Except from destructive tests, non-destructive experiments have also been performed. F. Boige et al. presented the degradation pattern and physical failure analysis for SiC MOSFETs from different manufacturers in [6]. Significant increase of gate leakage current (I_{gss}) and the presence of crack of the oxide were observed. The [7] applied SC stress to the 2$^{\mathrm{nd}}$ and 3$^{\mathrm{rd}}$ generation planar device for up to 700 and 1000 times, respectively. Static parameters such as threshold voltage (V_{th}), on-state resistance (R_{on}) and I_{gss} were observed to have rather significant degradation. However, none of these studies focus on the degradation of dynamic parameters, and it still lacks a qualitative reliability evaluation among devices with different structures. Thus, this paper aims to conduct repetitive SC tests on planar, symmetrical and asymmetrical SiC MOSFETs to compare their reliability and comprehensively investigate degradation of parameters, which would provide useful information for device selection and technology improvement [8]–[10].

The content of the paper is arranged as follows: Section II introduces the experimental platform and the test condition. The current and voltage waveforms for three devices before and after the SC test are compared. Section III and Section IV investigated the degradation trend and mechanism of static and dynamic parameters. Section V concludes the paper.

II. Experiment Setup

A. Experiment Setup

The devices under test (DUTs) are Rohm's planar SiC MOSFET, symmetrical SiC MOSFET, and Infineon's asymmetrical SiC MOSFET with same voltage rating and similar current rating. Detailed device parameters are shown in Table

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1, and the structures of three devices are illustrated in [11]. In repetitive SC events, the DUTs are tested at room temperature. The gate driver provides +15/-5 V voltage to safely turn on and turn off the device. The gate resistance (R_g) in SC experiment is 20Ω. The dc-link voltage is selected to be lower, which is 400 V, since the purpose is to extend the cycle to observe the degradation patterns and avoid destructive failure. The SC time is chosen to be 10 μs, the typical required time for Si IGBT [12], [13]. For each cycle, the period is set to be 5 s to enable enough time to dissipate the heat. The SC test rig is shown in Fig. 1(a), where the SC current is measured by the Rogowski coil (CWT1), and the high voltage is tested by the differential probe (GW-Instek GDP-100). The current and voltage waveforms are recorded by the Keysight MSO7104 A 1-GHz 4 GSa/s oscilloscope.

The repetitive test lasts 5000 cycles at most and stops immediately once the device fails. Typically, the static and dynamic parameters are tested right after 1, 5, 50, 500, 1000, 1500... to 5000 cycles to avoid parameters from recovery, but in order to obtain useful data, test cycles are taken smaller once obvious degradation or abnormity happens. The source measure unit (Keysight B2902A) is used to test the degradation of static parameters, as shown in Fig. 1(b). The double pulse test (DPT) rig, shown in Fig. 1(c), is used to test turn-on/off performance, through which dynamic parameters can be measured and calculated.

TABLE I
KEY PARAMETERS OF SIC MOSFETS

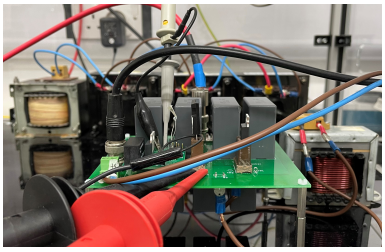
Device	SCT2160	SCT3160	IMW120R140M1H
Manufacturer	Rohm	Rohm	Infineon
Structure	Planar	Sym-DT	Asym-DT
Voltage rating (V)	1200	1200	1200
Current rating (V)	22	17	19
Die Area (mm×mm)	4.41×5.56	2.36×2.44	1.9×1.9
R_{on} (mΩ)	160	160	140
V_{th} (V)	3.23	4.13	4.23
I_{gss} (nA)	100	100	100
C_{iss} (pF)	1200	398	454
C_{oss} (pF)	45	41	25
C_{rss} (pF)	7	18	3
t_{on} (ns)	48	32	7.4
t_{off} (ns)	94	49	23.4
E_{on} (μJ)	126	62	11
E_{off} (μJ)	55	12	97

B. Experiment Results

In experiments, planar device has the highest reliability and is able to withstand 5000 times of SC shock. The symmetrical device can only withstand 141 cycles of SC events, after which three electrodes are SC together and the device performance can no longer be tested. The asymmetrical device suffers from

(a)

(b)



(c)

Fig. 1. Experiment setup (a) Short Circuit Test Rig, (b) Static Parameter Test Rig, (c) DPT Test Rig.

1000 times of SC shock and fails to turn on in the DPT. The resistance between gate and source is greatly lowered, but resistances between other electrodes remain large. The waveform of I_{ds} and V_{gs} of three devices at the initial and last cycle are compared in Fig. 2 and Fig. 3. It can be seen that the waveforms of the planar device overlap well with each other, and the device does not show any trend of degradation. For symmetrical device, I_{ds} at the last cycle exhibits large distortion, and V_{gs} is greatly lowered, indicating that there might be a fatal damage in the gate oxide that makes the device uncontrollable. With regard to the asymmetrical device, both I_{ds} and V_{gs} are reduced to some extent. The lowered input voltage reduces the actual V_{gs} applied to the device, which is responsible for higher R_{on} and lower I_{ds}.

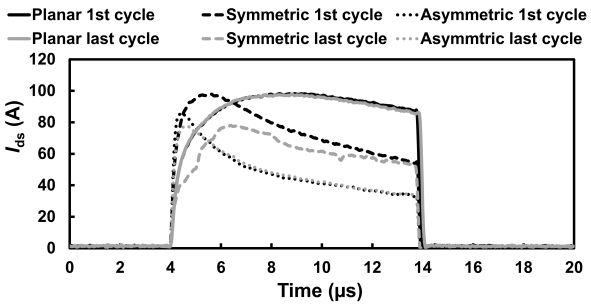


Fig. 2. SC current of three devices at the first and corresponding last cycle.

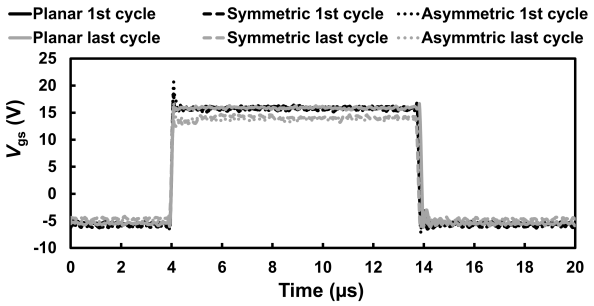


Fig. 3. Gate voltage of three devices at the first and corresponding last cycle.

As in Table I, planar device has the largest chip area, followed by symmetrical and asymmetrical device, which indicates the planar device has the best heat dissipation capability while the asymmetrical device has the worst heat transfer capability if same power are generated. In order to compare three devices in the same scale, the average SC energy (E_{sc}) density is calculated by dividing the SC energy by the chip area. The comparison of the results is shown in Fig. 4, where the planar device has the least energy density, and the value for asymmetrical device is slightly higher than symmetrical device. Thus, it can be inferred that the significantly lowered energy density of planar device contributes to higher reliability. However, the reduced test cycles of symmetrical device compared with asymmetrical device may not be related to the chip area. One assumption is that the reliability of the gate oxide for symmetrical device is worse than asymmetrical device.

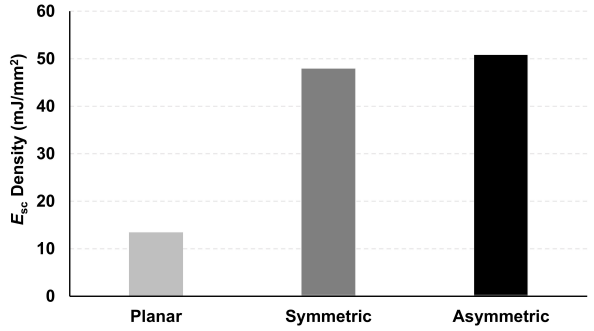


Fig. 4. SC energy density comparison of three devices at the first cycle.

III. Degradation of Static Parameters

A. V_{th}

In experiment, V_{th} is tested under the condition of V_{ds}= 0 V, I_{ds}= 2.5 mA. As can be seen in Fig. 5, the V_{th} of planar device roughly maintains stable at 3.2-3.3 V, which indicates that there no degradation in the gate oxide. There is a minor voltage drop for symmetrical device (from 4.93 V at the first cycle to 4.73 V before failure), which implies that positive charges might be trapped in the oxide [14]. According to [15], the holes come from the impact ionization in the drift region, and due to the influence of low gate voltage and drain voltage, the direction of the combined electric field injects the holes into the trench corner. With regard to asymmetrical device, V_{th} falls sharply from 4.73 V to 3.96 V at the first 100 cycles, where the gate oxide is gradually degraded similar to symmetric device, but it is still intact. Henceforth, the V_{th} rises and reaches 4.23 V at the end and the gate oxide is irreversibly damaged.

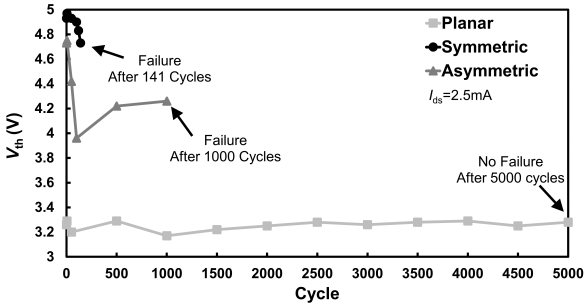


Fig. 5. Variation of V_{th} of three SiC MOSFET.

B. R_{on}

R_{on} is contributed by different parts in SiC MOSFET. At low V_{gs}, the channel resistance (R_{ch}) accounts for the majority of the resistance, while the drift region resistance (R_{drift}) predominates at high V_{gs}. Thus, it is necessary to measure R_{on} under different voltage to locate the degraded part.

According to Fig. 6(a), the R_{on} of planar device only has little variation and shows no degradation at 10 V V_{gs}. R_{on} of symmetrical device fluctuates around 540 Ω at the first 100 cycles. Then, it decreases and reaches to 510 Ω at the last cycle. With regard to R_{on} of asymmetrical device, it decreases as the experiment proceeds, decreasing by 23.66% at the end of the test. Since R_{ch} increases as V_{th} decreases according to [16], the gradually accumulated positive charges indirectly increase the R_{on} for symmetrical and asymmetrical devices. When applied V_{gs} is elevated to 20 V, it can be seen from Fig. 6(b) that all resistances decrease. In this case, the R_{on} of planar and symmetrical devices remains stable and has little variation, which means there is no obvious degradation inside the drift region. However, the R_{on} of the asymmetrical device increases, which is different from the trend at low V_{gs}.

C. I_{gss}

I_{gss} is a direct indicator of the gate oxide quality. Although I_{gss} is 100 nA for all three devices in the datasheet, the value is quite conservative. In experiment, I_{gss} is tested three times and averaged to avoid random error at V_{gs}= 20 V, V_{ds}= 0 V for all devices. The degradation of the I_{gss} is shown in Fig. 7. For planar device, the overall trend is quite flat despite some fluctuation in the middle of the curve. Also, the order of magnitude keeps stable at negative ten ampere, which means the gate oxide of the planar device is still intact. I_{gss} for symmetrical and asymmetrical devices rises substantially after 50 cycles, indicating initial degradation has emerged and finally turns to the irreversible damage. For symmetrical device, I_{gss} rises from several nA to 46.3 mA at the 140 cycle. Then, the device cannot be turned on and all electrodes are short-circuit together. For asymmetrical device, I_{gss} rises from several nA to 99.8 mA at the 1000 cycle. Then, the device

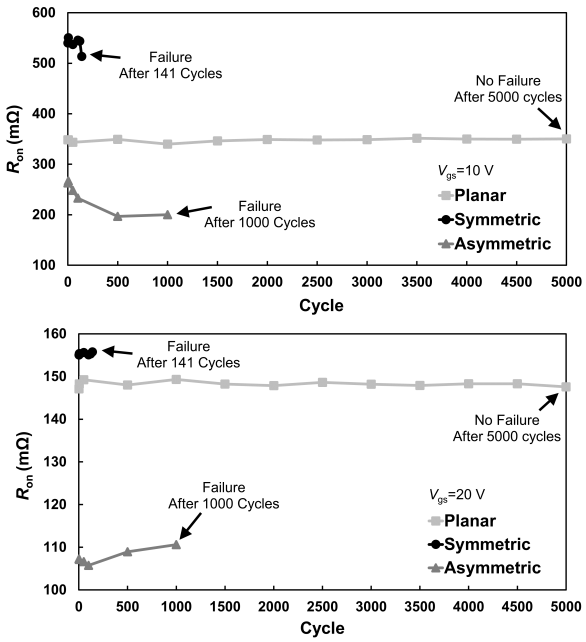


Fig. 6. Variation of R_{on} of three devices (a) at low V_{gs}, (b) at high V_{gs}.

fails in the DPT. It should be noted that since I_{gss} increases with test cycles, the voltage drop caused by the internal R_g will be increased. In this way, the effective V_{gs} applied on the die will be decreased, which explains the increased R_{on} for asymmetric device at 20 V.

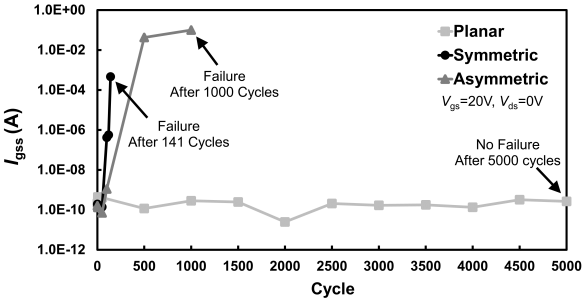


Fig. 7. Variation of I_{gss} for different SiC MOSFETs.

IV. Degradation of Dynamic Parameters

1) Current and Voltage Waveforms: In order to analyze the degradation of the dynamic parameters, DPT is carried out at V_{ds}= 400 V, I_{ds}= 12 A. The inductor in the test is 2.2 mH, and R_g is selected to be 100 Ω so that the details in the switching waveforms can be fully captured. The turn-off/on V_{ds}, I_{ds} of three devices are plotted in Fig. 8. It can be seen that the asymmetric device has the fastest switching speed, and the planar device switches the slowest. The oscillation in the turn-off period is always stronger than the turn-on period. For planar device, the turn-off oscillation increases as the experiment proceeds, but the turn-on switching waveforms seem unchanged. The asymmetric device is turned off/on in advance at 100 cycles, which is caused by the sudden decrease in V_{th} as exhibited in Fig. 5. Since then, the device oscillates with lower magnitude because of the increase in R_{on}, and the device finally fails to turn off/on after 1000 cycles.

A. t_{off} and t_{on}

t_{on} and t_{off} are key parameters that directly reflect the dynamic performance of SiC MOSFET. In experiment, t_{off} is defined as the time from 90% V_{gs} to 90% V_{ds}, and t_{on} is defined as the time from 10% V_{gs} to 10% V_{ds} [17]. The variation of t_{off} and t_{on} are plotted in Fig. 9. It can be seen that among three devices, the planar SiC MOSFET switches the slowoyejuedewest, and both t_{off} and t_{on} show little change after 5000 SC shocks. For symmetrical device, t_{off} increases slightly while t_{on} decreases slightly. This is because the decreased V_{th} makes the time longer when V_{gs} falls from high level to V_{th}, but makes it shorter when V_{gs} increases from low level to reach the V_{th}. With regard to asymmetrical device, it has the fastest turn-on speed, but its turn-off speed is relatively even with symmetrical device. t_{on} decreases and increases with V_{th}, but t_{off} barely changes. It should be noted that the asymmetrical device failed during the DPT at the 1000 cycle, so the dynamic parameters are missing.

B. *Turn-off* d*i*/d*t* *and* d*v*/d*t*

d*i*/d*t* and d*v*/d*t* for three devices show relatively large variation in Fig. 10, especially for asymmetrical devices. At first few cycles (before 50 cycles), the variation of d*i*/d*t* and d*v*/d*t* behaves normal. The relatively large variation is caused by the fast switching speed. After 50 cycles, both d*i*/d*t* and d*v*/d*t* are significantly lowered because of the damage in the oxide. For the planar device, d*i*/d*t* and d*v*/d*t* increase a little near the end of the test. For the symmetrical device, d*i*/d*t* maintains a stable value and decreases at the last cycle, but d*v*/d*t* keeps increasing after 50 cycles.

C. *Turn-on* d*i*/d*t* *and* d*v*/d*t*

Compared with turn-off d*i*/d*t* and d*v*/d*t*, the variation for turn-on d*i*/d*t* and d*v*/d*t* show less variation because of slower switching speed. The turn-on speed for planar device seems unchanged through 5000 cycles in Fig. 11, proving the high reliability of the device. For the symmetrical device, the turn-on behavior is not significantly affected. d*i*/d*t* fluctuates a little during the test and d*v*/d*t* slightly decreases after 50 cycles for symmetric device. With regard to the asymmetrical device, both d*i*/d*t* and d*v*/d*t* increases once the test begins and start to decrease after 100 cycles. It should be noted that the trend of d*i*/d*t* and d*v*/d*t* is similar to the trend of V_{th}, which implies the switching speed is strongly related to the V_{th}.

D. *Switching Energy*

The test results for three devices are plotted in Fig. 12. For the planar device, E_{off} increases because the oscillation increases as the experiment proceeds, but E_{on} barely changes because the oscillation is less in the turn-on stage. However, E_{off} and E_{on} change quite randomly, since the switching

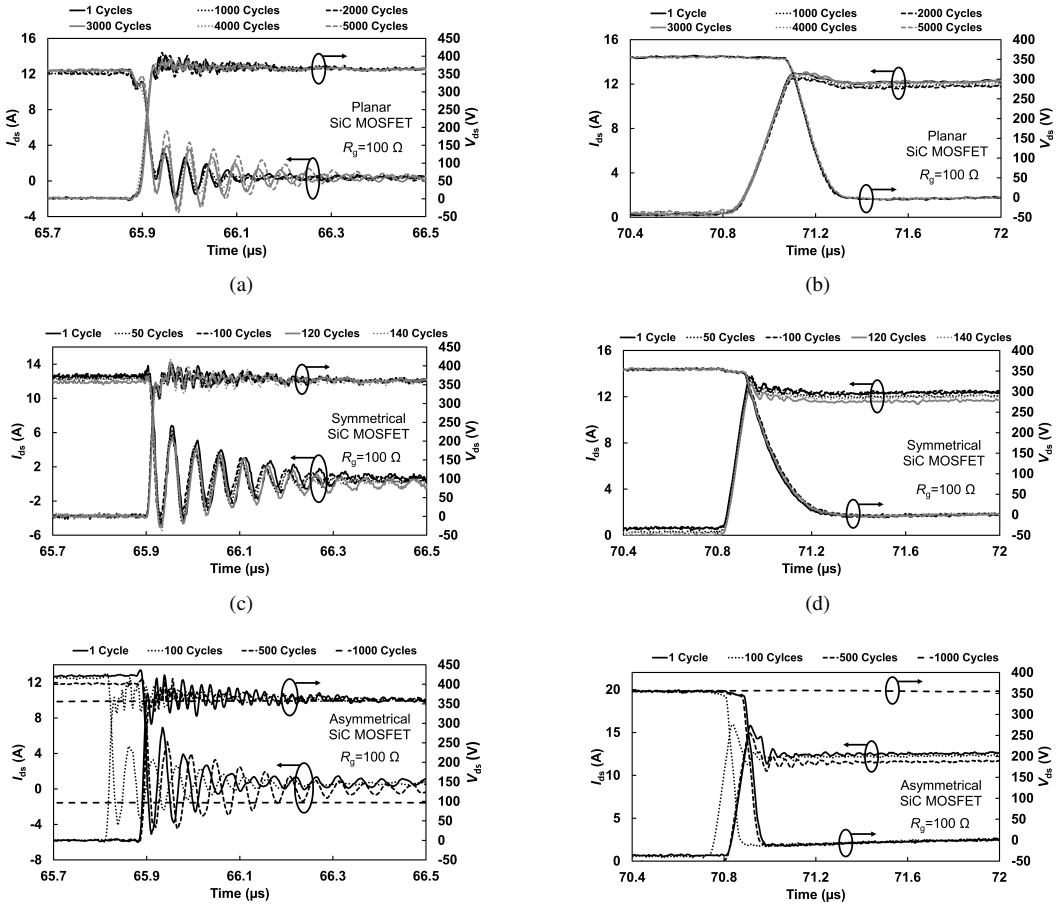


Fig. 8. Turn off and Turn on waveforms at 25 °C. (a) Turn-off waveforms of planar device, (b) Turn-on waveforms of planar device, (c) Turn-off waveforms of symmetric device, (d) Turn-on waveforms of symmetric device, (e) Turn-off waveforms of asymmetric device, (f) Turn-on waveforms of asymmetric device.

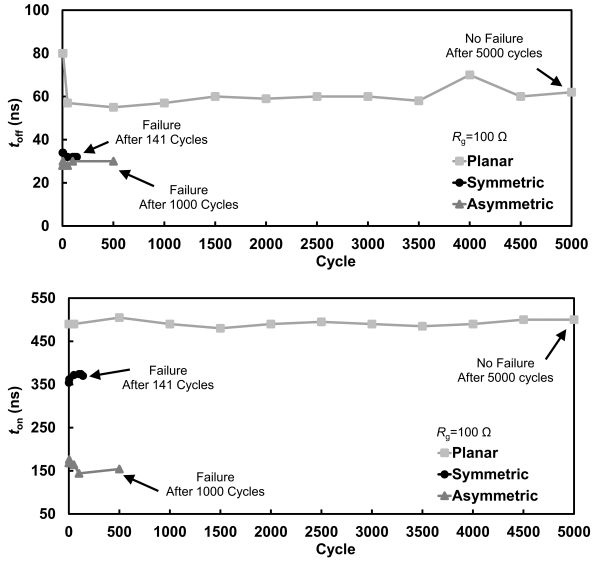


Fig. 9. Switching time at R_g = 100 Ω at (a) Turn-off, (b) Turn-on.

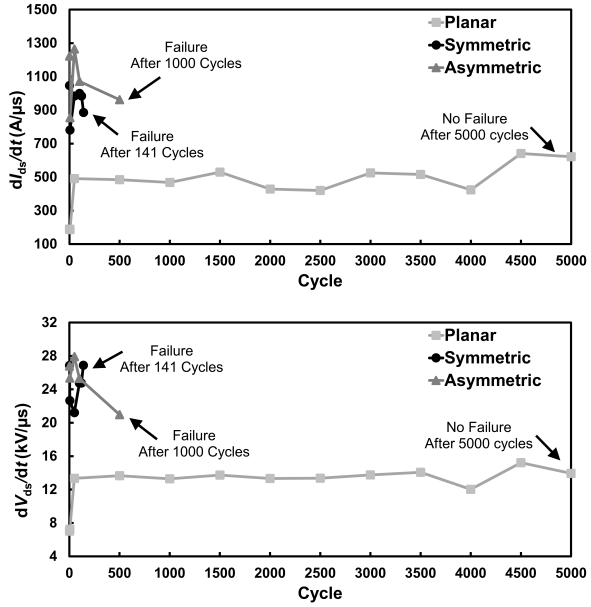


Fig. 10. Turn-off speed of three devices at R_g = 100 Ω (a) d*i*/d*t*, (b) d*v*/d*t*.

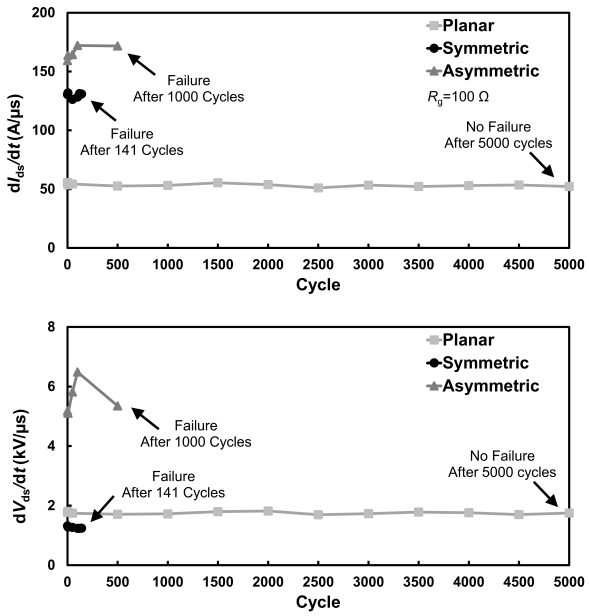


Fig. 11. Turn-on speed of three devices at R_g = 100 Ω (a) di/dt, (b) dv/dt.

energy is not only affected by the switching time, but is also influenced by the oscillation. It is hard to relate the change in switching energy to degradation of parameters.

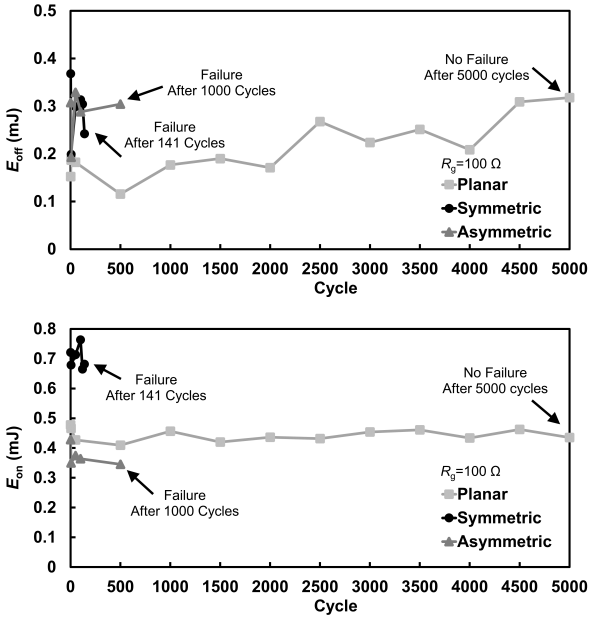


Fig. 12. Switching of three devices at R_g = 100 Ω (a) E_{off}, (b) E_{on}.

V. Conclusion

In this paper, degradation of static and dynamic parameters for planar, symmetrical and asymmetrical SiC MOSFETs after repetitive SC shocks are comprehensively investigated and compared. According to the experimental results, the planar device has the highest reliability because of the largest chip area, and almost no parameters show obvious change after 5000 cycles. The symmetrical device has the lowest reliability, which exhibits obvious degradation after 50 cycles and finally fails at 141 cycles. The asymmetrical device has average reliability and fails after 1000 cycles, but both static and dynamic degrades rapidly after 100 cycles. For both symmetric and asymmetric device, the vulnerability of the gate oxide is the root cause for parameter drift, and I_{gss} has exhibited large increase at the end of the test. Besides, the static parameters have better sensitivity in reflecting the device degradation under SC events, and dynamic parameters exhibit the degradation trend only when the device is significantly degraded. In the future, the degradation pattern of parameters for three devices will be investigated at higher dc-link voltage and elevated temperature.

References

[1] J. Wang and et al., "Short-circuit ruggedness and failure mechanisms of si/sic hybrid switch," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2771–2780, 2018.

[2] E. Bashar and et al., "Comparison of short circuit failure modes in sic planar mosfets, sic trench mosfets and sic cascode jfets," in *IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2021, pp. 384–388.

[3] Z. Wang and et al., "Temperature-dependent short-circuit capability of silicon carbide power mosfets," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1555–1566, 2015.

[4] R. Wu and et al., "Measurement and simulation of short circuit current sharing under parallel connection: Sic mosfets and sic cascode jfets," *Microelectronics Reliability*, vol. 126, p. 114271, 2021.

[5] L. Cao and et al., "Comparative evaluation of the short circuit capability of sic planar and trench power mosfet," in *IEEE 2nd International Electrical and Energy Conference (CIEEC)*, 2018, pp. 653–656.

[6] F. Boige and et al., "Gate leakage-current analysis and modelling of planar and trench power sic mosfet devices in extreme short-circuit operation," *Microelectronics Reliability*, vol. 76, pp. 532–538, 2017.

[7] J. Wang and et al., "Investigations on the short-circuit degradation and its mechanism of 1.2-kv 19-a sic power mosfets," in *IEEE 26th Int. Sym. on Physical and Failure Analysis of Integrated Circuits*, 2019, pp. 1–4.

[8] J. Yang and et al., "Impact of temperature and switching rate on properties of crosstalk on symmetrical & asymmetrical double-trench sic power mosfet," in *IECON – 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1–6.

[9] R. Wu and et al., "Current sharing of parallel sic mosfets under short circuit conditions," in *23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 2021, pp. 1–9.

[10] R. Wu and et al., "Performance of parallel connected sic mosfets under short circuits conditions," *Energies*, vol. 14, no. 20, 6834, 2021.

[11] J. Yang and et al., "Crosstalk induced shoot-through in bti-stressed symmetrical & asymmetrical double-trench sic power mosfets," *IEEE Open Journal of Industrial Electronics Society*, vol. 3, p. 188, 2022.

[12] L. Ceccarelli and et al., "A survey of sic power mosfets short-circuit robustness and failure mode analysis," *Microelectronics Reliability*, vol. 76, pp. 272–276, 2017.

[13] B. Kakarla and et al., "Short circuit ruggedness of new generation 1.2 kV SiC MOSFETs," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2018, pp. 118–124.

[14] X. Zhou and et al., "Investigations on the degradation of 1.2-kv 4h-sic mosfets under repetitive short-circuit tests," *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4346–4351, 2016.

[15] Y. Li and et al., "Gate bias dependence of v th degradation in planar and trench sic mosfets under repetitive short circuit tests," *IEEE Transactions on Electron Devices*, vol. 69, no. 5, pp. 2521–2527, 2022.

[16] J. Baliga, *Fundamental of power semiconductor device*. Springer, 2010.

[17] J. Wei and et al., "Comprehensive analysis of electrical parameters degradations for sic power mosfets under repetitive short-circuit stress," *IEEE Trans. on Electron Devices*, vol. 65, no. 12, pp. 5440–5447, 2018.