Impact of Electrothermal Bias Temperature Instability Stress on Threshold Voltage Drift of GaN Cascode Power Modules

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***Abstract*—In this digest, the threshold voltage drift of the GaN cascode power modules is analysed in comparison with similarly-rated Silicon power MOSFET modules under a range of electrothermal gate bias stress. The drift is plotted again a range of gate voltage magnitudes, applied for a verity of stress periods to comprehensively understand how the gate of the low-voltage Silicon MOSFET in the cascode structure of the GaN module would perform in comparison with a fully-rated Silicon MOSFET, and how does this impact the performance of the high voltage GaN HEMT device, enabling the cascode structure. The importance of the trapping effects on the threshold voltage instability and its drift is revealed for the two devices, with particular attention to possibility of the turn-around effect in a range of temperatures.**

***Keywords*—GaN Cascode, threshold voltage instability, gate stress, module packaging.**

I. Introduction

GaN based devices are promising power devices for the power applications due to their higher switching speed and blocking capability in comparison with traditional Silicon based power MOSFETs, albeit their lower thermal conductivity requires thorough thermal management design [1]–[4]. These devices can be separated into two groups, normally-on and -off. The normally-on devices are less preferable in current power application because of the reliability issues. To make normally off devices, some methods have been developed, those are cascode configuration, and the p-GaN gate devices, both of which are commercially available power devices. In cascode configuration, a low voltage Silicon MOSFET is connected to the depletion mode high voltage GaN HEMT [5]–[7] in series, effectively acting as the gate of the device [8].

The gate stressing test has become the significant reliability test in that the threshold voltage degradation [9], [10]. The threshold voltage drift happens under extended gate stressing. It is really demanding the understand the operation of the gate stressing in GaN cascode devices, due to fact that the multiple layers of the devices and in series with low voltage Silicon MOSFET means lots of probable locations for trapping [11]–[13]. Here, the gate of the device is biased by a DC source and detect the drift of the threshold voltage due to serious amount of charge trapping. It is already been studied that reversible threshold voltage drift under adjusted gate stressing due to the increase of the carrier trapping in the prior oxide traps [14], [15].

In this paper, measurements of the threshold voltage drift of commercially available GaN cascode modules and Silicon power MOSFETs will be carried out in off state at room and elevated temperatures. The threshold voltage drift is analyzed by adjusting stress magnitudes and periods.

II. Experimental Setup

The commercially available 600 V GaN power hybrid HEMT half bridge module (TPD3215M) and 600 V Silicon power MOSFET module (IXFN82N60P) are evaluated. The Keysight B2902A Precision Source/Measure unit is used to perform these two devices with stressing their gate terminals, then sweeping with 0.4 V drain voltage and measuring their drain currents and gate source voltages. The threshold voltage of the power modules are analysed after each stress periods from 1 ms to 1,000 sec and levels from 15 V to 45 V. The durations of the stress levels and the sweeping voltage value and its time after each stress periods are illustrated in Fig. 1. Furthermore, to analyse the impact of the 35 V stress level on drift of threshold voltage, another test has been set up to see the impact of the 35 V in details. In this test the stress duration is increased from 0 sec to 5,000 sec in steps of 1,000 sec as well as it is increased to 10,000 sec. Furthermore, the temperature also varied from 25°C to 175°C. The schematic of GaN cascode at stressing and relaxation, together with the GaN Module under test are shown in Fig. 2.

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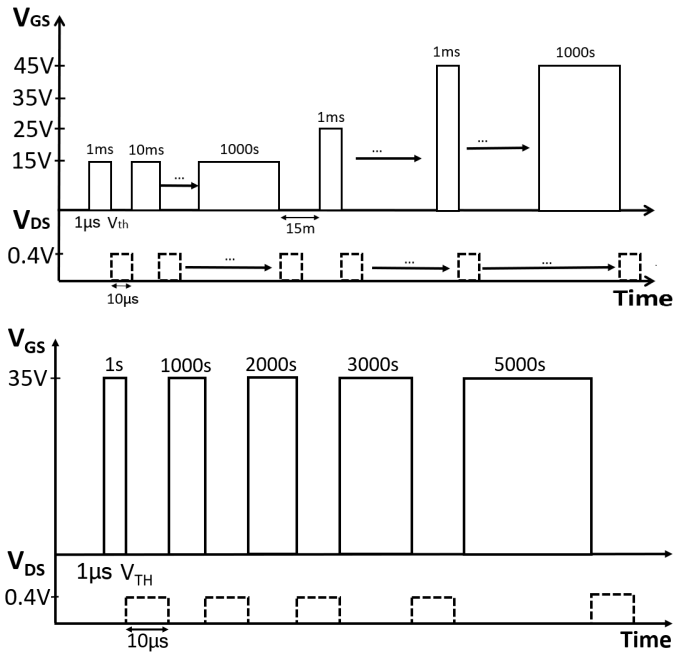

Fig. 1. The variety of stress levels applied from 0 sec to 1,000 sec with different stress levels and periods.

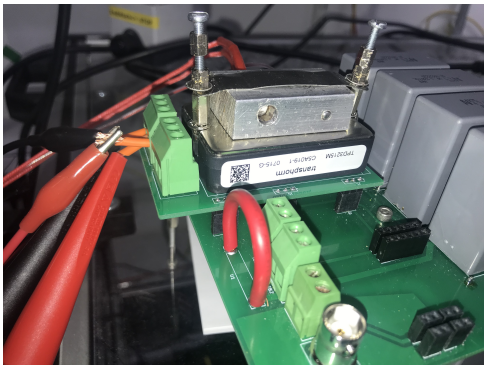

Fig. 2. Schematic of GaN cascode at stressing and relaxation, together with the GaN Module under test.

III. Results Analysis

A. Variety of stress levels and period on gate terminal

The stress voltage values are adjusted between 15 V and 45 V in steps of 10 V to see the impact of the magnitudes of the voltage stress to the gate terminal of the GaN and Silicon power modules as well as the period of the each stress level is logarithmically increased from 0 sec to 1,000 sec to observe the effect of the prolonged electrothermal stress periods.

The drain current and gate source voltage plots under 35 V and 45 V stress level with their zoomed views for GaN power module are demonstrated in Fig. 3. Moreover, it illustrates the threshold voltage drifts after each stress levels at 5 mA drain current for GaN cascode power module. As for the figures of the GaN power module, the threshold voltage drift has the most clearly seen for the 35 V stress level with approximately 0.7 V after 10 sec period, following by 0.3 V under 15 V stress level. With respect to negative threshold voltage drift in I_D-V_{GS} plots of the GaN, it is most probably related to traps that are placed in the AlGaN/GaN interface, in the buffer layer and the interface between buffer and AlGaN layer. In addition to this, the low stress level are not enough to regulate the traps in the buffer layer, indicating that gate traps are immobile.

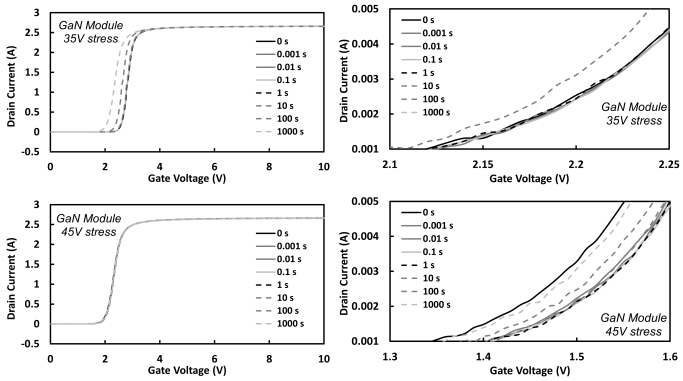

Fig. 3. Drain current against gate source voltage of 600 V GaN cascode power module under 35 V and 45 V bias from 1 ms to 1,000 sec at 25°C with the zoomed view of the same parameters between 1 mA and 5 mA.

Fig. 4 demonstrates the drain current and gate source voltage trends of Silicon power module under 35 V and 45 V stress. Additionally, it illustrates the threshold voltage drifts under all four stress levels during the period of up to 1,000 sec for Silicon power module. Regarding the effect of the stress levels and durations for the Silicon power module, the drift in threshold voltage appears to be small, even when the gate voltage magnitude is set to 45 V and the stress duration is prolonged to 1,000 sec.

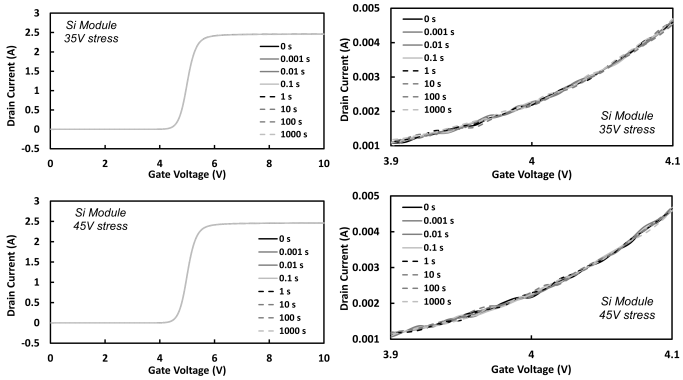

Fig. 4. Drain current against gate source voltage of the 600 V Silicon power module under 35 V and 45 V bias from 1 ms to 1,000 sec at 25°C with the zoomed view of the same parameters between 1 mA and 5 mA.

The threshold voltage drift under various stress levels and periods for GaN and Silicon power modules are demonstrated in Fig. 5. It is clearly seen that the GaN power module has more drift than the Silicon power device with 0.3 V after 1,000 sec duration of 15 V stress level while this is further increased to about 0.6 V when the stress period is increased to 35 V. The drift in the Silicon module is negligible.

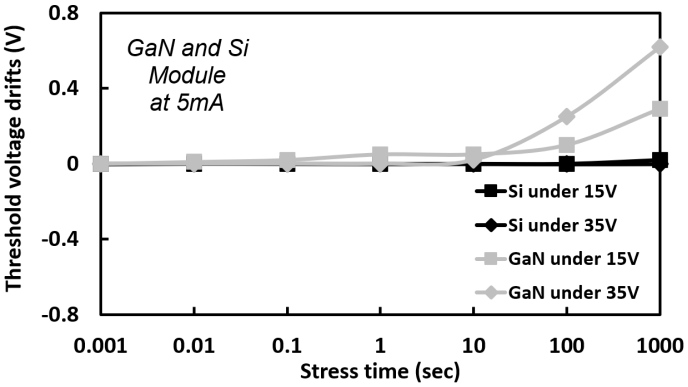

Fig. 5. The threshold voltage drifts under 15 V and 35 V stress levels at 5 mA drain current for 600 V GaN cascode and Silicon MOSFET power modules at room temperature.

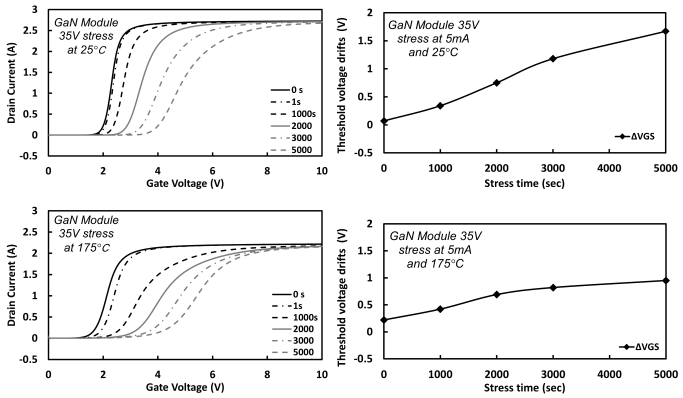

Fig. 6. The drain current against gate source voltage of the 600 V GaN cascode power module under 35 V bias with stress durations from 1 ms to 5,000 sec at 25°C and 175°C. The threshold voltage drifts at 5mA drain current for 600 V GaN cascode power module after each stress period.

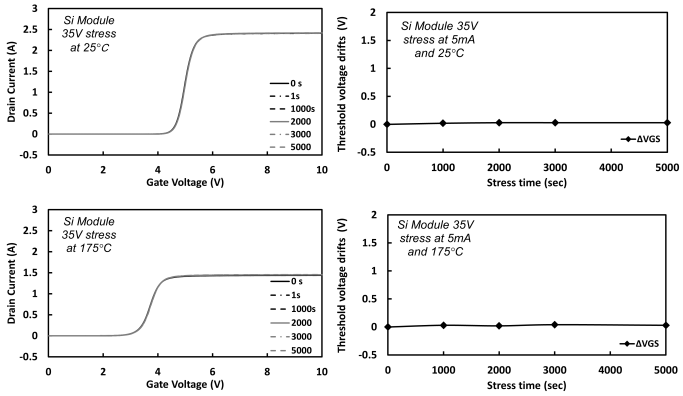

Fig. 7. The drain current against gate source voltage of the 600 V Silicon power MOSFET module under 35 V bias with stress durations from 1 ms to 5,000 sec at 25°C and 175°C. The threshold voltage drifts at 5 mA drain current for 600 V Silicon power MOSFET module after each stress period.

As it seen in previous part, when the voltage stress level is larger than 35 V, the trends of the drain current and gate source voltage graphs are drifting clearly. To evaluate the impact of this stress level have been observed under two different temperatures, 25°C and 175°C and longer stress periods from 0 sec to 5,000 sec in steps of 1,000 sec. The I_D-V_{GS} plots and the threshold voltage drifts of the GaN power module under previously described conditions are illustrated in Fig. 6. As it is obviously seen that the GaN power module has almost 1.8 V and 0.7 V drift in threshold voltage after 5,000 sec at 25°C and 175°C, respectively. Regarding to threshold voltage drift of GaN cascode power module, it is likely that the former traps locate between GaN channel and electron tunnels that leads a rise in threshold voltage drift. Moreover, the high electron density in GaN channel might cause a rise in hole density at the edges which leads a positive threshold voltage drift. Similar conditions have been set up for Silicon power module as well to make an apparent comparison between both devices. The drain current against gate source voltage and threshold voltage drift plots of Silicon power module are highlighted in Fig. 7. The threshold voltage drift is stable after 2,000 sec with 30 msV drift at room temperature, whilst it shows a little increase to 40 msV at higher temperatures.

Lastly, to clarify the difference in the I_D-V_{GS} trends and threshold voltage drifts of GaN and Silicon power modules at 25°C and 175°C are presented in Fig. 8. As obviously seen in the plots, Silicon power module has very small drift in its threshold voltage compared to GaN module.

B. Variety of the stress levels and period on drain terminal

Regarding to the threshold voltage drift investigation on power cascode devices with stressing gate terminal of the whole devices is predominantly related low voltage Silicon MOSFET that is used as a gate for the GaN HEMT device. The cascode devices are normally off devices although it has normally on devices like JFET and HEMT in their structures. When the voltage is biased across the drain source terminals of the devices, this voltage creates a negative voltage at the gate terminal of these normally-on devices and becomes off-state resulting in the blocking voltage across the devices [16]. From this perspective, the drain terminal of the power cascode device is stressed to investigate whether indirectly stress on gate terminals of the GaN HEMT in cascode structure have an impact on threshold voltage drift of this cascode device. Fig. 9 demonstrates that the transfer characteristics of GaN power module under -20 V and 20 V drain stress with the duration of 5000 sec and 1000 sec at 25°C and 175°C. It is clearly seen that there is no threshold voltage drift as it is seen gate stress in the GaN power module even with prolonged stress periods.

With respect to transfer characteristics of Silicon power module that are shown in Fig. 10, there is no impact of the drain stress on the Silicon power module at 25°C and 175°C.

The stress level is increased to 40 V and subject to the drain terminals of the power modules are stressed for 5000 sec while there is no threshold voltage drift or difference as it is illustrated in Fig. 11.

The negative voltage is directly subjected to the drain terminal of the power module and the only difference is seen

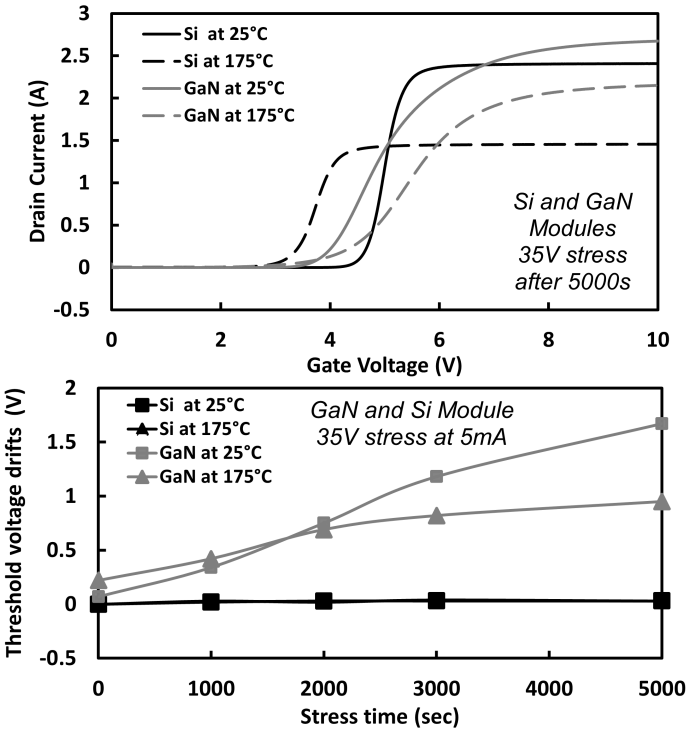

Fig. 8. The drain current against gate source voltage of the 600 V GaN cascode module and Silicon power MOSFET module under 35 V bias after 5,000 sec stress at 25°C and 175°C.

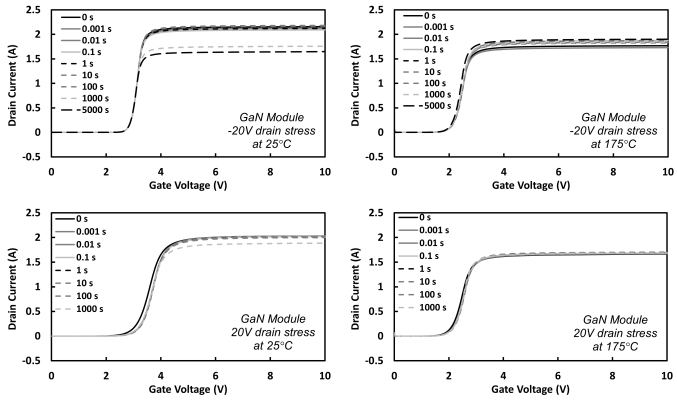

Fig. 9. Drain current against gate source voltage of the 600 V GaN power module under -20 V and 20 V stress on the drain terminal from 1 ms to 5,000 sec at 25°C and 175°C

in the drain current of the GaN power module as highlighted in Fig. 12, whereas this difference is decreasing with the temperature rise as illustrated in Fig. 12. In order to expand the investigation of the impact to the transfer characteristics of the power module with stress on drain terminals of the devices, the stress level is increased as demonstrated in Fig. 12. Even the stress level on drain is increased to 40 V, there is no effect on IV curve of the power modules as well. Regarding the threshold voltage drifts of the power modules under vary stresses on drain terminals, the threshold drift can be negligible except for the 20 V stress as illustrated in Fig. 12.

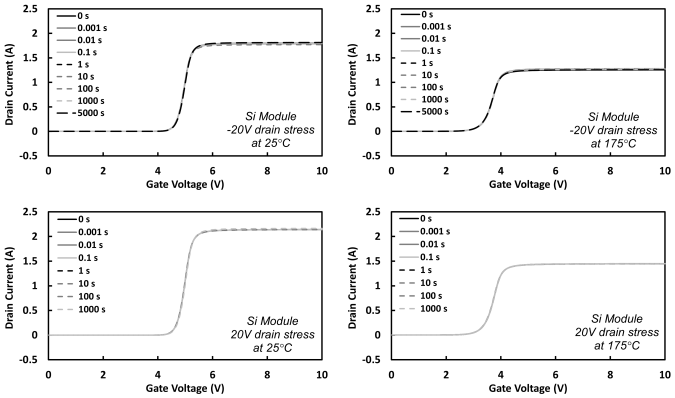

Fig. 10. Drain current against gate source voltage of the 600 V Silicon power module under -20 V and 20 V stress on the drain terminal from 1 ms to 5,000 sec at 25°C and 175°C

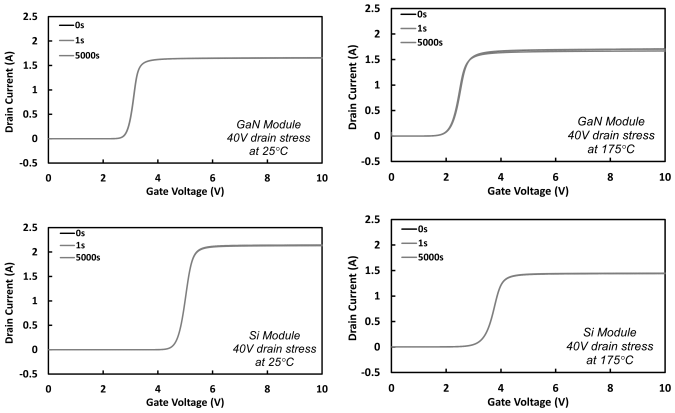

Fig. 11. Drain current against gate source voltage of the 600 V GaN and Silicon power modules under 40 V stress on the drain terminals for 5,000 sec at 25°C and 175°C

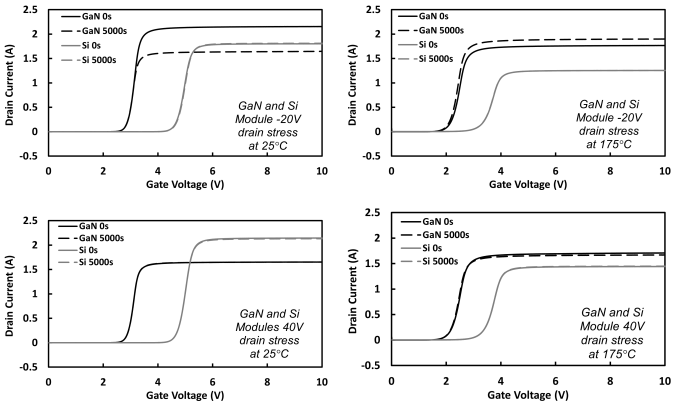

Fig. 12. Drain current against gate source voltage of the 600 V Silicon and GaN power modules under -20 V & 40 V stress on the drain terminal after 5,000 sec at 25°C & 175°C .

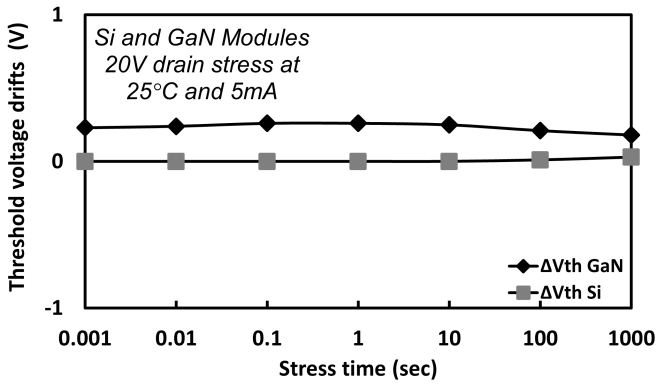

Fig. 13. The threshold voltage drift of the 600 V Silicon and GaN power modules under 20 V stress on the drain terminal after 1,000 sec at room temperature.

In regards to the drain current reduction in Silicon power module at high temperature, Silicon power module only includes a Silicon power MOSFET, hence the device shows typical MOSFET behavior and the threshold voltage as well as the carrier mobility decreases at higher temperature. The reduction of the carrier mobility dominates the threshold voltage reduction and the drain current decreases.

The stressing the drain of the GaN power module with negative voltage causes the differences in drain current after each stress pulses. This stress relatively biases the gate terminal of the GaN HEMT positively that might lead the increase of the trap density in the interfaces between layers under gate oxide layer and hetero-interfaces. These traps can cause the decrease of the threshold voltage of the GaN HEMT in cascode structure by reason of positive charges are injected into the heterointerface where 2DEG is formed, from the gate [17]. This threshold voltage decrease can lead to increase of the drain current of the whole cascode devices. However the decrease of the drain current is related to the increase of the threshold voltage of the GaN HEMT in cascode structure that is results from the charge trapping in the gate oxide layers and the traps between gate and channel [18].

C. Variety of the stress levels and period on source terminal

As it is seen in previous part the stresses on drain terminal of the power modules does not have an effect on the threshold voltage drifts of the power module even with higher temperature as well as variety of stress levels. To carry out the difference in the drain currents after stressing the drain terminal by negative voltage, the source terminals of the power modules are directly stressed by -20 V and 20 V stress pulses with the duration 1000 sec. The transfer characteristics of the GaN module under both stresses on source terminal of the GaN cascode device that means the gate terminal of the GaN HEMT device that results in shrinks of the drain current as it is shown in Fig. 14. Considering the Silicon power module, the transfer characteristic of this device is invariant under these stresses on source terminal even at higher temperature as pointed out in 15.

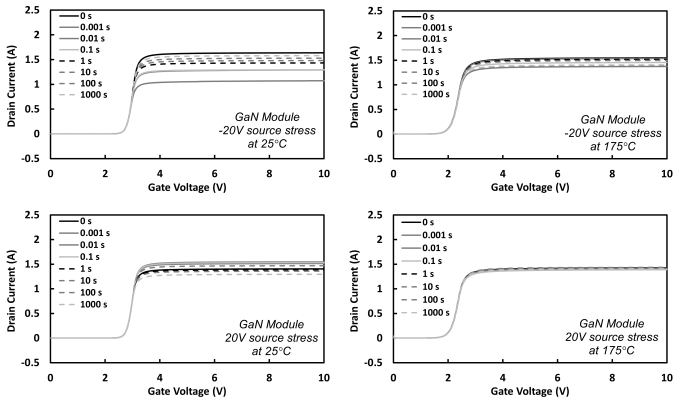

Fig. 14. IV curves of the 600 V GaN power module under -20 V and 20 V stress on the source terminal from 1 ms to 1,000 sec at 25°C and 175°C

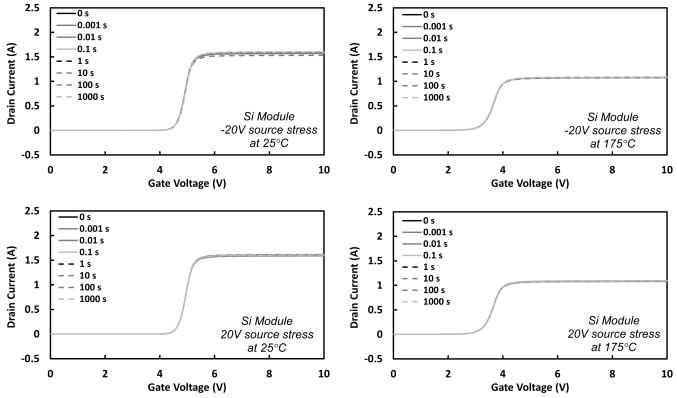

Fig. 15. IV curves of the 600 V Silicon power module under -20 V and 20 V stress on the source terminal from 1 ms to 1,000 sec at 25°C and 175°C

The stress on the source terminal causes a turn around effect in drain currents of the GaN power module at 25°C and 175°C. At room temperature, this turn around effect is much larger than that at high temperature. As for the transfer characteristics of the GaN power module at high temperature, it recover itself under 20 V stress on the source and the turn around effect is disappeared.

The IV curves of the power modules are compared each other under 20 V stress on the source terminals of them at 25°C and 175°C as it is demonstrated in Fig. 16.

The threshold voltage drifts of the both modules after stressing the source terminal of the power modules with -20 V is shown in Fig. 17

The stresses on the source terminal of the GaN power module causes the shrink of the drain current as well. This can be related to trap concentration in the heterojunction and under gate oxide layer of the GaN HEMT in the cascode structure similar to drain stress.

Considering shrinks of the drain current by increasing temperature, it can be related to threshold voltage reduction with

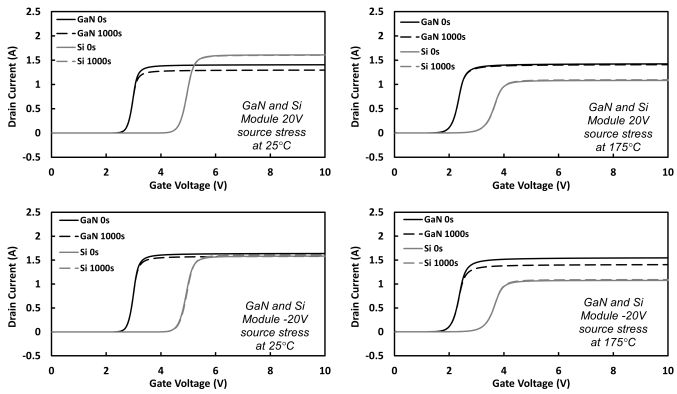

Fig. 16. IV curves of the 600 V Silicon and GaN power modules under 20 V & -20 V stress on the source terminal after 1,000 sec at 25°C & 175°C.

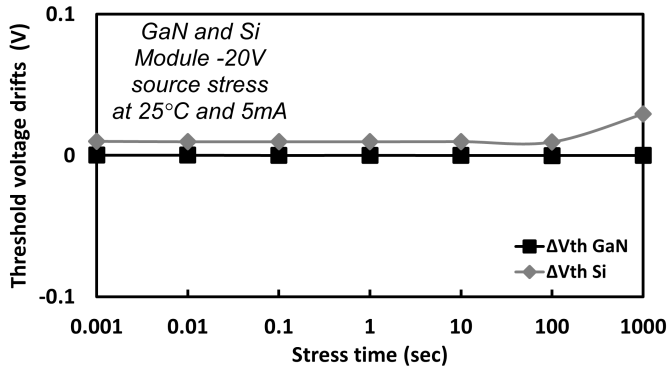

Fig. 17. Threshold voltage drifts of the 600 V Silicon and GaN power modules under -20 V stress on the source terminal after 5,000 sec at 25°C.

temperature due to elevated carrier density from the induced bandgap narrowing, whereas the mobility of the carriers are decreased due to the limitation of relaxation period by cause of the phonon scattering. As it is reported in [19], the transconduction might be decreased with higher temperature for the GaN power module. Moreover, at high temperature, the carrier mobility decrease subjugates threshold voltage drop from elevated carrier density.

As for the threshold voltage drifting in GaN power module under drain and source stresses, it can be negligible. When the drain and source terminal of the cascode device is stressed, these stresses does not have a great impact on the gate of whole device that is completely related to separated a low-voltage Silicon MOSFET. These stresses directly bias on the terminals of the upper device.

IV. Conclusion

The threshold voltage drift of GaN Cascode module and Silicon power MOSFET module compared with each other under a range of stress levels, stress periods and temperatures. As it is seen in the measurements, the GaN module has a significant drift after high level gate stress with prolonged periods and high temperature, while the drift is very low in Silicon power module. Given that the driving transistor in cascodes is also a low-voltage Silicon MOSFET, the results suggest that the GaN HEMT in the module is influencing the overall gate threshold of the cascode configuration in the module through temperature-sensitive charge traps in its AlGaN/GaN 2DEG layer. By applying the voltage bias to the drain-source of the cascode structure which would in turn apply the stress to the gate of the high voltage GaN HEMT, enabling better understanding of the drift in the gate of the GaN HEMT when connected in a cascode structure.

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