Analysis of 1st & 3rd Quadrant Electrothermal Robustness of Symmetrical and Asymmetrical Double-Trench SiC Power MOSFETs Under UIS

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***Abstract*—In this digest, the performance of four generations of power MOSFETs, namely the 950-V, 14-A Silicon Super-Junction MOSFET, 1.2-KV, 22-A Silicon Carbide (SiC) Planar MOSFET, and the 1.2-KV, 17-A Symmetrical and 1.2-KV, 19-A Asymmetrical Double-trench SiC MOSFETs are discussed in terms of the reverse recovery characteristics and its impact on the avalanche ruggedness of the device, based on different failure mechanisms. The experimental measurements are performed at a wide range of switching rates and temperatures ranging from 25°C to 175°C. Two different experimental test circuits are used for the double pulse measurements of the body diode and the unclamped inductor switching experiments. The DC link voltage in UIS tests have been increased step by step till the failure of the devices. The measurements indicate that the SiC planar MOSFET has the largest reverse recovery charge among the SiC devices, only seconded to the significant reverse recovery charge of the Silicon Superjunction device. The measurements of the avalanche ruggedness indicate that the Symmetrical double-trench SiC MOSFET is more rugged compared to other device at room temperature while the Asymmetrical double-trench SiC MOSFET is more rugged at high temperatures.**

***Keywords*—SiC MOSFET, Reverse recovery, body diode, avalanche breakdown, electrothermal ruggedness**

I. Introduction

In the last few decades, Silicon Carbide MOSFETs have become considerably important owing to the fact that they possess a number of features that make them outshine their Silicon counterparts. These materials have higher critical electric field than that of silicon, subsequently they are capable of blocking higher voltages for a thinner drift region. At the same time, they have higher thermal conductivity compared to the Si MOSFETs that mitigates the likelihood of their failure at high temperature operations. Conventional Silicon power MOSFET regardless of its capability of high switching rate suffers from high on-state resistance resulting in high conduction losses. To cope with this problem a new generation of Silicon power MOSFETs called Silicon superjunction MOSFETs were introduced, [1]–[5] that are able to block high voltages with thinner and less resistive drift region. But, on the whole, Si-based MOSFETs are followed by some limitations in high voltage and high temperature applications that result in catching the attention of manufacturers to the Wide-bandgap semiconductors such as SiC so as to ameliorate the performance of the power MOSFETs. Fig. 1 illustrates the cross-sectional schematics of the four MOSFETs under test.

One downside of the SiC planar structure based on the Fig. 1 (a) is high on-state resistance which is mainly attributed to the channel and JFET region resistances. Accordingly, to deal with this problem gate-trench MOSFETs were emerged with its superiority in higher power density and higher level of integration compared to the former types. [6]–[10] But, they had also the problem of gate oxide reliability which is the concentration of the electric field at the gate trench bottom that can result in oxide breakdown if it exceeds the breakdown electric field. Eventually Third generation of SiC MOSFETs Called double-trench MOSFETs were introduced by ROHM in which two deep P-regions are fabricated within the source-body cells that suppress the density of the electric field at gate trench bottom. [11]–[15] However, the existence of these p pillars not only re-establish an additional JFET section, but also restrict the down-scaling of the cell pitch; therefore, Asymmetrical trench MOSFET was introduced by Infineon.

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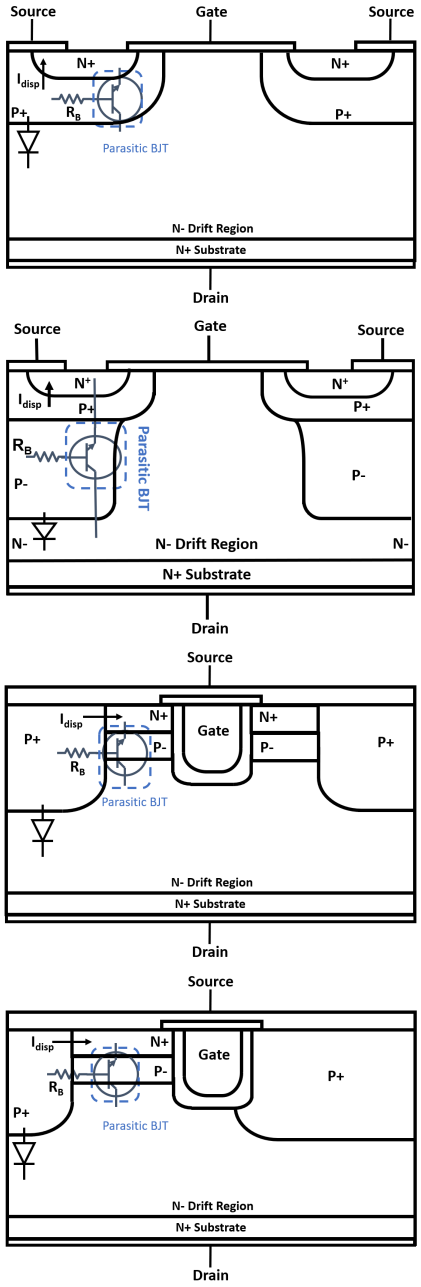

Fig. 1. Cross-section schematics of devices, from top: Silicon Superjunction MOSFET, SiC Planar MOSFET, SiC Symmetrical Double-Trench MOSFET & SiC Asymmetrical Trench MOSFET.

In recent years, some experimental investigations have been done on reliability and ruggedness of Silicon superjunction, silicon and SiC planar and trench MOSFETs through UIS avalanche ruggedness test. But just a few papers are available regarding the ruggedness of the Symmetrical and Asymmetrical double-trench MOSFETs have been carried out specially at high temperatures. For instance, in [16], avalanche ruggedness of Asymmetrical trench MOSFET has been tested for L_p= 64 μs in which maximum avalanche current and drain-source voltage is 20 A and 1560 V, respectively. Another comparison of ruggedness between SiC planar and trench MOSFETS have been accomplished in [17] that shows at the same avalanche current, SiC planar MOSFET is more rugged compared to the SiC trench one based on avalanche energy per area [18], [19].

This paper is divided into two main sections. In the first section, the reverse recovery characteristics of the power MOSFETs is analysed by double- pulse test, and then in the second section the avalanche ruggedness of the MOSFETs against electrothermal stress as a result of different failure mechanisms is investigated under UIS. Finally, a comparison between the performance of the MOSFETs is carried out.

II. Double-Pulse Test

In order to do the experimental measurements and investigation of the dynamic behaviors of the mentioned power devices particularly their body diode characteristics, a clamped inductive switching test is used as illustrated in Figs. 2(a) and 3(a) which is based on double-pulse method. [20], [21] The process of the double-pulse test consists of four stages. Two voltage pulses are generated in this test with different pulse widths. By applying the first pulse the transistor in the low side is turned ON, and the inductor stores energy by the power supply through the transistor, so its current increases. in the next stage when the transistor is turned off, the current commutates in the high-side free-wheeling diode which is the body diode of the transistor in this case. This stage is almost short so as to maintain the inductor current to a constant value. It should be noted that, the type of the devices in the low and high sides are the same technology in this test. When the second turn-ON pulse is applied the low-side transistor and the body diode of the high-side transistor are turned ON and OFF, respectively. In this stage the body diode goes into reverse recovery mode so,this pulse needs to be long enough for the measurements to be taken. Finally, the low-side transistor is turned-OFF again till its current reaches zero.

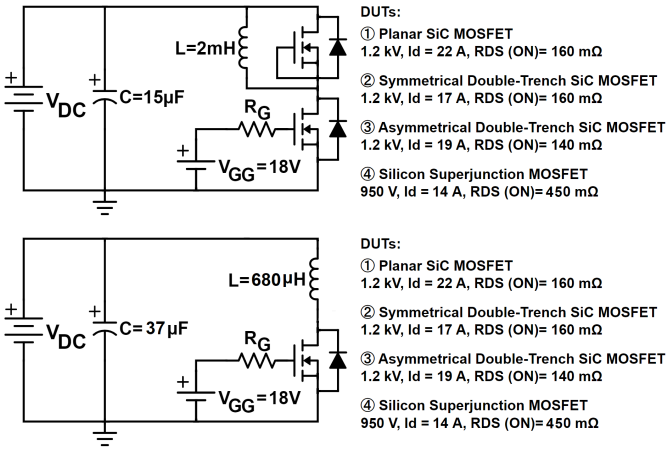

Fig. 2. Schematic of (top) Clamp inductive circuit and DUTs & (bottom) Unclamped inductive switching (UIS) test and DUTs.

III. The 3rd Quadrant Performance

Figs. 4(a-d) demonstrate the body diode reverse recovery characteristics of the proposed MOSFETs at three different temperatures and for three different gate resistances in order

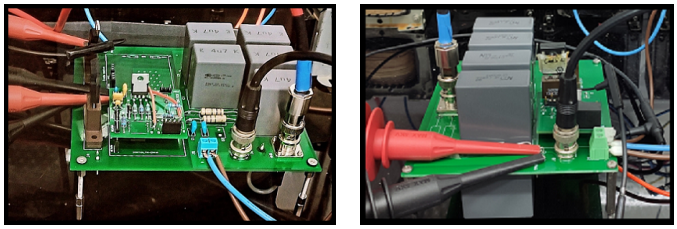

Fig. 3. Experimental test setup (a) Double pulse test board, (b) Unclamped inductive switching test board.

to evaluate the impact of temperature and switching rate of the low-side MOSFET on the reverse recovery current. It is obvious that the Silicon superjunction MOSFET has the largest reverse recovery charge compared to the other three devices which is attributed the structure of two parallel PN^-N and PP^-N diodes because of the alternate p and n doped pillars. In the former, holes are the minority carriers while in the latter electrons are the minority carriers. As electrons have higher carrier lifetime compared to the holes, the rate of recombination of them during the body diode switching-off is lower. Consequently, Silicon superjunction MOSFET has that high reverse recovery. In addition, the reverse recovery charge in Silicon Superjunction MOSFET increases by temperature owing to the fact that minority carrier lifetime grows in the drift region resulting in existence of more charge to be extracted during turn-off.

Reverse recovery charge and time of SiC devices are much lower compared to the Silicon superjunction MOSFET, and are almost negligible. This can be explained by the low minority carrier lifetime of the SiC along with the smaller drift region for blocking the same voltage compared to the Silicon one. The body diode of the SiC MOSFETs performs almost invariable with temperature which is attributed to the very low carrier lifetime in SiC and the smaller dimensions of the die in SiC. Regarding the switching rate it is clear that reverse recovery current increases by increasing the switching rate in all four devices, and at lower gate resistance the reverse recovery has a higher peak in all cases.

Apart from Silicon superjunction MOSFET body diode reverse recovery, in the other devices the reverse recovery becomes more snappy by increasing the switching rate which can bring about the reliability problems. More importantly, the reverse recovery charge is reduced in all cases and this reduction is more vivid in SiC MOSFETs. This matter can be explained by the time of reverse recovery which is longer for lower gate resistance that means more charge will be recombined in the drift region.

The reverse recovery current is sum of the minority carrier injection to the drift region at the same time the discharge current of the junction capacitance [22]. On account of the compact structure of the SiC double-trench MOSFETs, the minority carriers injection is less than the SiC planar one while the junction capacitance is increased in double-trench MOSFETs. On the whole, the impact of the lower minority carrier injection prevails the second factor resulting

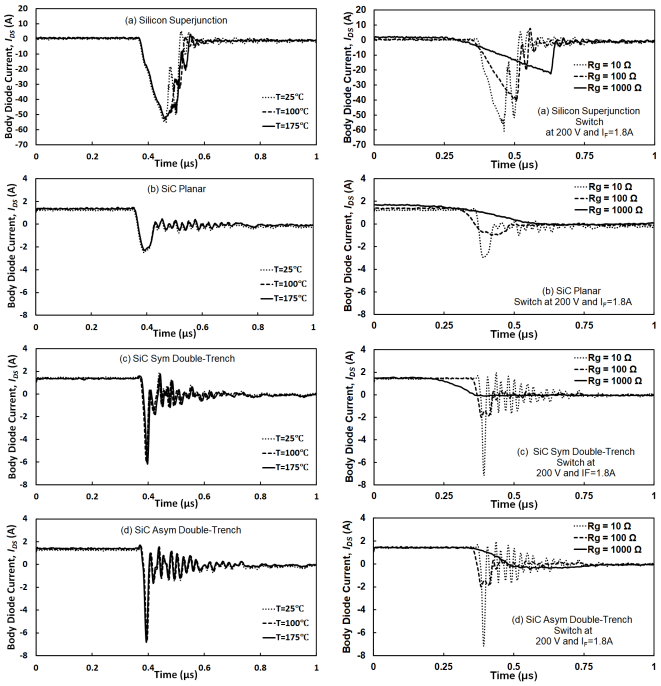

Fig. 4. Reverse Recovery of body diode in the four devices at different temperatures and for various gate resistors.

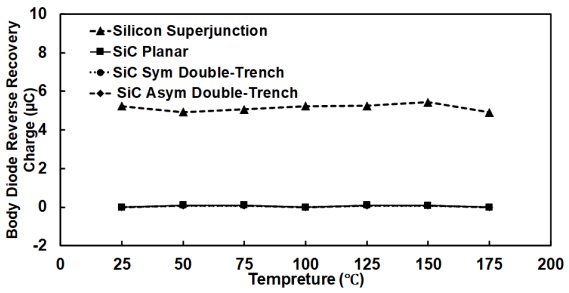

Fig. 5. Comparison of the reverse recovery charge stored in the body diodes of four devices.

in less reverse recovery of double-trench MOSFETs than planar MOSFET. Having said that, however, this difference is insignificant. Fig. 5 shows the stored reverse recovery charge in the body diode of all four device structure technologies versus temperature. As can be seen, Silicon superjunction body diode follows an increasing trend while the reverse recovery charge in the body diode of the SiC MOSFETs is almost constant in all cases.

IV. Double-Trench Avalanche Ruggedness

As the reliability of devices in an irregular condition is of a crucial importance, avalanche failure mechanisms and capability of devices are evaluated in this section by utilizing the unclamped inductive switching (UIS) test based of Fig. 2 (b). Fig. 3(b) depicts the test setup of this experiment in which a single gate pulse with duration of 40 μs is applied to the device. According to Fig. 2 (b), firstly a gate pulse is applied to the DUT and turns it on, during this time interval the

inductor starts to be charged by the power supply through the DUT until it reaches the avalanche current peak. Secondly, the DUT is switched off resulting in formation a high voltage across the DUT which exceeds the breakdown voltage of the device, simultaneously as the power inductor current cannot be changed to zero promptly, this current will flow from drain to the source of the DUT as the avalanche current bringing about the DUT goes into the avalanche mode. In order to evaluate and compare the avalanche ruggedness of the devices avalanche energy as an important parameter is used [23]–[25].

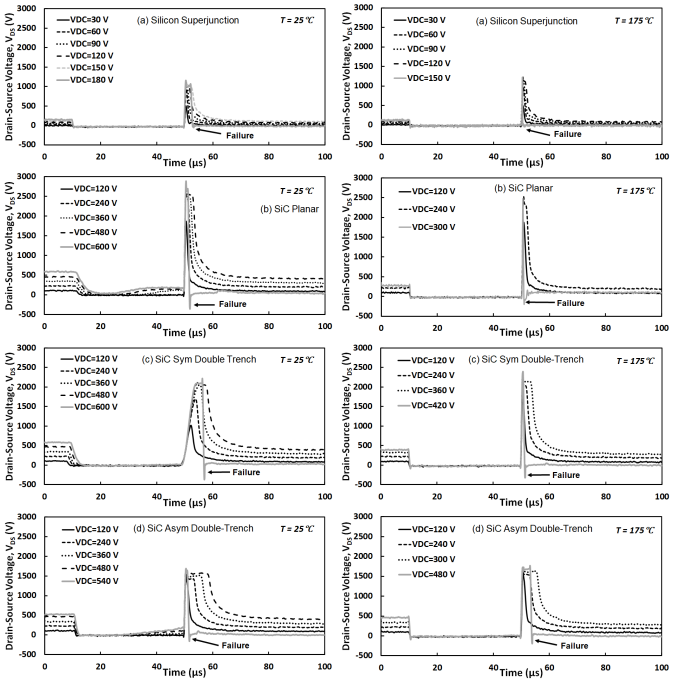

Fig. 6. Drain-source voltage of the four devices for various DC-link voltage until the devices failed at 25°C and 175°C.

Due to the different structure of the devices, their failure mechanisms differ from each other. For example, while the main failure mechanisms in Silicon superjunction MOSFET and SiC planar MOSFET are parasitic BJT latch-up and fracture of the PN junction as a result of high junction temperature, the main failure mechanisms in SiC double-trench MOSFETS are gate oxide degradation accompanied by thermal damage. Based on the Fig. 1(a), inside structure of the planar MOSFET is composed of a bipolar BJT as a result of N drift region, p-body along with the N^+ region of the source. When the device enters the avalanche Mode, a high electric field higher than critical electric field is formed across the junction of N drift region and the p-body, so an avalanche current starts flowing from the drain to the source through the PN junction. During this process a part of this current flows horizontally in the p-body region and pass through its resistance R_b and brings about a voltage drop of V_b between the p-body and the N^+ region of the source. If this voltage drop exceeds the built-in voltage PN junction, the parasitic BJT latches up resulting an avalanche failure. Coexistence of a high electric field and high avalanche current density increase the temperature of the

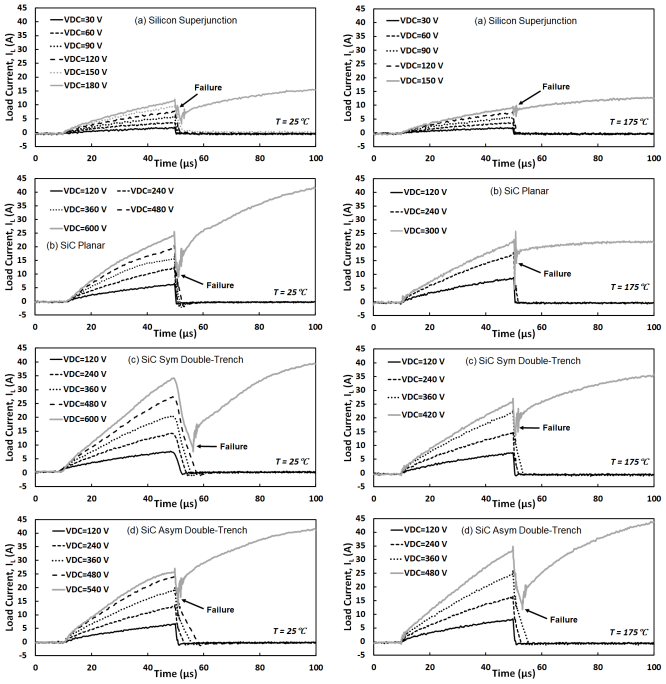

Fig. 7. Avalanche load current of the four devices for various DC-link voltage until the devices failed at 25°C and 175°C.

junction and if it exceeds the critical junction temperature another kind of avalanche mechanism will happen.

Although source trench suppress the density of the electric field at gate trench bottom it doesn't eliminate it totally. therefore in avalanche mode a high electric field is formed in the corner of the gate trench bottom that can result in the gate oxide degradation. In the case of Asymmetrical double-trench MOSFET since the p pillar has a wider area and common cross-section with N drift region it is more likely to suffer from thermal fraction of the PN junction as the avalanche failure mechanism. Moreover, the likelihood of BJT latch-up is almost zero in the SiC double-trench MOSFET. Because in avalanche mode most of the avalanche current flowing from drain to the source as a result of high electric field across the PN junction passes through N drift region and the p-body under trench source vertically, and the likelihood of flowing enough current horizontally through the p-body region resistance R_b to trigger the parasitic BJT is very low. Fig. 6(a-d) and Fig. 7(a-d) show the waveforms of avalanche drain-source voltage and avalanche load current of the devices at 25°C and 175°C, respectively.. It can be seen that the rate of failure of Silicon superjunction, SiC planar and Asymmetrical Double-trench MOSFETs is higher than the symmetrical double-trench MOSFET at 25°C. Moreover, Silicon Superjunction MOSFET and the Asymmetrical double-trench MOSFET fail at lower DC-link voltage compared to the two other ones. By increasing the temperature all the four devices fail at lower DC-link voltages, but Silicon superjunction and SiC planar MOSFET are influenced more. In Fig. 8 avalanche energy of the four devices are calculated and compared at 25°C and 175°C. It is obvious that by increasing the temperature

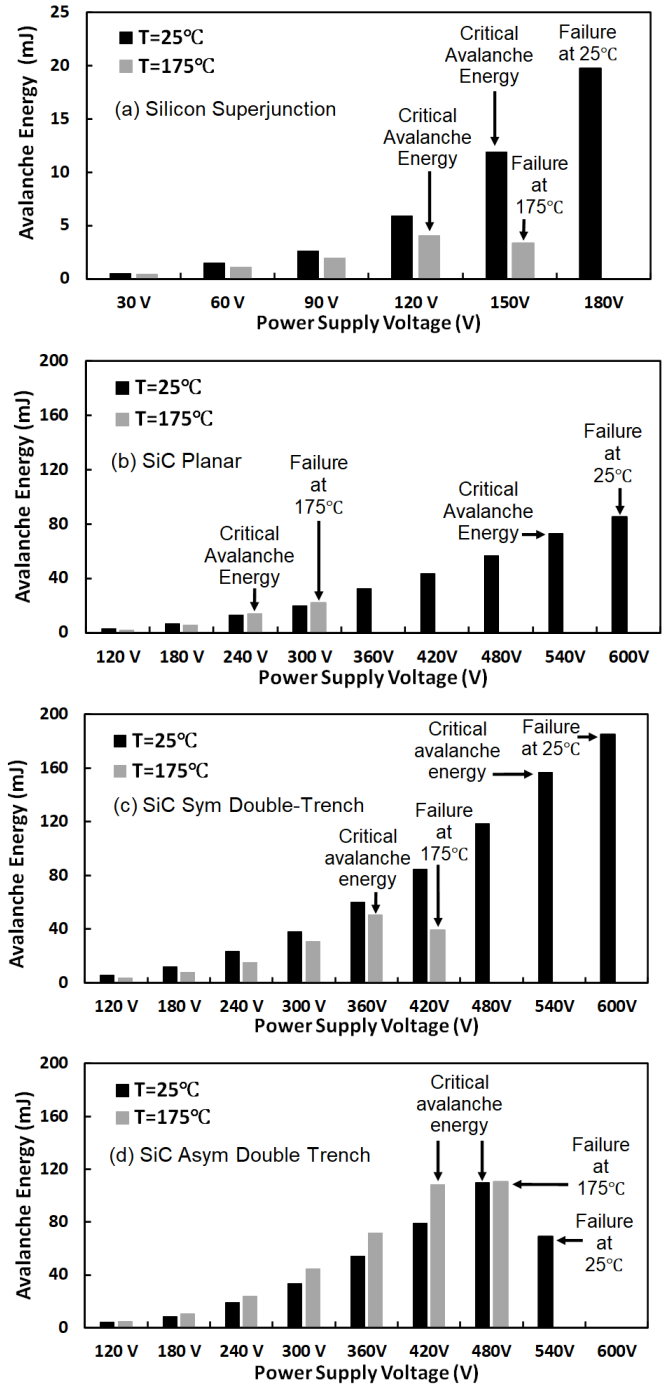

Fig. 8. UIS test avalanche Energy of the four devices for various DC-link voltage at 25°C and 175°C.

from 25°C to 175°C avalanche failure happens in lower DC-link voltage in all cases which is justifiable. for example in BJT latch-up mechanism, because of the positive and negative coefficient of the R_b and voltage drop of V_b, respectively BJT will be triggered sooner as the temperature increases. Regarding critical avalanche energy which is the maximum avalanche energy that a device can sustain before failure, it should be noted that symmetrical double-trench MOSFET can

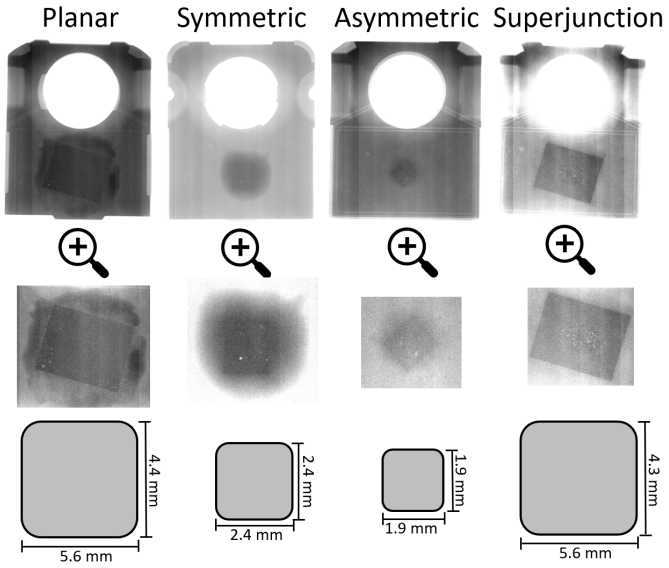

Fig. 9. Die sizes of the four power MOSFETs.

withstand higher critical avalanche energy equals to 157 mJ compared to others. Fig. 9 illustrates the die sizes of the four power MOSFET technologies and based on their sizes avalanche energy density of the devices have been calculated that are shown in Fig. 10. It is clear that while SiC planar MOSFET has the largest die size which is almost near to the size of silicon superjunction MOSFET, Asymmetrical double-trench SiC MOSFET hast the smallest die size. Regarding the avalanche energy density, Asymmetrical double-trench SiC MOSFET has the largest avalanche energy density which is followed by Symmetrical double-trench SiC MOSFET. overall, it can be deduced that at room temperature Symmetrical double-trench SiC MOSFET is more rugged compared to others owing to the fact that not only does it fail at higher DC-link voltage but also it sustains higher critical avalanche energy before failure. At high temperatures (175°C) Asymmetrical double-trench SiC MOSFET is More rugged compared to the others for the same reason. Regarding the instability of the threshold voltage in all four devices it should be noted that by doing the test at high temperatures, the threshold voltage which is a temperature sensitive parameter has been reduced due to the intrinsic charge carrier density having a positive temperature coefficient together with interface charge traps.

V. Conclusion

In this digest, the reverse recovery characteristics and avalanche ruggedness of four generations of power MOSFETs have been examined through two sets of experiments. Based on the experimental results, Silicon superjunction MOSFET and SiC planar MOSFET have the largest reverse recovery charge, respectively. Regarding the avalanche ruggedness, the Symmetrical double-trench SiC MOSFET excels over others at room temperature, while Asymmetrical double-trench MOSFET surpasses other devices at 175°C.

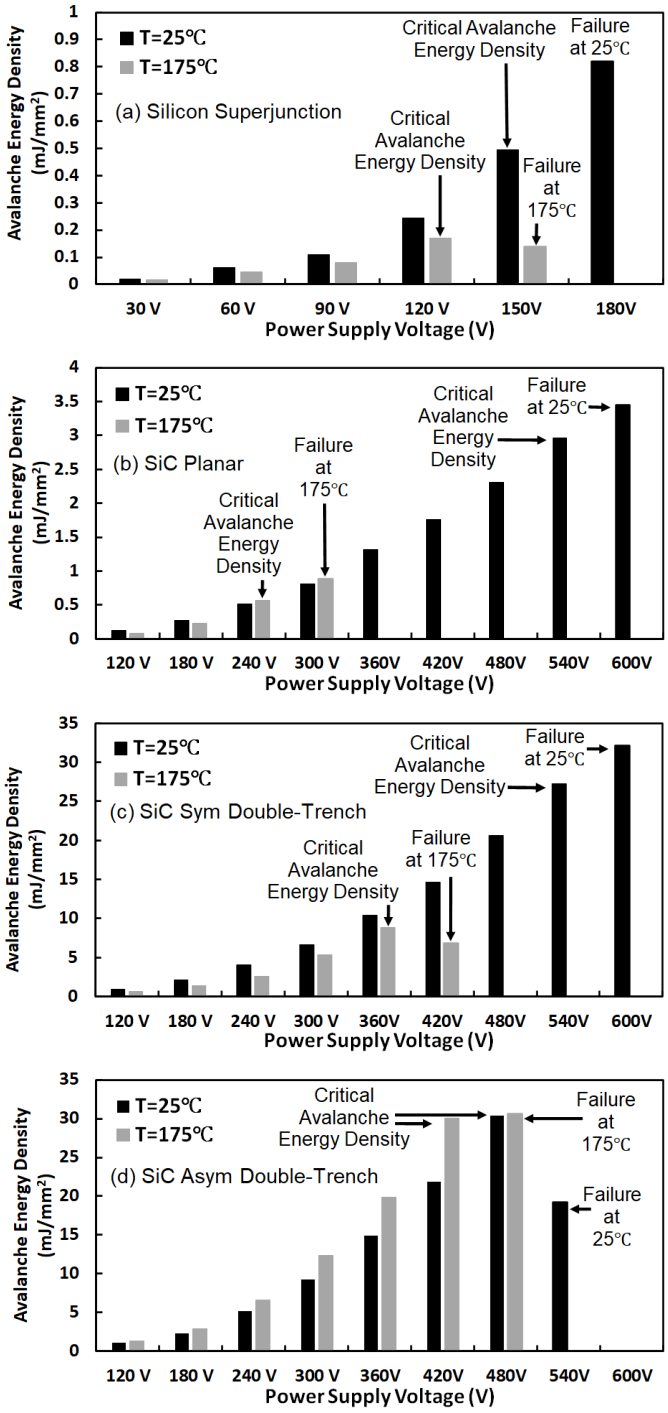

Fig. 10. UIS test avalanche Energy density of the four devices for various DC-link voltage at 25°C and 175°C.

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