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Structural and Electronic Properties of Polycrystalline InAs Thin Films Deposited on Silicon Dioxide and Glass at Temperatures below 500 °C

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Abstract: Polycrystalline indium arsenide (poly InAs) thin films grown at 475 °C by metal organic vapor phase epitaxy (MOVPE) are explored as possible candidates for low-temperature-grown semiconducting materials. Structural and transport properties of the films are reported, with electron mobilities of ~100 $cm^2/V{\cdot}s$ achieved at room temperature, and values reaching 155 $cm^2/V{\cdot}s$ for a heterostructure including the polycrystalline InAs film. Test structures fabricated with an aluminum oxide (Al_2O_3) top-gate dielectric show that transistor-type behavior is possible when poly InAs films are implemented as the channel material, with maximum $I_{ON}/I_{OFF} > 250$ achieved at −50 °C and $I_{ON}/I_{OFF} = 90$ at room temperature. Factors limiting the I_{ON}/I_{OFF} ratio are investigated and recommendations are made for future implementation of this material.

Keywords: polycrystalline; InAs; thin films

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1. Introduction

Low-temperature-grown (<500 °C) semiconducting materials have garnered much attention in recent years for a number of applications such as display technologies, sensors integrated above integrated circuits (IC), and back-end-of-line integration. For these applications, high-temperature processing may not be compatible with the substrate type or previously deposited layers [1]. During conventional semiconductor device processing, dopant activation is often the highest-temperature step, indicating a need for semiconducting materials which do not require a high-temperature dopant activation step. A number of different materials are being explored for these purposes, including InGaZnO [2], InSnO [3], and 2D materials [4,5]. InAs is known to exhibit a high surface electron density in the absence of any intentional doping. This 2D electron gas on the surface of crystalline InAs has been postulated to originate from In adatoms and adsorption of H adatoms [6]. The 2D electron gas reported for crystalline InAs suggests that polycrystalline InAs may be a potential semiconductor candidate for low-temperature processing. Further to this, if a dopant is required, *n*- and *p*-type dopant activation energies in InAs are very low (0.02 eV for Si and 0.01 eV Zn, which are *n*- and *p*-type dopants, respectively) [7]. III-V materials have the added benefit of higher carrier velocities than Si: in InAs, electron mobilities are ≥40,000 $cm^2/V{\cdot}s$, resulting in the potential to allow for a decrease in the operating voltage without compromising the switching speed [8]. Although a 2D electron gas marks

a departure from traditional transistor physics, functional InAs thin-film transistors have been demonstrated through a process of bonding crystalline InAs to a Si substrate [9,10]. It has been shown that poly InAs can be grown at low temperatures on amorphous substrates (SiO_2 and glass) and, through Zn doping, can achieve *p*-type mobilities of >5 $cm^2/V{\cdot}s$, with no optimization [11]. This is an important consideration if this material is to be implemented in CMOS architectures in the future. In this paper, we investigate the properties of this material system as grown, and whether low-temperature-grown (max temperature <500 °C) poly InAs also exhibits a high electron density on the surface without intentional doping. In addition, transistor test structures utilizing the low-temperature-grown poly InAs as a channel material are fabricated and characterized to assess the suitability of the material system for use as a MOSFET channel material in the future.

2. Materials and Methods

Poly InAs thin films (nominally 10–100 nm thick) were grown by MOVPE (or MOCVD, as it is often referred to) at low pressure (80 mbar) in a commercial horizontal Aixtron 200 reactor with purified N_2 as the carrier gas [12,13], on corning "smartphone-grade" glass and Si/SiO_2 substrates at 475 °C, with In droplets serving as nucleation sites. Different thicknesses were achieved by different growth times, with the growth rate remaining constant. Precursors used were trimethylindium (TMIn) and arsine (AsH_3). For selected samples, a polycrystalline GaAs buffer layer was added to form GaAs/InAs heterostructures. The same droplet epitaxy technique was employed, using trimethylgallium or triethylgallium (TMGa or TEGa) and arsine (AsH_3) precursors. For samples containing zinc or phosphorous, diethylzinc (DEZn) or phosphine (PH_3) precursors were used [11]. Samples were prepared for cross-sectional transmission electron microscopy (XTEM) using a Dual Beam Focused Ion Beam (FIB) FEI Helios NanoLab 600i. Carbon and platinum protective layers were deposited before the lamella was removed and thinned to <200 nm thickness. Transmission electron microscopy (TEM) analysis was performed using a JEOL JEM-2100. Hall effect measurements presented in this paper were performed at room temperature unless otherwise stated and were measured on LakeShore Model 8404 AC/DC Hall effect measurement system. Samples for Hall effect measurements were ~1×1 cm^2 and van der Pauw configuration was used. Top-gated transistor test devices were fabricated, utilizing the poly InAs films as their channel material. Patterning of contacts was achieved using photolithography. Source/drain contact metal Au(14 nm):Ge(14 nm):Au(14 nm):Ni(11 nm):Au(200 nm) was deposited by e-beam evaporation and defined using the standard lift-off process. The definition of the channel and source/drain regions was achieved through wet etching using 20:1 $C_6H_8O_7$:H_2O_2 (etch rate > 2 nm/s). Surface passivation was achieved using a 10 min dip in 10% $(NH_4)_2S$ [14]. Following the surface treatment, 15 nm Al_2O_3 gate oxide was deposited by atomic layer deposition (ALD) at 300 °C using trimethyl aluminum (TMA) precursor and H_2O, followed by 200 nm palladium (Pd) gate contact deposited by e-beam evaporation. Electrical characteristics of the devices, both at room temperature and variable temperatures, were extracted using a semiconductor device parameter analyzer, the Agilent B1500, and a semi-automatic Cascade probe station.

3. Results

3.1. Poly InAs Film Properties

The expected polycrystalline nature of the InAs film was confirmed by XTEM, and energy-dispersive X-ray analysis (EDX) was used to confirm that the composition of the lamella was InAs. Figure 1a shows a cross-section, with a lamella thickness of $\leq$ 200 nm. The poly InAs film appears continuous, with some local areas where the film does not have complete closure, possibly resulting in the difference in contrast seen towards the right-hand side of Figure 1a. The area shown in Figure 1b was used to determine the average thickness of the film deposited. Maximum and minimum thicknesses were 55.5 and 40.9 nm, respectively, with the average thickness determined to be 49.5 nm. The grain size can be determined from the XTEM image and is seen to be in the order of 10s of nanometers.

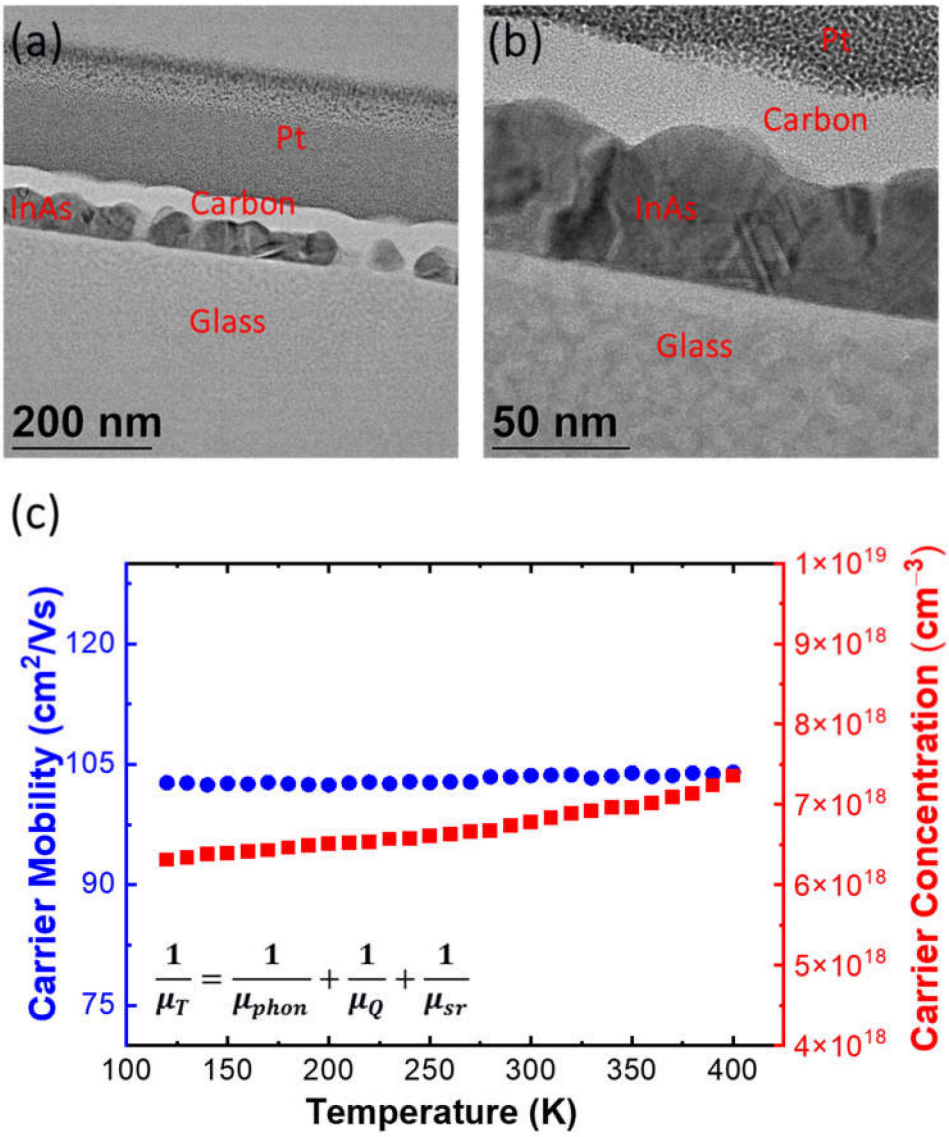

Figure 1. (**a**,**b**) Cross-sectional TEM images of polycrystalline InAs film grown at 475 °C directly on a glass substrate. (**c**) Temperature-dependent Hall effect measurements of a nominally 25 nm poly InAs film on glass (inset: contributions to the overall electron mobility, see text). Measurements taken in AC mode with magnetic field of 0.6 T.

Despite the film not being entirely uniform in the cross-sectional image of the TEM lamella, it was possible to measure an electron mobility of ~100 $cm^2/V{\cdot}s$ at room temperature, suggesting that there are percolation paths present in the 3D geometry. Figure 1c shows the temperature dependence of the carrier mobility and concentration in poly InAs, determined by Hall effect measurements over a temperature range of 125–400 K. As expected, the majority carrier type are electrons, and the carrier mobility in the poly InAs film is seen to be almost independent of temperature. Based on the Matthiessen rule [15], the equation governing the total mobility (μ_T) can be expressed as shown in Figure 1, where the mobility contributions are comprised of: phonon scattering (μ_{phon}), Coulomb interactions (μ_Q), and surface roughness (μ_{sr}). As surface roughness is the only factor of the three which is not strongly temperature-dependent, we can conclude that this is the dominant factor limiting the electron mobility in the poly InAs film [16]. It is well known that the mobility of polycrystalline Si is limited by grain boundary scattering. It is observed that a poly Si film with lower doping shows an increase in mobility with temperature (due to thermionic emission over potential barriers at grain boundaries), while for a poly Si film with higher doping, a decrease

in mobility with temperature (phonon-limited) is shown as the grain boundary defects are saturated and the potential barrier at the grain boundary regions tends to zero [17]. If our unintentionally doped poly InAs behaved in the same way, we would expect the mobility to increase with temperature in the lower temperature range and begin to decrease with temperature at the higher temperature range as the potential barrier is removed and the mobility becomes phonon-limited. However, we do not observe this, as, due to our high electron concentration (and smaller bandgap than Si), the grain boundaries are saturated and the dominant factor limiting the mobility is surface roughness, with the mobility remaining relatively constant over the entire measurement range of temperatures as a result.

Hall effect measurements of films with varying thicknesses (10–100 nm nominal thickness) showed the expected scaling of the sheet carrier concentration with thickness (data shown in Supplementary Materials, Table S1), meaning that there was not exclusively a surface charge present as had been seen in the literature, but also a contribution from a bulk charge in the poly InAs film. Table 1 shows the carrier mobility and concentration results obtained from room-temperature Hall effect measurements performed on differing poly InAs films. The nominally 10 nm InAs film grown directly on glass was not capable of being measured using the Hall effect apparatus, as it lacked sufficient continuity to obtain reliable data. The three other samples in Table 1 showed an increase in mobility and sheet carrier concentration with an increase in poly InAs film thickness.

Table 1. Room-temperature Hall effect measurement results of poly InAs films 10 or 25 nm in nominal thickness, with or without prior 25 nm poly GaAs buffer layer, grown on glass. Carrier type for all films was found to be electrons.

	Carrier Mobility (cm^2/Vs)	**Carrier Density (cm^{-3})**	**Sheet Carrier Density (cm^{-2})**
25 nm InAs	73	7×10^{18}	1.75×10^{11}
25 nm GaAs + 10 nm InAs	29	9.6×10^{18}	9.6×10^{10}
25 nm GaAs + 25 nm InAs	155	8×10^{18}	2×10^{11}

Several efforts were made to increase the electron mobility and improve the uniformity of the poly InAs thin films, with a view to implementation in transistor test devices. The benefits of depositing a polycrystalline GaAs (poly GaAs) layer prior to poly InAs such as minimizing roughness and improving continuity have been discussed elsewhere [11]. These benefits are evident as the mobility and concentration could be determined for the 10 nm InAs layer with a GaAs buffer layer, but not for the sample without. Figure 2 shows XTEM images of a 25 nm poly GaAs + 25 nm poly InAs film on glass, with InAs directly on glass as a comparison. Figure 2a shows greater uniformity than the film shown in Figure 1a, and Figure 2b,c illustrate the difference in the thickness of the poly InAs, despite having the same nominal thickness value. It is noted that a contribution to the carrier concentration and mobility from the 25 nm GaAs buffer layer can be discarded, as this layer measured in isolation yields a carrier concentration of 1×10^{16} cm^{-3} and electron mobility of 0.14 $cm^2/V{\cdot}s$. Secondly, as these films were intended for use in a junctionless transistor architecture [18], there was concern that the carrier concentrations measured in the InAs film (10^{18}–1019 cm^{-3}) would be too high to allow full depletion of the InAs channel of the transistor [19]. For this reason, Zn was incorporated as a *p*-type dopant into the poly InAs film during growth. This Zn incorporation effectively modulated the carrier concentration in the poly InAs thin films by ~three orders of magnitude with no reduction in mobility evident [11]. The observation that the electron mobility was not degraded by additional doping is consistent with a mobility limited by surface roughness.

Exposure of the InAs surface to air is expected to result in oxide formation on the surface and subsequent Fermi level pinning, with detrimental effects for contact resistance and gate oxide formation. The effect of a number of surface treatments designed to remove native oxides and/or passivate the poly InAs surface prior to metal contact deposition was studied (Figure 3). Post-treatment properties were extracted from circular transmission line model (cTLM) measurements. Buffered oxide etch (BOE) (which is a mixture of a buffering

agent and HF) caused the specific contact resistance to increase compared to a sample which had received no treatment. HCl treatment achieved a clear improvement in electrical characteristics; however, a combination of BOE/HCl/$(NH_4)_2$ S resulted in consistently superior electrical results than those of the sample which received no treatment and the samples which received BOE or HCl treatments in isolation.

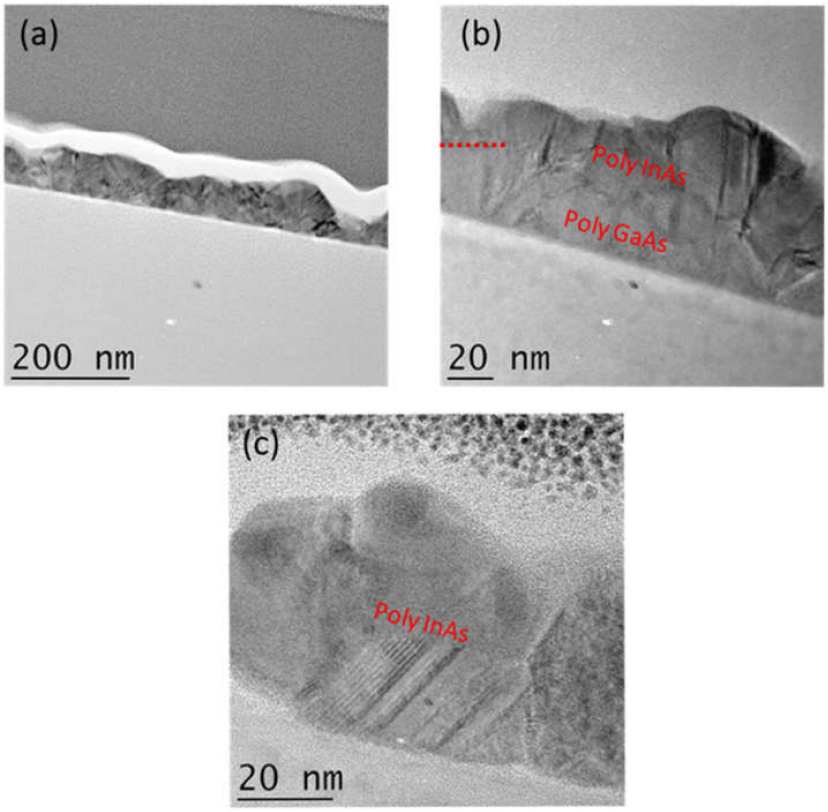

Figure 2. XTEM images of (**a**,**b**) 25 nm poly GaAs + 25 nm poly InAs (dotted line in (**b**) indicates the position of the interface at the left-hand side of the image) and (**c**) 25 nm poly InAs on glass.

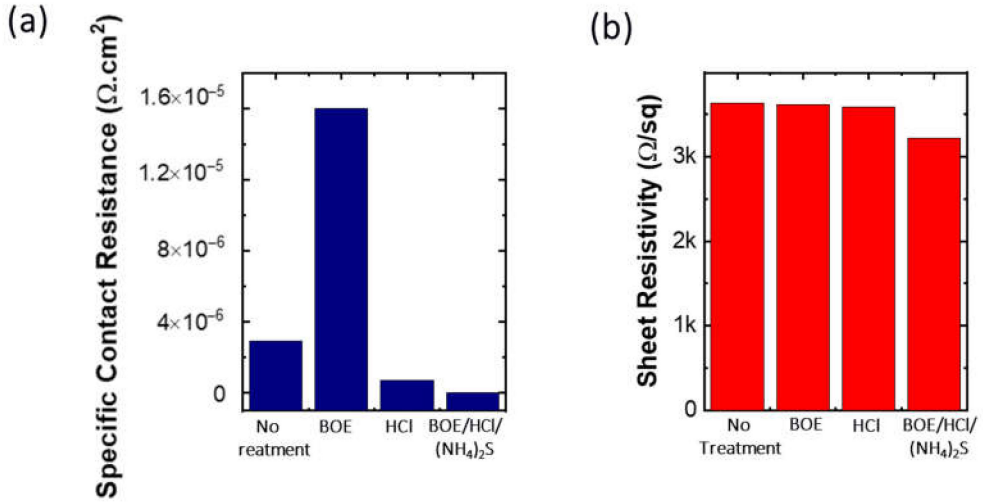

Figure 3. Effect of surface treatments on (**a**) specific contact resistance and (**b**) sheet resistivity of nominally 25 nm poly InAs (transfer length measurements shown in Supplementary Materials, Figure S1).

3.2. Transistor Test Structures

Top-gated transistor test devices were fabricated using a heterostructure consisting of 25 nm poly GaAs + 10 nm Zn-doped poly InAs(P) as the channel material. As discussed previously [11], phosphorous was included as a surfactant during the growth process. Based on previous research, 10% $(NH_4)_2S$ for 10 min at room temperature was used prior to gate oxide deposition during the top-gated transistor device fabrication [14]. Ammonium sulfide, $(NH_4)_2S$, has been shown to remove InAs surface oxides; however, it can have deleterious effects, damaging the patterns previously etched, and forming an undercut. These effects are mitigated through the sulfurization of the surface by $(NH_4)_2S$ itself and dilution of the $(NH_4)_2S$ solution before use [20]. For this reason, a 10% $(NH_4)_2S$ solution only was used for surface treatment of poly InAs films [12]. Following the etching of the InAs/GaAs to form the active area of the device, and 10% $(NH_4)_2S$ surface passivation, the Al_2O_3 (15 nm) top-gate oxide was formed by ALD. The ALD process is also reported to be effective in reducing or removing native oxides present on the III-V surface [21].

Electrical characterization was performed on the top-gated transistor test devices. Output characteristics, Figure 4c, show classical transistor behavior. Transfer characteristics are shown in Figure 4d. The clockwise hysteresis observed in transfer characteristics (Supplementary Materials, Figure S2) originates from electron trapping and de-trapping in the Al_2O_3 gate oxide [22]. It is evident that the drain-source current can be modulated using the gate voltage, and I_{ON}/I_{OFF} of ~90 is achieved. The threshold voltage was determined by extrapolation from the maximum transconductance, $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, and was found to be −2.16 V.

Carrier mobility and concentration values for this film were measured through Hall effect measurements prior to device processing and were found to be 18 $cm^2/V{\cdot}s$ and 7.7×10^{15} cm^{-3}, respectively. Field-effect mobility, Figure 4e, peaks at ~7 $cm^2/V{\cdot}s$, exhibiting a reduction from the Hall mobility as expected for the transistor structure. While the carrier concentration had been effectively controlled through Zn doping, it is noted that the carrier concentration, Figure 4f, is in excess of the 7.7×10^{15} cm^{-3} determined from Hall analysis. This increase in the electron concentration is consistent with the observation from other works that ALD-deposited Al_2O_3, prior to any post-deposition annealing, exhibits a net positive fixed oxide charge density for film thickness values in excess of ~5 nm. Based on values previously reported [22], the 15 nm Al_2O_3 would exhibit an equivalent net positive charge density of $\sim 5.5 \times 10^{12}$ cm^{-2} at the InAs/Al_2O_3 interface. The corresponding electrostatically induced negative charge in the InAs of 5.5×10^{12} cm^{-2} is equivalent to $5.5 \times 10^{18} cm^{-3}$ based on the nominal thickness of 10 nm for the InAs. This is consistent with the levels of channel charge determined for the InAs transistor around the threshold voltage.

While the drain-source current values above the threshold voltage are in good agreement with the Hall mobility value prior to device processing, the off-state current limits the I_{ON}/I_{OFF} ratio of the device. The origin of the off-state current was investigated by varying the substrate and InAs parameters. MOSFETs with varying InAs thicknesses, substrate types (Si/SiO_2 vs. glass), and absence/presence of the poly GaAs buffer layer were tested to rule out any of these variables as detrimental to the I_{ON}/I_{OFF} ratio. All samples exhibited comparable gate modulation, hysteresis in transfer characteristics, and a similar I_{ON}/I_{OFF} value, ruling out the substrate and parasitic conduction through the GaAs buffer layer as the cause of the off-state current (corresponding device characteristics are shown in Supplementary Materials, Figure S3).

Temperature-dependent current-voltage measurements were performed to gain further understanding of the physical process limiting the I_{ON}/I_{OFF} ratio. Results are presented for InAs channel MOSFETs on a silicon substrate (Figure 5a) and a glass substrate (Figure 5b), with the corresponding variation in I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} with device temperature shown in Figure 5c,d. From Figure 5c,d it is noted that the I_{ON}/I_{OFF} ratio is more strongly temperature-dependent for the sample with a poly GaAs layer than that without, with the highest values for each being >250 and ~10, respectively. When components of the

ratio are separated out, the difference in the final ratio is seen to be due to a lower I_{OFF} for the sample with a poly GaAs buffer layer, with I_{ON} for both samples being relatively comparable. One explanation of this is potential Ga incorporation into the poly InAs channel during growth, widening the energy gap and allowing for a lower I_{OFF} to be achieved. The presence of a low level of Ga in the InAs channel is confirmed through secondary ion mass spectrometry (SIMS) (see Supplementary Materials, Figure S4).

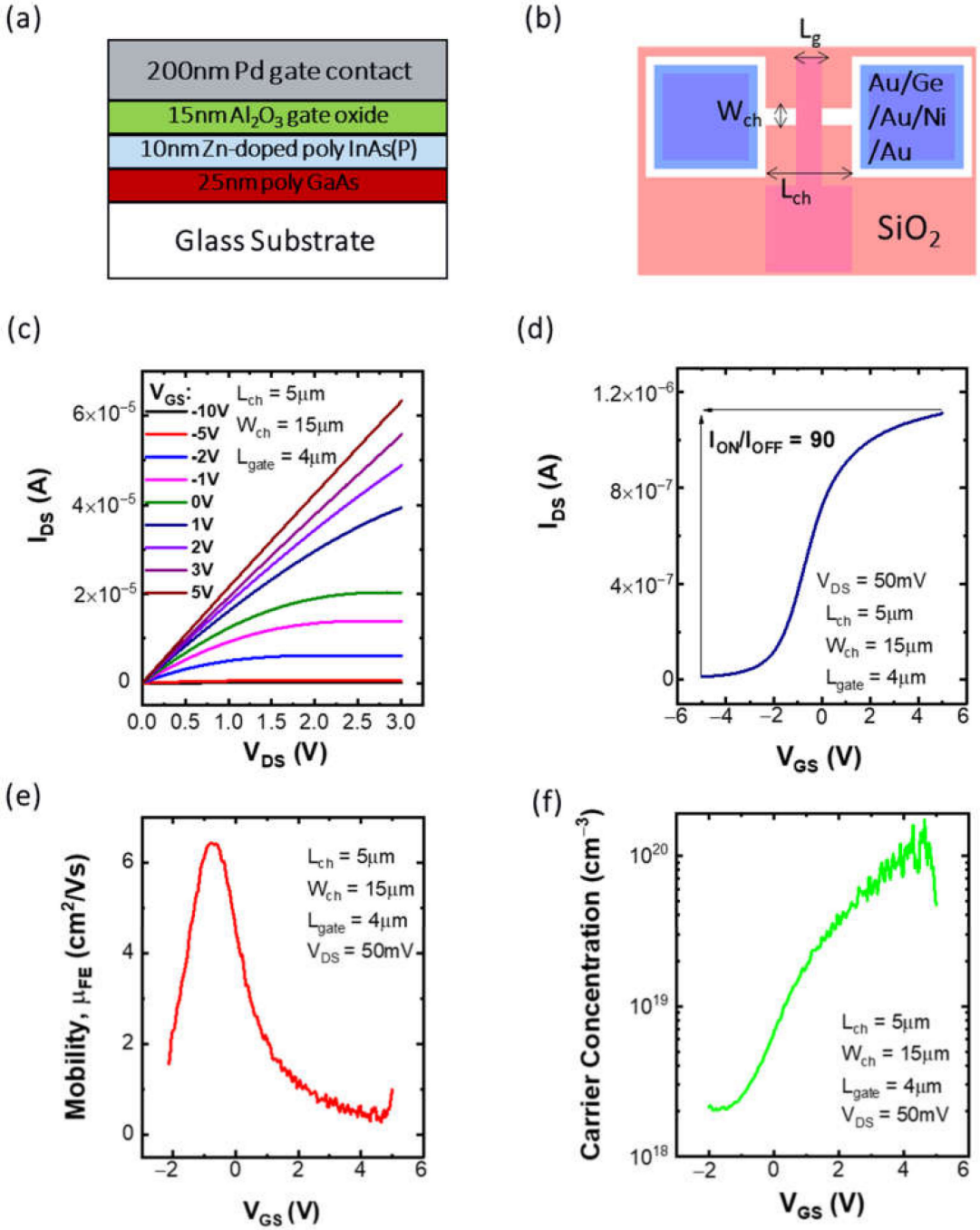

Figure 4. (**a**) Schematic cross-section of film structure in the channel region of the device where gate oxide Al_2O_3 and gate metal Pd were used. (**b**) Plan-view of device layout. (**c**) Device output and (**d**) transfer characteristics at room temperature. (**e**) Field-effect mobility, and (**f**) carrier concentration extracted from transconductance (method in Supplementary Materials). Hall mobility prior to device fabrication = 18 $cm^2/V{\cdot}s$.

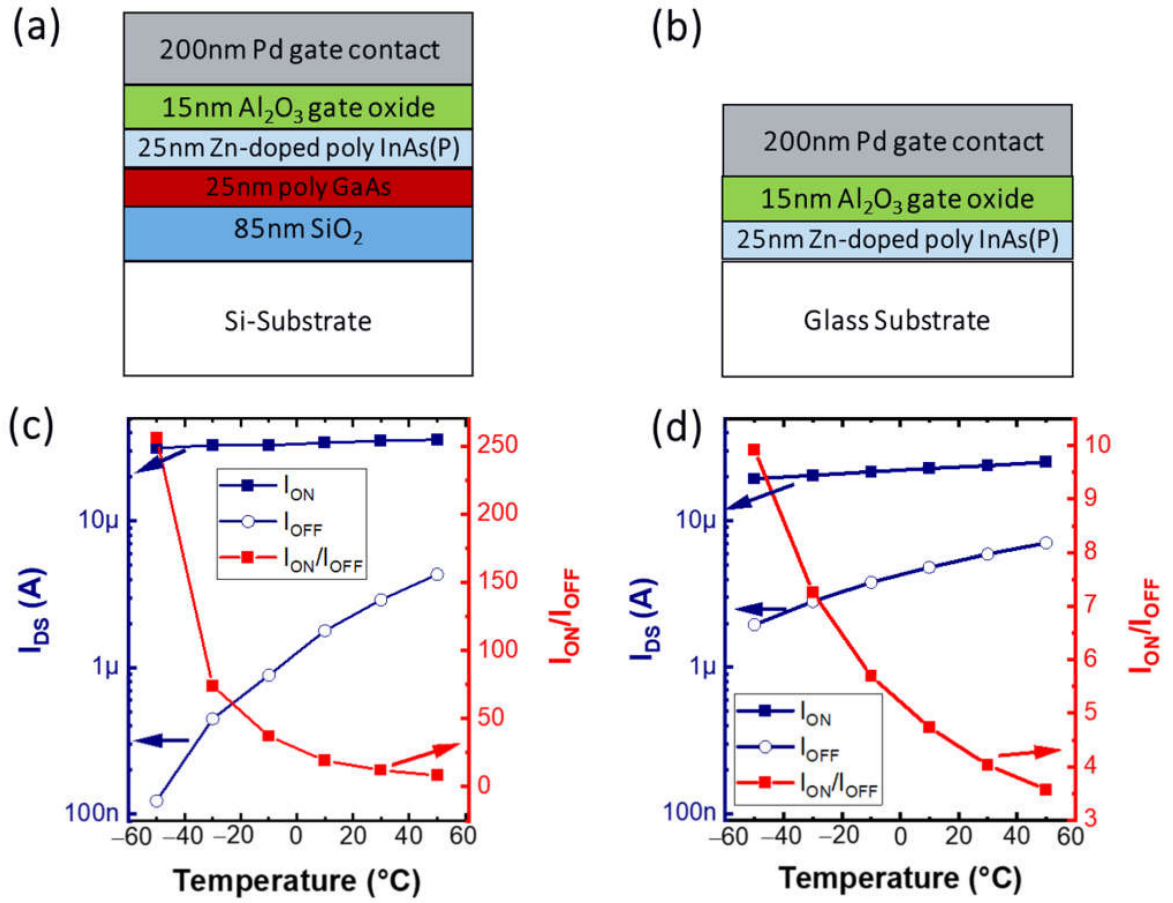

Figure 5. Schematic structure of (**a**) sample with GaAs/InAs heterostructure on Si/SiO_2 and (**b**) sample with InAs directly on glass. (**c**) I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} vs. temperature for sample in Figure 6a, (**d**) I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratio vs. temperature for sample in Figure 6b. V_{DS} = 1.5 V, I_{ON} was taken at V_{GS} = 5 V, and I_{OFF} was taken at V_{GS} = −5 V for Figure 4c,d.

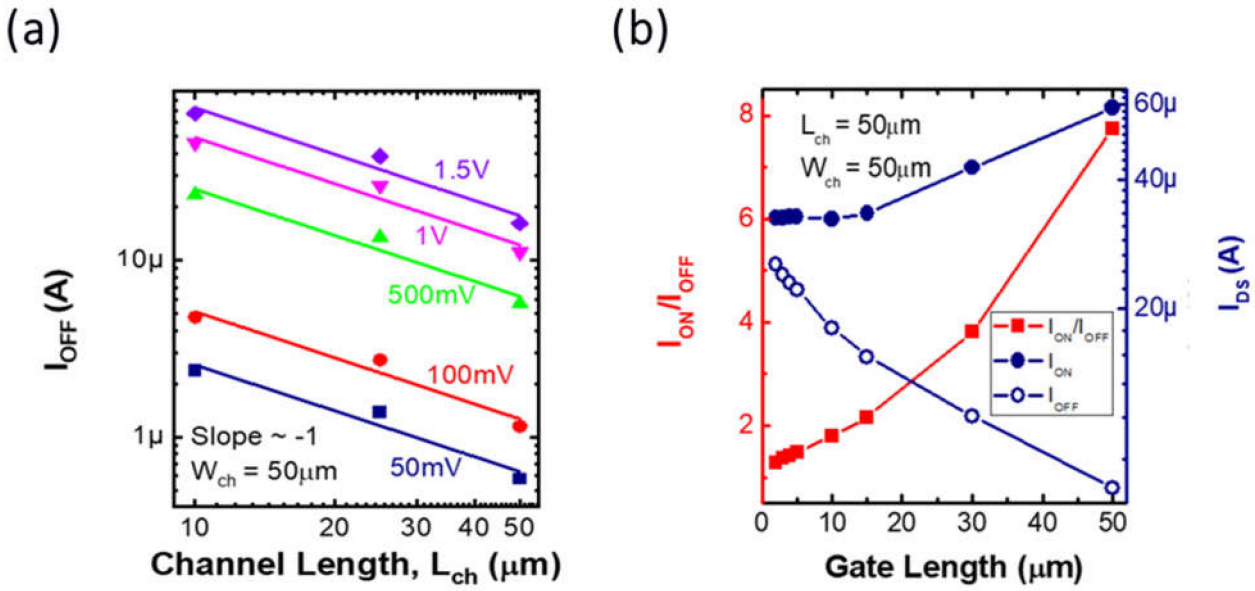

Figure 6. (**a**) I_{OFF} dependence on channel length for 25 nm InAs grown directly on glass, with V_{DS} values next to corresponding line (V_{GS} = −5 V). (**b**) I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} vs. gate length for the same sample (V_{DS} = 1 V, I_{ON} V_{GS} = 5 V, I_{OFF} V_{GS} = −5 V), shown in Figure 5b.

Both of the nominally 25 nm films shown in Figure 5 failed to achieve similarly high room temperature I_{ON}/I_{OFF} ratios to the 10 nm film shown in Figure 4 (~5–15 for 25 nm films compared to ~90 for 10 nm film). Due to the decrease in I_{ON}/I_{OFF} with increasing InAs film thickness, the possibility that the channel was not being fully depleted was investigated. If the InAs layer is not fully depleted, this would leave a resistive conduction path at the InAs/glass or InAs/GaAs interface, which is not modulated by the top-gate voltage. Figure 6a shows the I_{OFF} dependence on the channel length for the 25 nm InAs sample on glass. The I_{OFF} vs. L relationship shows a slope ≈ -1, implying a $1/L$ relationship which would be expected for a resistor. The same I_{OFF} proportional to the $1/L$ relationship is obtained for the 25 nm InAs sample on the GaAs buffer layer. As can be seen from the device architecture shown in Figure 4b, the ratio of gate length to channel length can be varied. Measurements were conducted over a range of gate lengths with a fixed channel length and width to determine how efficiently the gate was controlling the channel. Results from the sample of 25 nm InAs grown directly on glass, shown in Figure 5b, are plotted in Figure 6b below. Figure 6b shows that the greater the proportion of the channel that is gated, the greater the I_{ON}/I_{OFF} ratio, with both ION and IOFF components being affected. However, when the entirety of the channel is gated, i.e., both L_{ch} and L_{gate} = 50 µm, I_{OFF} is still significantly higher than expected for this film. Due to this, and the fact that neither of the 25 nm films in Figure 5 could achieve the same room temperature I_{ON}/I_{OFF} ratio as the 10 nm film in Figure 4, it can be concluded that the entirety of the channel is not being depleted. This also explains the resistor-like behavior observed in Figure 6a.

4. Discussion

We have shown the ability of low-temperature-grown (<500 °C) poly InAs thin films to achieve remarkable electron mobilities when measured at room temperature (~100 $cm^2/V{\cdot}s$), despite appearing non-uniform. The room-temperature Hall electron mobility of 155 $cm^2/V{\cdot}s$ achieved for a heterostructure consisting of 25 nm poly GaAs + 25 nm poly InAs grown on glass (Table 1) exceeds the reported Hall mobility values of a number of other low-temperature-grown thin-film materials, such as polycrystalline silicon [23], Hf-doped In_2O_3 [24], ITO [25], and ZnO [26,27]. Temperature-dependent Hall effect measurements showed that surface roughness is the dominant factor limiting the electron mobility in the films, which points towards developing a planarization method for poly InAs films. Surface treatments and device processing methods were developed, resulting in functional top-gated transistor test structures. Through temperature-dependent measurements, it was found that I_{OFF} limits the final I_{ON}/I_{OFF} ratio. Moving forward, it is advised to employ thinner poly InAs films to maximize the performance of this semiconductor channel for applications where the thermal budget is restricted. While the transistor test structures demonstrated in this paper have a relatively low I_{ON}/I_{OFF}, this marks a significant step towards achieving poly InAs channel MOSFETs grown at a suitable temperature for above IC integration. Finally, it is noted that there is great scope for III-V heterostructure designs which implement these high-mobility, low-temperature-grown poly InAs thin films while being optimized for applications including display technologies, sensors integrated above IC, and back-end-of-line integration.

Supplementary Materials: The following are available online at https://www.mdpi.com/2073-4352/11/2/160/s1, Table S1: Room-temperature Hall effect measurement results for different thicknesses of Zn-doped InAs(P) grown on Si/SiO_2 with 25 nm poly GaAs seed layer. Figure S1: (a) cTLM structure layout from which measurements were taken for Figure 2 in the main paper. (b) Linear IVs from which the parameters in Figure 2 in main paper were extracted. (c) Transfer length, and (d) resistivity results for 25 nm poly InAs film which received each of the surface treatments, and reference sample which received no surface treatment. Figure S2: Clockwise hysteresis observed for transfer characteristics of 10 nm Zn-doped poly InAs(P) with 25 nm poly GaAs seed layer grown on a glass substrate with junctionless transistor device structure. Figure S3: Transfer characteristics of (a) 25 nm Zn-doped InAs(P) with 25 nm poly GaAs seed layer grown on Si/SiO_2 substrate, (b) 25 nm Zn-doped InAs(P) grown directly on glass substrate, and (c) 25 nm Zn-doped InAs(P) grown directly on Si/SiO_2 substrate. Structures through channel region shown below each corresponding to IV.

Figure S4: TOF-SIMS results showing level of (a) Ga, (b) In, and (c) As present vs. depth from surface, for sample consisting of nominally 25 nm poly GaAs buffer layer + 25 nm Zn-doped poly InAs(P).

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