ATHENIS_3D: Automotive Tested High-voltage and Embedded Non-volatile Integrated SoC platform with 3D Technology

E. Wachmann*, S. Saponara^, C. Zambelli[+], P. Tisserand[$], J. Charbonnier[#], T. Erlbacher[x], S. Gruenler[x], C. Hartler*, J. Siegert*, P. Chassard[$], D. M. Ton[$], L. Ferrari^, L. Fanucci^

*ams AG, Unterpremstätten (A); [+]University of Ferrara, Dip. Ingegneria, Ferrara (I); [#]Univ. Grenoble Alpes, CEA, LETI MINATEC Campus, Grenoble (F); ^University of Pisa, Dip. Ingegneria Informazione, Pisa (I); [x]Fraunhofer IISB, Erlangen (D); [$]Valeo Electrical System, Créteil (F); contact: http://www.athenis3d.eu/

***Abstract* - The ATHENIS_3D FP7 EU project aims at providing new enabling technologies (analog, digital and power components) for high-voltage and high-temperature applications, tested for power systems of new hybrid/electrical vehicles. Innovation is exploited at process/device level (3D chip stacking, wafer level packaging, trench capacitors and TSV-inductors integrated in the interposer, high-reliable non-volatile Magnetic RAM), circuit-level (inductorless high-voltage DC DC converter, high-temperature 28nm System-on-Chip platform) and system-level (compact 3D embedded power mechatronic system). Enabling high integration levels of complex systems, operating in harsh environments, in a single packaged 3D device, ATHENIS_3D allows for one order of magnitude area reduction vs. today PCB-based power and control systems. Integration costs will be consequently reduced in key industrial sectors for Europe where high-voltage/temperature operations are mandatory (vehicles, avionics, space/defence, industrial automation, energy).**

***Keywords*— 3D technology, integrated passive devices, power electronics, System-on-chip/in-package (SoC/SiP), electric vehicles**

I. INTRODUCTION

FP7 EU project ATHENIS_3D targets the industry's first 3D heterogeneous integration technology platform for harshest automotive conditions utilizing Through Silicon Vias (TSV) and Wafer Level Packaging (WLP) with Die to Wafer (D2W) stacking. Innovative key building blocks (analog, digital and power) for high-voltage and high-temperature applications will be tested for power systems of new hybrid/electrical vehicles. Indeed the automotive industry trend is to have in a vehicle, electrical engines, on one hand producing standard electrical energy and on the other hand, producing torque for hauling. Toyota recent announced to target to cut emission by 90% by 2050 for its new vehicles and the "dieselgate" in Europe/US [1] will accelerate the evolution towards electric/hybrid mobility. Usual engines are synchronous machines with power range from kW to hundreds of kW. To control such machines, electronics devices are more and more present with a need of strong integration, raising questions about dimensions and reliability with an objective of product costs optimization. In addition, constraints have to be considered in a car environment such as vibrations, EMC, high voltages/currents, high temperatures, high-density integration. To address these issues in ATHENIS_3D innovation is exploited both at semiconductor process/device level (3D chip stacking, wafer level packaging, trench based high voltage capacitors, high-reliable and high temperature capable non-volatile MRAM) and circuit/system-level (inductorless 48V DC DC converter, first high-temperature 28 nm SoC platform designed and fabricated in Europe). For this purpose, substantial technological barriers have to be overcome for the first time such as 3D integration with TSV technology and WLP on a HVCMOS Si interposer, meeting reliability requirements up to 200°C application temperatures. The ATHENIS_3D main targets are:

-Demonstrate reliable high-performance and low system cost 3D heterogeneous integration technology platform using TSV and WLP that meets harshest automotive requirements

- Define integration concepts based on automotive system specifications and from the ATHENIS_3D heterogeneous integration technology platform by combination of 0.18/0.35 µm HVCMOS with TSV and Back-side Rerouting Distribution Layer (BRDL), embedded non-volatile MRAM, integrated passive devices IPDs and stacked nanoCMOS

- Develop analog and digital IP blocks (inductorless 48V DC-DC converter, high temperature capable 28nm SoC processing unit) and circuit design for the 3D IC demonstrators

- Develop novel methods for the simulation, characterization and the reliability investigation, including new predictive reliability models, of the HVCMOS interposer, the high temperature capable MRAM, the 3D stacked 28nm nanoCMOS processor, and the integrated passive devices,

The ATHENIS_3D consortium addressing the above challenges includes 12 partners from 5 countries, both from industry (big industries and SME) and Academia: AMS AG, Austria; Valeo Equipements Electriques Moteur SAS, France; Crocus Technology SA, France; Fraunhofer Gesellschaft – IIS and IISB institutes, both from Germany; Technical University Vienna, Austria; Active Technologies S.R.L., Italy; Maser Engineering B.V., Netherlands; BESI Austria GmbH, Austria; CEA LETI, France; Universities of Pisa and Ferrara, Italy.

After this introduction, Section II presents innovation and results about the 3D chip stacking and wafer level packaging. Characterization of non-volatile MRAM, integrated in the back-end of the semiconductor process, is addressed in Section III. Section IV discusses new processes that have been set-up for the integration of passive devices through trench-based capacitors and TSV-inductors. To show how these process innovations are exploited at circuit and system level, Section V shows the design of a complete mechatronic power and control module with key blocks such as inductorless 48V DC DC converter and 28 nm SoC computing platform. Section VI draws some conclusions.

II. 3D CHIP STACKING AND WAFER LEVEL PACKAGING

3D integration technology improves the functionality of microchips. This is done by connecting chips with different functionalities into a single chip or package [2-4]. Compared with the classical system PCB (Printed Circuit Board) level, not only the required form factor is reduced but also resistances and signal paths. Due to the demands for high temperatures and voltages from the automotive market, the limits of this technology need to be examined in this new context. Three major technologies are key modules for 3D integration: the redistribution layer (RDL), TSV and the stacking of chips. Among all the ongoing studies on 3D integration, this project will focus on the stacking of dies. The interconnection between the chips, which provides the electrical contact, is analyzed in more detail by using flip chip methods and several types of interconnections in this project, see Fig. 1.

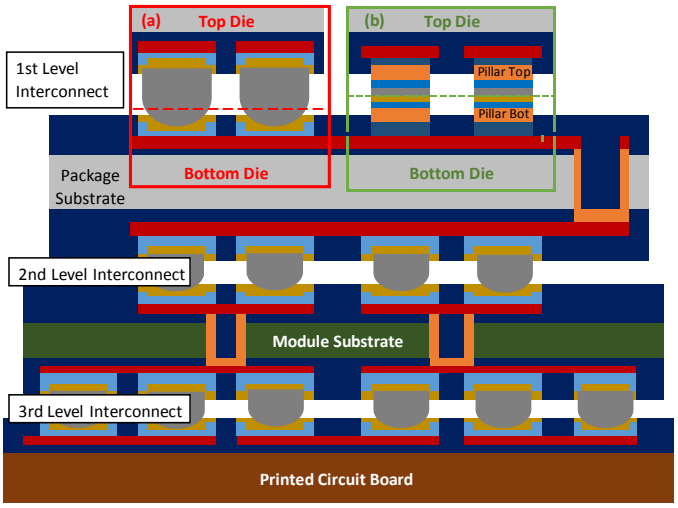

Fig. 1: Integration of two stacked dies by solder balls (a) and copper pillars (b) using the flip chip method.

An optimized design has been developed, see Fig. 2, which allows a direct comparison between the chosen interconnection types in terms of reliability to environmental stresses that can be evaluated at wafer level. A single layout includes top and bottom dies with widely varying designs. The six different kinds of bottom and top dies are defined by interconnections pitches of 40, 65, 80, 130, 250 and 500 µm for interconnections diameters of 20, 30, 40, 70, 150 and 325 µm, respectively. Each test vehicle includes modular Kelvin test structures for the electrical characterization and daisy chain structures of 48 and 96 interconnections. For the first tests two interconnection types have been considered: solder balls and copper pillars.

The integration for solder balls can be seen in Fig. 1(a). Top and bottom dies receive an under ball metallization (UBM), at pad opening on RDL location. The solder balls are placed on the UBM of the top dies. Optical images of the realized 70 µm balls are shown in Figs. 3(a) and 3(b). The stacking of the top to bottom part is achieved by using the so-called controlled collapse chip connection process (C4).

Concerning the integration of copper pillars in Fig. 1 (b), micro bumps are placed on the top dies, which consists of copper, nickel as diffusion barrier and a solder alloy, whereas on the bottom dies micro pillars are placed. The micro pillars are made of copper, another Ni layer as a diffusion barrier and a gold capping. Pillars with a diameter of 70 µm for top and bottom dies have been realized and are shown in Figs. 3(c) and (d). The connection of bottom to top dies can be established either by chip connection processes or by thermal compression bonding.

To simulate the high temperature demands of the automotive industry, dedicated setups for extreme thermal cycling (TC) from -65°C to 200°C and unbiased highly accelerated stress test (uHAST) have been developed for the device stress tests. The tests are conducted on wafer level to improve the statistical sample. Before the actual test, the wafers are preconditioned according to the JEDEC standard JESD22-A11. The results from this interconnection study will allow the determination of the application field and the lifetime of balls and copper pillars type of interconnection for several diameters. The final goal is to define in the context of harsh working conditions, the most reliable and resistant type of interconnection for each level.

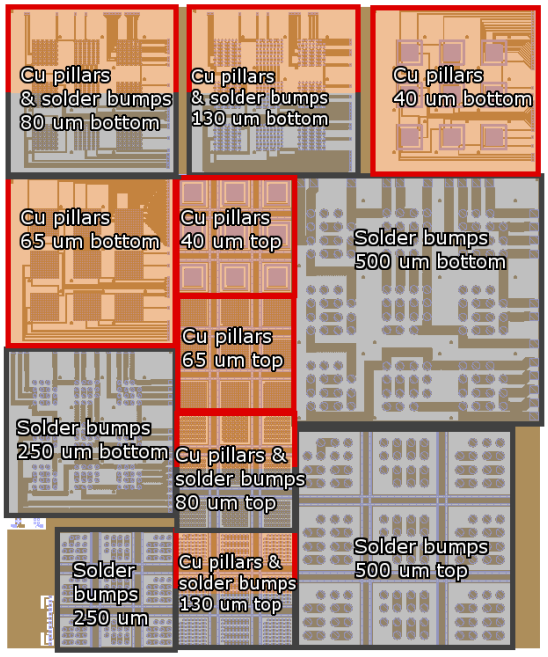

Fig. 2: Test vehicle layout developed on purpose (top and bottom dies)

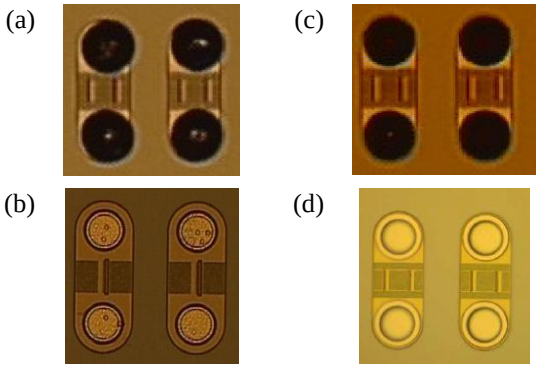

Fig. 3: Realized test vehicle for an interconnection diameter of 70 µm, where (a) is the top and (b) is the bottom die for stacking with solder balls on UBM. (c) and (d) are the top and bottom die respectively of the copper bumps and pillar.(not to scale)

III. HIGH-RELIABLE NON-VOLATILE MRAM

Non-volatile memory (NVM) modules are an essential block for SoC solutions. The majority of the memory technologies is integrated in the front-end of the semiconductor process and

suffer from the same reliability problems. The reliability is degraded both due to the attenuation of the isolation capability and by the thermal activation of charge loss according to the Arrhenius equation. In such condition, most of the embedded NVM solutions are guaranteed to operate for temperatures below 125°C thus not being suited for harsh environments applications such as automotive. On the contrary, memory technologies integrated in the back-end of the semiconductor process exploits special materials able to work reliably above 125°C for extended periods. Magnetic Random Access Memories (MRAM) are one of the most promising candidates to replace traditional Flash in future non-volatile memories generations [5]. Among the MRAM paradigms under investigation, the Thermally Assisted Switching (TAS) represents a good candidate for a replacement of the standard embedded flash memories in harsh environments [6, 7]. The information storage mechanism is based on the current-induced magnetization switch of a magnetic material [8]: dependently on the imposed field direction with respect to that of a reference layer, a defined resistance of the material can be achieved. Such a technology is already at an intermediate maturity level that calls for the evaluation of its potentialities at an integrated array level in embedded solutions. In the ATHENIS_3D project, the reliability and the cell-to-cell variability during the typical automotive tests (i.e., 500k write cycles and 200°C data retention targets) have been evaluated by extracting a set of characteristic parameters from measurements performed on 1kbit arrays manufactured with different back-end processes. The measurements were executed with an Automated Test Equipment developed within this project [9]. The 1 kbit-memory devices integrated into a CMOS process are made of a 32x32 array. Cell and the test array architecture are made by:

- The Magnetic Tunnel Junction (MTJ) device, composed of two ferromagnetic layers separated by an insulating layer.
- Three sense pads SP1, SP2 and SP3 used during read operations. SP1 is on the top of the MTJ, SP2 is connected right below the MTJ and SP3 is between a poly 500 Ω resistance and a select transistor.

To change the state of a memory cell, two different writing operations are available: Write '0' (W0) and Write '1' (W1). Both operations require two voltages: V_{FORCE} is required to locally heat the magnetic material, whereas V_{SWITCH} allows changing the magnetic field polarization after heating. All write operations have been performed with T_{FORCE} = 500ns, T_{SWITCH} = 600ns and $T_{rise/fall}$ = 500ns for both voltages in order to avoid overshoot issues. All read operations have been performed with V_{SWITCH} = 0V, V_{FORCE} = 0.3V, T_{FORCE} = 10µs and $T_{rise/fall}$ = 1µs. The MRAM characterization started in this project by extracting a set of characteristic parameters describing the technology in terms of cell-to-cell variability and switching reliability to define the most reliable working conditions. Fig. 4(a) shows the average resistances measured during switching voltage hysteresis and the switching parameters extracted for further analysis of W0 and W1 operations: $<R_{W0}>$ and $<R_{W1}>$ are the average values of resistance R_{W0} and R_{W1}, respectively measured at V_{SWITCH} = 5V and V_{SWITCH} = −5V. $<V_{W0}>$ and $<V_{W1}>$ are the average switching voltages that allow obtaining a variation ΔR = 1k of the average measured resistance values. Figs. 4 (b)-(c) show the switching voltage and the heating voltage hysteresis evolution during cycling: an equal resistance fluctuation can be observed, thus keeping the resistance difference constant during cycling. 500k cycles have been performed with different V_{FORCE} values and $|V_{SWITCH}|$ = 5V: $<R_{W0}>$ and $<R_{W1}>$ measured during cycling are reported in Fig. 4 (a). The dispersion coefficients (i.e. standard deviation over mean value) for R_{W1} and R_{W0}, evaluated during cycling are reported in [10]: a rapid increase can be observed before the breakdown. The cumulative distributions of the V_{W0} and V_{W1} parameters measured during cycling are also reported in [10]. The cumulative number of cells do not reach 1k because a limited number of cells do not reach, in switching, the assumed ΔR = 1k. The minimum cell-to-cell variability and the highest cumulative number of switched cells during the endurance test are obtained by using V_{FORCE} = 1.4 V. Using higher heating voltages results in a reduced yield (lower percentages of cells reaching the requested ΔR) and in a faster breakdown.

After the parameters optimization 1 million endurance switching cycling have been performed on full chips, constituted by repeated consecutive W0 and W1 operations interleaved by a read operation at fixed cycles. The results of the characterization of a TAS-MRAM array are shown in Fig. 5, where the average read resistance and standard deviation for both logical states are shown. Excellent reliability is proven under heavy cycling conditions. Another typical NVM test that is suitable for evaluating the TAS-MRAM intrinsic reliability is the read disturb test, which consists in consecutive read operations applied on the same set of cells in the array. This test represents the most frequent access mode for the integrated MRAM in the SoC. The reliability once again has been proven to be excellent in 1 million read disturb test. Data retention tests will be performed on the next project steps using dedicated test structures and test equipment solutions to prove the TAS-MRAM reliability in automotive environments up to 200°C.

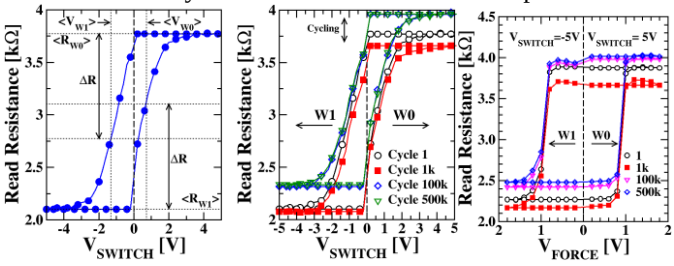

Fig. 4: V_{SWITCH} hysteresis and switching parameters at cycle 1 (a), and at different cycles (b), with V_{FORCE} = 1.4V during W0 and W1 operations. V_{FORCE} hysteresis during W0 and W1 operations at different cycles with $|V_{SWITCH}|$ = 5V (c)

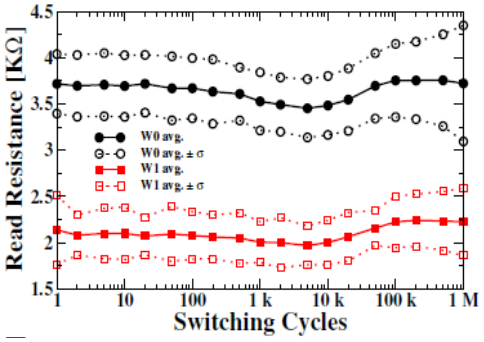

Fig. 5: Endurance behavior in 1 M write cycles test in MRAM arrays.

IV. Integrated Passive devices

Another key innovation of ATHENIS_3D, besides 3D chip stacking and WLP and high-realiable non-volatile TAS-MRAM, is the on-chip integration of passive devices (inductor and capacitors) operating at high voltages and high temperatures. Particularly, in this project, two dielectric stacks consisting of SiO_2 and Si_3N_4 were utilized as dielectric materials for 3D capacitors. These dielectric materials enable the implementation of highly integrated capacitors with operating voltage of 48 V in contrast to the high-k dielectric materials [11]. Additionally their compatibility with HV-CMOS and silicon interposer fabrication makes them an excellent candidate for our purpose. Fabrication sequence is based on area enlargement by an advanced silicon etch (ASE) process that is also used for TSV implementation. A structural characterization using scanning-electron-microscopy (SEM) is shown in Fig. 6. To achive an optimized pattern suitable for high integration density, dependance of the hole-depth on the exposed area, Fig. 7(a), as well as on the hole-diameter, Fig. 7(b), was studied. The lower the patterned area, the deeper the hole-structures for a given etching process, which is the basis for integration of TSV-based capacitors into silicon interposers. Deeper hole-structures lead to a higher surface enlargement and consequently larger integration density. For 50% exposed area during etching , the integration density of a capacitor with hole-diameters of 8 µm and 78 µm depth is 36nF/mm^3, while this value for hole-patterns of a 3µm diameter and depth of 40 µm is 22.5 nF/mm^3.

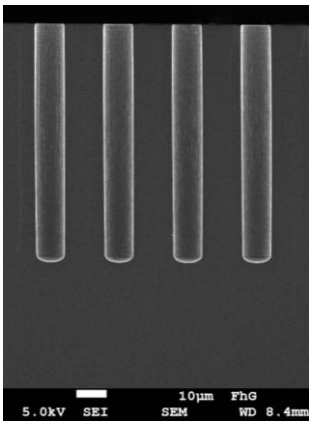

Fig. 6: Cross-section SEM image of hole-structures

a) b)

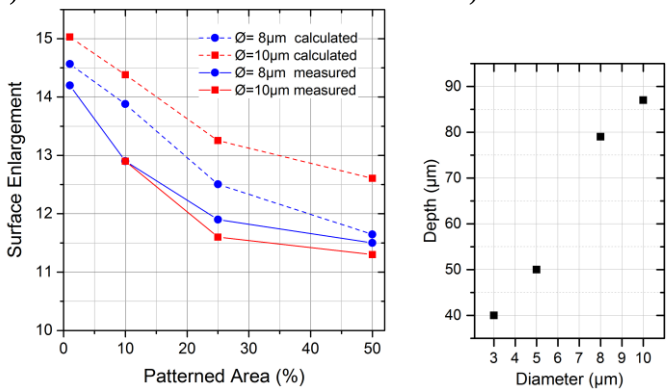

Fig. 7: a) Area enlargement as a function of patterned area, and b) variation of hole-depth in terms of hole-diameter

The measured capacitance shown in Fig. 8 for a capacitor at full accumulation at room temperature is 12 times larger than that of the planar-capacitor with identical dielectric layers. By considering 50% of silicon surface patterned with 8 µm holes, the obtained integration density of 36 nF/mm^3 is higher than the typical value for the class 1 ceramic capacitors offering an integration density of 10 nF/mm^3 [12]. Although the integration density of commerically available low voltage 3D capacitors is up to 250 nF/mm^3 [13], these capacitors operate at only 6 V which is far below the operating voltage required in hybrid/ electric vehicles where 48 V DC bus [14,15] is used. 6 V is also below the requirement of current vehicle industry where 12 V (cars) or 24 V (trucks) are required. On the contrary the 3D integrated capacitors developed in this work outperform the state of art indicating an integration density below 32nF/mm^3 for a scaled 48V dielectric. Current-voltage measurements carried out on wafer level suggest a continuous use voltage of 46 V (corresponding to an electric field of 8 MV/cm) for capacitors with 8 µm hole-diameter and 5 µm distance between holes covering 25% of the silicon surface (see Fig. 9).

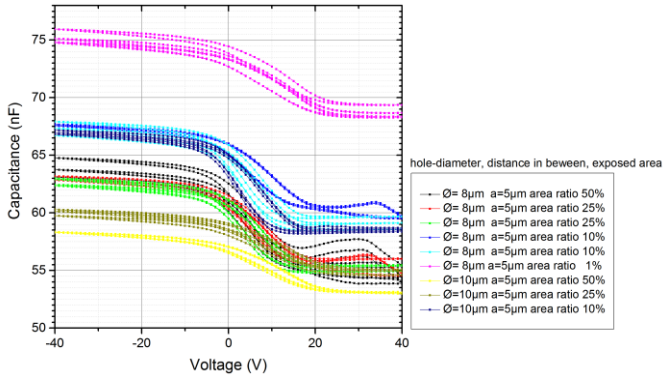

Fig. 8: C-V characteristics of the capacitors with different hole-patterns and exposed areas

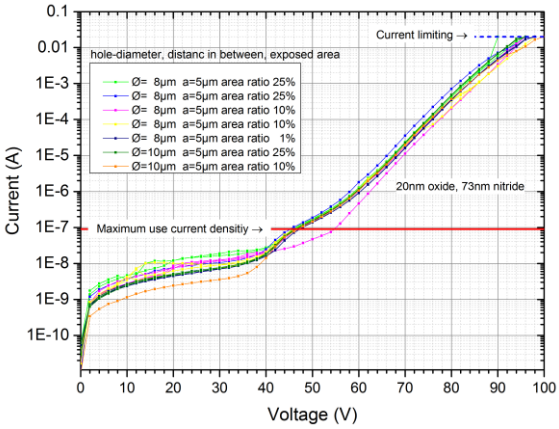

Fig. 9: I-V characteristics of the capacitors operating at 48V

Similar activity has been carried out to realize inductors exploiting TSV which, as discussed in Section I, are always present for the interconnection in 3D SoC. For sake of space just the main results are reported: By exploiting TSV in 3D technology inductors up to 1 nH can be realized with working frequencies up to 5 MHz, enough for vehicles.

V. 3D INTEGRATED POWER MECHATRONIC SYSTEM

As proof-of-concept demonstrator of the capabilities offered at system level by the innovations at process/device level the project aims at developing an electrical belt system generator-alternator for 48 V micro/mild hybrid applications. This module, see Fig. 10, has a digital control for the current in the rotor and commands the drivers of the power MOSFETs of the inverter. Inputs are taken from several sensors and hence analog, digital and power devices have to be integrated in the same 3D platform, thus realizing an embedded mechatronic system. To this aim, the results of ATHENIS_3D allow to assemble die on die from different technologies thanks to TSV and interposer: e.g. non-volatile TAS-MRAM can be directly stacked on a 28 nm SoC processor in charge of all digital control and interface tasks of the system in Fig.10. The 3D allows routing between dies with RDL technology and enables power components (e.g. the H-Bridge for rotor current control in Fig. 10) to be integrated on substrate thanks to bumps. In addition, discrete components such as ceramic capacitors can be mounted on top of the die with combination of deep trench substrate capacitors within the die.

Insulation between the different voltage domains of the power system of Fig. 10 are ensured by an inductorless multi-output DC-DC converter architecture, patented in [16]. By exploiting the switching capacitor approach the converter avoids the use of cumbersome inductors and transformers, difficult to be integrated in a semiconductor process.

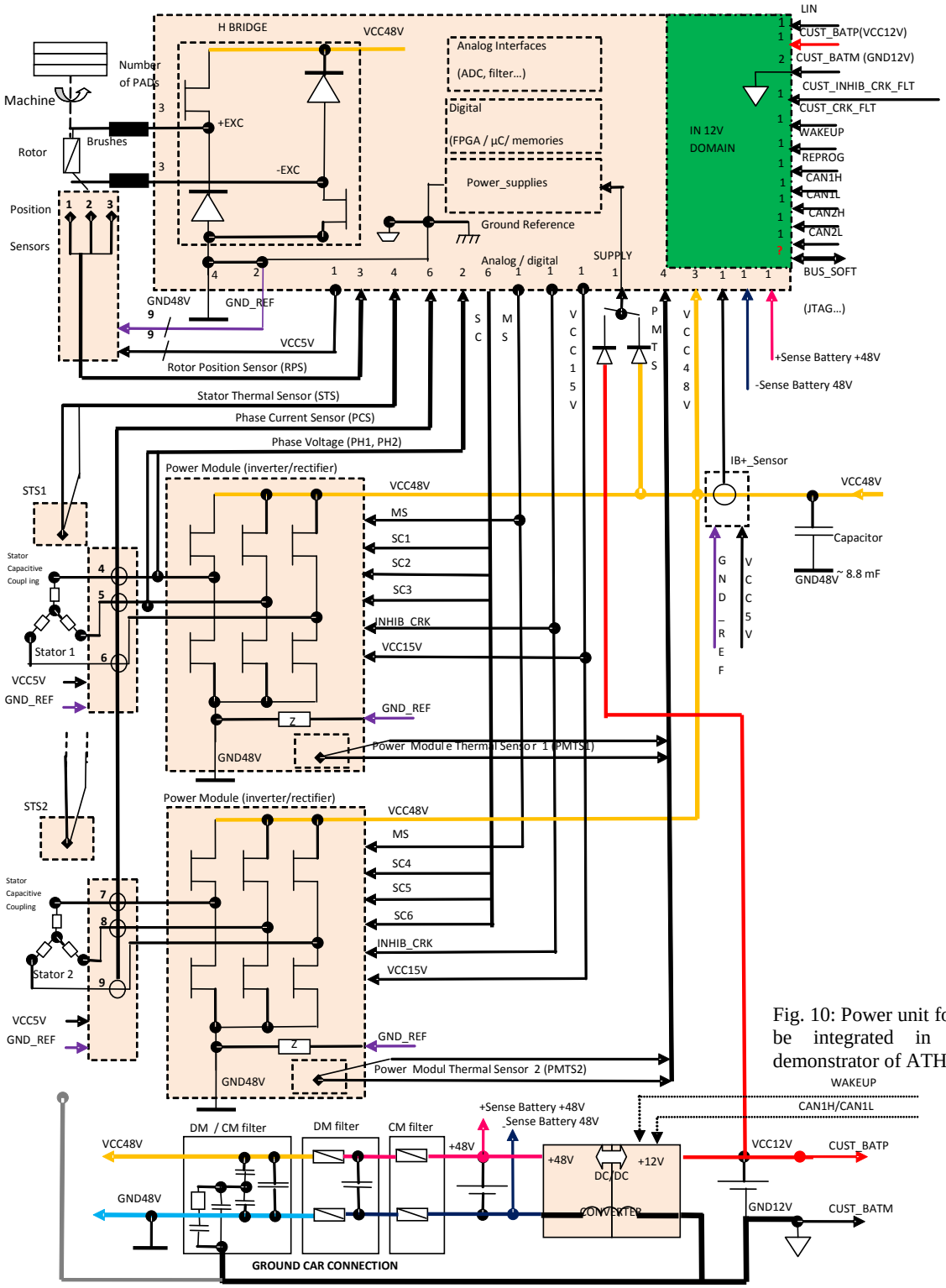

Fig. 10: Power unit for hybrid/electric vehicle to be integrated in 3D as proof-of-concpt demonstrator of ATHENIS_3D innovations

The DC DC converter regulates the 48V power DC domain to lower voltage outputs required by analog parts, sensors and digital parts (memory, processor, interface) at 12V, ±5V, 1.5V. The design has been realized in a 0.35 µm HVMOS technology with transistors operating up to 70 V at a main frequency of 90 kHz. The frequency value has been derived after careful EMI/EMC analysis in the automotive environment. To keep the power efficiency comparable to that of conventional DC DC switching converters using inductors, in our design the jump between input and output voltages is realized in multiple cascade stages. Indeed in switched capacitor power converters poor efficiency values are obatined with large ratios between input and output voltages. As result, without using inductors but just capacitors (with values from 100 nF to 10 uF) the design allows to regulate high input voltages (nominal 48V, but facing drops down to 6V due to battery cranking or overvalues up to 60V) to several values down to 1.5 V. The power efficiency is up to 85%, the power supply rejection ratio (PSRR) is at least 40 dB at low frequencies (-90 dB at the switching frequency) and the voltage ripple is less than 8 mV. Galvanic isolaton is still ensured with series cpacitive isolator without using heavy and cumbersome ferromagnetic cores. The swicthing phases are generated internally starting from a ring oscillatr operating at 32 MHz and are modulated according to a skip-mode algorithm, similar to a PWM control but without using a fixed frequency. This allows for a spreading of the generated electromagnetic noise and hence improve EMI performance of the circuit.

Another key block of the ATHENIS_3D platform is the SoC realized in 28 nm including a 32-bit MIPS microAPTIVE CPU, enhanced by a DSP co-procssor engine with floating point units, on chip memory, 12bit embedded SAR ADC, I/O peripherals (SPI, UART, JTAG, GPIO) and external memory interface to the non volatile TAS-MRAM. Target clock frequency is 200 MHz. This SoC processing platform will be the first in Euope characterized at high temepatures to work safely up to 200 ^{0}C worst case (although at reduced speed as the temperature increseas) while state of art processing platforms in scaled 14/28 nm technologies are limited at 100/125 ^{0}C. Moreover the SOC28 nm processing unit will be integrated with non-volatile TAS-MRAM and passive devices in a compact 3D device, as showed in Fig. 11.

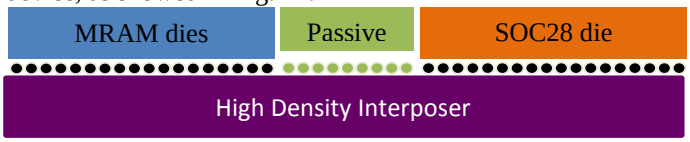

Fig. 11: 3D assembling of MRAM with the SoC28 die

All the innovations of ATHNIS3D will permit a revolution at system level where complex power and mechatronic systems operating at high temperature and high voltage, see Fig. 12, can be integrated in 3D in an embedded mechatronic module where the size and weight is reduced by more than one order of magnitude ("empty" contol module in Fig. 12) vs. conventional solutions with off-chip passive devices, and power FETs, digital processors and memories assembled on a PCB.

VI. Conclusions

Innovations in ATHENIS_3D at process/device levels (3D chip stacking, WLP, integrated passive devices, high-reliable NV-MRAM), operating at high voltage and high temperature enable the realization of complex power and control modules for electric/hybrid vehicles in a 3D structure with one order of magnitude area reduction vs. classic PCB-based systems. The 3D approach allows using the best technology for each subsystem: 0.35 µm HVMOS for the 48 V DC DC converter, 28 nm CMOS for the SoC computing platform, Magnetic material for high-reliable NV memory, trench-capacitor and TSV- inductors for integrated passive devices.

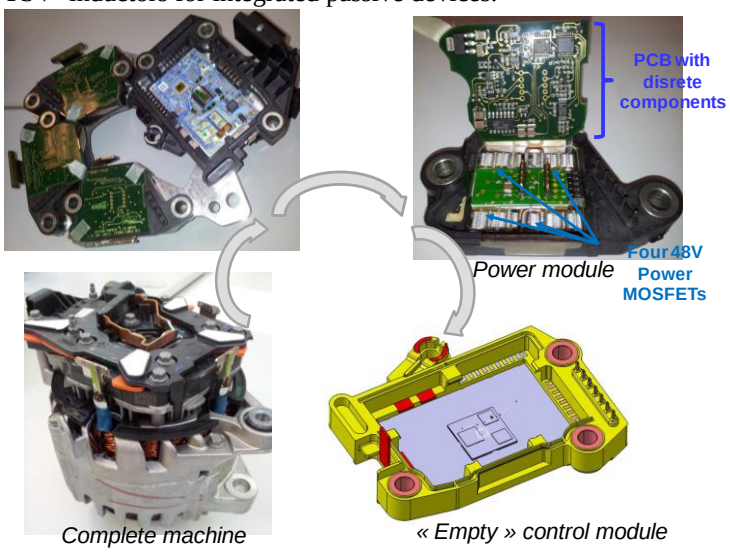

Fig. 12: Evolution from a classic power unit to a compact 3D integrated embedded power mechatronic system

References

[1] L. Yang et al., "NOx control technologies for Euro 6 diesel passenger cars", Int. Council Clean Transportation, White Paper, pp. 1-22, Sept. 2015
[2] K. Sakuma et al., "3D chip stacking technology with low-volume lead-free interconnections," IEEE ECTC 2007, pp. 627–632
[3] P. Coudrain, et al., "3D Integration of CMOS image sensor with coprocessor using TSV last and microbumps technologies," IEEE ECTC 2013, pp.674–682
[4] G. Pares, et al.,"Full integration of a 3D demonstrator with TSV first interposer, ultra thin die stacking and wafer level packaging," ECTC 2013, pp. 305–306
[5] W. Gallagher et al., "Recent advances in MRAM technology," IEEE VLSI TSA Int. Symp., 2005, pp. 72–73
[6] R. Sousa, et al. "Tunneling hot spots and heating in magnetic tunnel junctions," J. of App. Phys., vol. 95, pp. 6783–6785, 2004
[7] J. Azevedo, et al., "A complete resistive-open defect analysis for thermally assisted switching MRAMs," IEEE Tran. VLSI Systems, vol.22, pp. 2326–2335, 2014
[8] I. Prejbeanu et al., "Thermally assisted MRAM," J. Phys. Condens. Matter, vol. 19, pp. 165 218–165 241, 2007
[9] A. Grossi, C. Zambelli, et al., "Automated characterization of TAS-MRAM test arrays," IEEE DTIS 2015, pp. 1–2
[10] A. Grossi, C. Zambelli, et al., "Reliability and Cell-to-Cell Variability of TAS-MRAM arrays under cycling conditions", 15th NVMTS, 2015.
[11] P. Jain, "Integrated thin-film capacitors," in Proc. CPES Annu. Rev., Blacksburg, VA, pp. 155–158, 2000.
[12] Commercially available SMD devices: Parts catalogues from Murata, AVX and EPCOS. 2015
[13] C. Bunel et al., "Silicon capacitors with extremely high stability and reliability ideal for high temperature applications," HiTEC2012, Baltimore
[14] N. Costantino et al., "Design and test of an HV-CMOS intelligent power switch with integrated protections and self-diagnostic for harsh automotive applications", IEEE Tran. on Industrial Electronics, vol. 58, p. 2715-2727,2011
[15] S. Saponara, "Slew-rate boosted amplifier integrated in a digital input driver for automotive actuator control units", Analog Integrated Circuits and Signal Processing, vol. 84, n. 2, pp 325-331, 2015
[16] P. Tisserand et al., "Convertisseur DC-DC integrable sur silicium avec isloation galvanique capacitive", French Patent n. 15/58664, 15/9/2015