Automated characterization of TAS-MRAM test arrays

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***Abstract*—In this work the characterization results of 1kbit TAS-MRAM arrays obtained through RIFLE Automated Test Equipment of 1Kbit array are reported. Such ATE, ensuring flexibility in terms of signals and timing, allowed evaluating hysteresis and to perform 50k write cycles in a very limited time, getting a first insight on TAS-MRAM arrays performance and reliability.**

I. Introduction

Magnetic Random Access Memories (MRAM) is considered an extremely promising nonvolatile memory technology [1], [2]. Among existing MRAM technologies, Thermally Assisted Switching (TAS) MRAM offers several advantages such as selectivity, single magnetic field and high integration density [3], [4]: the information storage mechanism is based on the current-induced magnetization switch of a magnetic material [5]. After that the performance of single cells structures have been deeply investigated [6], [7] and a maturity level of the technology has been reached, the performance evaluation at integrated array level is mandatory. MRAM cells show endurance capabilities up to 1 million cycles, thus faster testing systems are required compared to standard flash memories to perform endurance and disturbs analysis in a reasonable time. To face these issues we have developed a new Automated Test Equipment (ATE) able to offer high computation capabilities and the flexibility required by research analysis on MRAM test arrays. In this work the preliminary characterization results obtained through ATE of 1Kbit array are reported: the switching voltage hysteresis variability has been deeply investigated, furthermore 50k write cycles have been performed in order to get a first insight on testing time and endurance performances.

II. Memory architecture and Experimental setup

The 1 Kbits memory device is made of a 32x32 array integrated into a CMOS process from Crocus Technologies. In order to change the state of the memory cells, two different writing operations are available: Write '0' (W0) and Write '1' (W1). Both operations require two pulses: V_{FORCE} is required to locally heat the magnetic material, whereas V_{SWITCH} allows changing the magnetic field polarization after heating. Functionality of magnetoresistive elements depend directly on the shape of magnetisation hysteresis loops [8]: switching voltage hysteresis has been evaluated on fresh devices increasing $|V_{SWITCH}|$ from 0.2 V to 5 V with $|\Delta V_{SWITCH}| = 0.2V$ with $|V_{FORCE}| = 1.4V$, $T_{FORCE} = 10\mu s$, $T_{SWITCH} = 20\mu s$ and $T_{rise/fall} = 1\mu s$ on both voltages in order to avoid overshoot issues. These timings are dictated by the architecture of the test chip and not by ATE limitations. The cell structure and the W0 hysteresis voltage scheme are depicted in Fig. 1: MTJ is the Magnetic Tunnel Junction device, $SP_{1,2,3}$ are sense pads used during read. W1 voltage scheme is not reported since it's equivalent to W0 scheme but decreasing V_{SWITCH} from -0.2 V to -5 V with $\Delta V_{SWITCH} = -0.2V$). All read operations have been performed with $V_{SWITCH} = 0V$, $V_{HEAT} = 0.3V$, $T_{HEAT} = 20\mu s$ and $T_{rise/fall} = 1\mu s$.

III. Experimental Results

The average resistance and standard deviation measured during switching voltage hysteresis are reported in Fig. 2. Cumulative distribution functions evolution measured during W0 (a) and W1 (b) hysteresis are shown in Fig. 3. The average resistance is strongly reduced after the first step ($V_{SWITCH} = 0.2V$) during W0 hysteresis, whereas W1 hysteresis requires higher voltages: the minimum inter-device variability is obtained with $V_{SWITCH} = -5V$. The distribution of the resistances measured during W0(R_{W0}) and W1 (R_{W1}) as a function of V_{SWITCH} are shown in Fig. 4. To preliminary evaluate the cells performance, the cycle to cycle variability, and reliability during cycling, 50k W0 and W1 operations been performed on a single page with $V_{FORCE} = 1.4V$ and $|V_{SWITCH}| = 5V$, $T_{FORCE} = 50\mu s$, $T_{SWITCH} = 60\mu s$ and $T_{rise/fall} = 1\mu s$: Fig. 5 shows the endurance results obtained in terms of average resistance and cumulative probability distributions. The tunnel magnetoresistance (TMR) [9] evolution during cycling has been analyzed in terms of average value and cumulative probability distributions: the results are shown in Fig. 6. The test lasted 30 minutes using full chip W0 and full chip W1 patterns. There are no limits in patterns application on the tested memory. If complex patterns like random device programming or checkerboards are applied on the memory, there are no significant time overheads.

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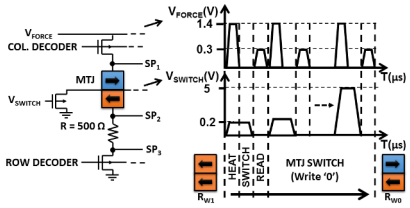


Fig. 1. V_{SWITCH} hysteresis measured during W0 and W1 operations with $V_{HEAT} = 1.4V$.

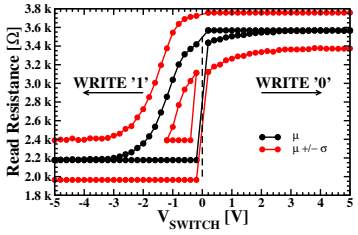
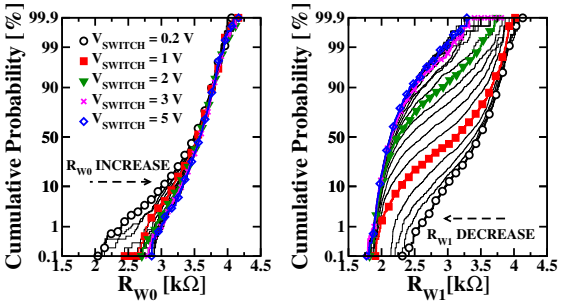


Fig. 2. V_{SWITCH} hysteresis measured during W0 and W1 operations with $V_{HEAT} = 1.4V$.



(a) (b)

Fig. 3. Cumulative density functions measured during V_{SWITCH} hysteresis in W0 (a) and W1 (b) operations on fresh device, with $V_{HEAT} = 1.4V$.

IV. Conclusions

The preliminary analysis performed on TAS-MRAM demonstrated the validity of the developed ATE, allowing to investigate and understand the hysteresis and endurance properties of the technology in terms of cell-to-cell variability and reliability.

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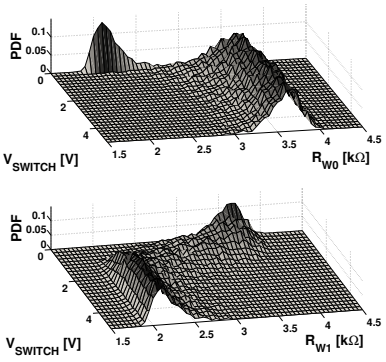
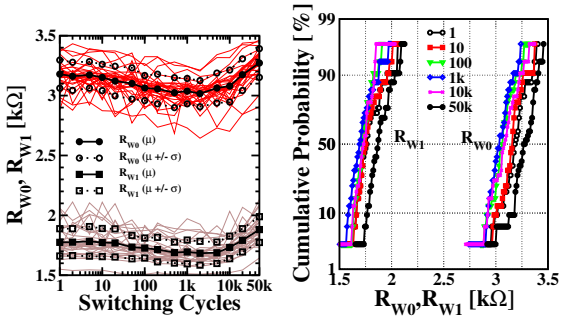
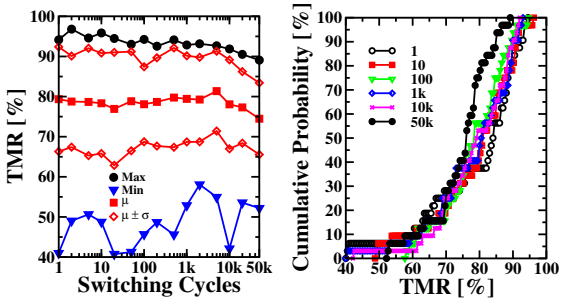


Fig. 4. 3D plot representing the R_{W0} and R_{W1} distributions during V_{SWITCH} hysteresis with $V_{HEAT} = 1.4V$.



(a) (b)

Fig. 5. R_{W0} and $RW1$ measured on a page during 50k cycles with $V_{HEAT} = 1.4V$, $V_{SWITCH} = 5V$ (a) and their cumulative probabilities (b).



(a) (b)

Fig. 6. TMR cumulative density function average value (a) and cumulative probability at different endurance cycles (b).

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