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Modelling and Regulation of Dual-Output LCLC Resonant Converters

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Abstract-**The analysis, design and control of 4th-order LCLC voltage-output series-parallel resonant converters (SPRCs) for the provision of multiple regulated outputs, is described. Specifically, state-variable concepts are employed and new analysis techniques are developed to establish operating mode boundaries with which to describe the internal behaviour of a dual-output resonant converter topology. The designer is guided through the most important criteria for realising a satisfactory converter, and the impact of parameter choices on performance is explored. Predictions from the resulting models are compared with those obtained from SPICE simulations and measurements from a prototype power supply under closed loop control.**

I. INTRODUCTION

With the increased power capability, improved control and reduced cost of power semiconductor devices, designers of electronic equipment, computers and electronic instrumentation are increasingly demanding higher energy and more efficient power supplies. Moreover, the trend towards miniaturisation of electronic systems, particularly for communication and entertainment products, and the emergence of improved power switch technologies, is leading to the use of switching frequencies in the 100s kHz to several MHz range. To improve the overall power density of resonant power supplies, research is now being directed towards converter topologies that can provide multiple regulated outputs—particular growth areas being the telecommunications, computer and microprocessor industries, with mobile phones, PDAs and handheld products typically requiring 3.3V, 5V, ±12V and ±15V supplies for various interfaces. However, cross-regulation errors that accompany output load variations, which manifests itself by the regulation of one output voltage impacting on the performance of others, can be a significant limitation for voltage sensitive electronic systems.

II. MULTI-OUTPUT CONVERTERS

To-date, several approaches have been explored to address cross-regulation, complexity and overall circuit performance issues of multi-output converters, the solutions being divided into three distinct categories. The first regulates a single primary output using closed-loop feedback, with the auxiliary outputs being semi-regulated and, therefore, subject to cross-regulation error. The second category achieves precise post-regulation of each output by using either linear regulators or hard-switched dc-dc converters. However, although relatively straightforward to design, such circuits are rarely used in practice due to cost constraints. The third category is specific to applications which require only two regulated outputs, as is commonly found in signal processing and microprocessor based systems. They avoid the need for post-regulation by utilising two closed-loop feedback configurations. A 3rd-order LLC converter with two independently controlled outputs was reported in [1]. However, optimum performance characteristics have yet to be forthcoming, primarily due to the significant complexity associated with the highly non-linear behaviour between the various outputs as a function of load. Nevertheless, it is a solution that broadly falls within this third category that is the subject of this paper. Specifically, dual-output resonant LCLC converters, are considered, with control of each output being achieved by switching the power devices asymmetrically over each half switching cycle using a combination of PWM and frequency control.

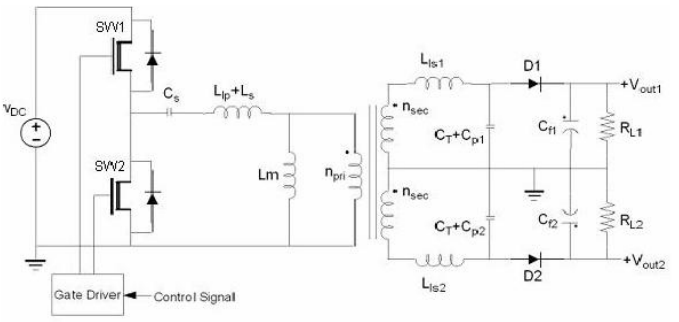
III. DUAL O/P LCLC-SPRC MODEL

A half-bridge LCLC-SPRC with two outputs is shown in Fig. 1(a). To demonstrate the ability of the converter to deliver asymmetrical output voltages under balanced load conditions, the transformer is constrained to have unity turns-ratios for both outputs and the high- and low-side parallel resonant capacitors are constrained to have identical values. Since current flows through the primary side of the transformer to the top and bottom sides of the rectifier during different half-cycles of tank excitation, see Fig. 1(b), each output is replenished with energy alternately.

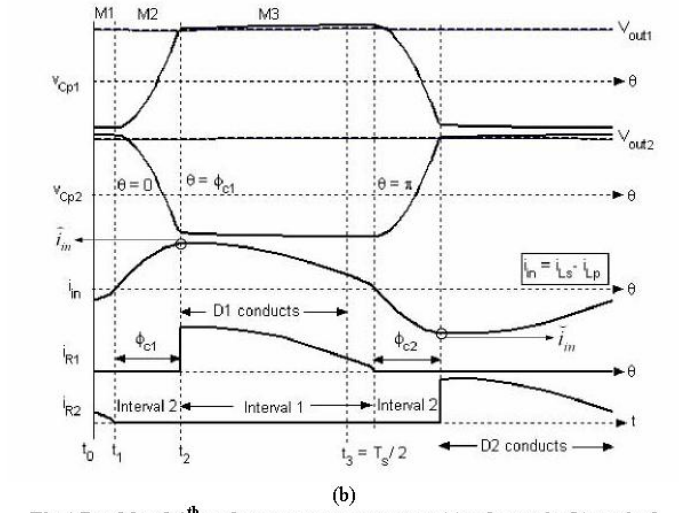
IV. PRINCIPLE OF OPERATION

To achieve zero-voltage switching, the converter is assumed to operate on the negative gradient of the input-output frequency characteristic, above the primary resonant peak. When operating in this region, the resulting waveforms can be sub-divided into two distinct time intervals, viz. intervals 1 and 2, as depicted in Fig. 1(b):

Interval 1: Clamping of the parallel capacitor voltage. Here, the combined series inductor L_s+L_{lp} and capacitor C_s provide resonant behaviour whilst the voltage across the effective parallel tank inductor and capacitor (L_p (L_m) and C_p) is clamped by the output voltage. As the current through the series inductor, L_s, decays to zero, C_p begins to contribute to resonant behaviour, and operation enters the second interval.



(a)



(b)

Fig.1 Dual-load 4th-order resonant converter (a) schematic (b) typical operating waveforms

Interval 2: Decoupling of the rectifier and output filter. Here, all the tank components contribute to resonant behaviour, with the rectifier effectively becoming reverse biased. Current into both the high- and low-side diodes remains zero, and the parallel capacitors are charged until their voltage is clamped at either $+V_{out1}$ or $-V_{out2}$, thereby providing the boundary at the end of this time interval. During each half-cycle of operation, three Modes, M1, M2, and M3 can be identified, as shown in Fig. 1(b).

Circuit Mode M1 $(t_0 \le t < t_1)$. At the start of M1, SW2 is turned off at t_0 and SW1 turned on. The series inductor current, i_{Ls}, is negative and flows through the internal diode of SW1, thereby facilitating ZVS of SW1. Also during this period, i_{Ls} allows D2 to conduct and transfer energy to support V_{out2}, whilst the voltage on C_{p2} is clamped to V_{out2}. All the rectifier current, therefore, flows to the load. At the end of M1, the rectifier current i_{R2} has decayed to zero, and both the high side and low side diodes, and the output filter, are effectively decoupled from the resonant tank.

Circuit Mode M2 $(t_1 \le t < t_2)$. Here, the series resonant inductor current i_{Ls} becomes positive. Since SW1 is turned on during M1, current flow is now through SW1. Initial conditions for this mode are that i_{Ls}=0 and v_{cp2}= V_{out2}. The inductor current i_{Ls} and parallel resonant capacitor voltages take on a sinusoidal characteristic. Since the outputs are effectively disconnected from the tank, both C_{p1} and C_{p2} contribute to resonant behaviour. Both rectifier currents are zero, and the converter outputs are in an 'idle' state with energy being supplied solely by the charge on the filter capacitors. By initially neglecting the rectifier on-state voltage, and noting that the effective parallel resonant capacitance C_p is the sum of the shunt network capacitances C_{p1} and C_{p2}, v_{Cp1} during the capacitor charging period is described by:

$$v_{Cp1}(t) = v_{Cp1}(t_1) + \frac{1}{C_p}\int_{t_1}^{t_2} \hat{i}_{in} \sin(2\pi f_s t)dt \qquad (1)$$

where $\hat{i}_{in} = i_{Ls} - i_{Lp}$. Evaluating (1) with initial conditions $v_R(t_1) = v_{Cp1}(t_1) = -V_{out2}$ yields:

$$v_{Cp1}(t_2) = -V_{out2} + \hat{i}_{in} \times \frac{1-\cos(2\pi f_s(t_2 - t_1))}{2\pi f_s C_p} \qquad (2)$$

The boundary for the end of the capacitor charging period is $v_{Cp1}(t_2) = +V_{out1}$, which yields the rectifier non-conduction angle, ϕ_{c1}, associated with a positive polarity of current, i_R, through the high side rectifier:

$$t_2 - t_1 = \frac{1}{2\pi f_s} \times \cos^{-1}(\phi_{c1}) \quad \phi_{c1} = \cos^{-1}\left(1 - \frac{2\pi f_s C_p v_{tot}}{\hat{i}_{in}}\right) \qquad (3)$$

where $v_{tot} = V_{out1} + V_{out2}$.

Circuit Mode M3 $(t_2 \le t < T_s/2)$. At $t = t_2$, D1 becomes forward biased whilst D2 reverse biased. The rectifier diode current i_{R2} remains zero throughout the duration of M3, and D1 clamps the capacitor voltage v_{cp1} to $+V_{out1}$ until i_{Ls} decays to zero, at which time the second half cycle of operation commences.

For 50% duty-cycle excitation, the 2nd half-cycle of operation is the mirror image of the first. However, for asymmetrical excitation, the output rectifier diode (D2) non-conduction angle, associated with the series resonant inductor current being of negative polarity, is given by:

$$\phi_{c2} = \cos^{-1}\left(1 - \frac{2\pi f_s C_p v_{tot}}{\breve{i}_{in}}\right) \qquad (4)$$

where $\breve{i}_{in} = -(i_{Ls} - i_{Lp})$. The voltage, v_{cp1}, across the parallel resonant capacitor can, therefore, be expressed as a function of the angle θ—see Fig. 1(b):

$$v_{Cp1}(\theta) = \begin{cases} -V_{out2} + \dfrac{\hat{i}_{in}}{2\pi f_s C_p} \times (1 - \cos(\theta)) & \text{for } \theta = 0 \ldots \phi_{c1} \\ +V_{out1} & \\ V_{out1} - \dfrac{\hat{i}_{in}}{2\pi f_s C_p} \times (1 - \cos(\theta)) & \text{for } \theta = \phi_{c1} \cdots \pi \\ -V_{out2} & \text{for } \theta = \pi \ldots \pi + \phi_{c2} \\ & \text{for } \theta = \pi + \phi_{c2} \ldots 2\pi \end{cases} \qquad (5)$$

Under steady-state conditions, the mean output current i_{out1}, flowing through D1 towards the output filter and load, can be determined from the mean current flowing through the rectifier when it is of positive polarity. Since this occurs during the interval $\phi_{c1} \le \theta < \pi$, i_{out1} is given by:

$$i_{out1} = \frac{1}{2\pi} \times \int_{\phi_{c1}}^{\pi} \hat{i}_{in} \sin(\theta) d\theta \tag{6}$$

Substituting (3) into (6) and evaluating the integral provides the solution for i_{out1}:

$$i_{out1} = \frac{\hat{i}_{in}}{2\pi} \times (1 + \cos(\phi_{c1})) = \frac{\hat{i}_{in} - \pi f_s C_p v_{tot}}{\pi} \tag{7}$$

Simple mathematical manipulation of (3) and (7) then gives the corresponding rectifier non-conduction angle ϕ_{c1}:

$$\phi_{c1} = \cos^{-1}\left(\frac{\pi i_{out1} - \pi f_s C_p v_{tot}}{\pi i_{out1} + \pi f_s C_p v_{tot}} \right) \tag{8}$$

V_{out1} is determined by assuming the output filter capacitance C_f is sufficiently large to impart negligible output voltage ripple. In this case:

$$V_{out1} = i_{out1} R_{L1} = \frac{\hat{i}_{in} R_{L1}}{2\pi} \times (1 + \cos(\phi_{c1})) = \frac{R_{L1}(\hat{i}_{in} - \pi f_s C_p v_{tot})}{\pi} = \frac{R_{L1}}{\pi} \times \frac{\hat{i}_{in} - \pi f_s C_p V_{out2}}{1 + R_L f_s C_p} \tag{9}$$

Equations (6) to (9) can be further manipulated to provide the complementary D2 non-conduction angle, ϕ_{c2}, and the output current, i_{out2}, and output voltage V_{out2}, as follows:

$$i_{out2} = \frac{\check{i}_{in}}{2\pi} \times (1 + \cos(\phi_{c2})), V_{out2} = \frac{R_{L2}}{\pi} \times \frac{\check{i}_{in} - \pi f_s C_p V_{out1}}{1 + R_L f_s C_p} \tag{10}$$

V. STATE-VARIABLE ANALYSIS

A state-variable model describing the behaviour of the dual-output converter can be obtained by considering the electrical network shown in Fig. 1 and separating the dynamics into 'fast' and 'slow' sub-systems, with their interaction related by a set of coupling equations. The fast sub-system is considered to describe the dynamics of the resonant tank and power switches:

$$\frac{dv_{Cs}}{dt} = \frac{i_{Ls}}{C_s}, \quad \frac{di_{Ls}}{dt} = \frac{V_{in} - v_{Cs} - v_{Lp}}{L_s}, \quad \frac{di_{Lp}}{dt} = \frac{v_{Lp}}{L_p}$$
$$\frac{dv_{Cp1}}{dt} = \frac{i_{Ls} - i_{Lp} - i_{R1} - i_{Cp2} - i_{R2}}{C_{p1}}, \quad \frac{dv_{Cp2}}{dt} = \frac{i_{Ls} - i_{Lp} - i_{R2} - i_{Cp1} - i_{R1}}{C_{p2}} \tag{11}$$

The output filter dynamics are described by:

$$\frac{dv_{cf1}}{dt} = \frac{i_{R1}}{C_{f1}} - \frac{v_{cf1}}{C_{f1} R_{L1}}, \quad \frac{dv_{cf2}}{dt} = \frac{i_{R2}}{C_{f2}} - \frac{v_{cf2}}{C_{f2} R_{L2}} \tag{12}$$

As discussed, during interval $t_1 \rightarrow t_2$ (see Fig. 1(b)) v_{cp1} is clamped to v_{cf1} during the positive half-cycle, and conversely, to -v_{cf2} during the negative half-cycle, due to the action of the diodes. By noting that there will be negligible current flowing through C_p during these periods, the rectifier input voltage is dependent on the direction of the current leaving the resonant tank inductances, i.e. $i_L = i_{Ls} - i_{Lp}$. The relevant coupling terms are, therefore, obtained by equating voltages at either side of the rectifier for each respective half-cycle:

$$v_{Cp1} = \text{sgn}(i_L)(V_{out1} + v_{diode}) = \text{sgn}(i_L)(v_{cf1} + v_{diode})$$
$$v_{Cp2} = \text{sgn}(i_L)(V_{out2} + v_{diode}) = \text{sgn}(i_L)(v_{cf2} + v_{diode}) \tag{13}$$

Assuming a constant rectifier voltage, (12) can be manipulated to:

$$\frac{dv_{Cp1}}{dt} = \text{sgn}(i_L) \frac{dv_{cf1}}{dt}, \quad \frac{dv_{Cp2}}{dt} = \text{sgn}(i_L) \frac{dv_{cf2}}{dt} \tag{14}$$

Considering the rectifier current, i_{R2}, to be zero during the positive half-cycle of the parallel capacitor voltage, the rectifier current i_{R1}, is given from:

$$\frac{i_L - i_{R1} - i_{Cp2} - i_{R2}}{C_{p1}} = \text{sgn}(i_L)\left(\frac{i_{R1}}{C_{f1}} - \frac{v_{cf1}}{C_{f1} R_{L1}} \right)$$
$$\therefore i_{R1} = \frac{C_{p1} C_{f1}}{\text{sgn}(i_L) C_{p1} + C_{f1}} \left(\frac{i_L - i_{Cp2} - i_{R2}}{C_{p1}} + \frac{\text{sgn}(i_L) v_{cf1}}{C_{f1} R_{L1}} \right) \tag{15}$$

This leads to the following coupling equations which describe the rectifier currents within each half of a switching cycle:

$$i_{R1} = \begin{cases} \dfrac{C_{p1} C_{f1}}{\text{sgn}(i_L) C_{p1} + C_{f1}} \left(\dfrac{i_L - i_{Cp2} - i_{R2}}{C_{p1}} + \dfrac{\text{sgn}(i_L) v_{cf1}}{C_{f1} R_{L1}} \right) & \text{for } v_{Cp1} = V_{out1} + v_{diode} \\ 0 & \text{for } v_{Cp1} < V_{out1} + v_{diode} \end{cases}$$

$$i_{R2} = \begin{cases} \dfrac{C_{p2} C_{f2}}{\text{sgn}(i_L) C_{p2} + C_{f2}} \left(\dfrac{i_L - i_{Cp1} - i_{R1}}{C_{p2}} + \dfrac{\text{sgn}(i_L) v_{cf2}}{C_{f2} R_{L2}} \right) & \text{for } v_{Cp2} = V_{out2} + v_{diode} \\ 0 & \text{for } v_{Cp2} < V_{out2} + v_{diode} \end{cases} \tag{16}$$

Notably, the voltage across L_p can be considered a reflection of the voltages across C_{p1} and C_{p2}, and the state vector for the parallel inductor current in the fast sub-system (see (11)) simplifies to $v_{Lp} = v_{Cp}$. The state-variable equations for the parallel resonant capacitor voltage (11) can be simplified to:

$$\frac{dv_{Cp1}}{dt} = \frac{i_{Ls} - i_{Lp} - i_R}{2C_{p1}}, \quad \frac{dv_{Cp2}}{dt} = \frac{i_{Ls} - i_{Lp} - i_R}{2C_{p2}} \tag{17}$$

The complete state-variable model of the dual load converter (excluding the effects of output leakage inductances) is, therefore, given by:

$$\dot{\mathbf{x}} = \begin{bmatrix} 0^{3\times3} & \mathbf{A}_1 & 0^{2\times3} \\ \mathbf{A}_2 & 0^{2\times2} & 0^{2\times2} \\ 0^{2\times3} & 0^{2\times2} & \mathbf{A}_3 \end{bmatrix} \mathbf{x} + \mathbf{B} \tag{18}$$

where

$$\mathbf{x} = \begin{bmatrix} v_{Cp1} & v_{Cp2} & v_{Cs} & i_{Lp} & i_{Ls} & v_{Cf1} & v_{Cf2} \end{bmatrix}^T$$

$$\mathbf{A}_1 = \begin{bmatrix} -\dfrac{1}{2C_{p1}} & \dfrac{1}{2C_{p1}} \\ -\dfrac{1}{2C_{p2}} & \dfrac{1}{2C_{p2}} \\ 0 & \dfrac{1}{C_s} \end{bmatrix}, \quad \mathbf{A}_2 = \begin{bmatrix} \dfrac{1}{L_p} & 0 & 0 \\ -\dfrac{1}{L_s} & 0 & -\dfrac{1}{L_s} \end{bmatrix}, \quad \mathbf{A}_3 = \begin{bmatrix} -\dfrac{1}{C_f R_{L1}} & 0 \\ 0 & -\dfrac{1}{C_{f2} R_{L2}} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} -\dfrac{i_R}{2C_{p1}} & -\dfrac{i_R}{2C_{p2}} & 0^{1\times2} & \dfrac{V_{in}}{L_s} & \dfrac{i_{R1}}{C_{f1}} & \dfrac{i_{R2}}{C_{f2}} \end{bmatrix}^T \tag{19}$$

The model can used to investigate the behaviour of dual load converters when subject to asymmetrical input excitation. By way of example, the parameters of a candidate converter are

given in Table I when supplied from a 30V dc link. A plot of the resulting steady-state output voltage characteristics of the converter, V_{out1} and V_{out2}, as a function of switching frequency and duty-cycle ratio is given in Fig. 2. It is evident that for operation above resonance, the sum of the output voltages applied to the loads increases as the operating frequency tends to the effective resonant frequency, for fixed values of duty-cycle ratio. Furthermore, for a 50% duty-cycle, giving symmetric square-wave excitation of the tank, the converter delivers identical voltages to both the high side and low side outputs, for a fixed operating frequency, as expected.

For a given operating frequency, a decrease in the duty-cycle ratio, from 50%, is seen to deliver more energy from the resonant tank to energize output V_{out1}, thereby yielding a correspondingly higher output voltage and power, and vice-versa. It is, therefore, clear that for balanced loads, the voltage and power distribution to each output can be independently influenced by a suitable choice of duty ratio and switching frequency. For completeness, Fig. 3 compares the ratio of the two realisable output voltages, from which it can be seen that the slope of the curve is greater for lower values of switching frequency. This implies that when a large difference between the output voltages is required, the converter should be operated close to resonance, leading to high efficiency operation, and zero voltage switching. However, this also means that the tank components are subjected to higher electrical stresses.

For asymmetric excitation of the converter, the duties of SW1 and SW2 are denoted, respectively, by D and 1-D, where D is the ratio of the turn-on period with respect to the switching period. Asymmetric switching therefore provides an asymmetrical voltage source V_{in} to excite the tank, of amplitude v_{DC}:

$$V_{in} = \begin{cases} v_{DC} & \theta = 0 \ldots 2\pi D \\ 0 & \theta = 2\pi D \ldots 2\pi \end{cases} \quad (20)$$

Assuming that only the fundamental component excites the resonant tank, and applying the relationship $\tan^{-1}(\cos(\theta)/\sin(\theta)) = \pi/2 + \theta$, the fundamental of the input voltage, $v_{in(1)}$, and its phase angle, $\phi_{vi(1)}$ are given by:

$$v_{i(1)} = \frac{2v_{DC}}{\pi}\sqrt{1-\cos(2\pi D)} \times \sin\left(\omega t + \phi_{vi(1)}\right) \qquad \phi_{vi(1)} = \frac{\pi}{2} - \pi D \quad (21)$$

The condition for inductive switching can now be written as $\beta_{in} \geq \pi(0.5 - D)$, where β_{in} is the phase lag between the fundamental of the input voltage and current).

TABLE I
CONVERTER MODEL PARAMETERS

Parameters	*Value*
Characteristic impedance (Ω)	2.5
Resonant frequency, f_o (kHz)	130
Resonant capacitance ratio, C_n	0.03
Resonant inductance ratio, L_n	0.01
Series load quality factor, Q_{op1}	6

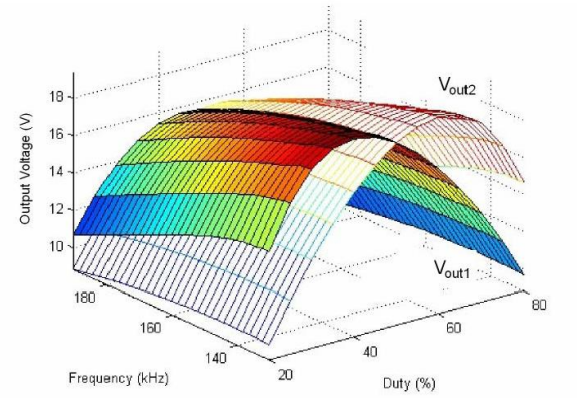


Fig.2 Variation of output voltage distribution with switching frequency and duty-cycle ratio

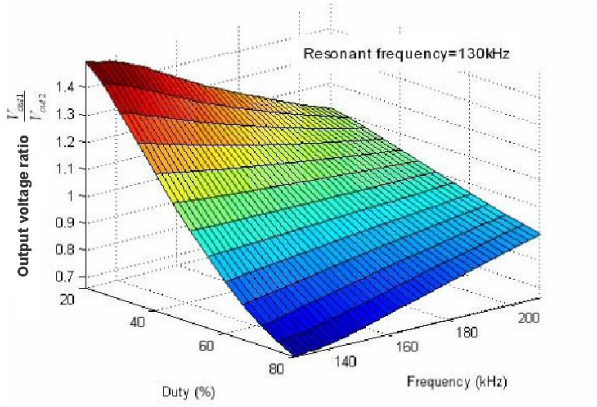


Fig.3 Variation of normalised asymmetrical output voltage with switching frequency and duty-cycle ratio

VI. EXPERIMENTAL RESULTS

Measured results have been obtained on an experimental converter with a step-down capability, the measured component values being given in Table II. A ferrite core, 3F3, suitable for high frequency applications, was used for both the transformer core and the resonant inductor. Since the transformer leakage inductances are dependent on the winding arrangement, the secondaries were bifilar wound adjacent to the core, beneath the primary winding, so as to reduce secondary leakage flux.

TABLE II
PROTOTYPE DUAL OUTPUT CONVERTER COMPONENT VALUES

Parameter	*Value*
DC link input voltage, v_{DC} (V)	15
Series resonant inductances, L_s (μH)	0.85
Series resonant capacitances, C_s (μF)	1.5
High side parallel resonant capacitances, C_{p1} (μF)	0.116
Low side parallel resonant capacitances, C_{p2} (μF)	0.116
Load resistance, R_L (Ω)	4
Transformer turns ratio	1
Filter capacitance, C_f (μF)	100
Transformer output leakage inductance, L_{ls} (μH)	0.1
Magnetising inductance, L_m (μH)	109
Transformer primary leakage inductance, L_{lp} (μH)	0.7

The parallel resonant inductor is designed to be on the transformer primary side, such that L_p utilises the magnetising inductance, L_m, of the transformer. The effective series inductance comprises of the series inductor, L_s, and the primary leakage inductance, L_{lp}, and was measured as 1.55µH. The transformer output networks have two identical inductances and the assignment of the polarity of the rectifier current is realised through winding orientation. A comparison of the output voltage obtained from the state variable model (11-19), simulated to steady-state, with SPICE simulation results and measurements, is given in Fig. 4. As is clearly evident, the correlation between the theoretical predictions and the experimental data is extremely good. Moreover, a comparison of simulated and measured characteristics, when duty-cycle ratio control is employed, has also been obtained at an operating frequency of f_s=150 kHz. The results are shown in Fig. 5 from which it can be seen that the proposed state-variable model provides sufficient accuracy for design and analysis purposes, the maximum error being <5%. The minimum duty-cycle ratio at f_s=150 kHz is selected to be 25% in order to prevent the converter from entering the capacitive conduction mode.

VII. CLOSED-LOOP CONTROL

A basic digital control scheme has been realised to demonstrate closed-loop regulation of both dual output voltages when subjected to load and line voltage disturbances. The structure of the control methodology, which employs two decoupled feedback loops for independent control of frequency and duty-cycle ratio, is shown in Fig. 6. Voltage feedback modulation is employed to avoid the need for relatively expensive current sensors, and the control structures are based on linear proportional compensators in this case, as a proof of principle. For design purposes, the output voltage versus switching frequency and duty-cycle ratio characteristics of the converter are approximated to be linear over the frequency range of interest (f_s=156 to 220 kHz). Although various methodologies could be considered for the design of the compensator gains, the controller parameters are selected empirically for robust tracking of the references. Here then, parameters for the decoupled SISO controllers are chosen for good transient response and disturbance rejection. Notably, the digital compensator is tuned to respond quickly to variations of V_{out1}, whilst the controller reacting to variations of V_{out2}, acts relatively slowly, thereby allowing an effective decoupling of the control loops, for simplicity. The prototype converter controller is shown in Fig. 7. The converter (see Table II for parameters) is required to provide regulated +5V and +3.3V outputs from a DC link input voltage in the range 15V to 20V.

Figure 8 shows the steady-state error between the reference voltages, V_{ref1} and V_{ref2}, and the resulting measured output voltages of the converter, over the specified range of DC link input voltages (15V to 20V) with a 5Ω load.

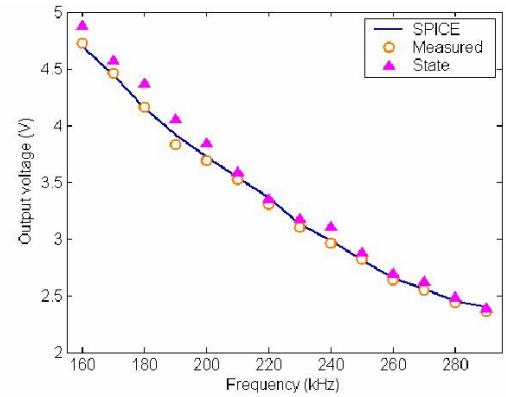
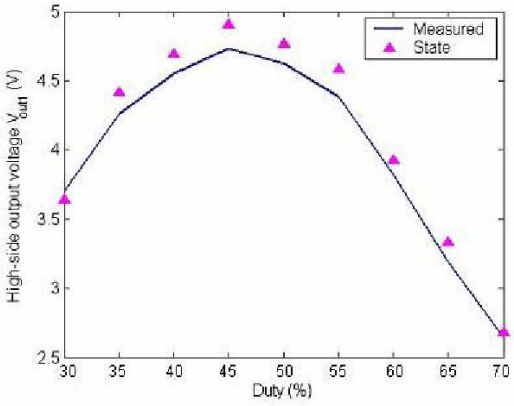
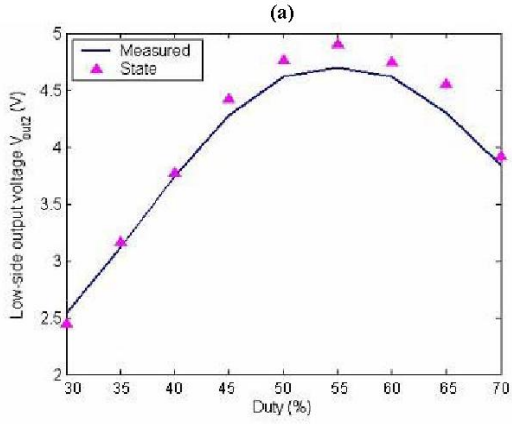


Fig. 4 Output voltage vs switching frequency



(a)



(b)

Fig. 5 Control characteristic curves for f_s=150 kHz (a) high side output, and (b) low side output.

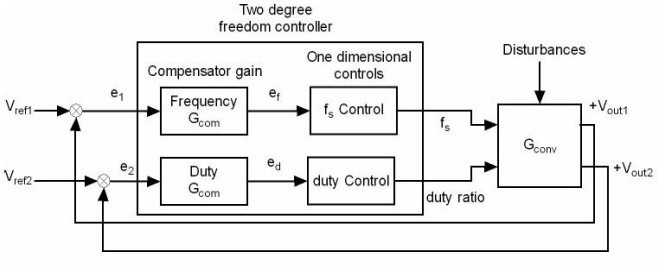


Fig. 6 Closed-loop control of the dual-load converter.

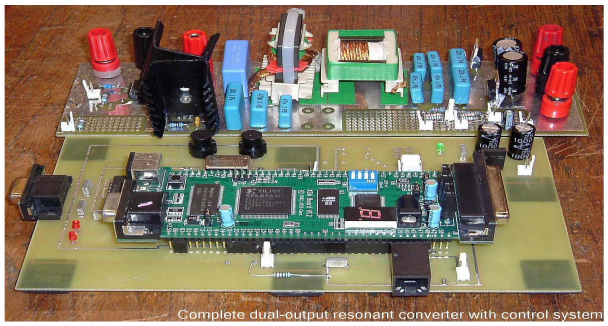


Fig. 7 Digital control of dual-output converter.

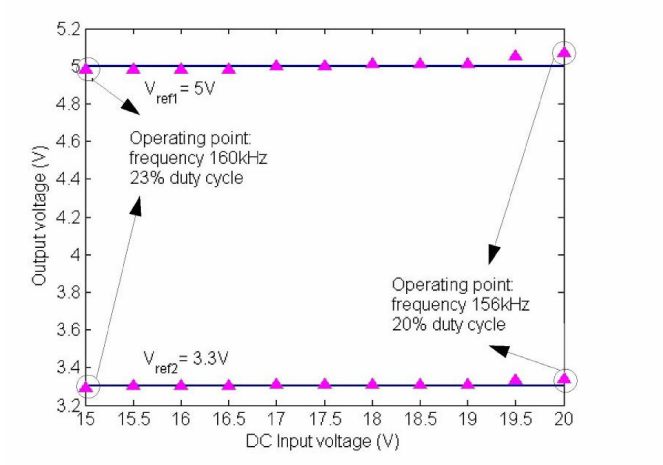


Fig. 8 Output voltage regulation vs. input voltage

It can be seen that the maximum regulation error for both outputs is <5%. Finally, Fig. 9 shows the response of the converter resulting from transient start-up conditions, for a range of applied input voltages and dual output voltage ratios. It can be seen that the converter voltages converge rapidly to the reference values, with an initial overshoot of ~10%, corresponding to an equivalent 2nd-order damping ratio of $\zeta \approx 0.6$.

VIII. CONCLUSIONS

The characteristics of dual-load, 4th-order LCLC voltage-output resonant converters, have been explored. State-variable models have been derived. From the output voltage distribution derived from an example converter, the impact of the converter design parameters on the attainable output voltage ratio has been investigated, and subsequent design trade-offs have been discussed. Furthermore, the condition and minimum frequency which is necessary to preserve ZVS has been given for high efficiency converter operation. A comparison of measurements from an experimental converter, capable of delivering 5V and 3.3V, with predictions from the derived state-variable model and SPICE simulations, shows that the state-variable model provides accurate predictions of output voltage under steady-state conditions. Moreover, a basic control scheme to allow reliable regulation of both outputs, has been realised, with steady-state measurements showing independent regulation using a combination of duty-cycle and frequency control, and good start-up transient behaviour on both outputs under a range of operating conditions.

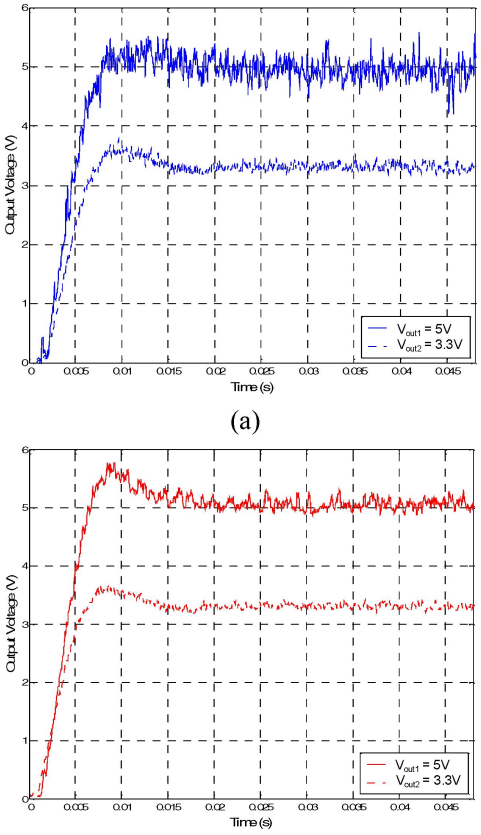


Fig. 9 Start-up transient response for various dual output voltage ratios and DC-link input voltages (a) v_{DC}=15V, V_{out1}=5V, V_{out2}=3.3V; (b) v_{DC}=20V, V_{out1}=5V, V_{out2}=3.3V

REFERENCES

[1] R. Elfrich and T. Duerbaum, "A new load resonant dual-output converter", *IEEE Power Electronics Specialists Conference Rec.*, 2002, pp. 1319-1324.

[2] S. Glozman and S. Ben-Yaakov, "Dynamic interaction of high frequency electronic ballasts and fluorescent lamps", *IEEE Power Electronics Specialists Conference Proc.*, 2000, pp. 1363-1368.

[3] J. A. Ferreira, "A series resonant converter for arc-striking applications", *IEEE Trans. on Industrial Electronics*, **45**, 1998, pp. 585-595.

[4] J. P. Agrawal, "Determination of cross regulation in multi output resonant converters", *IEEE Trans. on Aerospace and Electronic Systems*, 36, 2000, pp.760-772.

[5] J.P. Agrawal and I. Batarseh, "Improving the dynamic modeling and static cross regulation in multi-output resonant converters", *IEEE Applied Power Electronics Conference Proc.*, 1993, pp. 65-70.

[6] I. Batarseh and C. Q. Lee, "Multi-output LLCC-type parallel resonant converter", *IEEE Industrial Electronics Society Conference Proc.*, 1990, pp. 850-856.

[7] Y. Ang, C. M. Bingham, M. P. Foster, D. A. Stone and D. Howe, "Design orientated analysis of 4th-order LCLC converters with capacitive output filter", *IEE Proc. - Electric Power Applications*, **152**, 2005, pp. 310-322.