

# Hybrid Modulation Technique With DC-Bus Voltage Control for Multiphase NPC Converters

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**Abstract**—The article presents a novel carrier-based pulsewidth modulation technique for multiphase neutral point clamped converters. The technique is aimed to actively control the neutral point (NP) potential while supplying the desired set of line-to-line voltages to the load. Standard techniques are either based on the sole common mode voltage injection or on the sole multistep switching mode; contrarily, the proposed algorithm combines these two approaches to take advantage of their main benefits. The technique performs well for each number of phases, for each modulation index, and for each type of load. It can control in closed-loop the NP voltage to any desirable value with a reduced number of switching transitions. The proposed approach has been experimentally validated and compared with other carrier-based algorithms.

**Index Terms**—Carrier based (CB), multiphase converters, neutral point clamped (NPC), pulsewidth modulation (PWM), voltage balancing.

## LIST OF SYMBOLS

|                      |                                                  |
|----------------------|--------------------------------------------------|
| $M$                  | Number of phases.                                |
| $v_{DC}$             | Total dc-bus voltage.                            |
| $v_{DC,B}; v_{DC,T}$ | Bottom/Top dc-bus capacitor's voltage.           |
| $s_{B,k}; s_{T,k}$   | Bottom/Top device firing signal ( $k$ th phase). |
| $d_{B,k}; d_{T,k}$   | Bottom/Top device duty-cycle ( $k$ th phase).    |
| $v_k; i_k$           | NPC leg output voltage/current ( $k$ th phase).  |
| $i_{NP,k}; i_{NP}$   | Partial ( $k$ th phase)/total NP current.        |
| $d_{NP,k}; \alpha_k$ | NP duty cycle/NP gain factor ( $k$ th phase).    |
| $d_{NP,max,k}$       | Maximum NP duty cycle value ( $k$ th phase).     |
| $d_{NP,max}(v_k^*)$  | Maximum NP duty cycle function.                  |
| $\tilde{v}_k^*$      | Output phase voltage reference ( $k$ th phase).  |
| $v_0^*$              | Common mode voltage reference.                   |
| $v_{0b,h}^*$         | Clamping voltage ( $h$ th breaking point).       |
| $T_c; \sigma_c$      | Modulation period/carrier signal.                |
| $C$                  | DC-bus capacitances.                             |

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## I. INTRODUCTION

MULTILEVEL converters are, nowadays, an established and industrially accepted technology for high-voltage and high-power applications, both in the field of the electrical drives and for grid-connected interfaces [1]–[4]. Indeed, at the expense of a higher number of switching devices, they guarantee several benefits with respect to conventional two-levels converters, like higher output voltage capabilities, reduced output voltage harmonic content, lower switching losses, and a better electromagnetic compatibility. Among the different architectures, the diode-clamped converter, first introduced in [5], is one of the most commonly used structures [1], [2], especially in its three-level form, which is commonly named neutral point clamped (NPC). Its basic leg circuit consists of four active switching devices (with their free-wheeling diodes) and two clamping diodes per leg. The dc bus is built of two series-connected capacitors with a neutral point (NP) rail. Given the presence of a common dc bus, the extension to a multiphase architecture is quite straightforward.

A key problem for NPC converters is to keep the dc-bus capacitors' voltages balanced, neutralizing the NP voltage drift and suppressing an undesired ripple [6]–[8]. Indeed, the current driven through the clamping diodes acts differently on the dc capacitors and, in some operating conditions, leads to low-frequency oscillations [6]–[8] or even to an unstable behavior [7]. These phenomena stress both the capacitors and the switching devices, reducing the life-span of the entire structure.

The equalization task can be performed either through additional hardware circuits, specially developed for the voltage balancing [9]–[12], or through software approaches, by properly acting on the switching devices firing signals. This article focuses on the software approaches.

Several pulsewidth modulation (PWM) techniques have been proposed in the technical literature for the NPC converter. As in the two-level case, they can be classified into three main categories: selective harmonic elimination (SHE), space vector (SV), and carrier based (CB), [13], [14].

The SHE approaches compute the devices' switching instants with the aim to supply a set of voltages with a desired harmonic content. Based on the load currents, the switching instants can be properly conditioned to control the NP potential [15], [16]. However, these strategies refer to the steady state behavior of the converter and require *a priori* knowledge of the supplied load for the estimation of the effects of the currents on the dc-bus voltages. As a result, they lack robustness and are not suited when the load is often subject to transients.

SV approaches for NPC converters are usually related to three-phase case where the available output voltage combinations are classified into “zero,” “small,” “medium,” and “large” vectors, according to their magnitude [13], [17], [18]. Only the small and medium vectors have a direct effect on the NP potential and can be effectively exploited for equalization purposes, which is achieved by properly setting their dwell times [17]–[27]. To counteract the poor NP potential control capabilities in case of high modulation indexes, some authors proposed slightly different approaches based on the definition of a set of virtual space vectors (VSVs) as proper linear combination of the original voltage vectors [28]–[30]. They allow full control of the NP potential but introduce more switching transitions in each modulation period. Nevertheless, SV techniques (including VSV-based ones) are usually not suited for multiphase converters, both due to the fast increase of the number of different output vectors with the increase of the number of phases and due to the appearance of the additional SV planes [31]–[35]. Many different approaches have been proposed in the technical literature to simplify the SV implementation on digital controllers [34], [35], but only few of them explicitly address the NP equalization at the same time.

Contrarily, CB approaches, by separately focusing on each converter’s phase, can be easily extended from three-phase to multiphase converters without requiring any intensive computational effort [35].

Most of the standard carrier-based pulsewidth modulation (CBPWM) techniques developed for the NPC compute the switching signals for each phase through a single-reference/multicarriers approach (i.e., by comparing a single duty cycle per phase with two common triangular carrier signals) [13], [14]. With this choice, in a single modulation period, the output node can either switch between the negative rail and the NP or between the NP and the positive rail, thus operating in single step (SS) switching mode. This choice, despite minimizing the switching transitions rate, binds the top/bottom switching signals to the sole phase reference output voltage, thus lacking the control of the NP current.

To counteract this phenomenon, a proper common mode injection (CMI) can be added to the reference leg voltages to condition the switching signals and regain control over the NP current [36]–[42]. This method is completely equivalent to the dwell-time adjustment with SV approaches [34], [35] but, like the SV modulation techniques, it fails to guarantee the desired control in case of high modulation indexes, given the constraint on the common mode voltage which can be injected.

A different strategy is based on allowing the output voltage to switch between the positive, negative, and NP nodes in the same modulation interval. This leads to an additional degree of freedom which can be exploited for the NP control [43]–[52]. This switching behavior can be referred as multistep (MS) mode and requires multiple reference signals for each phase, in order to separately control each switching device [45], [46]. The extreme case is achieved by forcing the top and bottom device to switch at the same time. When it happens, the converter’s leg acts as an equivalent two-level converter leg and this behavior can be referred as two-level (TL) mode. However, all the MS-based approaches, despite being generalizable to any number of

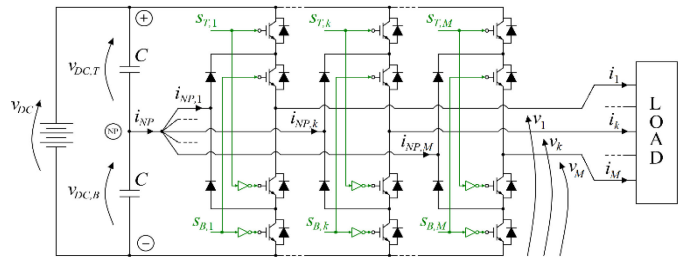


Fig. 1. Power circuit of an  $M$ -phase neutral point clamped converter.

phases and being able to completely control the NP current (thus, removing the NP voltage oscillations), by switching between more levels, lead to an increase of the losses [45].

This article proposes a novel carrier-based modulation technique which, by properly combining the MS mode and an optimal CMI, is able to effectively exploit all the degrees of freedom offered by a multiphase NPC structure. It takes advantage of the main benefits of the two approaches, while at the same time neutralizing some of their main drawbacks.

This article is an extension of the hybrid technique proposed by the authors in [52], where the focus was on a three-phase NPC converter which allowed to establish a deterministic way to combine the CMI with the MS capability and to show that having only one leg working in MS mode is sufficient to guarantee the full NP voltage control. However, this property is not true for multiphase systems and, therefore, the generalization of the proposed hybrid technique to a multiphase converter requires a refined procedure to properly exploit all the degrees of freedom offered by the structure. The generalization to multiphase systems makes the proposed approach particularly suited for high-power/high-reliability applications, like for electric ship propulsion or wind turbines, where multiphase drives are more and more frequently adopted [31].

This article is organized as follows. First, in Section II, the mathematical model of the converter’s leg is obtained, with a special emphasis on the switching constraints to be respected; it is then expanded to a generic  $M$ -phases/ $M$ -wires system to highlight all the available degrees of freedom. In Section III, some different approaches are discussed. After addressing some CMI- and MS-based solutions already available in the technical literature, the proposed hybrid method is presented and discussed. Section IV shows the experimental validation of this technique, together with a proper comparison with some other approaches. Finally, Section V concludes this article.

## II. MATHEMATICAL MODEL

The considered architecture consists of an  $M$ -phase NPC converter, feeding a generic  $M$ -phases/ $M$ -wires load (see Fig. 1). The neutral wire is absent and, consequently, the converter’s common mode current is constrained to zero. The positive and the negative dc rails are connected to a dc source with an almost constant total voltage  $v_{DC} = v_{DC,B} + v_{DC,T}$ . The NP rail is connected to the NPC legs through the clamping diodes.

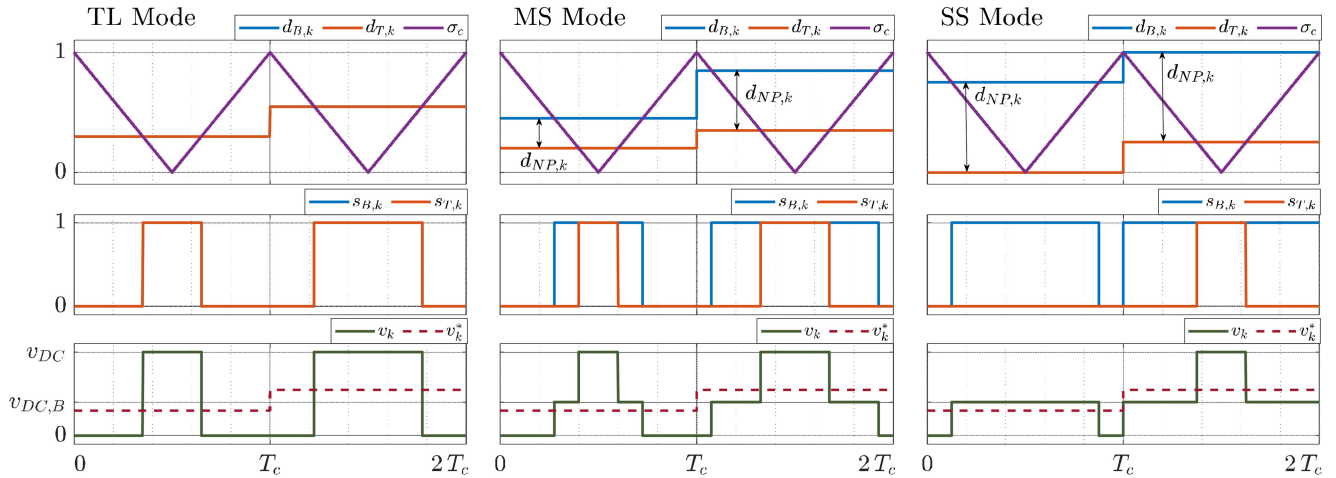


Fig. 2. Qualitative behavior of the different switching modes for the same leg output voltage reference  $v_k^*$  (left: Two-level, middle: Multistep, right: Single-Step).

TABLE I  
NPC  $k$ TH PHASE SWITCHING STATES

| State | $s_{T,k}$ | $s_{B,k}$ | $v_k$                                   | $i_{NP,k}$ |
|-------|-----------|-----------|-----------------------------------------|------------|
| {0,0} | 0         | 0         | 0                                       | 0          |
| {0,1} | 0         | 1         | $v_{DC,B}$                              | $i_k$      |
| {1,0} | 1         | 0         | $v_{DC} \cdot (1 - \text{sign}(i_k))/2$ | 0          |
| {1,1} | 1         | 1         | $v_{DC}$                                | 0          |

### A. Mathematical Model of an NPC Converter's Leg

With reference to Fig. 1, the  $k$ th converter leg (with  $k = 1, \dots, M$ ) can be connected to the three dc-bus nodes through the active devices and the clamping diodes. Each top/bottom device can be controlled through the corresponding switching signal  $s_{(T/B),k} \in \{0; 1\}$ , while its complementary device is controlled by the signal  $(1 - s_{(T/B),k})$ . The four possible switching states, together with the corresponding values of the obtained leg voltage  $v_k$  and NP current  $i_{NP,k}$ , are summarized in Table I. The state  $\{1; 0\}$  makes the output voltage dependent on the sign of the output current and, as a result, it is useless for control purposes. As can be seen from Table I, a simple way to avoid its exploitation is to guarantee  $0 \leq s_{T,k} \leq s_{B,k} \leq 1$ .

Further on, to take into account all the possible switching modes (SS, MS, and TL), the switching signals are considered as obtained through a multireferences single-carrier PWM technique. This means that each  $s_{(T/B),k}$  is computed through the comparison of a corresponding duty-cycle  $d_{(T/B),k} \in [0; 1]$  with a common triangular carrier  $\sigma_c$ , varying linearly in the same  $[0; 1]$  interval with period  $T_c$ . The different switching modes are exemplified in Fig. 2. Note that in Fig. 2, a general case is shown where the upper and the lower dc-bus capacitors have different voltages (i.e.,  $v_{DC,B} \neq v_{DC,T} \neq v_{DC}/2$ ).

As can be deduced from the graphical interpretation, the switching constraints  $0 \leq s_{T,k} \leq s_{B,k} \leq 1$  are automatically met once the corresponding duty-cycles satisfy

$$0 \leq d_{T,k} \leq d_{B,k} \leq 1. \quad (1)$$

Also, from Fig. 2 note that for SS and TL mode the duty cycles  $d_{T,k}$  and  $d_{B,k}$  are uniquely determined for a given leg reference voltage  $v_k^*$ . This is not the case for MS mode; the illustration in Fig. 2 is only one possible choice of  $d_{T,k}$  and  $d_{B,k}$ .

By neglecting the voltage drops and the leakage currents in the semiconductor devices and by applying a standard averaging procedure over a  $T_c$  time interval, the average  $k$ th converter's leg voltage and NP current are found to be

$$\begin{aligned} \bar{v}_k &= d_{B,k} \cdot \bar{v}_{DC,B} + d_{T,k} \cdot \bar{v}_{DC,T} \\ \bar{i}_{NP,k} &= (d_{B,k} - d_{T,k}) \cdot \bar{i}_k = d_{NP,k} \cdot \bar{i}_k. \end{aligned} \quad (2)$$

Overbar symbol denotes average value of the signal during  $T_c$ . To keep notation simple, the overbar will be omitted further on, meaning that all the variables will implicitly refer to their average values over a modulation period.

The difference  $d_{NP,k} = d_{B,k} - d_{T,k}$ , that appears in (2) for  $i_{NP,k}$ , is an important parameter. Based on (1) one can see that it is always a nonnegative value and represents the fraction of the modulation period  $T_c$  for which the output of the  $k$ th leg is connected to the NP. As mentioned, for MS mode the same reference voltage can be obtained by using different values of  $d_{T,k}$  and  $d_{B,k}$ , thus, by using different value of  $d_{NP,k}$ . Therefore, from the MS modulation perspective and based on (2),  $d_{NP,k}$  can be considered as a degree of freedom for the NP current control.

The minimum value of  $d_{NP,k}$  is zero and is obtained in TL mode (see Fig. 2-left). The maximum value is obtained in SS mode (see Fig. 2-right) and depends on the reference leg voltage  $v_k^*$ : if  $v_k^* < v_{DC,B}$  (as shown in Fig. 2-right from 0 to  $T_c$ ) then  $d_{NP,max,k} = v_k^*/v_{DC,B}$ ; if the reference is  $v_k^* > v_{DC,B}$  (as shown in Fig. 2-right from  $T_c$  to  $2T_c$ ) then  $d_{NP,max,k} = (v_{DC} - v_k^*)/v_{DC,T}$ . Hence, the maximum NP duty-cycle of each leg can be expressed as a function of the corresponding leg voltage reference as

$$d_{NP,max,k} = d_{NP,max}(v_k^*) = \min \left\{ \frac{v_k^*}{v_{DC,B}}; \frac{v_{DC} - v_k^*}{v_{DC,T}} \right\}. \quad (3)$$



The function  $d_{NP,max}(v_k^*)$  is the same for all  $M$  converter legs, but for each leg it should be evaluated in correspondence to its reference leg voltage  $v_k^*$  (which, in general, differs from leg to leg). From (3) one can see that  $d_{NP,max}(v_k^*)$  is a piecewise linear function that linearly increases from 0 to 1 in the interval  $0 \leq v_k^* \leq v_{DC,B}$  and linearly decreases from 1 to 0 in the interval  $v_{DC,B} \leq v_k^* \leq v_{DC}$ . All the intermediate values of  $d_{NP,k}$  (between 0 and  $d_{NP,max,k}$ ) are the possible choices for MS mode (see Fig. 2-middle). Thus, SS and TL mode can be also considered as special cases of MS mode.

Instead of dealing with  $d_{NP,k}$  which is in range from 0 to  $d_{NP,max}(v_k^*)$  (and which is different for each leg), it is convenient to introduce the following normalization:

$$\alpha_k = d_{NP,k}/d_{NP,max,k} = d_{NP,k}/d_{NP,max}(v_k^*). \quad (4)$$

The parameter  $\alpha_k$  is named gain factor and is in range from 0 to 1. It represents percentage of  $d_{NP,max,k}$  used in that switching period by the  $k$ th NPC leg. The gain factor can be used to identify the switching mode of each leg ( $\alpha_k = 0$ : TL Mode;  $0 < \alpha_k < 1$ : MS Mode;  $\alpha_k = 1$ : SS Mode).

From (4), one can write  $d_{B,k} - d_{T,k} = d_{NP,k} = \alpha_k \cdot d_{NP,max}(v_k^*)$ . Substituting this into (2), one can see that by properly adjusting  $\alpha_k$  it is possible to vary the NP current  $i_{NP,k}$  absorbed by the  $k$ th converter leg in each switching period, while keeping the average value of the obtained leg voltage equal to the reference  $v_k^*$ . This capability of the MS mode can be conveniently exploited for the NP voltage control but, as a drawback, it introduces additional switching transitions comparing to the SS mode.

### B. Multiphase NPC Mathematical Model

The average dynamic of the dc-bus capacitors' voltage unbalance can be found through superposition of each phase contribution to the average NP current (see Fig. 1)

$$\begin{aligned} C \frac{d}{dt} (v_{DC,T} - v_{DC,B}) &= i_{NP} \\ &= \sum_{k=1}^M i_{NP,k} = \sum_{k=1}^M i_k \cdot \alpha_k \cdot d_{NP,max}(v_k^*). \end{aligned} \quad (5)$$

In absence of a neutral wire connection the converter's common mode voltage does not have any influence on the behavior of the load (because the phase-to-phase voltages stay unchanged). A common mode voltage reference  $v_0^*$  can be therefore injected in the NPC leg voltages to influence the converter's behavior (in this case the dc-bus voltages) without altering the voltages and currents of the supplied load. Each NPC reference leg voltage  $v_k^*$  can be expressed as a sum of the corresponding reference phase voltage  $\tilde{v}_k^*$  and of the reference common mode voltage  $v_0^*$  as

$$v_k^* = \tilde{v}_k^* + v_0^*, \quad \text{with} \quad v_0^* = (1/M) \cdot \sum_{k=1}^M v_k^*. \quad (6)$$

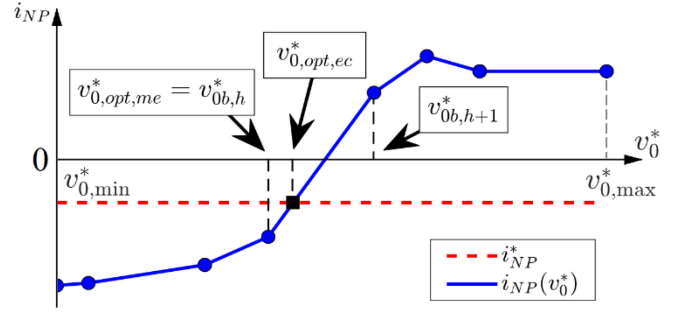


Fig. 3. Optimal common mode voltage reference with the minimum breaking point error ( $v_{0,opt,me}^*$ ) and with the error cancellation ( $v_{0,opt,ec}^*$ ).

By substituting (6) into (5) one gets

$$C \frac{d}{dt} (v_{DC,T} - v_{DC,B}) = \sum_{k=1}^M i_k \cdot \alpha_k \cdot d_{NP,max}(\tilde{v}_k^* + v_0^*). \quad (7)$$

This expression formulates the NP voltage dynamics in its most general way by highlighting all the involved parameters and allowing to separate the controllable ones ( $v_0^*$  and all  $\alpha_k$  values) from the uncontrollable ones (all  $\tilde{v}_k^*$  and  $i_k$ ).

To analyze (7) first note that, since  $0 \leq v_k^* \leq v_{DC}$  must be satisfied for all NPC legs, the value of  $v_0^*$  is constrained to be within the feasible interval, whose extremes are

$$\begin{aligned} v_{0,min}^* &= |\min_k \{\tilde{v}_k^*\}| = -\min_k \{\tilde{v}_k^*\} \\ v_{0,max}^* &= v_{DC} - |\max_k \{\tilde{v}_k^*\}| = v_{DC} - \max_k \{\tilde{v}_k^*\}. \end{aligned} \quad (8)$$

Going further, note that once a feasible set of reference phase voltages  $\tilde{v}_k^*$  and of gain factors  $\alpha_k$  are chosen, the NP current  $i_{NP}$  is a piece-wise linear function of the common mode voltage reference  $v_0^*$ . This is because  $d_{NP,max}(v_k^*)$  (as explained in Section II-A) is a two-segment piecewise linear function and, from (7),  $i_{NP}$  is the sum of  $M$  of such functions (each of which has its own breaking points defined by the argument  $v_k^* = \tilde{v}_k^* + v_0^*$  and is weighted by  $i_k \cdot \alpha_k$ ). One example of  $i_{NP}$  as a function of  $v_0^*$  is shown in Fig. 3. The breaking points appear when one converter's leg voltage is clamped to one of the dc-bus nodes [38]. Since the conditions  $v_k^* = 0$  and  $v_k^* = v_{DC}$  are verified only when  $v_0^* = v_{0,min}^*$  and  $v_0^* = v_{0,max}^*$ , while the condition  $v_k^* = v_{DC,B}$  might be satisfied by any leg, there are at most  $M + 2$  different clamping voltages/breaking points (further on denoted as  $v_{0b,1}^*, v_{0b,2}^*, \dots$ ).

Finally, note that the above analysis is valid for any  $M$ -wire system, including nonlinear and nonsymmetrical loads.

### III. HYBRID CMI-MS MODULATION STRATEGY

Based on (7), to actively control the NP voltage, the NPC modulation strategy should be designed to achieve the full control of the current  $i_{NP}$ , which should be driven toward a desired reference  $i_{NP}^*$  (coming, for example, from a closed loop feedback controller). However, this capability should not interfere with the main converter purpose, which is to supply a desired set of phase voltages  $\tilde{v}_k^*$ . Similarly, the output currents  $i_k$ ,

depend on the supplied load, thus cannot be directly used for the NP voltage control. Therefore, as already stated, the available degrees of freedom are the common mode voltage reference  $v_0^*$  and the gain factors  $\alpha_k$ . Depending on the exploited degrees of freedom, different strategies are defined.

### A. Standard CBPWM

The standard CBPWM does not address the NP current control and all the converter's legs work in SS mode (i.e., all the gain factors are set to  $\alpha_k = 1$  meaning that, in each modulation interval, the converter's legs are connected to the NP for the maximum available time). This is automatically achieved with most of the standard single-reference multicarriers PWM techniques (like all the level-shifted methods). The common mode voltage is usually chosen to extend the linear modulation region, for example through a standard min-max injection [35]

$$\begin{aligned} v_0^* &= v_{0,avg}^* = (v_{0,min}^* + v_{0,max}^*) / 2 \\ &= v_{DC} / 2 + (|\min_k \{\tilde{v}_k^*\}| - |\max_k \{\tilde{v}_k^*\}|) / 2. \end{aligned} \quad (9)$$

### B. CMI-Based Techniques

Some authors, as discussed in Section I, propose the exploitation of the sole common mode voltage  $v_0^*$  for the NP current control. The converter works in SS mode (i.e., all the  $\alpha_k = 1$ ) and, again, the modulation can be realized through a single-reference multicarriers comparison technique. The number of transitions per period is minimized and, together with it, also the corresponding switching losses [36]–[42].

In [37] and [38], the choice of the common mode reference voltage is performed by evaluating the NP current  $i_{NP}(v_0^*)$  at the breaking points (as shown in Fig. 3) and then by selecting the clamping voltage  $v_{0,opt,me}^*$  which minimizes the error  $|i_{NP}(v_0^*) - i_{NP}^*|$  from the reference NP current

$$v_0^* = v_{0,opt,me}^* = \operatorname{argmin}_{v_{0b,h}^*} \{|i_{NP}(v_{0b,h}^*) - i_{NP}^*|\}. \quad (10)$$

Since the breaking points  $v_{0b,h}^*$  are obtained when one of the converter's legs is clamped to one of the dc-bus nodes, that means that this approach results in no switching in one phase during each modulation interval. Therefore, some discontinuous PWM techniques (DPWM), like the one of [42], can be interpreted as particular cases of this procedure.

A refined approach consists in choosing, when possible, the common mode voltage reference able to set the NP current exactly to the desired reference. If a zero-crossing of the error function  $|i_{NP}(v_0^*) - i_{NP}^*|$  is detected between the  $h$ th and  $(h+1)$ th breaking point ( $v_{0b,h}^*$  and  $v_{0b,h+1}^*$ ), then the optimal  $v_0^*$  is easily obtained via linear interpolation as

$$\begin{aligned} v_0^* &= v_{0,opt,ec}^* \\ &= v_{0b,h}^* + (v_{0b,h+1}^* - v_{0b,h}^*) \cdot \frac{i_{NP}^* - i_{NP}(v_{0b,h}^*)}{i_{NP}(v_{0b,h+1}^*) - i_{NP}(v_{0b,h}^*)}. \end{aligned} \quad (11)$$

For the three-phase case, this coincides to the method proposed in [38] with the so-called ‘‘Precise Calculation Algorithm.’’

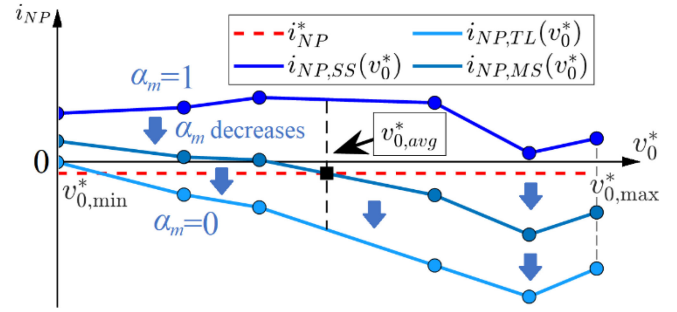


Fig. 4. Effect of the modification of the current gain factor on a phase:  $i_{NP,SS}$  (SS mode),  $i_{NP,TL}$  (TL mode), and  $i_{NP,MS}$  (Optimal MS mode).

A qualitative picture of these two approaches is shown in Fig. 3, where the piece-wise linear function  $i_{NP}(v_0^*)$  is compared with the desired reference  $i_{NP}^*$ . The common mode voltages selected by both (10) and (11) are clearly denoted.

The CMI-based algorithms allow to keep number of switching transitions low and, therefore, the corresponding losses. However, from the NP voltage control perspective, they perform poorly in case of high modulation indexes, where the feasible common mode voltage injection interval  $[v_{0,min}^*, v_{0,max}^*]$  is narrow. This effect is critical in case of low power factor operations (i.e., dominant reactive effect) [37], [38] or for unbalanced loads [7].

### C. MS Switching Mode Based Techniques

As discussed in Section I, a different approach involves the exploitation of the MS switching mode to control the NP voltage [43]–[50]. These techniques modify the gain factors  $\alpha_k$  and require several modulation signals, corresponding to the duty cycles of each device; therefore, standard single-reference multicarriers approaches cannot be used. The choice of which phases to be used in the MS mode (i.e., which  $\alpha_k$  to be different from 1) defines the different approaches. The common mode reference voltage  $v_0^*$  is not exploited for equalization purposes in these algorithms and is chosen by other criteria.

In [43], the common mode reference voltage is obtained by the min-max injection criterion given by (9). Then, a recursive method is performed to choose the minimum number of phases needed to switch in MS mode to get closer to the NP current reference (because more legs in MS mode means higher switching losses). In particular, by starting with all the legs in SS mode, the algorithm selects at each iteration one extra leg to switch in MS mode until either the corresponding NP current intersects the reference or it is able to affect the voltages in the desired direction with an acceptable slope (i.e., without exceeding the reference NP current magnitude).

The reduction of one or more gain factors (i.e., exploiting the MS mode) modifies the shape of the functional relation between the NP current and the common mode voltage. This can be graphically interpreted with the example given in Fig. 4. The original function (obtained with all legs in SS mode)  $i_{NP,SS}(v_0^*)$  can be modified by reducing one gain factor  $\alpha_m$  up to the function  $i_{NP,TL}(v_0^*)$ , obtained when the selected

$m$ th NPC leg is in TL mode. The optimal gain factor is obtained when the function intersects the reference  $i_{NP}^*$  with the chosen voltage  $v_0^* = v_{0,avg}^*$ ; the corresponding function is  $i_{NP,MS}(v_0^*)$ .

The MS-based algorithms are always capable of guaranteeing the desired control over the NP voltage, but usually introduce many switching transitions, thus reducing the efficiency of the converter and worsening the output voltage harmonic content, especially for low power factor operations.

#### D. Proposed Hybrid Technique

A proper combination of a common mode voltage injection and MS operation can allow to take advantage of their main benefits, while partially neutralizing their respective drawbacks. The proposed hybrid technique, by controlling both  $v_0^*$  and  $\alpha_k$ , is aimed to seek the desired reference NP current while keeping the average switching frequency low.

The proposed algorithm starts with all the legs in SS mode (i.e.,  $\alpha_k = 1$ ) and, by using the same reasoning as in [38], examines all the breaking points of  $i_{NP}(v_0^*)$ , looking for an intersection with the reference value  $i_{NP}^*$ . If an intersection is found, the optimal common mode voltage injection is found by applying (11), thus behaving like in Fig. 4. In case that there is no intersection, the algorithm evaluates the NP current function in correspondence to the clamping voltage  $v_{0,opt,me}^*$  given by (10), which guarantees the minimum distance from the reference NP current  $i_{NP}^*$ . If the corresponding NP current  $i_{NP,me} = i_{NP}(v_{0,opt,me}^*)$  affects the dc-bus voltages in the desired way and with an acceptable slope (i.e., when either  $0 < i_{NP,me} \leq i_{NP}^*$  or  $i_{NP}^* \leq i_{NP,me} < 0$ ), the algorithm identifies a *Natural Balancing Mechanism* and stops. If natural balancing is not identified, it is necessary to start modulating at least one leg in MS mode. As shown in [52], no more than one leg is needed to work in MS mode for a three-phase converter; nevertheless this is not the case for a multiphase system. Therefore, an iterative algorithm is executed to identify the phases needed to be modulated in MS mode. Only one extra phase to be operated in MS mode is selected in each iteration and it is chosen according to the effect of the corresponding NP current on the dc-bus voltages.

- 1) If the NP voltage is to evolve in the wrong direction (i.e.,  $i_{NP,me}$  and  $i_{NP}^*$  have the opposite sign), the selected phase is the most unbalancing one.
- 2) If the NP voltage is to evolve in the correct direction, but with an excessive slope (i.e.,  $i_{NP,me}$  and  $i_{NP}^*$  have the same sign, but  $|i_{NP,me}| > |i_{NP}^*|$ ), the selected phase is the most balancing one.

The most balancing/unbalancing phase can be found from (7) by identifying the highest or lowest value among all the NP currents  $i_{NP,k} = i_k \cdot d_{NP,max}(\tilde{v}_k^* + v_{0,opt,me}^*)$ .

By denoting with  $m$  the leg selected to work in MS mode, the corresponding gain factor is found as

$$\alpha_m = 1 - (i_{NP,me} - i_{NP}^*) / i_{NP,m}. \quad (12)$$

If  $\alpha_m < 0$  in (12), it means that the choice of single leg to operate in MS mode is not enough to guarantee the desired

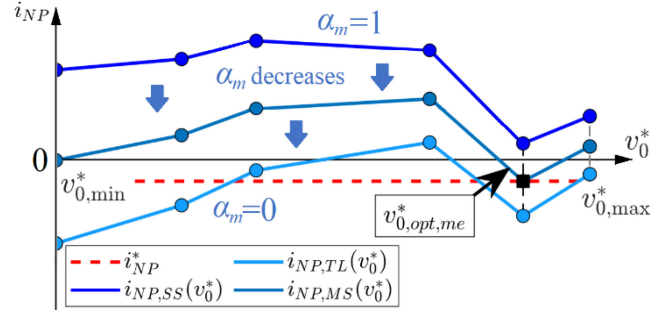


Fig. 5. Neutral point current modification through the proposed hybrid method:  $i_{NP,SS}$  (SS mode),  $i_{NP,TL}$  (TL mode),  $i_{NP,MS}$  (Optimal MS mode).

current. Then, the algorithm sets  $\alpha_m$  to 0 (i.e., the  $m$ th phase works in TL mode) and the iterative procedure is repeated with a new search of the minimum error breaking point and with the selection of another phase to operate in MS mode. A qualitative effect of this method onto the  $i_{NP}(v_0^*)$  waveform is shown in Fig. 5 to allow a graphical interpretation.

At the end of this procedure, the algorithm has selected both the common mode voltage reference  $v_0^*$  and the gain factors  $\alpha_k$  for all phases. Then, both the leg voltage reference  $v_k^*$  and the NP duty cycle  $d_{NP,k}$  are uniquely determined for each  $k$ th NPC leg and the corresponding top/bottom device's duty-cycles are evaluated by substituting (4) and (6) in (2), resulting in

$$\begin{aligned} d_{T,k} &= [(\tilde{v}_k^* + v_0^*) - v_{DC,B} \cdot \alpha_k \cdot d_{NP,max}(\tilde{v}_k^* + v_0^*)] / v_{DC} \\ d_{B,k} &= [(\tilde{v}_k^* + v_0^*) + v_{DC,T} \cdot \alpha_k \cdot d_{NP,max}(\tilde{v}_k^* + v_0^*)] / v_{DC}. \end{aligned} \quad (13)$$

The flowchart of the proposed strategy is illustrated in Fig. 6. First,  $v_{0,min}^*$  and  $v_{0,max}^*$  are found by (8): they represent the extreme clamping voltages for  $v_0^*$ . Then, the internal clamping voltages are found by setting  $v_k^* = \tilde{v}_k^* + v_0^* = v_{DC,B}$  (for each  $k$ th converter's leg) and by verifying that the resulting common mode voltage is included in  $[v_{0,min}^*, v_{0,max}^*]$ . The gain factors  $\alpha_k$  are initialized to 1 and NP current is evaluated via (7) and compared to the reference value  $i_{NP}^*$  for each breaking point. If an intersection is possible (i.e., the error function has at least one zero-crossing point), the optimal common mode voltage is found via (11), otherwise the MS iterative cycle is executed until either it is possible to impose  $i_{NP} = i_{NP}^*$  (by reducing one or more gain factors  $\alpha_k$ ) or a natural balancing mechanism is recognized. Finally, the top/bottom devices' duty cycles are found by (13) and compared to the common triangular carrier signal  $\sigma_c$  (which is in range from 0 to 1). From the computational point of view, the NP current evaluation at the breaking points can be performed in a faster way by storing the NP current contributions  $i_k \cdot d_{NP,max}(\tilde{v}_k^* + v_{0b,h}^*)$  in a  $M \times (M + 2)$  matrix at the beginning of each modulation interval.

With respect to the sole exploitation of the common mode voltage, the proposed technique can overcome the limitations existing in case of high modulation indexes. With respect to the sole exploitation of the MS switching mode, the automatic choice of the optimal common mode voltage can ensure faster control with less switching transitions.



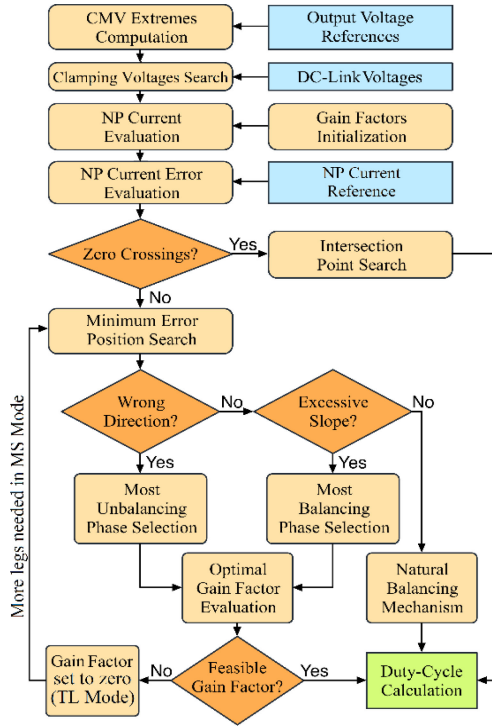


Fig. 6. Flowchart of the proposed hybrid modulation technique.

Moreover, since  $i_{NP}(v_0^*)$  is always a piece-wise linear function, when the MS mode is activated, the simultaneous common mode voltage injection automatically chooses  $v_0^*$  among its breaking points, leading to a voltage clamping for one of the converter's legs. The clamped leg does not bring any switching transition and mitigates the increase of the switching losses caused by the MS mode. Given this property, some enhanced DPWM techniques can be conceived as special cases of the proposed approach. As an example, the technique proposed in [52] for three-phase converters can be obtained by discarding the error cancellation algorithm (11) in case of SS mode and by imposing  $i_{NP}^* = 0$  for MS mode operations.

#### IV. NUMERICAL AND EXPERIMENTAL RESULTS

The proposed modulation technique has been validated experimentally on a custom-made multiphase NPC prototype. To highlight its effectiveness, the approach has been compared with the modulation techniques proposed in [38] and [43], (which can be respectively considered as the state-of-the-art techniques based on the sole CMI or on the sole MS mode) and with a standard CBPWM technique, which does not actively address the NP voltage control.

The converter is based on Semikron SKM50GB12T4 modules. The switching frequency has been chosen to be 2 kHz, while the dead time for the semiconductor switching transitions has been set in hardware to 6  $\mu$ s. Both the top and the bottom dc capacitances have been set to 300  $\mu$ F and realized through the parallel connection of three Kemet C4AE polypropylene capacitors. The overall converter dc voltage has been supplied through a Sorensen SGI 600/25 and stabilized to 300 V.

TABLE II  
AVERAGE NUMBER OF SWITCHING TRANSITIONS IN THE STEADY STATE TEST FOR THE THREE-PHASE RL LOAD

| [V]/[Hz] | Proposed method | CMI method | MS method | Standard CBPWM |
|----------|-----------------|------------|-----------|----------------|
| 100/20   | 199             | 201        | 267       | 198            |
| 150/20   | 207             | 140        | 266       | 198            |
| 173/20   | 211             | 135        | 272       | 198            |

All the modulation techniques have been implemented on a dSpace ds1006 platform with a 2 kHz sampling rate, while the measurements have been recorded through a Tektronix DPO/MSO 2014 oscilloscope. As in [52], the NP current reference  $i_{NP}^*$  has been set through a feedback predictive controller acting on the voltage unbalance ( $v_{DC,T} - v_{DC,B}$ ).

Several tests have been performed in different scenarios. For each test, the displayed waveforms are the bottom and the top dc-bus voltage ( $v_{DC,B}$  and  $v_{DC,T}$ , in light blue and magenta, respectively) and the 1st converter's leg voltage and current ( $v_1$  and  $i_1$ , in dark blue and green, respectively).

#### A. Steady State Behavior for Three-Phase RL Load

The test has been performed by supplying a set of symmetrical and sinusoidal voltage references to a balanced three-phase ohmic-inductive load with  $R \approx 20 \Omega$  and  $L \approx 360$  mH. To better highlight the NP voltage fluctuation the supply frequency has been set to 20 Hz. To consider different operating conditions the magnitude of the phase voltage references  $\tilde{v}_k^*$  has been set to 100 V (i.e., below  $v_{DC}/2$ ), to 150 V (i.e., equal to  $v_{DC}/2$ ) and to 173.3 V (i.e., equal to  $v_{DC}/\sqrt{3}$ ). By defining the modulation index  $M_{ind}$  as the ratio between the peak reference voltage and  $v_{DC}/2$ , the testing scenarios correspond to modulation index values of 0.66, 1.00, and 1.15. The results are shown in Fig. 7. Table II summarizes the average number of switching transitions per leg in one fundamental period.

For the test at 100 V, it can be easily noted that all the techniques, with the only exception of the standard CBPWM, are able to suppress the NP voltage ripple. In this context, given the sufficient range of the  $v_0^*$  feasibility interval, the proposed approach does not need to operate in MS mode and applies the same leg output voltages as CMI method proposed in [38]. Both methods show fewer switching transitions than the pure MS-based technique described in [43] (about 25% less, Table II).

When the reference voltage is 150 V, the feasibility interval for the CMI is narrow and the technique of [38] is unable to suppress the NP voltage fluctuation, whose magnitude is only slightly lower than the corresponding fluctuation obtained with the standard CBPWM method. On the other hand, the MS approaches (including the proposed one) are able to keep the dc-bus voltages equalized. It can be easily observed that, for the proposed approach, the CMI makes it possible to exploit the MS operation for reduced amount of time when compared to the pure MS-based approach. Moreover, the clamping of the leg voltage to the dc rails further reduces the number of switching transitions (about 22% less, Table II).

A similar behavior can be seen when the reference voltages are set to 173.3 V. Again, CBPWM and pure CMI-based modulation

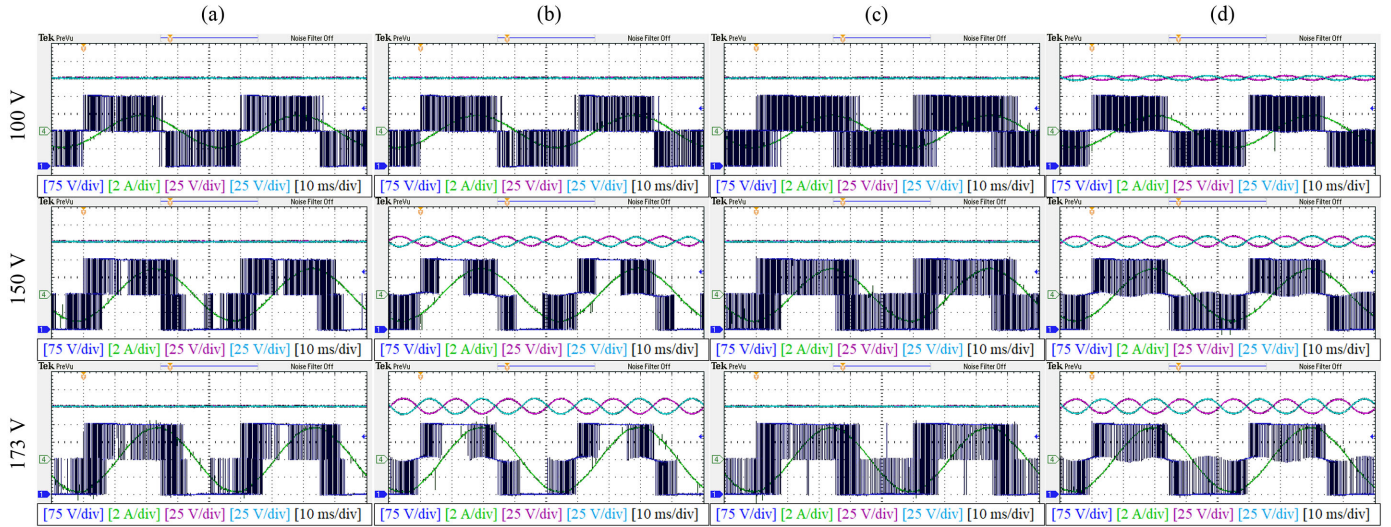


Fig. 7. Steady state results on the symmetrical three-phase system ( $RL$  load; 20 Hz). (a) Proposed method. (b) CMI method. (c) MS method. (d) Standard CBPWM method.

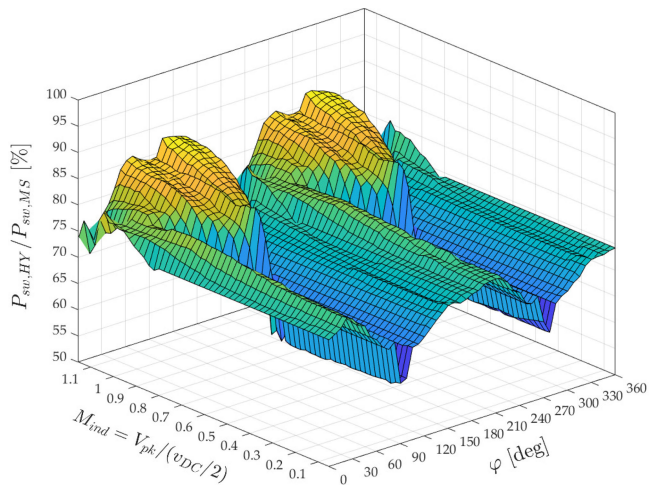


Fig. 8. Ratio between the estimated switching losses with the proposed hybrid algorithm and with the pure MS algorithm.

perform poorly, while the proposed technique is able to suppress the NP voltage ripple with fewer transitions than the pure MS-based approach (about 22% less, Table II).

A comparison of the estimated switching losses obtained with the proposed algorithm and with the MS-based approach (which are the only methods always able to perform the NP voltage control) is shown in Fig. 8. The comparison is provided for different values of the modulation index  $M_{ind}$  and for different load power factor angles  $\varphi$ . The losses have been estimated through numerical simulations by assuming a linear evolution of the transistor's voltage and currents during each switching transition. Results have been averaged over 30 periods of the 20 Hz fundamental frequency.

As can be noted, the estimated losses with the proposed algorithm are always lower than 90% of the ones obtained with the MS approach. For high power factor loads (i.e., when  $\varphi = 0^\circ$

and  $\varphi = 180^\circ$ ) the losses ratio is around 75% for the whole range of  $M_{ind}$ . On the contrary, when the load is prevalently reactive (i.e.,  $\varphi = 90^\circ$  and  $\varphi = 270^\circ$ ), the losses have the lowest ratios for low modulation indexes (around 60% up to  $M_{ind} = 0.6$ ) and the highest ratios for high modulation indexes (around 85%).

For the experimental results depicted in Fig. 7, the load power factor angle is always  $\varphi \approx 66^\circ$  and the power losses ratios have been found to be  $P_{sw,HY}/P_{sw,MS} \approx 73\%$  for the 100 V test ( $M_{ind} \approx 0.66$ ),  $P_{sw,HY}/P_{sw,MS} \approx 84\%$  for the 150 V test ( $M_{ind} \approx 1.00$ ), and  $P_{sw,HY}/P_{sw,MS} \approx 83\%$  for the 173 V test ( $M_{ind} \approx 1.15$ ), thus matching the numerical results.

### B. Transient Behavior for Three-Phase RL Load

Again, the test has been performed by supplying a set of symmetrical and sinusoidal voltage references with both 100 and 150 V peak amplitude to the balanced three-phase load of the previous test. Each controller is initially driven to set  $v_{DC,B}$  to the 40% of the total dc-bus voltage and is then switched to the equalization mode. Since the standard CBPWM cannot control  $v_{DC,B}$ , the initial asymmetry is forced through the pure MS-based approach of [43] [see the gray-shaded area in Fig. 9(d)]. After 40 ms, the mode is changed from MS to CBPWM. The results are shown in Fig. 9.

For the 100 V test, it is easy to notice the similarity between the pure CMI based and the proposed method, which complete the equalization in a 20 ms time window. The pure MS-based approach performs more slowly due to the natural balancing mechanism recognition, which tends to avoid the MS behavior when it is not needed. The standard CBPWM evolves toward the equalized state in almost 360 ms and, as in the previous test, exhibits a superimposed NP ripple.

The 150 V test again highlights the main differences between the different approaches. As in the previous scenario, the pure CMI-based technique suffers with NP voltage ripple, which is present both with the unbalanced and with the balanced dc-bus



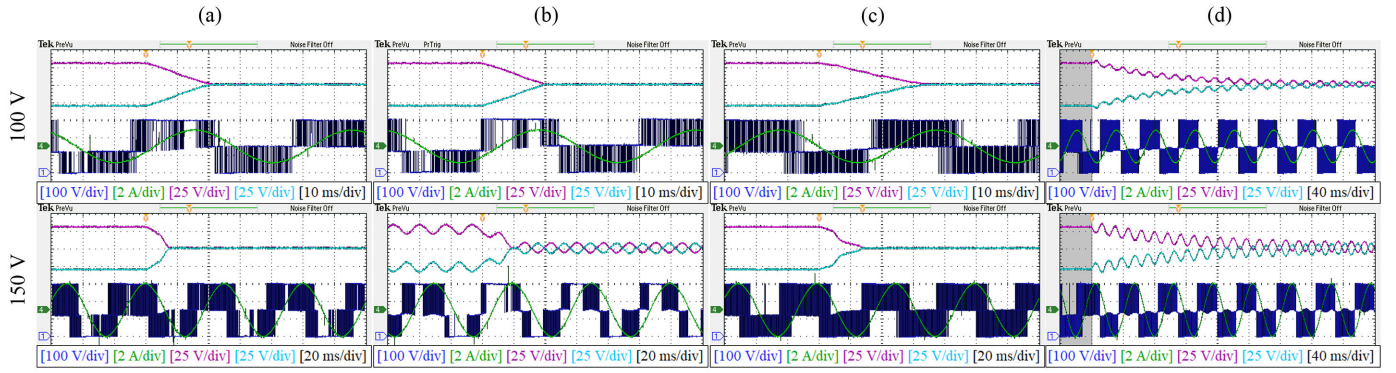


Fig. 9. Transient results on the symmetrical three-phase system ( $RL$  load; 20 Hz). (a) Proposed method. (b) CMI method. (c) MS method. (d) Standard CBPWM method.

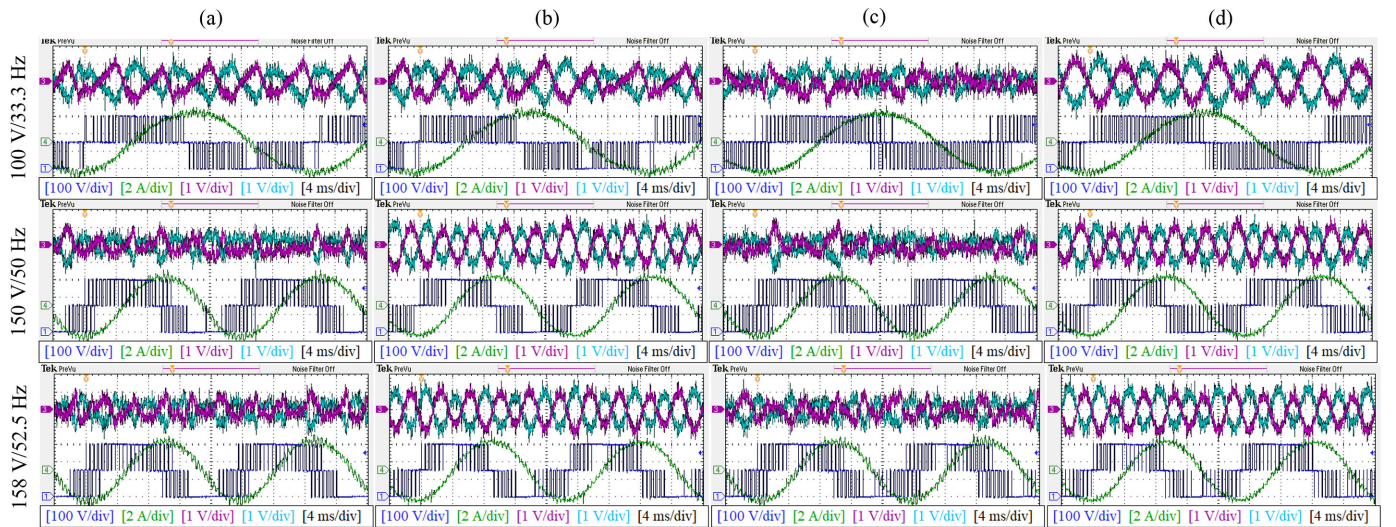


Fig. 10. Steady state results on the symmetrical five-phase system (induction machine;  $V/f$  control). (a) Proposed method. (b) CMI method. (c) MS method. (d) Standard CBPWM method.

TABLE III  
FIVE-PHASE INDUCTION MACHINE'S PARAMETERS

| Parameter                 | Symbol   | Value         |
|---------------------------|----------|---------------|
| No. of pole pairs         | $P$      | 2             |
| Stator resistance         | $R_s$    | $0.75 \Omega$ |
| Rotor resistance          | $R_r$    | $0.75 \Omega$ |
| Stator leakage inductance | $L_{ls}$ | 11.25 mH      |
| Rotor leakage inductance  | $L_{lr}$ | 3.75 mH       |
| Magnetizing inductance    | $L_m$    | 128.75 mH     |

capacitors. This effect is completely absent in the other active balancing modulation techniques. The proposed approach is faster than the one given in [43] due to the exploitation of a proper CMI.

### C. Steady State Behavior for Five-Phase Induction Machine

The test has been performed by supplying a set of symmetrical and sinusoidal voltage references to a custom-made five-phase induction machine working at no load. Its electrical parameters are summarized in Table III.

TABLE IV  
AVERAGE NUMBER OF SWITCHING TRANSITIONS IN THE STEADY STATE TEST FOR THE FIVE-PHASE INDUCTION MACHINE

| [V]/[Hz] | Proposed method | CMI method | MS method | Standard CBPWM |
|----------|-----------------|------------|-----------|----------------|
| 100/33.3 | 110             | 112        | 138       | 120            |
| 150/50   | 81              | 64         | 98        | 83             |
| 158/52.5 | 77              | 63         | 84        | 76             |

The machine has been supplied in  $V/f$  mode in three different conditions. The results are depicted in Fig. 10 and the number of switching transitions per fundamental period of the examined converter leg are summarized in Table IV.

The presence of more phases in a symmetrical configuration contributes to a reduction of the NP voltage fluctuation with respect to the three-phase scenario (note that in Fig. 10 for dc-bus voltages, only the ripple is shown, and the scale is set to 1 V/div). Again, the peculiar properties of each method are evident from the leg voltage waveforms.

For the 100 V/33.3 Hz test the proposed method performs similarly to the CMI-based one, while the effect of the MS

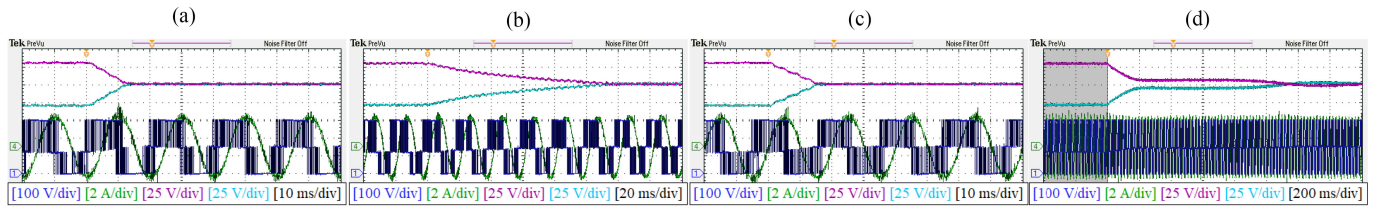


Fig. 11. Transient results on the symmetrical five-phase system (induction machine; 150 V / 50 Hz). (a) Proposed method. (b) CMI method. (c) MS method. (d) Standard CBPWM method.

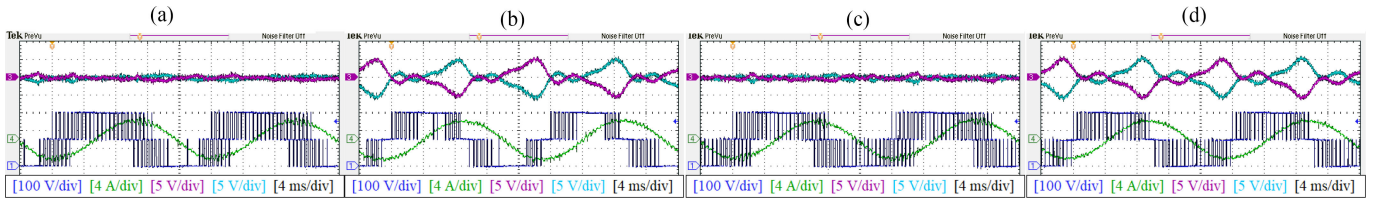


Fig. 12. Steady state results on the unbalanced five-phase system (induction machine with external resistor in phase 5; 150 V / 50 Hz). (a) Proposed method. (b) CMI method. (c) MS method. (d) Standard CBPWM method.

behavior of the technique proposed in [43] is evident in the leg voltage waveform. All the techniques are able to guarantee an NP peak-to-peak voltage ripple of about 1.5 V, but the MS approach has about 20% more transitions (see Table IV). For both the 150 V/50 Hz and the 158 V/52.5 Hz scenarios, the pure CMI-based technique shows a slightly higher fluctuation due to the reduced feasibility interval for  $v_0^*$ . The proposed approach introduces an MS behavior and performs similarly to the technique proposed in [43], but with less switching transitions (about 17% and 8% less, respectively; Table IV). This is due to the simultaneous action of the CMI, which clamps the leg voltage to the negative dc-bus rail for a longer interval.

#### D. Transient Behavior for Five-Phase Induction Machine

This test has been performed for a single scenario, with the reference voltages set to 150 V (peak), 50 Hz. Similarly to the corresponding three-phase test, the control commences the equalization process starting from an unbalanced dc bus (with  $v_{DC,B} = 40\% \cdot v_{DC}$ ). The results are depicted in Fig. 11.

As can be easily observed, both the proposed and the pure MS method are able to perform the equalization within 15 ms, while the pure CMI-based technique needs almost 120 ms due to the narrow feasibility interval of  $v_0^*$ . Note the difference in the time scale in Fig. 11 subplots. Given the symmetrical load, the standard CBPWM naturally evolves toward the equalization, but in a longer time window (more than 1 s).

#### E. Steady State for Unbalanced Five-Phase Induction Machine

Finally, the capabilities of the methods have been studied for an asymmetrical load. To obtain the asymmetry an external 5  $\Omega$  resistor has been connected in series to the fifth phase, thus making the machine electrically unbalanced. The references

TABLE V  
AVERAGE NUMBER OF SWITCHING TRANSITIONS IN THE STEADY STATE TEST FOR THE UNBALANCED FIVE-PHASE INDUCTION MACHINE

| [V]/[Hz] | Proposed method | CMI method | MS method | Standard CBPWM |
|----------|-----------------|------------|-----------|----------------|
| 150/50   | 91              | 53         | 102       | 80             |

were set again to 150 V/50 Hz. The results are shown in Fig. 12 and the corresponding average number of switching transitions per period are summarized in Table V.

As evident, this condition shows a significantly higher NP voltage fluctuation if compared to the balanced load (note that the scaling for  $v_{DC,B}$  and  $v_{DC,T}$  is now set to 5 V/div). Standard CBPWM shows the highest peak-to-peak voltage deviation (of about 10 V). The CMI-based technique, given the high modulation index, is unable to suppress this ripple and behaves poorly. On the contrary, the other two approaches guarantee the equalization and, as expected, the proposed technique operates with fewer switching transitions (about 11% less, Table V) due to the leg voltage clamping allowed by  $v_0^*$ .

## V. CONCLUSION

This article presented a carrier-based PWM technique for multiphase NPC converters with the dc-bus NP voltage control capability. The proposed strategy exploits all the available degrees of freedom of the system and optimally combines two standard approaches for this kind of control. Those standard approaches are either based on the sole injection of a proper common mode signal into the leg voltage references or on the sole MS working principle. The proposed approach guarantees the desired control in all the converter's working conditions, including high modulation indexes and unbalanced loads. It follows an iterative procedure aimed to reduce the switching transition rate, and hence the corresponding switching losses. The approach has been experimentally tested on a three-phase



and on a five-phase test-bench and compared with some other techniques available in the technical literature. The results show satisfactory behavior in all the testing scenarios and the proposed method is especially suited for high modulation indexes. It combines the benefits of both degrees of freedom for capacitors voltage balancing (CMI and MS operation) resulting in faster transient responses and in reduced transition rates.

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