Sarebanzadeh, Hosseinzadeh, M. A., Garcia, C., Babaei, E., Islam, S., & Rodriguez, J. (2021). Reduced Switch Multilevel Inverter Topologies for Renewable Energy Sources. *IEEE Access, 9,* 120580–120595.

Available online: https://doi.org/10.1109/ACCESS.2021.3105832

IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received July 14, 2021, accepted July 18, 2021, date of publication August 18, 2021, date of current version September 8, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3105832

Reduced Switch Multilevel Inverter Topologies for Renewable Energy Sources

MARYAM SAREBANZADEH[1], (Member, IEEE), MOHAMMAD ALI HOSSEINZADEH[1], (Member, IEEE), CRISTIAN GARCIA[1], (Member, IEEE), EBRAHIM BABAEI[2,3], (Senior Member, IEEE), SYED ISLAM[4], (Fellow, IEEE), AND JOSE RODRIGUEZ[5], (Life Fellow, IEEE)

[1]Faculty of Engineering, University of Talca, Talca 3460000, Chile
[2]Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 5166616471, Iran
[3]Faculty of Engineering, Near East University, Nicosia, 99138 Mersin, Turkey
[4]School of Engineering, Federation University Australia, Ballarat, VIC 3350, Australia
[5]Department of Engineering Science, Universidad Andres Bello, Santiago 8370146, Chile

Corresponding author: Maryam Sarebanzadeh (maryam_sarbanzadeh@yahoo.com)

This work was supported in part by the Agencia Nacional de Investigación y Desarrollo (ANID) through the Project under Grant Fondo Nacional de Desarrollo Científico y Tecnológico (FONDECYT) 11180235 and Grant ACT192013.

ABSTRACT This article proposes two generalized multilevel inverter configurations that reduce the number of switching devices, isolated DC sources, and total standing voltage on power switches, making them suitable for renewable energy sources. The main topology is a multilevel inverter that handles two isolated DC sources with ten power switches to create 25 voltage levels. Based on the main proposed topology, two generalized multilevel inverters are introduced to provide flexibility in the design and to minimize the number of elements. The optimal topologies for both extensive multilevel inverters are derived from different design objectives such as minimizing the number of elements (gate drivers, DC sources), achieving a large number of levels, and minimizing the total standing voltage. The main advantages of the proposed topologies are a reduced number of elements compared to those required by other existing multilevel inverter topologies. The power loss analysis and standalone PV application of the proposed topologies are discussed. Experimental results are presented for the proposed topology to demonstrate its correct operation.

INDEX TERMS DC-AC power converters, pulse width modulation converters, inverters, renewable energy sources, photovoltaic systems.

I. INTRODUCTION

The nominal power of energy generation and distribution systems has increased significantly in recent years. This has given rise to the need for increased power in high-power systems. Multilevel power inverters (MLIs) are a suitable topology for operating high-power systems since they overcome the limitation of the voltage rating of power switches [1], [2]. MLIs can share the input DC-link voltage between the power switches and decrease the standing voltage of power semiconductors more easily than their two-level inverter counterparts. The other advantage of MLIs is that they provide a large number of levels, which leads them to have a lower voltage distortion as well as lower dv/dt and a lower common-mode voltage [3], [4]. Therefore, MLIs can be applied in Renewable Energy Sources (RES), Variable Frequency Drives (VFD), Flexible Alternating Current Transmission System (FACTS) Devices, and Electrical Vehicles (EV) [5], [6].

Switched-diode based MLIs (SD-MLIs), switched-capacitor based MLIs (SC-MLI), and DC source based MLIs (DCS-MLIs) are three well-known multilevel inverter configurations [7], [8]. Discrete diodes, rather than switches, are used in SD-MLIs to minimize the number of power switches in order to incorporate a simple modulation technique. These classes of MLIs are limited in their ability to handle low power factors due to the use of diodes [9], [10]. The second class is SC-MLIs; they use capacitors rather than DC sources, which reduces the number of independent DC sources. Although SC-MLIs considerably decrease the number of isolated DC sources, they require a complicated control method to regulate the capacitor voltages. Additionally, SC-MLI

The associate editor coordinating the review of this manuscript and approving it for publication was Inam Nutkani.

capacitors store a large amount of energy, which results in high power losses [11], [12].

DCS-MLIs have two advantages over other multilevel inverters: they require neither capacitors, which involve a special voltage control technique, nor discrete diodes, which allows them to operate at low power factors. On the other hand, the drawback of DCS-MLIs is that they require a large number of power electronic devices and isolated DC sources to supply their many levels. This weakness leads to these inverters having complex control techniques, low efficiency, and high costs [13], [14]. Recently, different multilevel inverter topologies that reduce the number of components, isolated DC sources and the total standing voltage and simplify the control technique have been reported in the literature [15]–[18].

An asymmetrical multilevel inverter configuration, which was developed for cascaded MLIs, has been reported in [15], [16]. The presented topology creates 17 voltage levels with four DC power supplies, eight bidirectional switches, and two unidirectional switches. The amount of DC power supplies is so high to produce a low voltage (17-level). Therefore, each DC source requires its own capacitor in industry applications, which causes power losses and reduces the inverter's efficiency.

The ST-Type multilevel inverter [17] is another cascaded MLI topology from the literature. This MLI handles four isolated DC sources by using 12 switches to generate 17 levels. This topology has the advantage of lowering the peak switch voltage, but its 12 switches increase the complexity of the control.

The MLI developed in [18] is a K-Type inverter with an advanced topology that is described in [17]. This topology generates 13 voltage levels using 14 power switches (with two additional unidirectional switches). Its aim was to overcome the number of DC sources, which use two capacitors instead of two DC sources. Despite the fact that the number of DC sources in the K-Type inverter has been reduced, the power switches still is so high that they decrease the system's efficiency and raise its cost.

[19] introduces a compact MLI topology for achieving high voltage levels. This basic structure requires ten switches for four isolated DC sources to create 17 voltage levels. In addition, this structure's connections are cascaded to minimize the number of required elements. The major weakness of this topology is that it uses four DC sources to produce its 17 levels.

A generalized MLI structure that uses a reduced basic unit has been reported in [20]. The basic MLI unit only generates nine levels using ten unidirectional switches. The basic structure has been presented in two fashions, extended and cascaded. The generalized structures reduce the total standing voltage and the number of elements. switches and four independent DC sources. The benefit of this topology is that it reduces the blocking voltage value while its drawback is that it requires a high number of DC sources.

Two reduced MLI structures have been reported in [22], [23]. The first reduced MLI [22] is a 15-level MLI that uses ten power switches and three unequal DC sources. In [23], this reduced structure has been expanded to 25 voltage levels by including two additional IGBT and one more DC supply. Although the 25-level structure reduces the number of switches, the value of the total blocking voltage is still high. In addition, the number of DC sources is also high, and they cannot be replaced by capacitors.

The aforementioned 25-level structure from [23] uses two unequal DC supplies that are controlled by 14 power switches. This structure has only been investigated for cascaded connections and not for generalized arrangements. The authors presented a simple balancing control method for charging and discharging input capacitors while increasing the number of switching devices.

[24] introduces a cascaded MLI topology based on an extendable basic unit that can generate 11 levels with eight switches and three DC sources. The advantage of this topology is that it reduces the number of switches. However, when a high level is required, many DC sources are required, which in turn necessitates the use of capacitors and leads to increased power losses.

Another MLI topology that aims to reduce the voltage stress and the component count has been reported in [25]. Even though this is a topology that can reduce voltage stress to produce high voltage levels, it still requires many DC sources to reach high voltage levels.

In [26], an extendable basic unit for multilevel inverter topologies is developed; it increases the number of levels while decreasing voltage stress. The number of switches and DC power supplies is still high, and some switches still endure high voltage stress.

Regarding switched-capacitor MLIs, different 25-level topologies have recently been reported in [27]–[30]. [27] presents a modified 5-level T-type inverter that needs only one capacitor instead of the two required in a conventional topography. By cascading two of the basic inverters, a 25-level structure is created that reduces the number of DC sources and capacitors. The disadvantage of this topology is that it still requires more DC sources to generate more voltage levels since its basic topology is not extendable.

A multi-source switched capacitor MLI has been presented in [28] for PV systems. By using two DC sources and two capacitors, it can generate 25 levels. Although the number of capacitors is reduced in this topology, the number of switches is still high. Furthermore, it needs an H-bridge inverter that increases the total standing voltage.

A grid-connected SC-MLI has been presented in [29]; it uses two PUC inverters and generates 25 levels. The advantage of this topology is its low TSV and reduced number of components. However, to charge the capacitors, it needs a proper control strategy as well as sensors, which make it complex and costly to achieve high voltage levels.

In [30], an extendable switched-capacitor MLI has been developed. The main topology is a 25-level switched-capacitor MLI that uses two DC sources and two capacitors. This MLI can be extended to reach high voltage levels by connecting the switched capacitor unit or by using multiple DC sources. This topology has reduced the voltage stress significantly, but the number of switches required to generate high voltage levels is still high. In addition, when multiple switched-capacitor units are used to achieve high voltage levels, the number of capacitors increases significantly, resulting in low efficiency.

Therefore, based on what was discussed above, the main drawbacks of MLI structures are a large number of DC sources and semiconductor devices, and high blocking voltage values. The aim of this article is to propose a new MLI configuration based on a reduced modular module that involves a low number of semiconductor devices and DC sources, thus making the proposed topology suitable for high power renewable energy sources.

First, in Section II, a basic module is suggested that produces 25 voltage levels using ten switches and two asymmetric DC sources. Then, in Section III, two MLI topologies are developed according to the modular topology. The proposed cascaded connections of the developed MLIs along with their optimal topologies are studied in sections IV and V. Section V presents the comparison studies between the proposed topologies and other MLIs to demonstrate the performance of the proposal. The power losses and PV applications of the proposed MLIs are discussed in detail in Section VI. Finally, the 25-level modular topology is tested using the experimental results to ensure that the proposed MLI operates correctly.

II. PROPOSED BASIC MODULE

The architecture of the proposed basic module is displayed in Fig. 1(a). It is based on the concept of a T-type converter. The benefit of the T-Type converter is that it uses a power switch to connect its output to the upper and lower DC-link, and it also requires an isolated DC-link to charge the input capacitors.

Specifically, the basic module is designed based on two T-Type converters that can create different paths by crossing capacitors. The proposed topology produces the inherent positive and negative levels, and it eliminates the limitation of high voltage rating on power switches in topologies that would require an h-bridge converter to change the polarity.

The proposed topology consists of ten power switches and two DC-links (four capacitors). The power switches $T_1, T_2, T_3,$ *and* T_4 work in complementary mode to produce negative and positive levels.

The basic module based on choosing the magnitude of DC-links can operate with symmetric and asymmetric DC sources. If the quantity of all DC-links or capacitors is considered symmetric ($V_1 = V_2 = 2V_{dc}$), the proposed converter generates nine voltage levels. If the magnitudes of the chosen DC-links are asymmetric, the proposed basic topology produces different voltage levels with the same number of components. Hence, by selecting the quantities of V_2 as multiples of V_1, the proposed basic topology can produce different voltage levels, which are given in Table 1. Renewable energy sources such as photovoltaic panels, fuel cells, supercapacitors, etc., can be used to supply the DC-link voltage (V_1, V_2).

In order to balance the input capacitor voltages in applications that have unregulated DC sources (such as photovoltaic systems), a typical DC-DC boost multilevel converter, as described in [31], is implemented and adjusted to the proposed topology. This circuit comprises one boost converter and three discrete diodes, as shown in Fig. 2(a). The input voltage (V_{in}) is boosted in (V_{Cb}), and, through on and off states of the switch (S), the boost capacitor (C_b) is paralleled with the capacitors (C_1) and (C_2), which are charged the value of the boost capacitor voltage. As a result, the capacitors' voltages are kept in balance during the variation of unregulated DC sources.

The proposed basic topology has various operating modes that are generated by the activation of the different switching devices. Fig. 1(b) shows its operation modes in the case of 25 levels (corresponding to Table 1). Table 2 gives the synthesis of the state of the switches that generate each level; the 32 switching states are shown by the on switches. As can be seen in Table 2, some levels produce redundancy.

TABLE 1. Different voltage levels of the proposed basic topology in the asymmetric mode.

	V_1	V_2	$V_{omax} = V_1 + V_2$	$N_L = 2V_{omax} + 1$
1	$2V_{dc}$	$4V_{dc}$	$6V_{dc}$	13
2	$2V_{dc}$	$6V_{dc}$	$8V_{dc}$	17
3	$2V_{dc}$	$8V_{dc}$	$10V_{dc}$	21
4	$2V_{dc}$	$10V_{dc}$	$12V_{dc}$	25

In the first mode, there are two states that generate $\pm 2V_{dc}$, so the switches [T_1, S_3, S_6, T_4] or [T_1, S_2, S_3, T_3] are turned on to generate the voltage level of $+V_{dc}$. Meanwhile, the switches [T_2, S_3, S_6, T_4] or [T_2, S_2, S_2, T_3] are turned on to generate $-V_{dc}$.

Much like in the first mode, there are two states for generating $\pm V_{dc}$ in the second mode. The switches [T_1, S_5, S_6, T_4] or [T_1, S_4, S_4, T_3] are turned on to generate the voltage level of $+V_{dc}$, while the switches [T_2, S_1, S_2, T_3] or [T_2, S_1, S_6, T_4] are turned on to generate $-V_{dc}$.

In the twelfth mode, the switches [T_1, S_5, S_6, T_3] are turned on to generate the voltage level of $+12V_{dc}$ while the switches [T_2, S_1, S_2, T_4] generate $-12V_{dc}$. From this mode, it is clear that all DC voltages ($V_1 + V_2$) are summed together to create maximum voltage levels. Similarly, the remaining levels are obtained based on valid switching patterns, as shown in Table 2.

An essential element is the maximum total standing voltage (TSV) to reduce the cost of multilevel converters. If this factor is low, the converter's final price will be reduced. This factor also determines the type and rating of power electronics

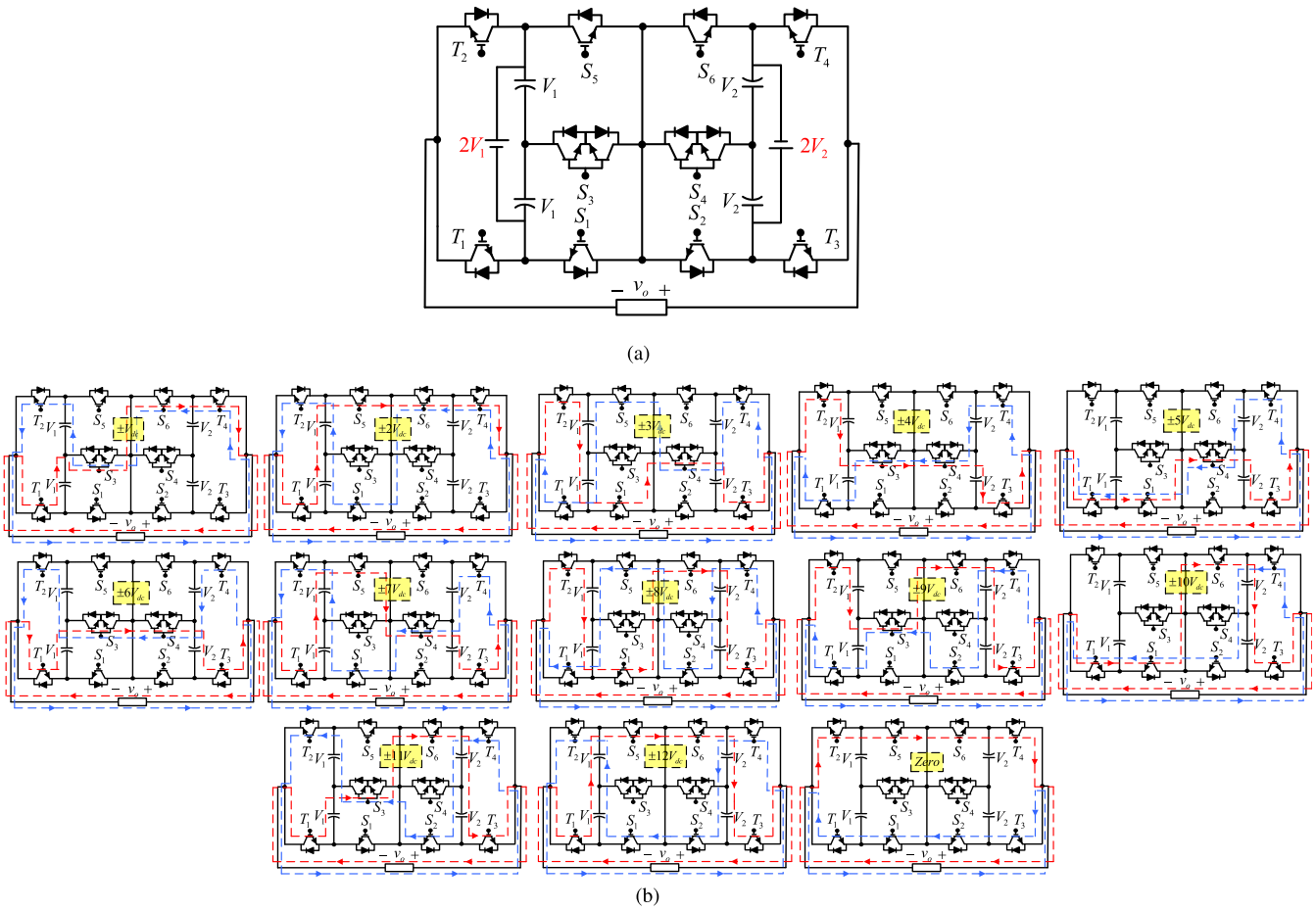


FIGURE 1. (a) Proposed basic module; (b) all operation modes of basic module.

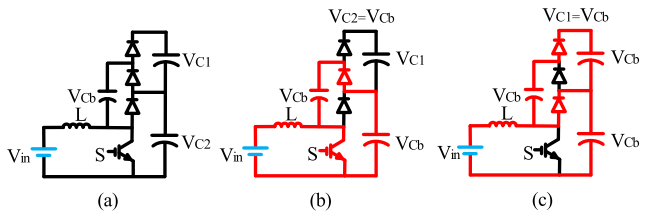


FIGURE 2. Conventional DC-DC boost multilevel converter presented in [31]; (a) on-state switch S; (b) off-state switch S.

devices (IGBTs, diodes). Thus, the maximum TSV of each power switch, in the proposed basic topology, is as follows:

$$TSV_{T_1} = TSV_{T_2} = TSV_{S_1} = TSV_{S_5} = 2V_1 \quad (1)$$

$$TSV_{T_3} = TSV_{T_4} = TSV_{S_2} = TSV_{S_6} = 2V_2 \quad (2)$$

$$TSV_{S_3} = V_1 \quad (3)$$

$$TSV_{S_4} = V_2 \quad (4)$$

In the proposed basic topology, the total standing voltage (TSV_{basic}) on power switches is the sum of the maximum voltage across each switch. Therefore, for the proposed basic topology, the TSV_{basic} value is:

$$TSV_{basic} = 9(V_1 + V_2) = \frac{9}{4}(N_{level} - 1)V_1 \quad (5)$$

III. PROPOSED MLI TOPOLOGIES

In this section, the proposed basic module is extended in two different ways. Two different MLI topologies are presented, and the relations between the number of elements, the number of voltage levels, and the maximum blocking voltage on the switches are calculated.

A. FIRST PROPOSED MLI

The first proposed MLI is illustrated in Fig. 2. In this topology, as in the basic topology, the magnitude of all DC voltages in part-a ($V_{1a}, V_{2a}, \ldots, V_{na}$) are the same, and similarly, the magnitude of all DC voltages in part-b ($V_{1b}, V_{2b}, \ldots, V_{nb}$) are the same. Hence, the magnitudes of the DC voltage sources are considered as follows:

$$V_{1a} = V_{2a} = \cdots = V_{na} = V_{dc} \quad (6)$$

$$V_{1b} = V_{2b} = \cdots = V_{nb} = (4N_{cell,a} + 1)V_{1a} \quad (7)$$

In the first proposed MLI, the number of components (number of DC sources (N_{DC}), number of drivers (N_{IGBT}), number of IGBTs (N_{Driver}) and the number of levels ($N_{L,F}$)) are obtained as follows:

$$N_{DC} = 2(N_{cell,a} + N_{cell,b}) = 2N_{cell} \quad (8)$$

TABLE 2. 32 Valid switching states of the proposed basic module.

States	On Switches	Output Voltage	V_o
1	T_1, S_1, S_2, T_3	0	0
2	T_2, S_5, S_6, T_4		
3	T_1, S_3, S_6, T_4	V_1	$+V_{dc}$
4	T_1, S_2, S_3, T_3		
5	T_2, S_3, S_6, T_4	$-V_1$	$-V_{dc}$
6	T_2, S_2, S_3, T_3		
7	T_1, S_5, S_6, T_4	$2V_1$	$+2V_{dc}$
8	T_2, S_2, S_3, T_3		
9	T_2, S_1, S_2, T_3	$-2V_1$	$-2V_{dc}$
10	T_2, S_1, S_6, T_4		
11	T_2, S_1, S_4, T_3	$V_2 - 2V_1$	$+3V_{dc}$
12	T_2, S_4, S_5, T_4	$-(V_2 - 2V_1)$	$-3V_{dc}$
13	T_2, S_3, S_4, T_3	$V_2 - V_1$	$+4V_{dc}$
14	T_1, S_3, S_4, T_4	$-(V_2 - V_1)$	$-4V_{dc}$
15	T_1, S_1, S_4, T_3	V_2	$+5V_{dc}$
16	T_2, S_4, S_5, T_3		
17	T_1, S_1, S_4, T_4	$-V_2$	$-5V_{dc}$
18	T_2, S_4, S_5, T_4		
19	T_1, S_3, S_4, T_3	$V_1 + V_2$	$+6V_{dc}$
20	T_2, S_3, S_4, T_4	$-(V_1 + V_2)$	$-6V_{dc}$
21	T_1, S_4, S_5, T_3	$2V_1 + V_2$	$+7V_{dc}$
22	T_2, S_1, S_4, T_4	$-(2V_1 + V_2)$	$-7V_{dc}$
23	T_2, S_1, S_6, T_3	$V_2 - 2V_1$	$+8V_{dc}$
24	T_1, S_2, S_5, T_4	$-(V_2 - 2V_1)$	$-8V_{dc}$
25	T_2, S_3, S_6, T_3	$V_2 - V_1$	$+9V_{dc}$
26	T_1, S_2, S_3, T_4	$-(V_2 - V_1)$	$-9V_{dc}$
27	T_1, S_1, S_6, T_3	$2V_2$	$+10V_{dc}$
28	T_1, S_1, S_2, T_4	$-2V_2$	$-10V_{dc}$
29	T_1, S_3, S_6, T_3	$V_1 + 2V_2$	$+11V_{dc}$
30	T_2, S_2, S_3, T_4	$-(V_1 + 2V_2)$	$-11V_{dc}$
31	T_1, S_5, S_6, T_3	$2V_1 + 2V_2$	$+12V_{dc}$
32	T_2, S_1, S_2, T_4	$-(2V_1 + 2V_2)$	$-12V_{dc}$

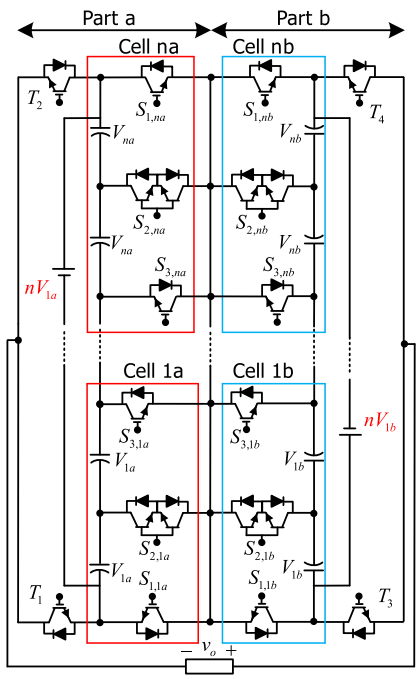


FIGURE 3. First proposed MLI configuration.

$$N_{IGBT} = 4N_{cell} + 4 \tag{9}$$
$$N_{Driver} = 2N_{cell} + 6 \tag{10}$$
$$N_{L,F} = (2N_{cell} + 1)^2 \tag{11}$$

Here, $N_{cell,a} and N_{cell,b}$ are the number of cells in part-a and part-b, respectively, and N_{cell} is the sum of $N_{cell,a} + N_{cell,b}$.

In the first proposed MLI (Fig. 2), the maximum standing voltage (MSV) value of the switches is related to the switch locations. The MSV is the maximum stress voltage that a switch can withstand. As a criterion, the MSV value in the first proposed MLI MSV_{F-MLI} is defined as the sum of the stress voltage of the switches. To calculate the MSV_{F-MLI} value, the first proposed MLI is divided into three parts. The first part comprises the power switches of part-a of the converter $S_{1,1a}, S_{2,1a}, S_{3,1a}, \cdots, S_{3,na}$, the second part comprises the switches of part-b of the converter $S_{1,1b}, S_{2,1b}, S_{3,1b}, \cdots, S_{3,nb}$, and the third part is made up of the four fixed power switches $T_1, T_2, T_3, and T_4$.

The $MSV_{F,a}$ is the MSV value of the power switches of part-a of the converter $S_{1,1a}, S_{2,1a}, \cdots, S_{3,na}$. They are calculated as follows:

$$[4N_{cell,a} + 4(N_{cell,a} - 2) + \cdots + N_{cell,a}]V_{1a} \tag{12}$$
$$MSV_{F,a} = [3N_{cell,a}^2 + 2N_{cell,a}]V_{1a} \tag{13}$$

Similarly, the $MSV_{F,b}$ is the MSV value for the power switches of part-b. It is obtained as follows:

$$MSV_{F,b} = [3N_{cell,b}^2 + 2N_{cell,b}]V_{1b} \tag{14}$$

$MSV_{F,T}$ is the maximum standing voltage of the four power switches of $T_1, T_2, T_3, and T_4$, which can be written as follows:

$$MSV_{F,T} = 4(N_{cell,a}V_{1a} + N_{cell,b}V_{1b}) \tag{15}$$

Since $N_{cell} = N_{cell,a} + N_{cell,b}$ and $N_{cell,a} = N_{cell,b}$, Eq. (13) and Eq. (15) can be rewritten as follows:

$$MSV_{F,a+b} = (\frac{3N_{cell}^2}{4} + N_{cell})(V_{1a} + V_{1b}) \tag{16}$$

Similarly, Eq. (16) can be rewritten as follows:

$$MSV_{F,T} = 2N_{cell}(V_{1a} + V_{1b}) \tag{17}$$

By referring to Eq. (16) and Eq. (17), the MSV value of the first proposed MLI for $N_{cell} = 2, 4, 6, \cdots$, can be obtained as follows:

$$\begin{aligned} MSV_{F-MLI} &= MSV_{F,a,b} + MSV_{F,T} \\ &= 3(\frac{N_{cell}^2}{4} + N_{cell})(V_{1a} + V_{1b}) \end{aligned} \tag{18}$$

B. SECOND PROPOSED MLI

The configuration of the second proposed MLI is illustrated in Fig. 3. In this topology, the magnitudes of the two DC voltage sources in each cell are the same, and they are different from those of other cells. Thus, the value of the DC voltage sources in each cell for part-a can be calculated as follows:

$$V_{1a} = V_{dc}, V_{2a} = 2V_{1a}, V_{3a} = 3V_{1a}, \cdots, V_{na} = nV_{1a} \tag{19}$$

And for part-b the values are as follows:

$$\begin{aligned} V_{1b} &= (2N_{cell,a}^2 + 2N_{cell,a} + 1)V_{1a}, \\ V_{2b} &= 2V_{1b}, V_{3b} = 3V_{1b}, \cdots, V_{nb} = nV_{1b} \end{aligned} \tag{20}$$

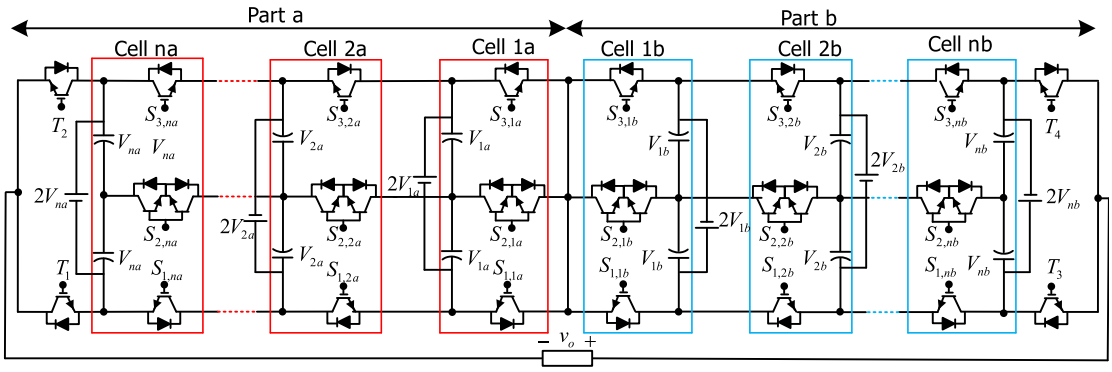


FIGURE 4. Second proposed MLI configuration.

In the second proposed MLI, the number of IGBTs and DC sources are the same as in the first proposed MLI (Eq. (8) and Eq. (9)), and the quantities of drivers ($N_{Driver,S}$) and levels ($N_{L,S}$) are obtained as follows:

$$N_{Driver,S} = 3N_{cell} + 4 \tag{21}$$

$$N_{L,S} = (\frac{N_{cell}^2}{2} + N_{cell} + 1)^2 \tag{22}$$

The maximum standing voltage of the switches in the second proposed MLI MSV_{S-MLI} (Fig. 3) is calculated similarly to the method presented for the first MLI. Hence, this configuration is divided into three parts. The first part contains the power switches of part-a, the second part contains the power switches of part-b, and the third part contains four fixed power switches $T_1, \cdots, T_4$. The $MSV_{S,a}$ is the sum of the standing voltage on the power switches in each cell of part-a of the converter $MSV_{cell-1a}, MSV_{cell-2a}, \cdots, MSV_{cell-na}$. They are calculated as follows:

For cell-1a:

$$\begin{aligned} MSV_{cell-1a} &= V_{S_{1,1a}} + V_{S_{2,1a}} + V_{S_{3,1a}} \\ &= 2V_{1a} + V_{1a} + 2V_{1a} = 5V_{1a} \end{aligned} \tag{23}$$

For cell-2a:

$$\begin{aligned} MSV_{cell-2a} &= V_{S_{1,2a}} + V_{S_{2,2a}} + V_{S_{3,2a}} \\ &= 2(V_{1a} + V_{2a}) + (V_{1a} + V_{2a}) + 2(V_{1a} + V_{2a}) \\ &= 5(V_{1a} + V_{2a}) \end{aligned} \tag{24}$$

For cell-na:

$$\begin{aligned} MSV_{cell-na} &= V_{S_{1,na}} + V_{S_{2,na}} + V_{S_{3,na}} \\ &= 2(V_{1a} + V_{2a} + \cdots + V_{na}) \\ &\quad +(V_{1a} + V_{2a} + \cdots + V_{na}) \\ &\quad +2(V_{1a} + V_{2a} + \cdots + V_{na}) \\ &= 5(V_{1a} + V_{2a} + \cdots + V_{na}) \end{aligned} \tag{25}$$

Therefore, $MSV_{S,a}$ is obtained as follows:

$$\begin{aligned} MSV_{S,a} &= MSV_{cell-1a} + MSV_{cell-2a} + \cdots + MSV_{cell-na} \\ &= 5[V_{1a} + (V_{1a} + V_{2a}) + \cdots + (V_{1a} \\ &\quad +V_{2a} + \cdots + V_{na})] \end{aligned} \tag{26}$$

By substituting Eq. (20) into Eq. (26), (26) can be rewritten as follows:

$$\begin{aligned} MSV_{S,a} &= 5V_{1a}(1 + 3 + 5 + \cdots + (2N_{cell,a} - 1)) \\ &= 5[\sum_{j=1}^{N_{cell,a}} (2j-1)V_{1a}] = 5N_{cell,a}^2 V_{1a} \end{aligned} \tag{27}$$

Here, $N_{cell,a}$ is the total number of cells in part-a.

Similarly, by considering Eq. (26) and Eq. (20), the value of $MSV_{S,b}$ for part-b is obtained:

$$MSV_{S,b} = 5N_{cell,b}^2 V_{1b} \tag{28}$$

Here, $N_{cell,b}$ is the total number of cells in part-b. $MSV_{S,T}$ is the maximum standing voltage of the four power switches of $T_1, \cdots, T_4$, which can be expressed as follows:

$$MSV_{S,T} = 4(N_{cell,a}V_{1a} + N_{cell,b}V_{1b}) \tag{29}$$

Meanwhile, $N_{cell} = N_{cell,a} + N_{cell,b}$ and $N_{cell,a} = N_{cell,b}$, Eq. (26) and Eq. (27), can be written as follows:

$$MSV_{S,a+b} = \frac{5N_{cell}^2}{4}(V_{1a} + V_{1b}) \tag{30}$$

Also, Eq. (28) can be written as follows:

$$MSV_{S,T} = 2N_{cell}(V_{1a} + V_{1b}) \tag{31}$$

According to the Eqs. (29)-(30), the MSV value for the second proposed MLI for $N_{cell} = 2, 4, 6, \cdots$, can be obtained as follows:

$$\begin{aligned} MSV_{S-MLI} &= MSV_{S,a+b} + MSV_{S,T} \\ &= (\frac{5N_{cell}^2}{4} + 2N_{cell})(V_{1a} + V_{1b}) \end{aligned} \tag{32}$$

IV. PROPOSED CASCADED CONNECTION

Two cascaded configurations are submitted based on the cascaded connection of the proposed MLIs to minimize the number of elements. Fig. 4 indicates the cascaded connection of the proposed multilevel inverters with a quantity k of the proposed basic modules. Since the maximum output voltage in the output of the proposed cascaded topology is the sum of the output voltage of each basic module, the output voltage of the proposed cascaded topology can be expressed as follows:

$$V_{out} = v_{o1} + v_{o2} + \cdots + v_{ok} \tag{33}$$

A. FIRST PROPOSED CASCADED TOPOLOGY

The aim of the first proposed cascaded topology is to maximize the number of voltage levels. In this configuration, the magnitudes of the DC voltage sources are arranged as follows:

For the first MLI:

$$V_{1a,1} = V_{dc} \tag{34}$$

$$V_{1b,1} = (4N_{cell,1a} + 1)V_{1a,1} \tag{35}$$

For the second MLI:

$$V_{1a,2} = V_{1a,1} + 4N_{cell,1a}\sum_{j=1}^{2} V_{ja,1} \tag{36}$$

$$V_{1b,2} = (4N_{cell,2a} + 1)V_{1a,2} \tag{37}$$

TABLE 3. Required number of components of the proposed cascaded topologies.

Number of Components	k number of First MLI	k number of Second MLI
Number of Switches	$k(2N_{cell}+6)$	$k(3N_{cell}+4)$
Number of IGBTs	$4k(N_{cell}+1)$	$4k(N_{cell}+1)$
Number of Diodes	$4k(N_{cell}+1)$	$4k(N_{cell}+1)$
Number of DC Sources	kN_{cell}	kN_{cell}

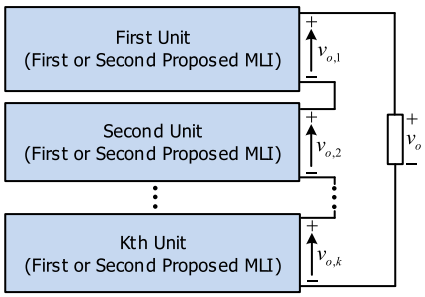


FIGURE 5. Proposed cascaded MLI configurations.

For the Kth MLI:

$$V_{1a,k} = V_{1a,1} + 4N_{cell,(k-1)a}\Big(\sum_{j=1}^{2}\sum_{i=1}^{k} V_{ja,i}\Big) \tag{38}$$

$$V_{1b,k} = (4N_{cell,ka} + 1)V_{1a,k} \tag{39}$$

Therefore, the number of levels for the first proposed cascaded topology $N_{L,F,cas}$ is obtained as follows:

$$N_{L,F,cas} = \prod_{i=1}^{K}(2N_{cell,i} + 1)^2 \tag{40}$$

Here, $N_{cell,i}$ is the total number of cells in the ith unit of the proposed cascaded topology.

As per Eq. (30), the total standing voltage of the power switches $TSV_{F,cas}$ in the first proposed cascaded topology can be calculated as follows:

$$TSV_{F,cas} = \sum_{i=1}^{k} 3\Big(\frac{N_{cell,i}^2}{4} + N_{cell,i}\Big)(V_{1a,i} + V_{1b,i}) \tag{41}$$

B. SECOND PROPOSED CASCADED TOPOLOGY

The aim of the second proposed cascaded topology is to minimize the number of levels. The magnitudes of the DC voltage sources in this configuration can be considered as follows:

For the first MLI:

$$V_{1a,1} = V_{dc},$$
$$V_{2a,1} = 2V_{1a,1}, \cdots, V_{na,1} = nV_{1a,1} \tag{42}$$
$$V_{1b,1} = (2N_{cell,a,1}^2 + 2N_{cell,a,1} + 1)V_{1a,1},$$
$$V_{2b,1} = 2V_{1b,1}, \cdots, V_{nb,1} = nV_{1b,1} \tag{43}$$

For the second MLI:

$$V_{1a,2} = N_{L,1}V_{dc},$$
$$V_{2a,2} = 2V_{1a,2}, \cdots, V_{na,2} = nV_{1a,2} \tag{44}$$
$$V_{1b,2} = (2N_{cell,a,2}^2 + 2N_{cell,a,2} + 1)V_{1a,2},$$
$$V_{2b,2} = 2V_{1b,2}, \cdots, V_{nb,2} = nV_{1b,2} \tag{45}$$

For the Kth MLI:

$$V_{1a,k} = N_{L,k-1}V_{dc},$$
$$V_{2a,k} = 2V_{1a,k}, \cdots, V_{na,k} = nV_{1a,k} \tag{46}$$
$$V_{1b,2k} = (2N_{cell,a,k}^2 + 2N_{cell,a,k} + 1)V_{1a,k},$$
$$V_{2b,k} = 2V_{1b,k}, \cdots, V_{nb,k} = nV_{1b,k} \tag{47}$$

Therefore, the number of levels for the second proposed cascaded topology $N_{L,S,cas}$ is obtained as follows:

$$N_{L,S,cas} = \prod_{i=1}^{K}\Big(\frac{N_{cell,i}^2}{2} + N_{cell,i} + 1\Big)^2 \tag{48}$$

Here, $N_{cell,i}$ is the total number of cells in the ith unit of the proposed cascaded topology.

As per Eq. (32), the total standing voltage of the power switches, $TSV_{S,cas}$, for the second proposed cascaded topology can be calculated as follows:

$$TSV_{S,cas} = \sum_{i=1}^{k}\Big(\frac{5N_{cell,i}^2}{4} + 2N_{cell,i}\Big)(V_{1a,i} + V_{1b,i}) \tag{49}$$

V. OPTIMAL TOPOLOGIES

The objective of extracting an optimal topology in the proposed cascaded topologies is either to maximize the number of output voltage levels with a fixed number of components or to minimize the number of elements required to generate a specific level. Therefore, there are two main factors to keep in mind when designing the optimal topology: the number of cells in each proposed MLI, N_{cell}, and the amount of series in each proposed MLI, k. Both factors impact the maximum magnitude of the output voltage. We consider the N_{cell} variable to obtain optimal topologies and k for the peak of the output voltage.

In the proposed cascaded MLIs, the number of levels is maximized when the number of cells is equal in each proposed MLI. That is:

$$N_{cell,1} = N_{cell,2} = \cdots = N_{cell,k} = N_{cell} \tag{50}$$

TABLE 4. Optimal topologies of the first and second proposed cascaded topologies.

Cascaded Conf.	First Scenario: Maximizing N_L with Constant N_{com} and TSV	N_{cell}	Second Scenario: Minimizing N_{comp} with Constant N_L and TSV	N_{cell}
First Proposed Topology	$N_{L,F,cas} = \underbrace{[(2N_{cell}+1)^{\frac{1}{N_{cell}+3}}]}_{A_1}^{N_{Driver}}$	2.5	$\frac{N_{Driver}}{lnN_{L,F,cas}} = \frac{N_{cell}+3}{ln(2N_{cell}+1)} = E_1$	2.5
	$N_{L,F,cas} = \underbrace{[(2N_{cell}+1)^{\frac{1}{2N_{cell}+2}}]}_{B_1}^{N_{IGBT}}$	2	$\frac{N_{IGBT}}{lnN_{L,F,cas}} = \frac{2N_{cell}+2}{ln(2N_{cell}+1)} = F_1$	2
	$N_{L,F,cas} = \underbrace{[(2N_{cell}+1)^{\frac{1}{N_{cell}}}]}_{C_1}^{N_{DC}}$	2	$\frac{N_{DC}}{lnN_{L,F,cas}} = \frac{N_{cell}}{ln(2N_{cell}+1)} = G_1$	2
	$\frac{N_{L,F,cas}-1}{V_{dc}TSV_{F,cas}} = \frac{8}{3N_{cell}+12} = D_1$	2	$\frac{TSV_{F,cas}}{V_{dc}(N_{L,F,cas}-1)} = \frac{3N_{cell}+12}{8} = H_1$	2
Second Proposed Topology	$N_{L,S,cas} = \underbrace{[(\frac{N_{cell}^2}{2}+N_{cell}+1)^{\frac{2}{3N_{cell}+4}}]}_{A_2}^{N_{Driver}}$	2.7	$\frac{N_{Driver}}{lnN_{L,S,cas}} = \frac{3N_{cell}+4}{2ln(\frac{N_{cell}^2}{2}+N_{cell}+1)} = E_2$	2
	$N_{L,S,cas} = \underbrace{(\frac{N_{cell}^2}{2}+N_{cell}+1)^{\frac{1}{2N_{cell}+2}}]}_{B_2}^{N_{IGBT}}$	2.5	$\frac{N_{IGBT}}{lnN_{L,S,cas}} = \frac{2N_{cell}+2}{ln(\frac{N_{cell}^2}{2}+N_{cell}+1)} = F_2$	2.6
	$N_{L,S,cas} = \underbrace{(\frac{N_{cell}^2}{2}+N_{cell}+1)^{\frac{1}{N_{cell}}}]}_{C_2}^{N_{DC}}$	2	$\frac{N_{DC}}{lnN_{L,F,cas}} = \frac{N_{cell}}{ln(\frac{N_{cell}^2}{2}+N_{cell}+1)} = G_2$	2
	$\frac{N_{L,S,cas}-1}{V_{dc}TSV_{F,cas}} = \frac{2N_{cell}+4}{5N_{cell}+8} = D_2$	2	$\frac{TSV_{S,cas}}{V_{dc}(N_{L,S,cas}-1)} = \frac{5N_{cell}+8}{2N_{cell}+4} = H_2$	2

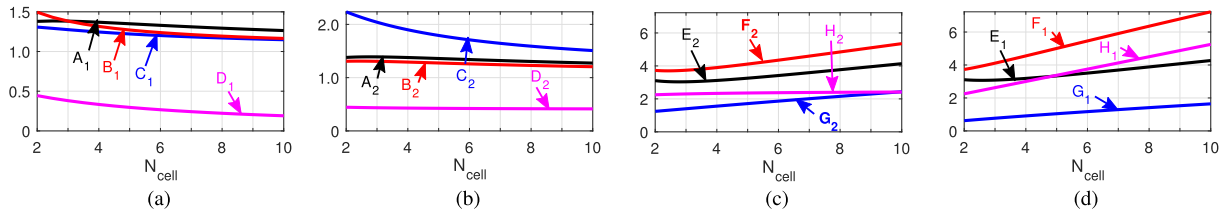


FIGURE 6. Optimal topologies; (a) first scenario for the first proposed MLI; (b) first scenario for the second proposed MLI; (c) second scenario for the first proposed MLI; (d) second scenario for the second proposed MLI.

Therefore, the number of components of the first proposed cascaded topology, shown in Table 3, can be expressed as follows:

$$N_{driver} = 2k(N_{cell}+3) \tag{51}$$

$$N_{IGBT} = 2k(2N_{cell}+2) \tag{52}$$

$$N_{DC} = 2kN_{cell} \tag{53}$$

And, considering Eq. (40) and Eq. (41), the number of levels and the TSV value can be expressed as follows:

$$N_{L,F,cas} = (2N_{cell}+1)^{2k} \tag{54}$$

$$TSV_{F,cas} = V_{dc} \times (\frac{3N_{cell}+12}{8})(N_{L,F,cas}-1) \tag{55}$$

For the second proposed cascaded topology, the number of IGBTs and DC sources is given by Eq. (51) and Eq. (52), respectively. As per Table 3, the number of drivers can be expressed as follows:

$$N_{driver} = k(4N_{cell}+3) \tag{56}$$

Taking Eq. (47) and Eq. (48) into consideration, the number of levels and the TSV value for the second proposed cascaded MLI can be expressed as follows:

$$N_{L,S,cas} = (\frac{N_{cell,i}^2}{2}+N_{cell,i}+1)^{2k} \tag{57}$$

$$TSV_{S,cas} = V_{dc} \times (\frac{5N_{cell}+8}{2N_{cell}+4})(N_{L,S,cas}-1) \tag{58}$$

There are two scenarios that achieve optimality for the two proposed cascaded topologies. The purpose of the first scenario is to produce the maximum number of levels at the output with a constant number of components (drivers, IGBTs, DC source) and a fixed TSV value.

The purpose of the second scenario is to minimize the number of components and the TSV value for a fixed number of output voltage levels.

The results of these two scenarios for both proposed cascaded MLIs are given in Table 4. All the equations given in Table 4 are obtained from Eqs. (50)-(57) for both proposed cascaded topologies. As Table 4 shows, in the first scenario, the number of levels is calculated based on a fixed number of components and the TSV value.

Using the first cascaded topology in this scenario, the indexes A1, B1, C1, and D1 should be maximized to

TABLE 5. All required parameters of the presented MLIs for comparison study correspond to DC power supplies' magnitude.

Conf.	M	N_{Switch}	N_{Diode}	N_{DC}	N_{Cap}	$N_{ON-Switch}$	PSV(p.u)	TBV(p.u)
NPC	R1	$2(N_L-1)$	$3N_L-1$	$(N_L-1)/2$	N_L-1	N_L-1	1	$2(N_L-1)$
FC	R2	$2(N_L-1)$	$2(N_L-1)$	2	N_L-2	N_L-1	1	$2(N_L-1)$
CHB	R3	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	-	N_L-1	1	$2(N_L-1)$
	R4	$4[\log_2^{(N_L+1)}-1]$	$4[\log_2^{(N_L+1)}-1]$	$[\log_2^{(N_L+1)}]-1$	-	$2[\log_2^{(N_L+1)}]-1$	$(N_L+1)/4$	$2(N_L-1)$
	R5	$4\log_3^{N_L}$	$4\log_3^{N_L}$	$\log_3^{N_L}$	-	$2\log_3^{N_L}$	$N_L/3$	$2(N_L-1)$
[23]	R6	$14[(N_L-1)/8]$	$14[(N_L-1)/8]$	$2[(N_L-1)/8]$	$4[(N_L-1)/8]$	$6[(N_L-1)/8]$	5	$35[(N_L-1)/12]$
	R7	$14\log_{25}^{N_L}$	$14\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$4\log_{25}^{N_L}$	$6\log_{25}^{N_L}$	$10N_L/25$	$35[(N_L-1)/12]$
[17]	R8	$12[(N_L-1)/8]$	$12[(N_L-1)/8]$	$(N_L-1)/2$	-	$5[(N_L-1)/8]$	4	$5(N_L-1)/2$
	R9	$12\log_{17}^{N_L}$	$12\log_{17}^{N_L}$	$4\log_{17}^{N_L}$	-	$5\log_{17}^{N_L}$	$8N_L/17$	$5(N_L-1)/2$
[18]	R10	$14[(N_L+6)/4]$	$14[(N_L+6)/4]$	$2(N_L+6)/4$	$2[(N_L+6)/4]$	$8[(N_L+6)/4]$	6	$4(N_L+6)$
	R11	$14[(N_L+10)/12]$	$14[(N_L+10)/12]$	$2(N_L+10)/12$	$2[(N_L+10)/12]$	$8[(N_L+10)/12]$	$6N_L/13$	$32[(N_L+10)/12]$
[19]	R12	$10[(N_L-1)/8]$	$10[(N_L-1)/8]$	$(N_L-1)/2$	-	$4[(N_L-1)/8]$	2	$9[(N_L-1)/4]$
	R13	$10\log_{17}^{N_L}$	$10\log_{17}^{N_L}$	$4\log_{17}^{N_L}$	-	$4\log_{17}^{N_L}$	$6N_L/17$	$9[(N_L-1)/4]$
[20]	R14	$10[(N_L-1)/8]$	$10[(N_L-1)/8]$	$(N_L-1)/2$	-	$5[(N_L-1)/8]$	2	$9[(N_L-1)/4]$
[21]	R15	$10\log_{17}^{N_L}$	$10\log_{17}^{N_L}$	$4\log_{17}^{N_L}$	-	$5\log_{17}^{N_L}$	$6N_L/13$	$9[(N_L-1)/4]$
[22]	R16	$12[(N_L-1)/6]$	$12[(N_L-1)/6$	$3[(N_L-1)/6$	-	(N_L-1)	2	$5[(N_L-5)/2]$+10
	R17	$0.2(N_L-5)+8$	$0.2(N_L-5)+8$	$0.1(N_L-5)+2$	-	$0.6(N_L-5)$	$0.4(N_L-5)$+2	$5[(N_L-5)/2]$+10
[24]	R18	$8[(N_L-1)/6]$	$8[(N_L-1)/6]$	$3[(N_L-1)/6]$	-	$4[(N_L-1)/6]$	3	$2(N_L+1)$
	R19	$8\log_{11}^{N_L}$	$8\log_{11}^{N_L}$	$3\log_{11}^{N_L}$	-	$4\log_{11}^{N_L}$	$5N_L/11$	$2(N_L+1)$
[25]	R20	N_L+1	N_L+1	$(N_L-1)/2$	-	$(N_L+1)/2$	3	$2(N_L+1)$
	R21	$2\log_2^{N_{L+1}}+2$	$2\log_2^{N_{L+1}}+2$	$3\log_2^{N_L+3}$	-	$\log_2^{N_L+3}+1$	$(N_L+3)/4$	$5(N_L-1)/2$
[26]	R22	$(N_L+13)/3$	$(N_L+13)/3$	$(N_L+7)/6$	-	$(N_L+13)/6$	$(N_L+19)/3$	$2(N_L+1)$
[27]	R23	$10\log_{25}^{N_L}$	$16\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$6N_L/25$	$10N_L/25$	$5[(N_L-1)/2]$
[28]	R24	$14\log_{25}^{N_L}$	$14\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$7N_L/25$	$12N_L/25$	$10[(N_L-1)/3]$
[29]	R25	$12\log_{25}^{N_L}$	$12\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$6N_L/25$	$10N_L/25$	$2(N_L-1)$
[30]	R26	$(N_L+53)/6$	$(N_L+31)/4$	2	$(N_L-1)/12$	$(N_L-1)/4$	$(N_L-1)/2$	$(3N_L+7)/4$
	R27	$(N_L+79)/8$	$(N_L+79)/8$	$(N_L+7)/16$	2	$(3N_L+71)/16$	$(N_L-1)/2$	$(13N_L+3)/16$
PT	I	$10[(N_L-1)/24]$	$12[(N_L-1)/24$	$2[(N_L-1)/24$	$4[(N_L-1)/24]$	$4[(N_L-1)/24]$	2	$9[(N_L-1)/4]$
	II	$10\log_{25}^{N_L}$	$10\log_{25}^{N_L}$	$2\log_{25}^{N_L}$	$4\log_{25}^{N_L}$	$4N_L/25$	$10N_L/25$	$9[(N_L-1)/4]$

produce the maximum number of levels. Hence, these indexes are plotted against N_{cell}, as shown in Fig. 6(a). This figure shows that the number of cells is equal to two because the equations of the second proposed MLI are obtained for an even number of cells. As Fig. 5(a) shows, indexes B1, C1, and D1 are maximized at $N_{cell} = 2$, and index A1 is maximized at $N_{cell} = 2.5$. Because N_cell should be an integer, the closest integer number must be chosen if an integer number is not obtained. Therefore, $N_{cell} = 2$ is chosen for index A1.

The first scenario is performed using the second proposed topology as well. The results are shown in Table 4. As shown in Fig. 6(b), the indexes of A2 and B2 are maximized when $N_{cell} = 2.5$ and 2.7, respectively. As previously mentioned, the number of cells should be an even integer, so $N_{cell} = 2$ is chosen for indexes A2 and B2. Indexes C2 and D2 are maximized at $N_{cell} = 2$.

The second scenario is performed for both proposed cascaded MLIs to minimize the number of components and the TSV value for a fixed number of levels. Table 4 and Fig. 6(c) show that, for the first proposed cascaded MLI, the number of cells for the three indexes F1, G1, and H1 is maximized when $N_{cell} = 2$ while index E1 is maximized when $N_{cell} = 2.5$. E1 should be an integer number, so we chose 2.0. Similarly, the second scenario is run using the second proposed cascaded MLI. Based on Table 4 and Fig. 6(d) for this configuration, indexes G2 and H2 are maximized when $N_{cell} = 2$. Indexes E2 and F2 are maximized when $N_{cell} = 3.2$ and 2.6, respectively; since they must be an even integer, we have chosen 2.0.

To conclude, as discussed above, the number of cells N_{cell} in each unit of the proposed MLIs should be two cells for both proposed cascaded configurations in both scenarios. This means that the optimal topologies consist of ten switches, 12 IGBTs, and four DC sources, as indicated by Eqs. (51)-(53).

VI. COMPARISON STUDIES

To demonstrate the advantages and drawbacks of the proposed cascaded MLI topologies, a comprehensive comparison is drawn between the proposed MLI topology and other cascaded MLI topologies. The comparative study considers the number of power switches, DC voltage sources, maximum on-state switches, peak switch voltage, and magnitude of TSV to validate the capabilities of the proposed topology as compared to other existing topologies [17]–[30].

Power switches are the most important component of multilevel inverters since they define the reliability and affect the level of sophistication of the control. The number of switches facing the number of voltage levels is exhibited in Fig. 7(a) for all discussed MLIs and proposed cascaded topologies. Fig. 6(a) confirms that, in both symmetric and asymmetric modes (proposals I and II, respectively), the proposed cascaded topology requires significantly fewer switches to produce the highest number of levels than those required in other MLIs (e.g., R26 and R27, which both use asymmetric configurations). This capability is valued as a specific merit for the proposed cascaded topologies because the control of this topology will be easier to control than other MLIs.

The numbers of DC voltage sources required to generate different voltage levels are compared in Fig. 7(b) for all MLI topologies. Here, it is clear that, in both symmetric and asymmetric modes (proposals I and II, respectively), the proposed cascaded MLIs require fewer DC sources; this is another strength of the proposed topologies. It should be noted that although [30] (R26) uses only two DC voltage sources to generate high voltage levels, it utilizes a high number of capacitors.

Fig. 7(c) compares the number of capacitors to the number of voltage levels, and it is clear that the proposed topology uses fewer capacitors than those required by other MLIs. The exception is [30], which needs only two capacitors but uses multiple DC sources.

Fig. 7(d) compares the maximum on-state switches to the number of levels. This factor impacts the power lost by MLIs. In the proposed topology, it is reduced in both modes of operation since the proposed topology requires fewer switches.

The peak switch voltage (PSV) comparison is exhibited in Fig. 7(e). This figure shows that the proposed topology performs well in terms of peak switch voltage in the symmetric DC source. It has a lower PSV than that of other recent MLIs, and in the asymmetric DC source category, it ranks after trinary CHB and [19]–[21], [25].

Fig. 7(f) compares the TSV values to the number of levels produced by the proposed topologies and all aforementioned MLIs. The conventional structures (NPC, FC, CHB) clearly have a low TSV value as does [30]; meanwhile, the proposed topology ranks third along with [19]–[21].

VII. POWER LOSSES

The power losses of semiconductor devices are divided into two types: conduction and switching losses [9], [13]. In power electronics devices, conduction losses appear while the semiconductor devices are in on-state mode. The type of switch used is an IGBT with a unit-parallel diode that can be expanded for MLIs. In instantaneous conduction, the power losses of a power switch are identical to:

$$P_{con}(t) = [V_{IGBT} + V_{diode} + R_{IGBT} I_p^{\beta}(t) + R_{diode} I_p(t)] I_p(t) \tag{59}$$

Here, V_{IGBT}, V_{diode}, R_{IGBT}, and R_{diode} are the threshold IGBT voltage, the diode voltage, the IGBT resistance, and the diode resistance, respectively, and β is a constant.

The proposed MLIs have low conduction losses because they use fewer on-state switches than other MLIs, as shown in Fig. 7(c).

Switching losses are defined as power that is wasted while the power is being turned off or turned on. This loss is calculated for the switch and the anti-parallel diode, which is highly correlated with the switching frequency (f_s), and the standing voltage of the switches. The switching frequency is dependent on modulation techniques, and the standing voltage depends on the converter circuit. The switching losses of anti-parallel diodes are generally neglected due to the fast conducting of diodes. The switching losses (P_{ON}, P_{OFF}) for N number of IGBTs can be obtained as follows:

$$P_{SW,ON,j} = \int_0^{t_{ON}} \left[\frac{I(t - t_{ON}) V_{stand,j} t}{t_{ON}} \right] dt = \frac{1}{6} \times I \times t_{ON} \times V_{stand,j} \tag{60}$$

$$P_{SW,OFF,j} = \frac{1}{6} \times I \times t_{OFF} \times V_{stand,j} \tag{61}$$

Here, $V_{stand,j}$, I, t_{ON}, and t_{OFF} are the voltage of IGBT in either off-state or on-state, the flowing current of the IGBT, and the on-state and off-state of the IGBT, respectively. The switching losses (P_{SW}) are equal to the sum of the energy lost during turn-on and turn-off in a fundamental cycle of the output voltage; this is computed as follows:

$$P_{SW} = \left[\sum_{k=1}^{N_{IGBT}} \left[\sum_{i=1}^{N_{ON,k}} P_{ON,ki} + \sum_{i=1}^{N_{OFF,k}} P_{off,ki} \right] \right] f \tag{62}$$

where f is the fundamental frequency, and $N_{ON,k}$ and $N_{OFF,k}$ are the number times the switch n is turned on and off during a period. $P_{ON,ki}$ and $P_{OFF,ki}$ are the power loss of the switch n during the ith instance that it is turned on or off, respectively. Then, considering the relationships expressed in (59) and (62), the total losses of the proposed MLIs are as follows:

$$P_{Loss} = P_{con} + P_{sw} \tag{63}$$

Therefore, the efficiency of proposed topology can be obtained as:

$$\eta_{MLI} = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{Loss}}{P_{in}} \tag{64}$$

Since the proposed topology requires a balancing circuit (two boost converters), its actual efficiency, considering the efficiency of the boost converter, can be obtained as follows:

$$\eta = \eta_{MLI} * \eta_{Boost} \tag{65}$$

By referring to [31], η_{Boost} can be computed as:

$$\eta_{Boost} = \frac{V_{Boost}}{2V_C} \tag{66}$$

where V_C is the capacitor voltage of the boost converter.

The power losses of the proposed 25-level MLI is calculated in PLECS software. The IGBT IKFW40N65ES5 is used for this study. The loss study simulation is run at 5[kW] output power. The input DC sources are considered as 100[V] and 500[V] to apply a maximum voltage of 500[V] to the modeled IGBTs with a resistance load of 25[Ω]. A phase-shift carrier-based PWM strategy with a switching frequency of 2[kHz] is applied to the proposed topology. Figs. 8(a) to 8(c) show the power losses and temperature of each switch separately. The initial temperature is 25[°C]. The maximum power loss is for switch T_2, which naturally has a higher temperature. Then, the switch (S_1, S_3) has experienced a greater power loss. It is worth noting that each switch (S_3, S_4) consists of two IGBTs, so each IGBT of S_3 has approximately half of the shown power loss value. The total

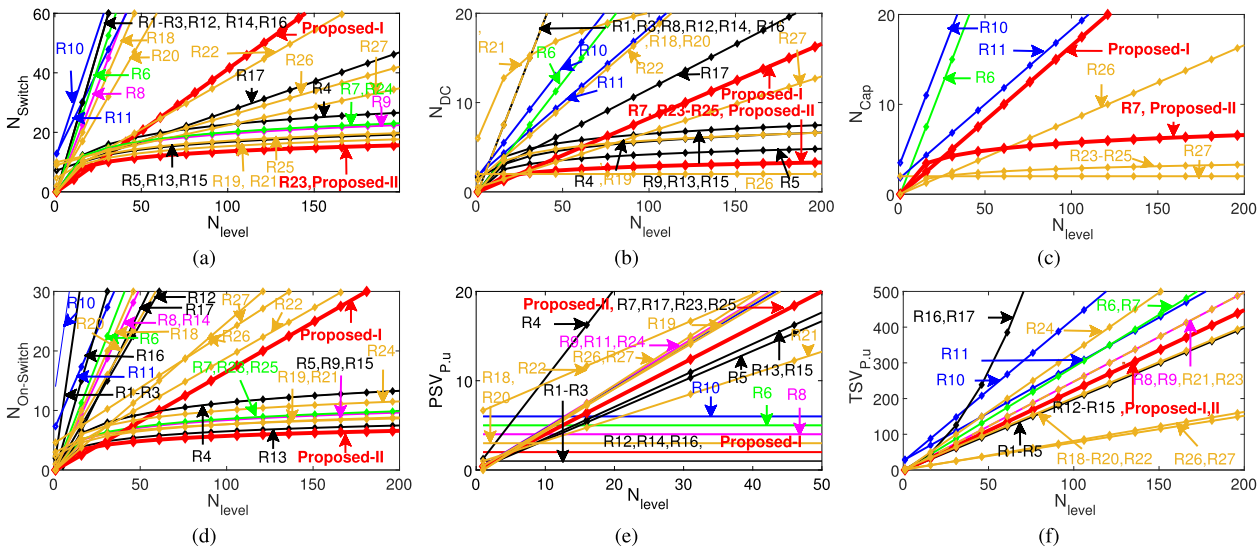


FIGURE 7. Comparison studies; (a) variation of N_{level} vs. N_{switch}; (b) variation of N_{level} vs. N_{DC}; (c) variation of N_{level} vs. N_{Cap}; (d) variation of N_{level} vs. $N_{On-Switch}$; (e) variation of N_{level} vs. $PSV_{P.u}$; (f) variation of N_{level} vs. $TSV_{P.u}$.

loss of the proposed 25-level inverter is 114[W], and it has an efficiency of 97.72% for 5[kW] output power, as shown in Fig. 8(d).

VIII. STANDALONE PV APPLICATION OF THE PROPOSED MULTILEVEL INVERTERS

One potential application of the proposed topologies is in standalone PV systems. In standalone PV systems, the critical challenge is to deliver high-quality power to the load using a highly efficient MLI [32]. The suggested topologies can enhance power quality by producing a large number of voltage levels that create a sin wave current waveform with low THD. In addition, they can increase efficiency since they use a smaller number of power semiconductor elements.

A. MODULATION TECHNIQUE

Pulse width modulation (PWM), fundamental frequency switching method, and staircase modulation are the most common modulation techniques used to commutate multilevel inverters. This article applies the staircase modulation approach to the proposed inverters [10]. The staircase modulation method utilizes a sinusoidal stepped waveform, as shown in Fig. 9. In this technique, the switching angles for $0 < \alpha j < \pi/2$ are computed by considering the total number of required levels (N_L) for the proposed inverters as:

$$\alpha_j = sin^{-1}(\frac{j-0.5}{N_L}) \quad for \quad j = 1, 2, \cdots, \frac{N_L - 1}{2} \tag{67}$$

Then, the switching angles generate the switching pulses of the proposed multilevel inverter; these pulses are determined individually based on the switching states in Table 2. The step timing is chosen based on the output frequency, and it is calculated offline.

B. STANDALONE PV APPLICATION

The control strategy for the proposed 25-level inverter in standalone PV systems is shown in Fig. 10. Two PV panels are used as DC-link voltage with two distinct powers, and high-power efficiency is achieved using two separate boost converters. The boost converters are single-input multi-output DC-DC converters, as reported in [31], and they are configured for the proposed inverter as detailed in Fig. 10.

The capacitors' voltages can be controlled by the duty cycles of two of the boost converters' switches (S_{b1}, S_{b2}). As a result, the magnitudes of the DC-link voltages (V_1, V_2) can be expressed in terms of PV panel voltages and duty cycles, as follows:

$$V_1 = \frac{V_{PV1}}{1 - D_1} \tag{68}$$

$$V_2 = \frac{V_{PV2}}{1 - D_2} \tag{69}$$

The DC-link voltage can be set to an appropriate magnitude by adjusting the power of the PV panels and the duty cycle of the boost converter switches. The Maximum Power Point (MPP) is derived by monitoring the voltage and current of the PV panels and using a proper MPPT algorithm. The duty cycles are then compared with the PWM signals to generate the switching pulses for the boost converters' switches.

The load voltage must be regulated by the proposed inverter to deliver power to the load at a constant nominal voltage. The capacitor voltages should therefore be adjusted to their reference values to maintain a constant voltage at the inverter's output. As a result, the capacitor voltages are balanced and set to their references using separate PI controllers. For the voltage drop on the filter and series impedance, an extra PI controller is coupled with the proposed voltage

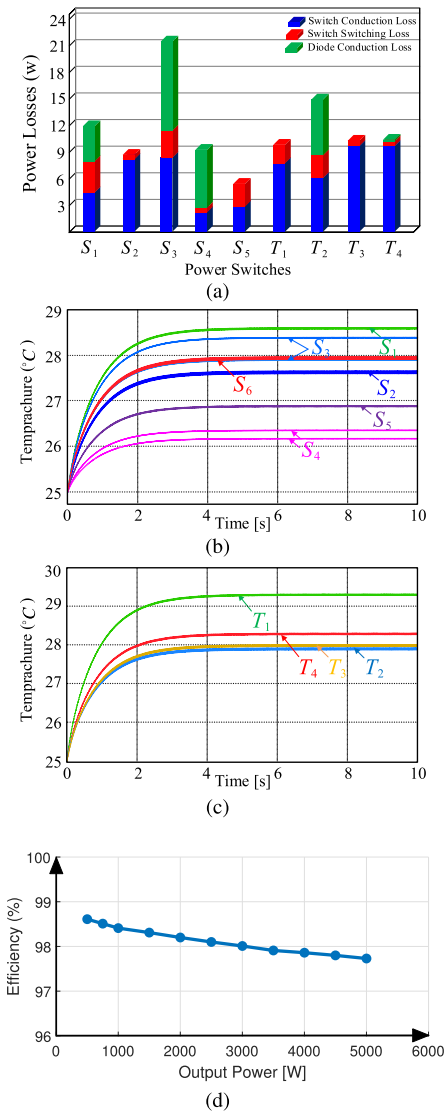


FIGURE 8. **Power loss study; (a) power loss of switches; (b) temperature of switches $S_1 - S_6$; (b) temperature of switches $T_1 - T_4$; (d) efficiency of the proposed topology.**

control system. The proper modulation index is obtained from the output of this PI controller, and the switching pulses of the proposed inverter are generated using the suggested FFM approach (see Fig. 9). The following well-known formula is used to compute the size of the inverter's capacitors:

$$C = \frac{I_{L,peak}}{\triangle V_C \times f_s} \tag{70}$$

The load peak current, the ripple voltage of the capacitor, and the switching frequency of the voltage of the system are represented as $I_{L,peak}$, $\triangle V_C$, and f_s, respectively.

IX. EXPERIMENTAL VALIDATION

In this section, to validate the performance of the proposal, the experimental results for the proposed 25-level topology are presented. The prototype of the proposed 25-level MLI is built using IGBTs as the switching devices. The

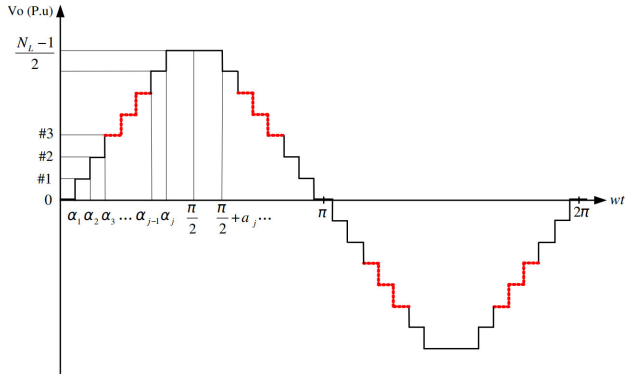


FIGURE 9. **Multilevel inverter output voltage waveform based on fundamental frequency modulation approach.**

experimental set-up diagram of the proposed 25-level MLI is shown in Fig. 11. The two circuits used to regulate the voltage of input capacitors of MLIs, such as the proposed topology, have been presented in [31]. Because the set-up of the proposed topology uses two regulated DC sources as the input DC-link, we implemented the circuit presented in [31]. The proposed control modulation technique (described in Section VIII) is applied to generate the switching pulses of the inverter. Table 6 lists the components used in the experimental set-up.

The field-programmable gate array (FPGA) is used in this study to generate pulses for the power switches. In Xiling software, the Verilog-language programs all the switching states of the proposed topology. Then, the switching states transfer to Basys 2 hardware. Eventually, the switching pulses are transferred to the gate driver circuits by optic-wires to fire the IGBTs of the proposed topology. To switch DC power supplies and create the 25-level output voltage for 90[Ω], 90[mH] AC load, FGH80N60FDTU IGBT power switches are used.

The DC voltage sources' input magnitudes are considered to be $V_1 = 20$[V] and $V_2 = 5V_1 = 100$[V]. Therefore, the proposed topology produces 25 voltage levels with a peak of 120[V] at the output. Fig. 10 illustrates the experimental results of the proposed 25-level MLI. The load voltage and current of the proposed topology for a pure resistance load of 90[Ω] are shown in Figs. 12(a) to 12(c). Figs. 12(d) and 12(e) show the load waveform and the input capacitor voltages, respectively, for a resistance inductive load of 90[Ω], 90[mH]. In the case of an R-L load, the output current possesses a sinusoidal waveform because of the existing inductive load. Also, the capacitor voltages of (C_1, C_2) are balanced at 10[V], and the capacitor voltages of (C_3, C_4) are balanced at 50[V]. The presented experimental results confirm that all 25 levels can be created with the proposed modulation technique and that the voltage of the capacitors are balanced by the proposed circuit. The THD percentage of the load voltage and load current in the case of an R-L Load are 3.85% and 0.8%, respectively.

Moreover, typical dynamic tests for MLIs connected to an R-L load consist of an unexpected load change, modulation

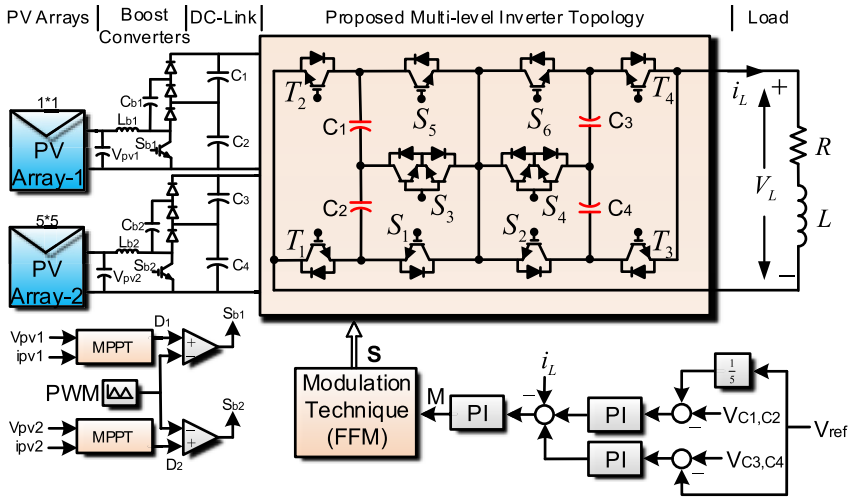


FIGURE 10. Control scheme of the proposed 25-level multilevel inverter in a standalone PV system.

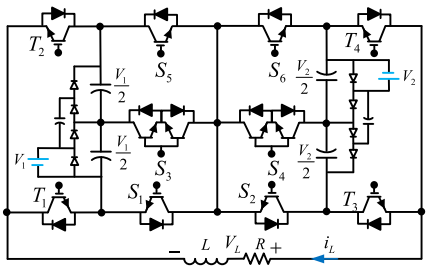


FIGURE 11. Experimental schematic set-up of proposed 25-level topology.

TABLE 6. Experimental parameters.

Parameters	Value	Unit
Regulated DC Sources	$V_1 = 20, V_2 = 100$	[V]
IGBT	FGH80N60FDTU, 600, 40	[V],[A]
Diode	RB088BM200FHTL 200,10	[V],[A]
FPGA Basys 2	Spartan 3E-100 CP132	-
Inverter output frequency (f_o)	50	[Hz]
Low voltage capacitors (C_1, C_2)	1200	[μF]
High voltage capacitors (C_3, C_4)	500	[μF]
Load (R,L)	90,90	[Ω],[mH]

index changes, and frequency changes (like those included in the simulation portion of this study). These tests are run to observe the performance of the proposed basic module. The results are shown in Figs. 12(d) to 12(f). Initially, the proposed topology delivers power to an R-L load with values of 90[Ω], 90[mH], and the values of the R-L load then suddenly switch to 60[Ω], 80[mH] in 5[ms]. Fig. 12(f) shows that the proposed 25-level MLI responds well to a sudden load change and that it can handle the load current without any change in the magnitude of the load or the phase voltage. Fig. 12(g) shows the capacitor voltages during a step change in the load. As can be seen, the capacitor voltages stay balanced in the input DC source magnitudes during this change.

The tests are then performed for the modulation and frequency changes. Fig. 12(h) shows the modulation index change, which decreased from unity to 0.7 at 5[ms]. As can be seen in this figure, the experimental results are like the simulation results in that the voltage levels decreased from 25 levels to 17 levels and the magnitude of the load current is reduced due to the decrease in the output voltage magnitude. Fig. 12(i) shows the response of the proposed 25-level MLI to a frequency change from 50[Hz] to 200[Hz]. This figure confirms that the proposed MLI can operate at a frequency of 200[Hz] without any variation in the shapes of the load voltage and current.

The stress voltage distribution of the power switches of the proposed topology in the maximum total blocking voltage is shown in Fig. 11(a). This chart shows that none of the power switches used withstand the peak output voltage, which is ($12\times V_{dc}$).

The experimental results of the standing voltage for all the used power switches of the proposed 25-level MLI are displayed in Figs. 13(b) to 13(d). Fig. 13(b) displays the standing voltage of the unidirectional power switches of part-a of the proposed basic module. These switches endure a low voltage magnitude of 20[V]. The standing voltage of the power switches of part-b is shown in Fig. 13(c). These switches endure a high voltage source magnitude of 100[V]. The standing voltage of the two bidirectional power switches, S_3 and S_4, is indicated in Fig. 13(d). The absolute voltage magnitude that these power switches support is 5[V] and 50[V].

The efficiency of the proposed 25-level multilevel inverter is obtained for different inverter loads. The output power is calculated by measuring the RMS value of the output voltage and current, and the input power is calculated by measuring the average value of the two DC source currents.

The efficiency from both the simulation and experimental results is depicted in Fig. 14. The lowest efficiency in both tests is for the low output power of 50[W]. On the other hand, the highest efficiency is for the 300[W] output power, which results in 97.53% in the simulation study and 96.48% in the experimental study.

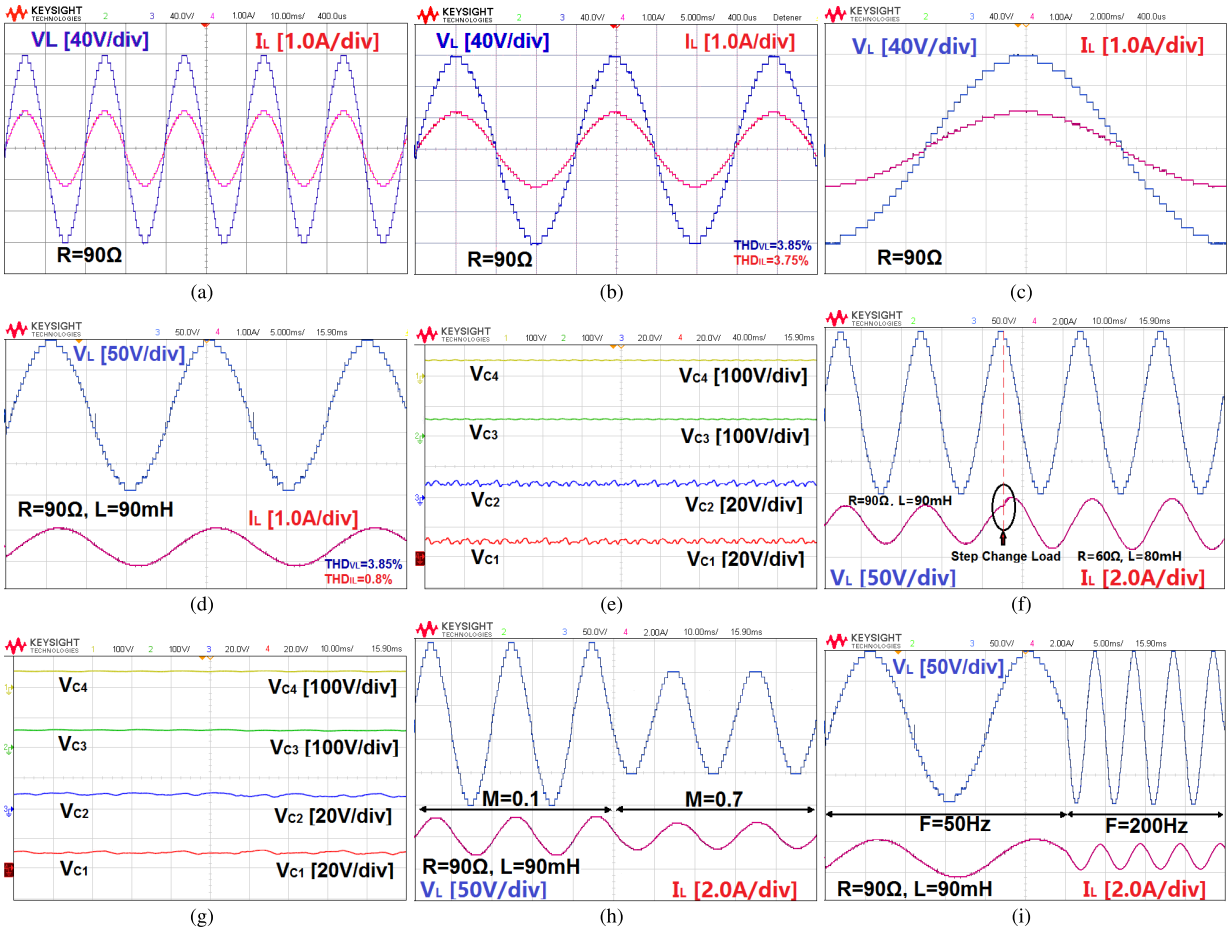


FIGURE 12. Experimental results of the proposed 25-level MLI; (a) the load voltage and load current waveform with an R-load; (b) a zoomed-in view of the load waveform in 5ms; (c) zoom of the load voltage and current waveform in 2ms; (d) the load voltage and load current waveform for an R-L load in 5[ms]; (e) the capacitor voltage waveform in R-L load for 40[ms]; (f) the response of MLI to a sudden load change; (g) the response of the MLI capacitor voltages to a sudden load change; (h) the MLI's response to a modulation index change; (i) the MLI's response to a frequency change.

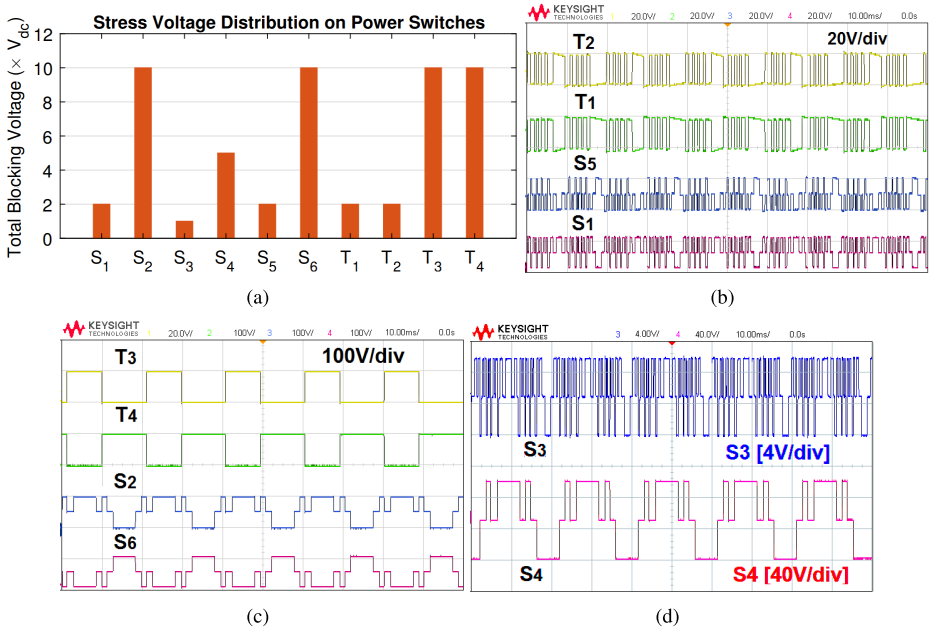


FIGURE 13. Experimental results of standing voltages on power switches; (a) voltage stress distribution on power switches; (b) standing voltage of power switches T_1, T_2, S_1, S_5; (c) standing voltages of power switches T_3, T_4, S_2, S_6; (d) standing voltage on the two bidirectional switches S_3, S_4.

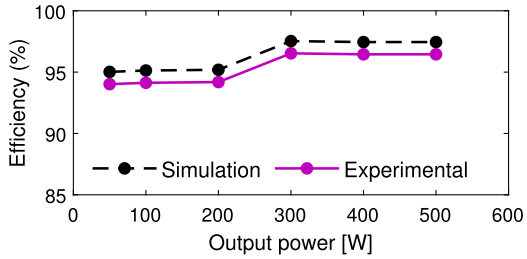


FIGURE 14. Simulation and experimental efficiency of the proposed 25-level multilevel inverter under varying output powers.

X. CONCLUSION

In this article, we have proposed a basic module for multilevel inverters with a reduced quantity of power electronics components for renewable energy source applications. The proposed basic module can produce 25 voltage levels by handling two unequal DC sources with ten power switches. To achieve a large number of voltage levels, the basic module was extended to two different methods, and their cascaded topologies were developed. Optimal topologies were defined based on different criteria to prove the flexibility and reliability of the proposed MLIs. We have obtained comprehensive results by comparing the proposal with other MLIs; these comparisons show that the proposed topologies required a small number of power electronics devices (switches, IGBTs, drivers, diodes) and isolated DC voltage sources. Furthermore, we have demonstrated that the proposed MLI topologies have a lower total standing voltage value than recently presented MLIs in both operation modes: symmetric and asymmetric DC sources. Finally, the experimental results were presented to verify the correct operation of the proposal.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[3] M. Ahmed, M. Orabi, S. S. M. Ghoneim, M. M. Al-Harthi, F. A. Salem, B. Alamri, and S. Mekhilef, "General mathematical solution for selective harmonic elimination," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4440–4456, Dec. 2020, doi: 10.1109/JESTPE.2019.2932933.

[4] C. M. N. Mukundan, K. Mithun, and P. Jayaprakash, "Modular five-level inverter with binary sources based DVR for power quality improvement," in *Proc. Int. Conf. Technol. Advancements Power Energy (TAP Energy)*, Kollam, Kerala, Dec. 2017, pp. 1–6.

[5] S. Du, B. Wu, and N. Zargari, "Delta-channel modular multilevel converter for a variable-speed motor drive application," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6131–6139, Aug. 2018.

[6] M. A. Hosseinzadeh, M. Sarbanzadeh, Y. Salgueiro, M. Rivera, and P. Wheeler, "Selective harmonic elimination in cascaded H-bridge multilevel inverter using genetic algorithm approach," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Melbourne, VIC, Australia, 2019, pp. 1527–1532.

[7] V. Jammala, S. Yellasiri, and A. K. Panda, "Development of a new hybrid multilevel inverter using modified carrier SPWM switching strategy," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8192–8197, Oct. 2018.

[8] S. Foti, S. De Caro, G. Scelba, T. Scimone, A. Testa, M. Cacciato, and G. Scarcella, "An optimal current control strategy for asymmetrical hybrid multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4425–4436, Sep./Oct. 2018.

[9] M. A. Hosseinzadeh, M. Sarbanzadeh, E. Sarbanzadeh, M. Rivera, E. Babaei, and J. Riveros, "New cascaded multilevel converters based on switched-diode six-level configuration," in *Proc. IEEE Southern Power Electron. Conf. (SPEC)*, Puerto Varas, Chile, Dec. 2017, pp. 1–6.

[10] M. A. Hosseinzadeh, M. Sarebanzadeh, M. Rivera, E. Babaei, and P. Wheeler, "A reduced single-phase switched-diode cascaded multilevel inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3556–3569, Jun. 2021, doi: 10.1109/JESTPE.2020.3010793.

[11] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, Sep. 2014.

[12] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. M. Kojabadi, and F. Blaabjerg, "A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6738–6754, Aug. 2018.

[13] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[14] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019.

[15] E. Babaei, M. Farhadi, and M. A. Hosseinzadeh, "Asymmetrical multilevel converter topology with reduced number of components," *IET Power Electron.*, vol. 6, no. 6, pp. 1188–1196, Jan. 2013.

[16] M. Sarbanzadeh, E. Babaei, M. A. Hosseinzadeh, and C. Cecati, "A new sub-multilevel inverter with reduced number of components," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016, pp. 3166–3171.

[17] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A square T-type (ST-type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.

[18] E. Samadaei, M. Kaviani, and K. Bertilsson, "A 13-levels module (K-type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019.

[19] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimization assessment of a new extended multilevel converter topology," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4530–4538, Jun. 2017.

[20] J. S. M. Ali, R. S. Alishah, and V. Krishnasamy, "A new generalized multilevel converter topology with reduced voltage on switches, power losses, and components," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1094–1106, Jun. 2019.

[21] J. S. M. Ali, R. S. Alishah, and N. Sandeep, "A new generalized multilevel converter topology based on cascaded connection of basic units," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2498–2512, Dec. 2019.

[22] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019.

[23] A. Taheri, A. Rasulkhani, and H. Ren, "An asymmetric switched capacitor multilevel inverter with component reduction," *IEEE Access*, vol. 7, pp. 127166–127176, 2019.

[24] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019.

[25] M. D. Siddique, A. Iqbal, M. A. Memon, and S. Mekhilef, "A new configurable topology for multilevel inverter with reduced switching components," *IEEE Access*, vol. 8, pp. 188726–188741, 2020.

[26] M. D. Siddique, S. Mekhilef, M. Rawa, A. Wahyudie, B. Chokaev, and I. Salamov, "Extended multilevel inverter topology with reduced switch count and voltage stress," *IEEE Access*, vol. 8, pp. 201835–201846, 2020.

[27] S. P. Gautam, "Novel H-bridge-based topology of multilevel inverter with reduced number of devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2323–2332, Dec. 2019.

[28] S. Ramaiah, N. Lakshminarasamma, and M. K. Mishra, "Multisource switched capacitor based boost multilevel inverter for photovoltaic-based systems," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2558–2570, Mar. 2020.

[29] N. Mishra, S. K. Yadav, B. Singh, S. Padmanaban, and F. Blaabjerg, "Binary-quintuple progression based 12-switch 25-level converter with nearest level modulation technique for grid-tied and standalone applications," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3214–3223, May 2021.

[30] P. R. Bana, K. P. Panda, S. Padmanaban, and G. Panda, "Extendable switched-capacitor multilevel inverter with reduced number of components and self-balancing capacitors," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3154–3163, May 2021.
[31] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A DC-DC multilevel boost converter," *IET Power Electron.*, vol. 3, no. 1, pp. 129–137, Jan. 2010.
[32] S.-C. Wang, H.-Y. Pai, G.-J. Chen, and Y.-H. Liu, "A fast and efficient maximum power tracking combining simplified state estimation with adaptive perturb and observe," *IEEE Access*, vol. 8, pp. 155319–155328, 2020.

MARYAM SAREBANZADEH (Member, IEEE) was born in Ahvaz, Iran. She received the B.Sc. and M.Sc. degrees in electrical engineering-electronics and electrical engineering-power from the Islamic Azad University Science and Research Branch, Tabriz, Iran, in 2012 and 2014, respectively. She is currently pursuing the Ph.D. degree in power electronics with the Universidad de Talca, Talca, Chile.

She received a scholarship from the Chilean National Research, Science and Technology Committee, in 2018. She is the author or coauthor of more than 30 published technical articles and has a patent in the area of power electronics inverters. Her research interests include design, modeling, and control of transformerless multilevel inverters in photovoltaic applications.

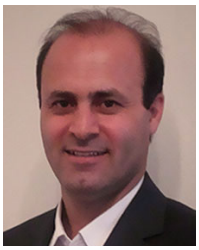
Ms. Sarebanzadeh received the IEEE Paper Assistance Award at the International Conference on Industrial Technology (ICIT), in 2019.

MOHAMMAD ALI HOSSEINZADEH (Member, IEEE) was born in Gonbad Kavus, Iran. He received the B.Sc. and M.Sc. degrees (Hons.) in electrical engineering-power from the Islamic Azad University Science and Research Branch, Tabriz, Iran, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree in power electronics with the Universidad de Talca, Talca, Chile.

He received a scholarship from the Chilean National Research, Science and Technology Committee, in 2018. He is the author or coauthor of more than 30 published technical articles. He also holds a patent in the area of power electronics converters. His research interests include design, modeling, and control of multilevel power converters and their applications as well as advanced model predictive control of power electronic systems in e-mobility applications.

Mr. Hosseinzadeh received the Best Thesis Award from the Islamic Azad University of Tabriz, in 2012, as well as the IEEE Paper Assistance Awards at the IEEE Southern Power Electronics Conference (SPEC) and the IEEE International Conference on Industrial Technology (ICIT), in 2017 and 2019, respectively.

CRISTIAN GARCIA (Member, IEEE) received the M.Sc. and Ph.D. degrees in electronics engineering from the Universidad Tecnica Federico Santa Maria (UTFSM), Valparaiso, Chile, in 2013 and 2017, respectively. He was a Visiting Ph.D. Student with the Power Electronics Machines and Control (PEMC) Group, University of Nottingham, U.K., in 2016. From 2017 to 2019, he was an Assistant Professor with the Engineering Faculty, Universidad Andres Bello, Santiago, Chile. Since 2019, he has been with the Department of Electrical Engineering, University of Talca, Curico, Chile, where he is currently an Assistant Professor. His research interests include electric transportation applications, variable-speed drives, and model predictive control of power converters and drives.



EBRAHIM BABAEI (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Tabriz, in 2007. He is the author or coauthor of one book and more than 550 journal articles and conference papers. He also holds 25 patents in the area of power electronics. His research interests include the analysis, modeling, design, and control of power electronics converters and their applications, renewable energy sources, and FACTS devices. He has been the technical program chair, track chair, organizer of different special sessions, and technical program committee member in the most important international conferences organized in the field of power electronics. Several times, he was a recipient of the Best Researcher Award from the University of Tabriz. He also received the 2016 Outstanding Reviewer Award from IEEE Transactions on Power Electronics. Since 2013, he has been the Editor-in-Chief of the *Journal of Electrical Engineering* of the University of Tabriz. He is currently an Associate Editor of the IEEE Transactions on Industrial Electronics, IEEE Transactions on Power Electronics, *Open Journal of the Industrial Electronics Society*, and the *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*. He has earned inclusion on the list of the Top One Percent of the World's Scientists and Academics according to Thomson Reuters' list, since 2015.

SYED ISLAM (Fellow, IEEE) is currently the Dean of the School of Science Engineering and Information Technology, Federation University Australia, Australia. He received the Dean's medallion for research at Curtin University, in 1999. He has been a Visiting Professor with the Shanghai University of Electrical Power, China. He has published more than 300 technical articles in his area of expertise. His research interests include the IoT, condition monitoring of transformers, wind energy conversion, and smart power systems. He is a fellow of the Engineers Australia, a fellow of the IET, and a Chartered Engineer in the U.K.

JOSE RODRIGUEZ (Life Fellow, IEEE) received the Engineering degree in electrical engineering from the Universidad Tecnica Federico Santa Maria, Valparaiso, Chile, in 1977, and the Dr.-Ing. degree in electrical engineering from the University of Erlangen, Erlangen, Germany, in 1985. Since 1977, he has been with the Department of Electronics Engineering, Universidad Tecnica Federico Santa Maria, where he was a Full Professor and the President. Since 2015, he has been the President of the Universidad Andres Bello in Santiago, Chile, where he has also been a Full Professor, since 2019. He has coauthored two books, several book chapters, and more than 400 journal articles and conference papers. His research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives. He is a member of the Chilean Academy of Engineering. He has received a number of best paper awards from various IEEE journals. He was a recipient of the National Award of Applied Sciences and Technology from the Government of Chile, in 2014, and the Eugene Mittelmann Award from the IEEE Industrial Electronics Society, in 2015. From 2014 to 2019, he was included in the list of Highly Cited Researchers published by Web of Science.