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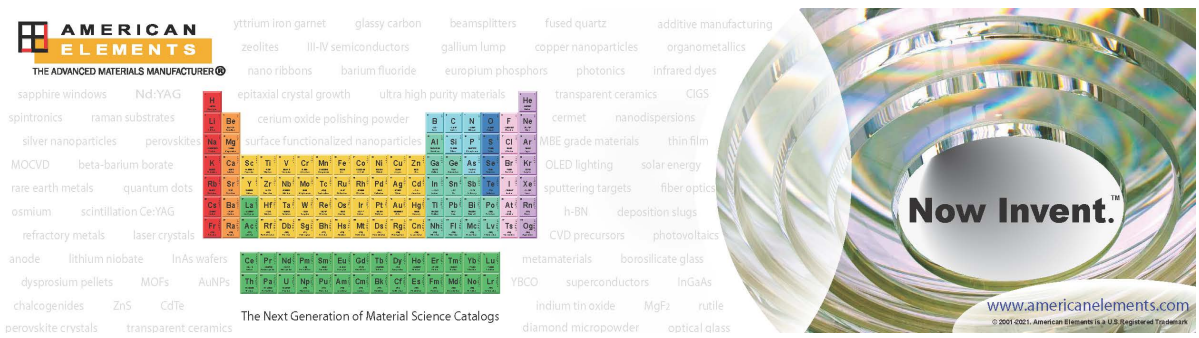

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ABSTRACT

Here, we investigate the effect of post-metallization anneal temperature on Ti/Au ohmic contact performance for (100)-oriented Ga_2O_3. A low contact resistance of ~2.49×10^{-5} Ω·cm^2 is achieved at an optimal anneal temperature of ~420 °C for (100) Ga_2O_3. This is lower than the widely-used temperature of 470 °C for (010)-oriented Ga_2O_3. However, drastic degradation of the (100)-oriented contact resistance to ~1.36×10^{-3} Ω·cm^2 is observed when the anneal temperature was increased to 520 °C. Microscopy at the degraded ohmic contact revealed that the reacted Ti–TiO_x interfacial layer has greatly expanded to 25–30 nm thickness and $GaAu_2$ inclusions have formed between (310)-Ga_2O_3 planes and the Ti–TiO_x layer. This degraded interface, which corresponds to the deterioration of ohmic contact properties, likely results from excess in-diffusion of Au and out-diffusion of Ga, concurrent with the expansion of the Ti–TiO_x layer. These results demonstrate the critical influence of Ga_2O_3 anisotropy on the optimal post-metallization anneal temperature. Moreover, the observed Ti/Au contact degradation occurs for relatively moderate anneal conditions (520 °C for 1 min in N_2), pointing to the urgent necessity of developing alternative metallization schemes for gallium oxide, including the use of Au-free electrodes.

INTRODUCTION

Possessing an ultra-wide bandgap nature of around 4.8 eV, beta-phase gallium oxide (β-Ga_2O_3) has attracted worldwide attention and research interest in the past decade owing to its excellent material properties. Ease of *n*-type doping over a wide-range (10^{16}–10^{19} cm^{-3}) by extrinsic group IV elements, such as Si, Sn, and Ge, makes the material an ideal candidate for next-generation power electronics.[1] Moreover, low-cost bulk substrate preparations have been realized using conventional melt-based methods (e.g., Czochralski growth and edge-fed growth), providing the advantage of inexpensive, readily available substrates.[2–4] In addition, high-quality homoepitaxy has been demonstrated with low impurity concentrations, low defect density, and excellent carrier mobility using metalorganicvapor-phase-epitaxy (MOVPE) methods,[5–9] enabling the realization of high-performance devices. Recently, the breakdown strength of a MOSFET based on Ga_2O_3 substrates has demonstrated performance that has surpassed the theoretical limit of GaN and SiC.[10]

Although exciting preliminary Ga_2O_3 device results have been reported, the Ga_2O_3 field is still at an early stage, with many fundamental material properties not yet fully explored. One key issue for technology development is the choice of substrate orientation. To date, three low-index crystalline planes have been primarily used for device epi-layers: (010), (001), and (100). Devices fabricated on (010) substrates are the most widely reported due to the relative ease of epi-film growth on this orientation.[1,11–13] (100)-oriented Ga_2O_3, on the other hand, aligns with the preferential cleavage plane, offering the potential for high-quality surface preparation,[13,14] which is of critical importance for device fabrication. Moreover,

based on surface energy calculations, the (100)-B plane has the lowest surface energy among the major Ga_2O_3 orientations,[14,15] indicating its structural stability and reduced tendency for surface reconstruction.[16] Recent advances in epitaxial growth on (100)-oriented Ga_2O_3 have enhanced the community's ability to grow high quality films.[7,14,17] In terms of device performance, Lee *et al.*[18] recently reported that, due to the anisotropic nature of gallium oxide, (100)-oriented substrates have dramatically reduced ohmic contact resistance compared to (010) substrates. Similarly, Lyle *et al.*[19] recently reported that Schottky barriers on (100) substrates demonstrate a strong correlation with metal work function. Thus, unlike contacts to (010) and (−201) substrates,[20–22] (100) Ga_2O_3 metal–semiconductor junctions can be tuned in predictable ways. These studies together suggest that the (100) crystalline orientation is a promising platform for Ga_2O_3 devices.

For gallium oxide's major application space–high-performance power devices–one of the key requirements is a fabrication process technology for low resistance ohmic contacts. In order to achieve high current density and low conduction loss, parasitic resistance from the ohmic electrodes must be suppressed. Various approaches to engineer the metal–semiconductor (M–S) junction have been used to realize ohmic contacts on gallium oxide, including heavily doping the semiconductor layer,[23,24] reactive-ion-etching the pre-metallization surface,[25] and use of a post-metallization anneal.[26,27] Among these, post-metallization rapid-thermal-annealing (RTA) has been shown to be a key step to achieve linear I–V characteristics.[1,26] Higashiwaki *et al.* reported that by using 470 °C 1-min RTA in N_2, ohmic conduction could be obtained at (010) Ga_2O_3/Ti–Au junctions.[27] Yao *et al.*[28] demonstrated that, on (−201) substrate, annealing Ti/Au metallization at 400 °C RTA in an Ar atmosphere gives the best I–V characteristics. Lee *et al.*[18] recently reported a low-resistance ohmic contact, with specific contact resistance, ρ_c, of 5.11×10^{-5} Ω·cm^2, achieved on (100) Ga_2O_3/Ti–Au using 470 °C RTA. Given the recent findings on orientation-dependence of many gallium oxide properties,[21,22,29,30] and the fact that research on ohmic contacts to (100) Ga_2O_3 substrates is rare[1] compared to that on other crystalline orientations, we here set out to determine the optimal window for post-metallization anneal of Ti/Au ohmic contacts to (100)-oriented Ga_2O_3. In addition, we note that the thermal budget limit for ohmic electrodes on any orientation has not yet been robustly established. Therefore, in this study, we aim to bridge these knowledge gaps by studying the effect of post-metallization RTA temperature on (100)-oriented Ga_2O_3 ohmic contacts and investigating the interfacial microstructure that occurs in conjunction with electrical performance degradation when the anneal temperature is increased above its optimal value.

By varying the RTA temperature, we found that the optimum condition for (100) Ga_2O_3 is slightly lower (~50 °C) than that on (010) Ga_2O_3. In addition, a drastic degradation in contact performance was observed after annealing at 520 °C, which suggests that the Ti/Au bilayer stack is not a stable ohmic contact, at least for (100) Ga_2O_3. To examine the cause of this degradation, we characterized the materials' interface by scanning/transmission electron microscopy (S/TEM). Substantial changes at the interface were observed in the degraded contacts: the Ti–TiO_x layer expands from ~2 nm when annealed at 470 °C [18] to ~25–30 nm thickness, with $GaAu_2$ inclusions precipitated at the boundary of Ga_2O_3/Ti–TiO_x. Moreover, the $GaAu_2$ is found to be formed preferentially on the (310) plane of Ga_2O_3, suggesting anisotropy in the reaction kinetics. The expanded Ti–TiO_x layer and the formation of $GaAu_2$ likely contributed to the deterioration of the contact electrical behavior. By correlating microscopy findings with electrical performance, this study provides valuable insights into the metallization design and thermal budget process required to enable next generation power devices.

EXPERIMENTAL SECTION

Substrates and epitaxial layers: (100)-oriented substrates were prepared from bulk β-Ga_2O_3 single crystals grown by the Czochralski method at the Leibniz-Institut für Kristallzüchtung.[2,31–35] The 2-inch diameter and 3-inch long bulk crystals were grown in a 20 vol. % oxygen environment using a 100 mm diameter iridium crucible, as described by Galazka *et al.*[31,33–35] To obtain crystals that are electrically insulating, 0.2 mol. % MgO was added to the Ga_2O_3 powder (5 N). The crystals were grown along the ⟨010⟩ crystallographic direction, and were found to be twin-free and crack-free with a rocking curve full width at half maximum less than 30 arcsec. Substrates for homoepitaxial growth by MOVPE were prepared in dimensions of $5 \times 5 \times 0.5$ mm^3 by cutting and chemical-mechanical polishing with an off-oriented (100) plane defined by a miscut of 4° toward [00$\bar{1}$] direction to avoid twin boundary formation and to enhance the film electrical properties, as discussed by Schewski *et al.*[14,36] and Fiedler *et al.*[37] To remove the top damaged layer from the polishing and prepare an epi-ready stepped surface, the substrates were wet etched for 15-min in a 140 °C phosphoric acid bath, subsequently annealed in O_2 at 900 °C for 1 hour.

Before loading into the MOVPE chamber, the substrates were soaked in hydrofluoric acid (5%) for 5 min and then rinsed with deionized water to reduce possible Si contaminants on the substrate surface.[38] An epitaxial layer was grown as shown in Fig. 1. The epi-growth experimental parameters follow previous reports.[7,39] The MOVPE system (Structured Materials Industries, Inc.-USA) used in this work for deposition of n-type β-Ga_2O_3 thin films consists of a vertical shower-head low-pressure reactor equipped with a rotating susceptor. The metal–organic precursors used were triethylgallium (TEGa) and tetraethylorthosilicate (TEOS). O_2 (5 N) was used as the oxidant, and high purity Ar (5 N) served as the carrier gas. A Laytec EpiNet optical head *in situ* process monitoring system was used to control the layer thickness. Atomic force microscopy (AFM) (Bruker Dimension Icon) was used to investigate the surface morphology of the epitaxial films. Room temperature Hall effect measurements were made using van der Pauw structures with InGa eutectic ohmic contacts to confirm the net doping concentration in each substrate. For these experiments, two substrates were used, having $N_D - N_A$ of 2.6×10^{18} and 2.8×10^{18} cm^{-3}.

Device fabrication

After epitaxial growth and dicing, all samples used in this study underwent a sequential solvent cleaning process with acetone, isopropyl alcohol, and methanol. Next, circular-transmission-line-method (CTLM) device structures were defined with conventional lithography followed by metal deposition with e-beam evaporated

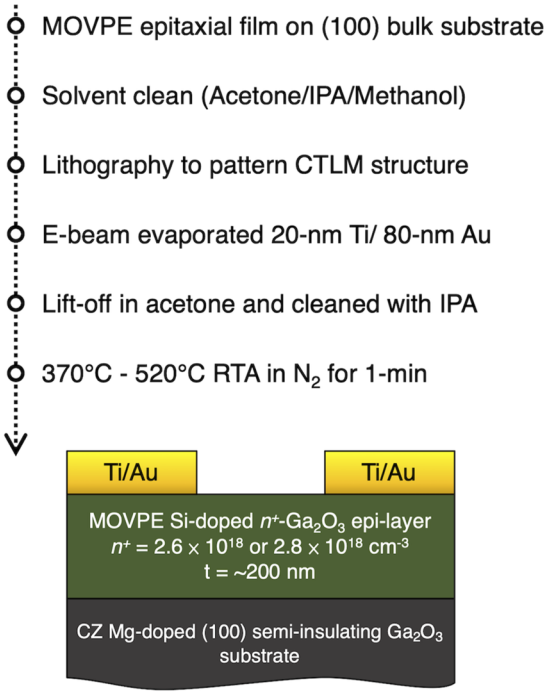

FIG. 1. Device fabrication process flow and schematic illustration of cross-sectional structure. All process parameters other than the temperature of the post-metallization RTA are kept the same for all samples.

20 nm Ti/80 nm Au and a lift-off process. To examine the effect of post-metallization anneal temperature, a 1-min RTA in N_2 environment was performed at temperatures ranging from 370 to 520 °C. Samples annealed at 370 or 420 °C are from the substrate with $N_D - N_A = 2.6 \times 10^{18}$, while those annealed at 470 or 520 °C are from the substrate with $N_D - N_A = 2.8 \times 10^{18}$. A schematic illustration of the fabrication steps and resulting cross-sectional structure is given in Fig. 1.

Electrical characterization

I–V characteristics of the fabricated CTLM devices were collected using a four-probe Kelvin configuration with a Keysight B1505A power device analyzer and Cascade MicroTech Tesla probe station. The applied voltage was swept from −200 to +200 mV with a 4 mV step while measuring the current in dark. As there is no noticeable hysteresis in double sweeps, all the electrical measurements shown here were taken using single (forward) sweeps. Three sets of CTLM structures were measured for each sample, and the average resistance value for each electrode spacing was used to extract the contact resistance.

TEM sample preparation and characterization

Conventional focused ion beam (FIB)-assisted lift-out was conducted to prepare [001]-oriented TEM lamella from the β-Ga_2O_3 substrate using a TFS Helios 650 Nanolab system. Carbon and platinum bilayer capping was deposited *in situ* to protect the device's top surface from FIB damage. To minimize lateral damage to the TEM specimen, the final milling processes were performed at 2 kV. The final thickness of the TEM specimens is estimated to be below 50 nm, based on our previous sample preparation results. Cross-sectional microscopy images were collected using a TFS Talos F200X G2 transmission electron microscope operating at 200 keV. The convergent and collective angles for STEM high-angle annular angle dark field (HAADF) imaging condition were 5 and 59–200 mrad, respectively. STEM energy-dispersive x-ray spectroscopy (EDX) elemental mappings were measured with four Super-X windowless detectors. TEM images and selective area electron diffraction (SAED) patterns were collected with a Gatan OneView camera.

RESULTS AND DISCUSSIONS

A schematic illustration of the fabrication steps and cross-sectional structure is shown in Fig. 1. The sample fabrication starts from the (100)-oriented Ga_2O_3 bulk sample preparation, MOVPE film growth, device fabrication (solvent clean, lithography, Ti/Au metallization and lift-off), to post-metallization anneal. To systematically investigate the effect of post-metallization anneal temperature on contact properties, all process parameters are kept the same while only varying the post-metallization RTA temperature. The net doping of all the samples was kept as similar as possible (i.e., 2.6×10^{18} and 2.8×10^{18} cm^{-3}) to minimize doping concentration effects on electron transport.

The *I–V* characteristics of samples annealed at 370, 420, 470, and 520 °C, as well as for an unannealed ("as-deposited") sample are shown in Fig. 2(a). All the samples that were treated with a post-metallization anneal exhibited linear *I–V* characteristics with higher current at the same applied voltage, compared to the unannealed sample: ohmic contacts were realized on all RTA-treated samples. To assess contact performance, the measured resistance vs electrode spacing of CTLM structures is plotted in Fig. 2(b). Based on theory,[40] the total measured resistance can be expressed as

$$R_T = \frac{R_{sh}}{2\pi r_i}\left(d + 2\sqrt{\rho_c / R_{sh}}\right)C,$$

where R_{sh} is the sheet resistance of the semiconductor, d is the electrode spacing ranging from 5 μm to 35 μm, r_i is the inner radius (here 200 μm) of the structures, and ρ_c is the specific contact resistivity, typically given in units of $\Omega{\cdot}cm^2$. C is a unitless geometrical correction factor given by $C = r_i/dln(1 + d/r_i)$. For simplicity, the plotted resistance (y-axis) in Fig. 2(b) corresponds to the measured total resistance divided by the correction factor, calculated individually for each value of d, i.e., $R_T(d)/C(d)$. The extracted contact resistance and sheet resistance are listed in Table I along with Hall measurement data. Figure 2(c) shows the specific contact resistance vs RTA temperature for the samples used in this study. For (100) Ga_2O_3/Ti–Au junctions, the lowest value of ρ_c (i.e., the best contact resistance) of 2.49×10^{-5} $\Omega{\cdot}cm^2$ occurs after 420 °C RTA. When annealed at a lower temperature (370 °C), the contact resistance is observed to increase. This increase is likely associated with incomplete interfacial reactions. As we increase the annealing temperature from 420 to 470 (470 °C is the most widely-used RTA temperature for (010) orientation[27]), the ρ_c

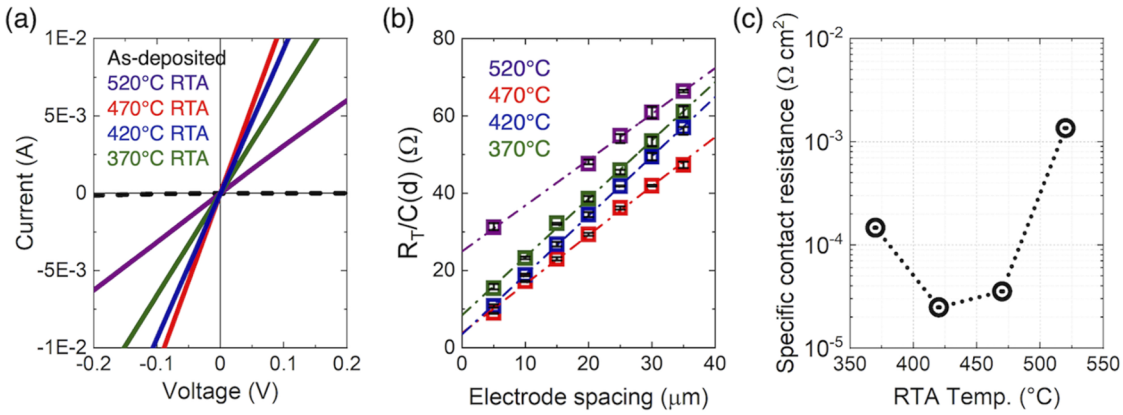

FIG. 2. (a) *I–V* characteristics of CTLM structures (with electrode spacing, *d*, of 5 μm) for samples with four different post-metallization anneal conditions. The *I–V* characteristic of the as-deposited condition is included to indicate the improvement of contact resistance with RTA. (b) CTLM plot of $R_T/C(d)$ vs electrode spacing. Dash-dotted lines are linear regression fit lines, where $R^2 > 0.996$. Each square symbol represents the average measured resistance of three structures with the same electrode spacing. The error bars show the range of the three measured resistances. (c) Specific contact resistance vs anneal temperature. The optimum RTA temperature for (100) Ga_2O_3 is around 420 °C. Drastic degradation of contact resistance is observed after a 520 °C anneal.

value increases by ~40%. Upon increasing the RTA temperature from 470 to 520 °C, the contact resistance drastically increases (+4000%) to 1.36×10^{-3} $\Omega \cdot cm^2$. These trends suggest that the optimal RTA temperature for (100)-oriented Ga_2O_3 is near 420 °C, slightly lower than the widely accepted value of 470 °C used for (010)-direction contacts.[1,26] Moreover, a considerable surge in the contact resistance is observed when the RTA temperature reached 520 °C, which indicates a possible degradation of the M–S contact interface.

Previously, we reported the observation of a relatively thin (~2–2.5 nm) *in situ* formed Ti–TiO_x layer on the (100) Ga_2O_3 after 470 °C RTA and the contact's excellent electrical performance was attributed to the thinness and flatness of this layer.[18] To investigate the degradation of ohmic properties observed following 520 °C RTA, cross-sectional S/TEM characterization was performed on the 520 °C-RTA sample. In the HAADF STEM images [Figs. 3(a) and 3(b)] and EDX elemental mapping [Figs. 3(c)–3(f)], a dark-contrast layer is observed at the interface, indicating an expanded Ti–TiO_x layer of 25–30 nm thickness. The bright contrast regions within the Ti–TiO_x layer and between Ga_2O_3 nano-facets, observed in HAADF [Figs. 3(a) and 3(b)], correspond to Au-rich regions in the EDX map [Fig. 3(f)]. This suggests the presence of Au-rich inclusions with non-zero Ga intensity [Fig. 3(c)]. An elemental mapping at higher magnification of the Au-rich inclusion can be found in Fig. S1. Here, it is observed that the Au-rich inclusions that occur at the boundary with the Ga_2O_3 substrate are preferentially aligned ~52 degrees off of the [010] Ga_2O_3 crystal direction. In addition, Ti-rich crystals are observed in the metallization layer. These Ti-rich crystals have a morphology similar to those previously reported for annealed Ti/Au–Ga_2O_3,[18,26,41,42] regardless of the crystalline orientation.

To further examine the nature of the Au-rich inclusions and the structure at the interface, Fig. 4 shows microscopy images at the boundary between the Ga_2O_3 substrate and Au-rich inclusions. In agreement with Fig. S1, in Fig. 4(a), the Au-rich inclusions appear to be formed with a preferential angle (~52.5 degrees off [010]) to the Ga_2O_3 substrate. This angle matches the (310) crystalline plane,

TABLE I. Summary of the electrical properties of samples with different post-metallization anneal temperatures.

Hall			CTLM				
N_D–N_A (cm^{-3})	μ ($cm^2V^{-1}s^{-1}$)	R_{sh} (Ω/sq)	RTA Temp. (°C)	Ohmic?	ρ_c ($\Omega \cdot cm^2$)	R_c ($\Omega \cdot mm$)	R_{sh} (Ω/sq)
			...	No	...	...	...
2.6×10^{18}	65	1850	370	Yes	1.47×10^{-4}	5.28	1900
			420	Yes	2.49×10^{-5}	2.19	1930
			...	No	...	...	...
2.8×10^{18}	69	1610	470	Yes	3.55×10^{-5}	2.38	1590
			520	Yes	1.36×10^{-3}	14.57	1570

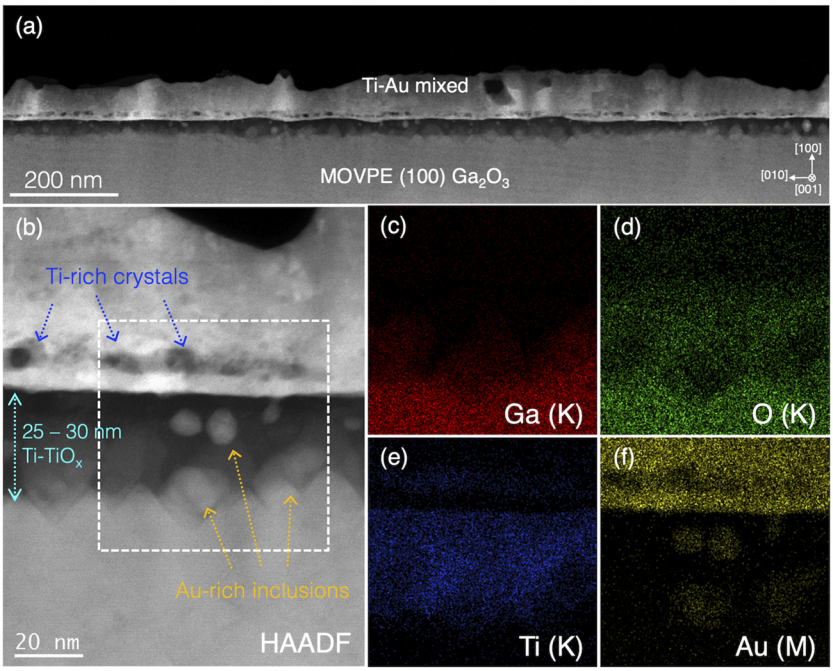

FIG. 3. (a) Cross-sectional STEM HAADF image of 520 °C annealed (100) Ga_2O_3/Ti–Au ohmic contact. (b) A higher-magnification STEM HAADF image of the interfacial region, where the Ti–TiO_x layer formed *in situ* is 25–30 nm thick and contains bright contrast regions. (c)-(f) EDX spectrum mappings of gallium, oxygen, titanium, and gold from the dashed-box in (b). The dark contrast layer in (b) corresponds to the Ti-rich layer, and the bright contrast regions within it correspond to Au-rich inclusions.

suggesting that this direction could be a potential seeding plane for the formation of secondary phases. Figure 4(b) shows a TEM image at the boundary between the Ga_2O_3 substrate and Au-rich inclusions. Lattice fringes can be observed. By comparing the measured interplanar spacing (*d*-spacing) of the Au-rich inclusion and spacings of various compounds, good agreement was found with the d_{002} of orthorhombic-$GaAu_2$. A table of interplanar spacings of possible compounds can be found in Table S1. Since no other possible compounds possess a *d*-spacing value close to the measured value of 0.348 nm, the identity of the Au-rich compounds is most likely to be orthorhombic-$GaAu_2$.

Compared with the sample annealed at 470 °C,[18] the Ti–TiO_x layer formed *in situ* appears to expand from 2–2.5 to 25–30 nm when the RTA temperature increases slightly to 520 °C, due at least in part to the addition of $GaAu_2$ inclusions within the Ti–TiO_x layer. The change in the Ti–TiO_x layer suggests that the interfacial reactions between (100) Ga_2O_3/Ti–Au are strongly modulated by thermal energy. Although a good ohmic contact can be formed with RTA

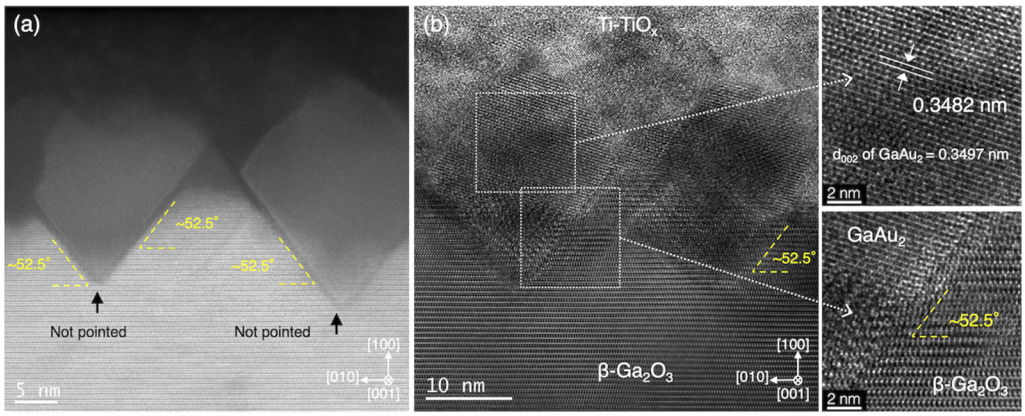

FIG. 4. (a) Cross-sectional STEM HAADF image of the interface between (100) Ga_2O_3/Ti–TiO_x, including Au-rich inclusions/secondary phases. The second phases form with a preferential angle to the substrate of ~52.5 degrees off [010], i.e., along the (310) plane of Ga_2O_3. The tip region of the second phase does not form a sharply pointed end. (b) Cross-sectional TEM bright-field image of the interface between (100) Ga_2O_3/Ti–TiO_x, including Au-rich secondary phases. Two zoomed-in insets indicate the secondary phase region and the substrate/secondary phase boundary. Based on the analysis of planar spacing, the secondary phase appears to be orthorhombic-$GaAu_2$.

at 400–500 °C and shows decent reliability,[18,41] for extremely high-temperature operation condition (>500 °C) or post-metallization device processing above 500 °C, the stability of the ohmic contacts could be a potential concern for device failure.

The higher post-metallization temperature also likely triggers and accelerates the formation of Au-rich inclusions (i.e., $GaAu_2$) within the Ti–TiO_x layer. The formation of $GaAu_2$ is likely the result of rapid Au in-diffusion and Ga out-diffusion, which may facilitate the expansion of the reacted interface. Similar formation of a Au–Ga solid solution and compounds ($GaAu_2$ and Ga_7Au_2) was observed within the *p*-GaN/Ni–Au ohmic contacts for anneals at or above 450 °C.[43,44] This suggests that gallium and gold tend to react aggressively in this temperature range, leaving the nearby substrate region with a high concentration of Ga vacancies. In the *p*-GaN system, this phenomenon may be beneficial for ohmic contact formation since cation vacancies act as acceptors. However, in *n*-Ga_2O_3, since V_{Ga} and its complexes are compensating deep acceptors, this process may adversely affect contact performance.[45,46] Thus, the degraded electrical properties of the sample annealed at 520 °C are likely the result of the expanded Ti–TiO_x layer, the formation of $GaAu_2$ inclusions, and the creation of excess gallium vacancies in the substrate. All these processes are accelerated by the 520 °C RTA.

To further examine the junction of $GaAu_2$ and (100) Ga_2O_3, Fig. 5 shows high-resolution HAADF STEM images of the edge termination. From Figs. 5(a) and 4(a), it is observed that the tip region of $GaAu_2$, pointing toward the Ga_2O_3 substrate, is not sharply pointed but is rather blunt, likely due to surface tension and stable interface boundaries. The sides of the $GaAu_2$ inclusion show good alignment with the (310) planes of Ga_2O_3. By matching the atomic columns in Fig. 5(b), it is confirmed that the boundary lies along the (310) plane. Furthermore, the edge of the (310) Ga_2O_3 surface appears to be Ga(II)-terminated. (Because the image was not aligned to the $GaAu_2$ zone axis and/or due to overlap with the Ga_2O_3 lattice, the edge structure of the $GaAu_2$ inclusion cannot be identified.) At the boundary between $GaAu_2$ and (310) Ga_2O_3, a consistently higher intensity on Ga(II) columns is observed compared to that on Ga(I) columns. This may indicate a preferential reaction of Ga(I) vs Ga(II) with the metallization layer. Further investigation and theoretical support will be needed to fully explain the intensity differences observed on the Ga columns.

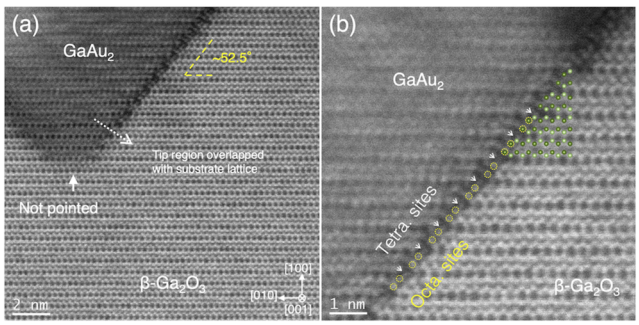

FIG. 5. (a) High-resolution STEM HAADF image of the structure at the boundary between the Ga_2O_3 substrate and the $GaAu_2$. The tip region of the $GaAu_2$ is not sharply pointed. (b) Atomic-resolution STEM HAADF image which shows the edge termination of the Ga_2O_3 substrate and the $GaAu_2$. Based on matching the atomic columns, the (310) plane is Ga(II) terminated, while a distinct feature of intensity difference between Ga(II) and Ga(I) is observed precisely at the boundary region.

CONCLUSIONS

In conclusion, the effects of post-metallization anneal are systematically and quantitatively investigated for (100)-oriented Ga_2O_3/Ti–Au ohmic contacts. A low specific contact resistance of 2.49×10^{-5} Ω·cm^2 is obtained when the RTA temperature is around 420 °C for 1-min in N_2 environment, with $N_D - N_A \cong 2.6 \times 10^{18}$ cm^{-3}. This optimal RTA temperature is found to be lower than the 470 °C value typically used for (010) substrates, suggesting that the anneal process window has an orientation dependence. Moreover, a drastic increase in contact resistance of around two orders of magnitude is observed when the annealing temperature is increased to 520 °C. Microscopy characterization of the degraded contact interface reveals that the interfacial region has undergone excess reactions. Various distinct features are found at the interface of the 520 °C-annealed sample, including: (1) an expanded Ti–TiO_x region is formed *in situ*, 25–30 nm in thickness; (2) the formation of $GaAu_2$ inclusions in the Ti–TiO_x region; (3) preferential (310) Ga_2O_3 crystalline alignment of the $GaAu_2$ inclusion boundaries; and (4) the edge of the Ga_2O_3 (310) plane appears to be Ga(II) terminated. Correlating the electrical performance and microscopy findings, the degraded ohmic contact is likely the result of aggressive Au in-diffusion and its reaction with Ga that has out-diffused, resulting in the increased thickness of the Ti–TiO_x layer, since it now also contains the $GaAu_2$ inclusions. The findings here indicate that Ti/Au metallization on (100)-oriented Ga_2O_3 may not be suitable for a very high temperature operation or post-metallization processes at > 500 °C, where elemental exchange and reactions may be accelerated in ways that are detrimental for ohmic contact stability. Thus, a re-design of the metallization scheme using Au-free electrodes or barrier layers may be needed to ensure robustness of the Ga_2O_3 ohmic contacts to high-temperature operation or processing. In addition, it may be interesting to examine the critical interfacial TiO_x thickness for the degraded ohmic contact and its dependence on substrate orientation. It would also be interesting to assess the effect of RTA on (100) contacts formed on heavily-doped Si layers made by ion implantation or epitaxial regrowth.

SUPPLEMENTARY MATERIAL

See the supplementary material for an additional HAADF STEM image and EDX mappings of the Au-rich inclusions and substrate region along with a table depicting interplanar spacings of possible Au-compounds based on crystallographic simulation.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Ming-Hsun Lee: Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Ta-Shun Chou**: Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – review & editing (supporting). **Saud Bin Anooz**: Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – review & editing (supporting). **Zbigniew Galazka**: Conceptualization (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (supporting). **Andreas Popp**: Conceptualization (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Writing – review & editing (supporting). **Rebecca L. Peterson**: Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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