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10.1016/j.egyr.2022.10.180

Iqbal, H., Tariq, M., Sarfraz, M., Sarwat, A. I., Alhosaini, W., Aldosari, O., & Aziz, A. (2022). Selective harmonic mitigation based two-scale frequency control of cascaded modified packed U-cell inverters. Energy Reports, 8, 15, 1009-1020. https://doi.org/10.1016/j.egyr.2022.10.180

Available online at www.sciencedirect.com
ScienceDirect
Energy Reports 8 (2022) 1009–1020
www.elsevier.com/locate/egyr

2022 The 5th International Conference on Renewable Energy and Environment Engineering (REEE 2022), 24–26 August, 2022, Brest, France

Selective harmonic mitigation based two-scale frequency control of cascaded modified packed U-Cell inverters

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Received 7 October 2022; accepted 9 October 2022
Available online xxxx

Abstract

A new Modified Packed U-Cell (MPUC) converter architecture with cascading is proposed in this paper. To provide an output voltage of 25 levels, the proposed cascaded MPUC needs only twelve power switches and four power sources. The converter comprises two cascaded MPUCs with DC supply in a ratio of 5:1. One converter is operating at low frequency (LF) and the other at high frequency (HF) that leads to lower power losses and higher levels. Besides, a variable frequency method is anticipated to produce a 25-level output voltage which has low harmonic content (THD) with the help of Selective Harmonic Mitigation (SHM). The optimum switching angles for SHM are obtained through solving the SHM equations using the Genetic Algorithm (GA). The designed controller is efficient and suitable for applications that require low-frequency operation either in stand-alone or grid-tied. The proposed inverter and its operation procedure have been investigated using MATLAB®/Simulink software, and the findings demonstrate that the proposed inverter output voltage has reduced THD significantly. The simulation results are verified using the typhoon HIL-402 emulator. Also, the power loss analysis is done using PLECS. The maximum efficiency of the converter is found to be around 98.34%. The simulation results justified the efficiency and viability of low 25-level THD voltages.

Peer-review under responsibility of the scientific committee of the 5th International Conference on Renewable Energy and Environment Engineering REEE, 2022.

Keywords: Selective harmonic mitigation; Modified packed U-cell; Two-scale frequency control; Genetic algorithm; Asymmetrical multi-level inverter

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https://doi.org/10.1016/j.egyr.2022.10.180

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1. Introduction

Over the past few years, there has seen a surge in the adoption of renewable energy sources globally, and this trend seems unlikely to slow down any time soon. People from many parts of the world are becoming increasingly interested in solar energy. To ensure grid power quality, appropriate power electronic devices should be developed [1]. The voltage source inverter (VSI) is the primary component required for photovoltaic systems since it converts DC power from distributed photovoltaic systems into AC power [2].

Further, the current fed into the grid should adhere to specific standards pertaining to the reduction of harmonic distortion, referred to as Total Harmonic Distortion (THD). To do this job using passive, active, or hybrid filters, the grid is connected to the converter output at the PCC (point of common coupling) [3].

With multi-level inverters (MLI), high-quality waveforms have been achieved, reliability has been increased, and power switches have been rated beyond their capacities. This has enabled them to be used in applications requiring high power. Several articles have been published in the last few decades regarding control and modulation techniques [4–6]. Most commonly studied MLI types are NPCs (neutral point clamped converters) [7], flying capacitors (FC) [8], and cascaded H-bridge converters (CHBs) [9]. CHB, which is modular and scalable, is the topology of choice for high-power applications. CHB has the disadvantage that it requires many separate voltage sources. The FC and NPC structures require more capacitors when there are more levels, as well as more DC sources in the CHB structure as there are H-bridges involved [10].

Recent studies have proposed various multi-level topologies aimed at reducing power switches count, dc sources, capacitors, and complexity. Here's one: the packed U-cell inverters (PUCs) [11]. There are two switches and one dc bus in a single U-cell. With the same number of devices, PUC inverters can generate a greater number of output levels than conventional multi-level topologies. The PUC inverter is capable of producing up to seven levels of voltage, depending on the voltage ratio between the main and secondary DC source. For 2:1 ratios, as many as five levels are generated, and for 3:1 ratios, as many as seven levels. However, PUC inverters with five levels (PUC5) have proven attractive even with fewer levels, thanks to the method of using redundant vectors to control floating capacitors without sensors [12].

In [13], a structure whose configuration creates up to five levels with two U-cells has been proposed and called modified packed U-cell (MPUC5). With the MPUC5 inverter, the maximum output voltage is determined by the combined voltages, whereas with the PUC5 inverter, the maximum output voltage is determined by the larger voltage DC supply. The amplitude of the sources usually dictates the classification of one-phase MLIs into symmetric (SMLIs) or asymmetric (AMLIs). The structure is symmetrical if the DC sources are equal; otherwise, it is asymmetric. Six switches and two capacitors are all you need for the packed U-cell AMLI. Due to the increased efficiency and fewer switches, AMLIs has been the subject of increased research over the past decade [14].

In this work, cascading of two MPUC5 is proposed with the 5:1 main source voltage ratio and the corresponding auxiliary source at 1:1 ratio, thus producing a 25-level output voltage. Employing a metaheuristic technique for computing switching angles, the authors present a cascaded operation of two MPUC5 that reduces THD in the output voltage. In power electronics control algorithms, metaheuristic techniques are extensively used [15]. Genetic Algorithm (GA) based selective harmonic mitigation (SHM) is applied here, a search-based method to solve optimization problems that are difficult to solve mathematically — either because the problem has a nonlinear structure or because it is too complex to solve. As long as the objective function is correctly defined, this method guarantees convergence.

Due to its ability to suppress a limited low order harmonics content, selective harmonic elimination (SHE) can reduce harmonic content in output signals. By using the SHM technique, however, the constraints utilized in SHE can be relaxed, and output waveforms, which exhibit better harmonic performance, are calculated according to actual grid regulations [16]. SHE makes it possible to cancel a limited number of harmonics, but the harmonics that are not canceled are not taken into account and can have a large magnitude. Due to this, it is impossible for them to remain below the desired value, resulting in a more extensive and expensive filter system. The flexibility of SHM, however, can allow for the application of different criteria to the lower and higher-order harmonic content. By reducing lower order harmonics beyond the specified limits in the grid code, reduced values can be achieved. SHE cannot control high-order harmonics, but SHM can. To fulfill the grid code in this paper, the SHM technique has been utilized with the aim of reducing the harmonic content as much as possible. To make filtering elements smaller, lighter, and cheaper, the main goal is to reduce the filter requirements [16].

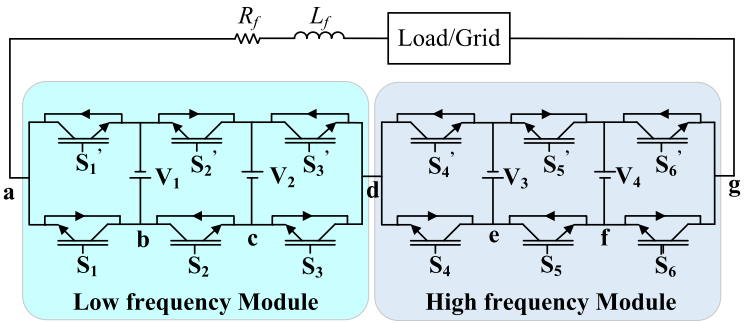

Fig. 1. Cascaded MPUC25 topology $V_1 = V2 = 100$ V, $V_3 = V4 = 20$ V.

The following sections comprise this study: in Section 2, the cascaded operation of two MPUC5 and corresponding generation of 25-levels is discussed. In Section 3, mathematical modeling of the designed topology for SHM is done employing the Fourier Series. In Section 4, the Genetic Algorithm is used for obtaining the optimal THD by calculating the desired switching angles. In Section 5, a two-level frequency is formulated for the proposed topology. A power loss analysis is performed with PLECS software in the next section. In Section 7, the results obtained for the topology in MATLAB/Simulink © environment are discussed. In Section 8, these results are real-time implemented using typhoon HIL-402. Finally, in the last section, conclusions and discussion are done.

2. Proposed cascaded MPUC topology

As shown in Fig. 1, two MPUC5 inverters are cascaded together in the proposed MPUC25 configuration. MPUC5 is an inverter that is made up of six switches and two DC sources. With this topology, it is possible to configure an inverter or converter for a one-phase system. Two identical DC links are being used by an MPUC5 converter to provide a five-level output voltage in a one-phase inverter mode [13]. By selecting Vdc/2 as the secondary source of voltage, the same converter topology also facilitates the generation of seven levels of output voltage (MPUC7) [17]. A cascaded MPUC inverter is comprised of two MPUC5 sub-modules connected in a cascade. A wide range of voltage levels can be achieved with a minimum number of switches by cascading. With Cascaded MPUC (CMPUC), so as to get 25 levels, the input side voltages have to be chosen in accordance with

$$V_1 = V_2 = 5V_3 = 5V_4 \tag{1}$$

where V_1 and V_3 are the primary DC sources and V_2 and V_4 are the auxiliary sources, respectively. This configuration has the main advantage of boosting the voltage greater than the maximum DC magnitude. Maximum voltage range:

$$V_{o,max} = \frac{12}{5}E = 2.4E \tag{2}$$

where E is the voltage source with the highest magnitude (V_1).

Two MPUC5 inverters with cascade connections were used to create 25-level waveforms using four voltage sources. In total, there are five transfer states (V_{DC}, $2V_{DC}$, 0, $-V_{DC}$, and $-2V_{DC}$) for individual converters. Auxiliary source voltages can cause these states when they are used in conjunction with the main source voltage. Also, in this configuration, redundant states exist, which can be used if switching failures happen. Two cascaded units with five output voltage levels can provide a maximum voltage of 25. In this configuration, isolated DC sources should be selected in a 1:5 or 5:1 ratio. Fig. 1 shows that 6 of the 12 switches operate at higher frequencies. By assigning a higher voltage to the low-frequency side of the switch, switching losses are substantially reduced.

An inverter with cascaded modified PUC25 (CMPUC25) consists of key pairs of the anti-parallel switch (S_1 and S_1'), (S_2 and S_2'), (S_3 and S_3'), (S_4 and S_4'), (S_5 and S_5'), & (S_6 and S_6'). In anti-parallel switch pairs, no two switches are turned on simultaneously (i.e., each switch works independently). The output voltage level of the CMPUC25 inverter is listed in Table 1. Switch operates according to

$$S_i = \begin{cases} 0 \; if \; S_i \; is \; off \\ 1 \; if \; S_i \; is \; on \end{cases} \quad i = 1, 2, 3, 4, 5, 6 \tag{3}$$

Table 1. Switching states for 25-level Cascaded MPUC inverter.

State	$S_1S_2S_3$	$S_4S_5S_6$	Converter1 $\mathbf{V_{ad}}$	Converter2 $\mathbf{V_{dg}}$	Terminal output $\mathbf{V_O}$
1.	101	101	$V_1 + V_2$	$V_3 + V_4$	12 E/5
2.	101	100	$V_1 + V_2$	V_3	11 E/5
3.	101	111	$V_1 + V_2$	0	10 E/5
4.	101	110	$V_1 + V_2$	$-V_4$	9 E/5
5.	101	010	$V_1 + V_2$	$-V_3 - V_4$	8 E/5
6.	100	101	V_1	$V_3 + V_4$	7 E/5
7.	100	100	V_1	V_3	6 E/5
8.	100	111	V_1	0	5 E/5
9.	100	110	V_1	$-V_4$	4 E/5
10.	001	010	V_2	$-V_3 - V_4$	3 E/5
11.	111	101	0	$V_3 + V_4$	2 E/5
12.	111	100	0	V_3	E/5
13.	111	111	0	0	0
14.	111	110	0	$-V_4$	−E/5
15.	000	010	0	$-V_3 - V_4$	−2 E/5
16.	011	101	$-V_1$	$V_3 + V_4$	−3 E/5
17.	110	100	$-V_2$	V_3	−4 E/5
18.	110	111	$-V_2$	0	−5 E/5
19.	110	110	$-V_2$	$-V_4$	−6 E/5
20.	110	010	$-V_2$	$-V_3 - V_4$	−7 E/5
21.	010	101	$-V_1 - V_2$	$V_3 + V_4$	−8 E/5
22.	010	100	$-V_1 - V_2$	V_3	−9 E/5
23.	010	111	$-V_1 - V_2$	0	−10 E/5
24.	010	110	$-V_1 - V_2$	$-V_4$	−11 E/5
25.	010	010	$-V_1 - V_2$	$-V_3 - V_4$	−12 E/5

A CMPUC25's output voltage (V_o) can be described as follows:

$$V_O = V_{ab} + V_{bc} + V_{cd} + V_{de} + V_{ef} + V_{fg} \tag{4}$$

where Fig. 1 shows a, b, c, d, e, f, e, and g. On the basis of the switching pulses, the output voltage is:

$$\left.\begin{aligned} V_{ab} &= (S_1 - 1)(V_1) \\ V_{bc} &= (1 - S_2)(V_1 - V_2) \\ V_{cd} &= (1 - S_3)(V_2) \\ V_{de} &= (S_4 - 1)(V_3) \\ V_{ef} &= (1 - S_5)(V_3 - V_4) \\ V_{fg} &= (1 - S_6)(V_4) \end{aligned}\right\} \tag{5}$$

V_1 & V_3 are the main DC sources, and V_2 & V_4 are the corresponding auxiliary voltage value. By substituting (5) into (4), (6) & (7) is obtained. (7) represents the output voltage depending on switching.

$$V_O = (S_1 - 1)(V_1) + (1 - S_2)(V_1 - V_2) + (1 - S_3)(V_2) + (S_4 - 1)(V_3) + (1 - S_5)(V_3 - V_4) + (1 - S_6)(V_4) \tag{6}$$

$$V_{ag} = (S_1 - S_2)(V_1) + (S_2 - S_3)(V_1) + (S_4 - S_5)(V_3) + (S_5 - S_6)(V_4) \tag{7}$$

In Table 1, it can be seen all the states of the converter, whose output signal is plotted in Fig. 2. In both MPUC units, the voltage level shift can be controlled with the selective harmonic mitigation (SHM) technique. In the proposed inverter module, 12 levels in the positive quarter are generated, and 12 levels in the negative cycles are generated, along with a zero-voltage level, as presented in Fig. 2. The GA is used to determine switching angles α_i. Voltage levels are selected in such a manner that they will have quarter symmetry.

3. SHM in CMPUC25

For an inverter to function efficiently, its harmonic distortion (THD) must be reduced. By using the selective harmonic mitigation (SHM) technique, total harmonic distortion in synthesized waves of inverters can be reduced

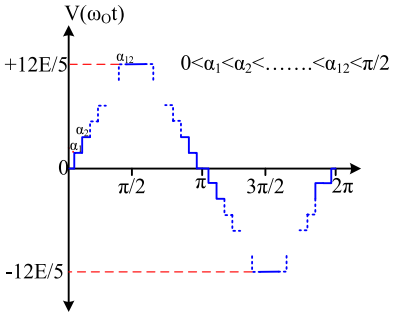

Fig. 2. Proposed output voltage levels of CMPUC25.

according to IEEE standards because the overall harmonic distortion is reduced. In order to obtain SHM equations, Fourier series analysis is applied to the output waveform of the inverter in Fig. 2.

As shown in Fig. 2, the proposed inverter is a 25-level waveform made up of steps:

$$\mathrm{V}\,(\mathrm{t}) = \mathrm{E}\left[\sum_{i=1}^{12} u\,(t-\alpha_i) - \sum_{i=1}^{12} u\,(t-(\pi-\alpha_i)) - \sum_{i=1}^{12} u\,(t-(\pi+\alpha_i)) + \sum_{i=1}^{12} u(t-(2\pi+\alpha_i))\right] \tag{8}$$

Considering that the waveform displays x-axis and y-axis symmetry, its Fourier series contains odd harmonics whose amplitudes are as follows:

$$\mathrm{V}_n = \frac{2}{T_o}\int_0^{t_0} V(t)\sin(n\omega_o t)dt \quad \forall n = 1, 3, 5, \ldots \tag{9}$$

Substituting V(t) from (8) into (9), gives to

$$\mathrm{V}_n = \frac{4}{n\pi}\left[\sum_{i=1}^{12} E\cos(n\alpha_i)\right] \quad \forall n = 1, 3, 5, \ldots \tag{10}$$

where $0 < \alpha_1 < \alpha_2 < \alpha_3 \cdots < \alpha_{12} < \pi/2$

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=3,5,\ldots}^{\infty}\left[\frac{4E}{n\pi}\sum_{i=1}^{12}\cos(n\alpha_i)\right]}}{\frac{4E}{\pi}\sum_{i=1}^{12}\cos(n\alpha_i)} \tag{11}$$

The nonlinearity of these SHM equations makes them challenging to analyze using conventional methods. In addition, traditional optimization methods require a starting point and derivative information of the functions. Since SHM equations involve complex equations, it is challenging to determine an initial point; furthermore, these methods can be driven by initial guesses and can create local minima. Research relies on modern algorithms inspired by nature to overcome traditional methods' problems. Holland developed genetic algorithms (GAs), which a well-known for their ability to tackle optimization problems, which are complex as well as nonlinear. The method used here is based on the GA for constraint minimization.

Ideally, for a fundamental voltage V_1, the switching angles $\alpha_1, \alpha_2, \alpha_3, \ldots \alpha_{12}$ can be calculated so that $V_0(\omega t) = V_1 sin(\omega t)$, and certain high-order harmonic content will be null. $n + 1$ equations are necessary to control the fundamental output voltage and minimize n harmonics. Solving the following equations simultaneously yields the SHE switching angles:

$$\left.\begin{array}{c}
\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cdots + \cos(\alpha_{12}) = \frac{4mE}{\pi} \\
\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cdots + \cos(3\alpha_{12}) = 0 \\
\cos(5\alpha_1) + \cos(5\theta_2) + \cos(5\alpha_3) + \cdots + \cos(5\alpha_{12}) = 0 \\
\vdots \\
\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cdots + \cos(n\alpha_{12}) = 0
\end{array}\right\} \tag{12}$$

Hence, the cost function f for SHM, which needed to be minimized, can be obtained by combining (12) and keeping the limits of each harmonic content within limits as per IEEE standards.

$$f(\alpha_1, \alpha_2, \alpha_3, \ldots \alpha_{12}) = p_1 |V_1 - V_m| + p_3 |V_3| + p_3 |V_3| + \cdots + p_n |V_n| \tag{13}$$

where $p_1, p_3, p_3, \ldots, p_n$ are penalty factors and defined by

$$p_i = \frac{4}{2i-1} \quad \forall i = 1, 2, 3, \ldots \tag{14}$$

4. Genetic algorithm

In real-world optimization problems that are inherently nonlinear, metaheuristic approaches have shown to be effective in solving problems that conventional techniques cannot handle or take a long time to resolve. In a variety of optimization applications, nature-inspired evolutionary methods are being used. The objective function derived from (13) in this paper is minimized using the Genetic Algorithm (GA). GA offers the following advantages: (i) convergence is assured (with a specific range of tolerance), and (ii) derivatives are not necessary (since iterations follow input–output mapping). A detailed flowchart supports the discussion of the required steps in the following subsections.

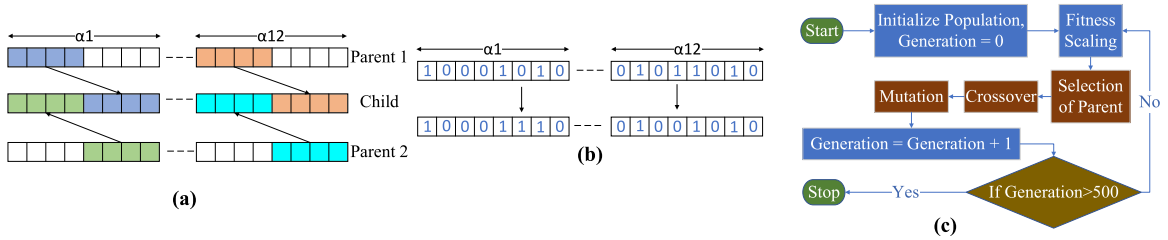

Fig. 3. GA (a) Crossover (b) Mutation (c) Flowchart.

4.1. Steps

4.1.1. Design algorithm

Fig. 3 (from α_1 to α_{12}) demonstrates the same angles as (12). Variables are formed by these angles and are to be correlated, as described in Fig. 2. This is done by randomly selecting 100 chromosomes. Chromosomes contain 12 bytes ($12 \times 8 = 96$ bits). A random sample is chosen as the initial population. The penalty factors $p_1, p_2, p_3, \ldots, p_n$ are such defined that $p_1 > p_2 > p_3 > \cdots > p_n$, with $p_1 = 4$. Harmonics to be eliminated are ranked according to priority.

4.1.2. Selection

Using probability, two parents are chosen randomly from the population after initialization. For this study, the Roulette wheel approach is used. By selecting parents randomly, the solution space is explored to the greatest extent possible.

4.1.3. Crossover and mutation

In a crossover, genes are blended in a certain way. A child's chromosome is made up of bits taken from each parent, half from the first parent and half from the second parent, as shown in Fig. 3(a). In essence, the mutation is the way the child gets better than its parent. Consequently, in GA techniques, the bits are flipped to achieve this. Fig. 3(b) shows a single byte of each chromosome of the child that has been altered. Additionally, it is not allowed to mutate the entire population of children.

Table 2. Switching angles (in radians) associated with different modulation index.

m	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}	α_{12}
1.10	0.055	0.165	0.278	0.393	0.514	0.647	0.791	0.961	1.209	1.263	1.368	1.469
1.05	0.042	0.124	0.207	0.295	0.382	0.471	0.566	0.674	0.778	0.906	1.05	1.276
1.00	0.043	0.124	0.207	0.295	0.383	0.472	0.568	0.67	0.781	0.905	1.051	1.277
0.95	0.042	0.123	0.21	0.294	0.381	0.474	0.566	0.671	0.78	0.906	1.05	1.277
0.90	0.042	0.126	0.205	0.296	0.382	0.473	0.568	0.669	0.781	0.905	1.05	1.277
0.85	0.042	0.124	0.209	0.294	0.382	0.472	0.569	0.67	0.78	0.906	1.049	1.276
0.80	0.044	0.136	0.224	0.32	0.415	0.516	0.624	0.737	0.868	1.018	1.241	1.464
0.75	0.045	0.135	0.23	0.319	0.418	0.518	0.629	0.742	0.874	1.026	1.258	1.469
0.70	0.043	0.124	0.207	0.296	0.381	0.472	0.568	0.669	0.781	0.905	1.049	1.273
0.65	0.045	0.134	0.228	0.317	0.417	0.515	0.622	0.738	0.866	1.017	1.239	1.362
0.60	0.042	0.123	0.209	0.293	0.383	0.471	0.567	0.671	0.779	0.904	1.05	1.271

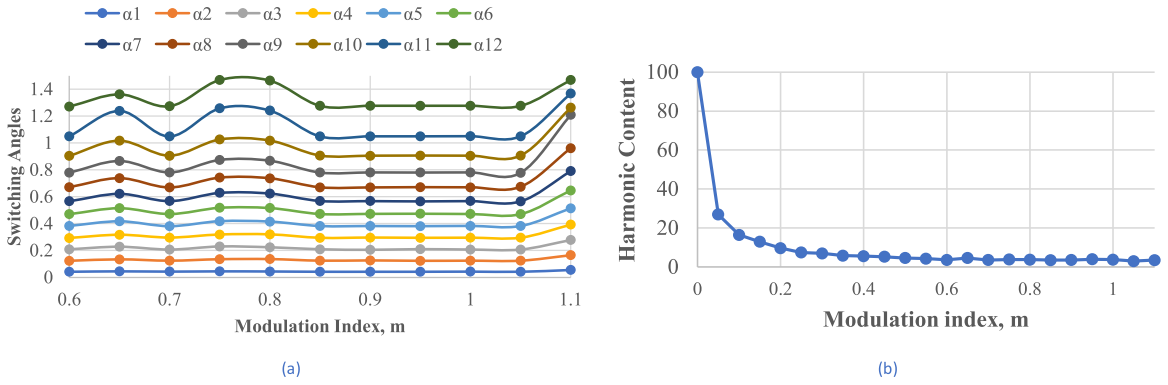

Fig. 4. (a) Variation in switching angles with corresponding modulation index. (b) Output Voltage THD (%) as a function of modulation index.

4.2. Methodology

Following initialization, the population is sorted by fitness. Afterward, the fifty mutant and non-mutated children get swapped with the current generation in accordance with their suitability. The offspring is discarded if its fitness is too low compared to the solution that is already available. Each iteration lasts until the predetermined number has not been reached. There are 500 iterations in this flowchart, as shown in Fig. 3(c), which is denoted by K. δ indicates the iteration number that is currently being executed. In this study, the switching angles are calculated for 51 modulation indices (m), where m is the ratio of the preferred voltage at fundamental frequency to the highest attainable level. In this case, the greatest attainable voltage is 2.4 times the largest DC source. Angles are derived for 51 samples of m, with values ranging from 0.60 to 1.10. Table 2 presents the optimal values of the 12 angles corresponding to the few m values generated. In Fig. 4(a), the variation in switching angles with corresponding modulating indices are plotted. Fig. 4(b) displays the voltage harmonic content as a function of the modulation index.

5. Two level frequency control

In order to control both MPUC units, selective harmonic mitigation (SHM) is applied for voltage level shifts. In the proposed inverter module, 12 levels in the positive cycles are generated, and 12-levels in the negative cycles are generated, including a zero level, as depicted in Fig. 2.

In Fig. 5, it can be seen that the switching frequency of S_2 & S_5 switches will be the least (at the fundamental frequency) compared to those of other switches in the converter; that is, the switching frequency of S_2 and S_2' in MPUC1 and S_5 and S_5' in MPUC2 will be the smallest of all the switches of the converter. As a whole, the switches have the following frequency behavior: $f_{S_6} = 2f_{S_4} = 3f_{S_5} = 4f_{S_3} = 5f_{S_1} = 6f_{S_2}$, with $f_{S_2} = 50$ Hz.

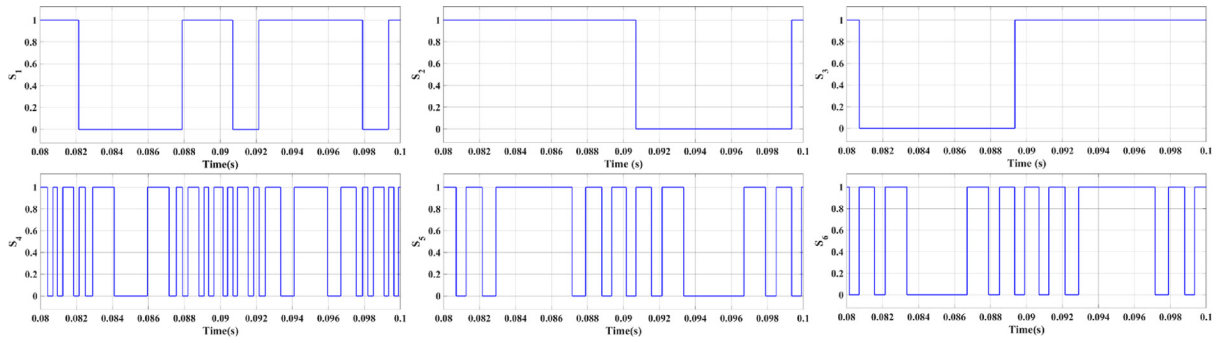

Fig. 5. Switching pattern for cascaded PUC inverters of MPUC1 and MPUC2.

Thus, the MPUC1 operates at a relatively lower frequency (60 Hz, 50 Hz, and 75 Hz) while the MPUC2 operates at a somewhat higher frequency (100 Hz, 150 Hz, and 300 Hz).

6. Power loss analysis

In general, power losses are accounted for by considering switching losses and forward conduction losses. This circuit uses only switches. PLECS software is used for power analysis after presenting a theoretical analysis of loss.

6.1. Switching losses

During switching on and off, there is a loss of power. For a single switch-on, the loss of power can be summarized as follows:

$$P_{sw\_on} = \int_0^{t_{on}} v(t)i(t)dt \tag{15}$$

Similarly, for turning off case:

$$P_{sw\_off} = \int_0^{t_{off}} v(t)i(t)dt \tag{16}$$

As a result of solving Eqs. (15) & (16) for switching losses, it is obtained as

$$P_{sw\_on} = \frac{V_{sw} \times I_{t_{on}}}{6} \tag{17}$$

$$P_{sw\_off} = \frac{V_{sw} \times I_{t_{off}}}{6} \tag{18}$$

Likewise, V_{sw} is the voltage across the switch, $I_{t_{on}}$ & $I_{t_{off}}$ are the currents during the process of turning the switch on and off, and t_{on}&t_{off} are the respective times of turning the switch on and off. During one complete switching cycle, P is equal to

$$P_{sw} = \frac{V_{sw} \times (I_{t_{on}} + I_{t_{off}})}{6} \tag{19}$$

6.2. Conduction losses

Switches and diodes lose energy due to conductivity. Because circuits consist only of switches, the conduction losses for any switch are

$$P_{ci} = [V_s + R_s i^{\gamma}(t)]i(t) \tag{20}$$

the voltage drop across the switch indicated by V_s, R_s refers to the switch's resistance, and γ is a specified value in the switch's characteristics. It is estimated that the total conduction loss is based on the following calculation:

$$P_c = \frac{1}{T}\int_0^{2\pi} \sum_{i=1}^{N_{switch}} P_{ci}(t) \tag{21}$$

As a result, the converter will have a total loss of

$$P_{loss} = P_{sw} + P_c \tag{22}$$

Power loss analysis of the CMPUC25 is done using PLECS software with the IKW40N65ES5_IGBT model provided by Infineon. Fig. 6(a) is for the turn-on characteristic, Fig. 6(b) is for the turn-off characteristic, and Fig. 6(c) is for the conduction losses of the above-mentioned model. Fig. 6(d) shows the switches' junction temperature with 25 °C environment temperature. At a load of 72 Watts, the converter is capable of achieving maximum efficiency of 98.34%, as indicated in Fig. 6(e). A comparison of efficiency and losses under various loading conditions is shown in Fig. 6(f).

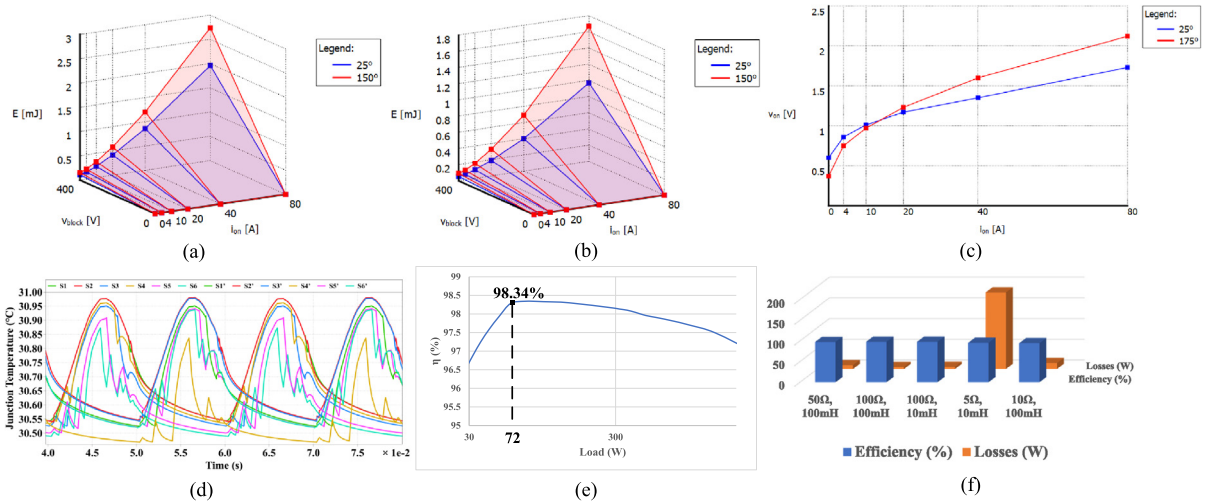

Fig. 6. (a) Turn-on characteristic of switch (b) Turn-off characteristic of switch (c) Conduction losses of switch (d) Switch junction temperature (e) Efficiency as a function of load (f) Efficiency and losses at different load.

7. Simulation results

The cascaded MPUC is simulated with parameters tabulated in Table 3 under MATLAB/Simulink environment. From Fig. 7, the stress across various switches of CMPUC25 can be observed as follows: $V_{s_2} = 2V_{s_1} = 2V_{s_3} = 10V_{s_4} = 5V_{s_5} = 10V_{s_6}$, with $V_{s_2} = 200$ V. The complementary switches also work similarly (i.e., $V_{s_2'} = 2V_{s_1'} = 2V_{s_3'} = 10V_{s_4'} = 5V_{s_5'} = 10V_{s_6'}$).

Table 3. Simulation parameters.

Particular	Values
DC link voltage 1(V_1)	100
DC link voltage 2 (V_3)	20 V
Load Parameters	10 Ω, 15 mH

Fig. 8(a) shows MPUC1's output voltage. The output voltage of MPUC-1 will be boosted with a maximum potential level of 200 V, and the boosted output voltage waveform of MPUC-2 is plotted with a maximum voltage level of 40 V, as illustrated in Fig. 8(b). It is evident from Figs. 5 and 7 that the switches of MPUC-1 must have a high-voltage, low-frequency rating, while the switches of MPUC-2 are operated at a low-voltage, high-frequency

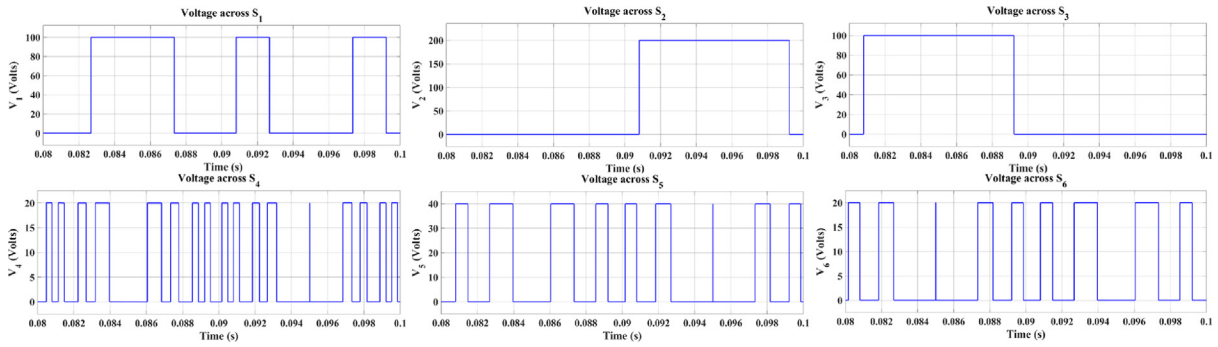

Fig. 7. Voltage across switches of CMPUC25.

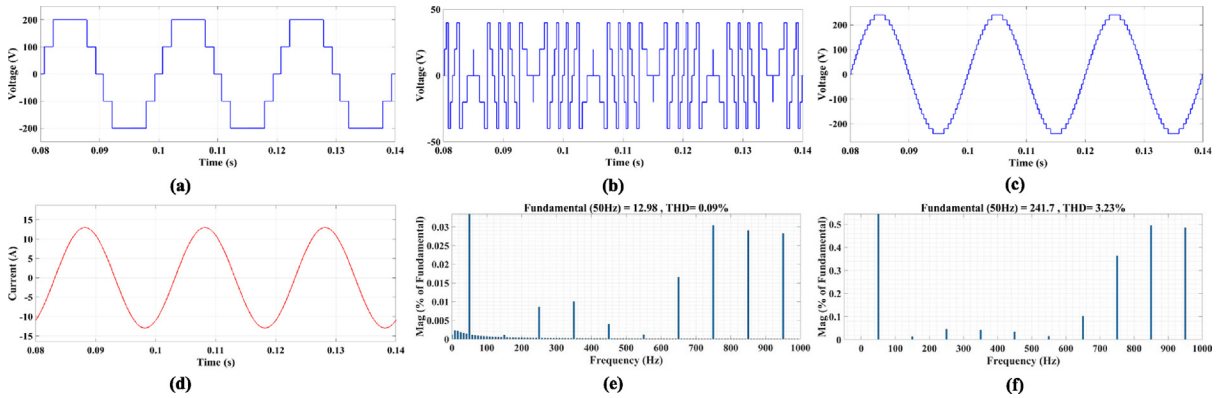

Fig. 8. Simulation results. (a) Output voltage of MPUC1. (b) Output voltage of MPUC2. (c) Output voltage of CMPUC25. (d) Output current waveform. (e) Output current THD. (f) Output voltage THD.

rating. MPUC-1, on the other hand, can be implemented with GTOs, while MPUC-2 can utilize IGBT or MOSFET. To simplify things, both MPUCs here are driven by IGBTs. The overall CMPUC25 output voltage is plotted in Fig. 8(c), having a THD of 3.23%, as illustrated in Fig. 8(f). 240 V is the highest voltage available, which is 2.4 times the maximum applied voltage described in (2). Fig. 8(d) shows the output current waveform having a THD of 0.09%, as shown in Fig. 8(e).

8. Hardware-in-loop validations

To validate the selective harmonic mitigation (SHM) technique, the two MPUCs are cascaded using the typhoon HIL 402 hardware emulators, and results are obtained on a digital oscilloscope. The CMPUC25 is tested in HIL mode, and the results are in agreement with the MATLAB/Simulink simulation performed in the previous section. MPUC-1 and MPUC-2 output voltage waveforms are shown in Fig. 9(a) and Fig. (b). The overall output waveform of the CMPUC25 is plotted in Fig. 9(c), showing twenty-five level waveforms. Fig. 9(d) shows the output current of the converter which is in agreement to Fig. 8(d).

9. Conclusions

The aim of this paper is to describe an asymmetrical inverter with boosted output. In this case, two 5-level modified packed u-cell (MPUC) inverters were cascaded using a 1:5 voltage ratio between the main DC sources and the same voltage level source for each converter. A detailed discussion of the switching states and the mathematical relation governing the output of the converter is presented in detail. In order to achieve selective harmonic mitigation, the individual harmonic equation is formulated in terms of the switching angles. For decreasing the harmonic content, the switching angles are calculated using a metaheuristic approach like GA. Based on the switching angles,

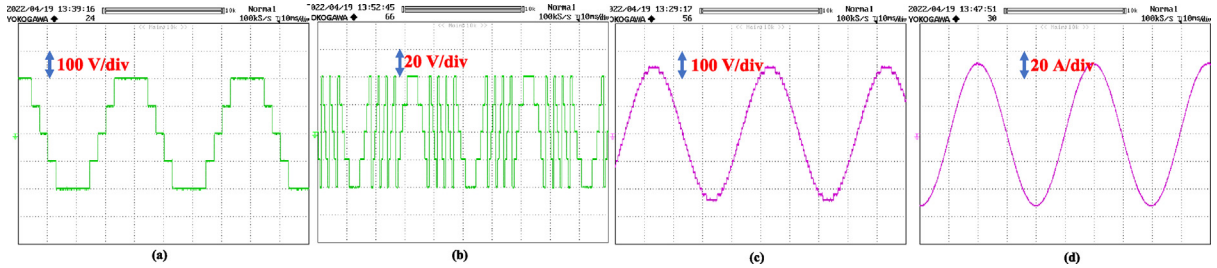

Fig. 9. HIL Results (a) Output Voltage of MPUC-1 (b) Output Voltage of MPUC-2 (c) Output Voltage of Converter (d) Output Current Waveform.

a simulation of the converter is performed using the MATLAB/Simulink environment, and then the same is verified using typhoon HIL 402 hardware emulators. Also, the switching loss analysis is done using PLECS software which shows that the converter offers a maximum efficiency of 98.34%, which shows a promising result. Furthermore, it shows a voltage THD of 3.23% and current having a THD of 0.09%.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

Acknowledgments

This work was funded by the Deanship of Scientific Research at Jouf University, Saudi Arabia under grant No (DSR-2021-02-03109).

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