Impact of non-idealities on the Performance of an Ultracapacitor based Bidirectional DC/DC Converter

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***Abstract*—This paper analyses the impact of non-idealities on the performance of an ultracapacitor based bidirectional DC/DC converter. In particular, this work analyses the impact of ON state resistance of the MOSFET switches on the performance of bidirectional DC/DC converter. It is shown that, under particular operating conditions, the ON state resistance of the MOSFET can have a significant impact on the performance of th DC/DC converter and can cause an unstable response. An analytical expression is derived to identify the operating conditions under which the non-idealities can have a significant impact on the performance of the DC/DC converter. Simulation results are presented to aid the analysis reported in this paper.**

I. Introduction

The increase in depletion of fossil fuels combined with environmental concerns and increase in power demand led to the pursuit of power generation using renewable energy sources. During the last decade, there has been a significant increase in the installed capacity of renewable energy systems. However, the major challenge involved in operation of systems with integrated renewable energy sources is the unpredictable nature of the power. One way to increase the reliability of renewable energy sources is to utilize the energy storage technologies. The state of the art energy storage technologies are capable of providing backup support in small scale power grids or microgrids and play a very important role in standalone microgrid applications [1], [2].

The most commonly used energy storage devices are batteries, ultracapacitor, and fuel cells. Ultracapacitor (UC) based energy storage systems are becoming popular (for short duration power support) due to their characteristics of high power density, high current capability, relatively more charging and discharging cycles. Typically, UC are stacked together and are integrated to a DC microgrid (i.e. the DC link bus) via a bidirectional DC/DC converter. The bidirectional DC/DC converter facilitates the flow of power from DC microgrid to energy storage device and vice-versa. When UC based converters are used in high power applications, the magnitude of current flowing through the switches of the converter is very high resulting in a small yet significant ON state voltage drop. Furthermore, the other non-idealities present in the circuit can also impact the performance of the converter during high currents. This paper aims to design a UC based bidirectional DC/DC converter considering non-idealities.

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The non-idealities present in the UC based bidirectional DC/DC bidirectional converter are, (a) resistance of inductor (b) ON state resistance of the switches, (c) ON state voltage drop of switches and (d) diode voltage drop. In addition, the equivalent parallel resistance (EPR) and equivalent series resistance (ESR) of the UC are also present. For low power applications, the non-idealities are significant and can easily be neglected during the design. This is however not the case with high power applications where in the effect of some of the non-idealities is significant. Typically, the current flowing through the EPR of UC (which is of the order of 1000Ω) is in the order of few milli-Ampere, and can be neglected for high and low power applications. The ON state voltage drop of switches and diodes can also be neglected as their value is less than 0.5V. However, the drop due to ON state resistance of the power MOSFET (which is usually in the range of 0.05Ω to 0.5Ω) is significant for high power applications. In addition, the ESR of UC which is typically of the order of 0.014Ω to 0.5Ω is also significant.

The aim of this paper is to deign and analyze the performance of a bidirectional DC/DC converter considering the non idealities of the ON state resistance of the switches, ESR of the UC stack and the resistance of the inductor. The paper is organized as follows : Section II of the paper describes the operation of bidirectional DC/DC converter and the selection of passive components. Section III describes the dynamic modeling and control of the DC/DC converter considering non-idealities. Sections IV and V report the simulation and experimental results of the proposed converter design respectively followed by conclusions in VI.

II. Bidirectional DC-DC Converter

The bidirectional DC/DC converter (comprising of two MOSFET switches and a filter inductor) that interfaces the UC stack to the DC Link is shown in Fig. 1. For most of the power electronics applications, the behavior of UC is analyzed using a lumped parameter equivalent circuit. The popular lumped circuit model employed for UC is the classical equivalent circuit [3] as shown in Fig. 2. For a given UC stack, the parameters of the equivalent circuit can be estimated from the

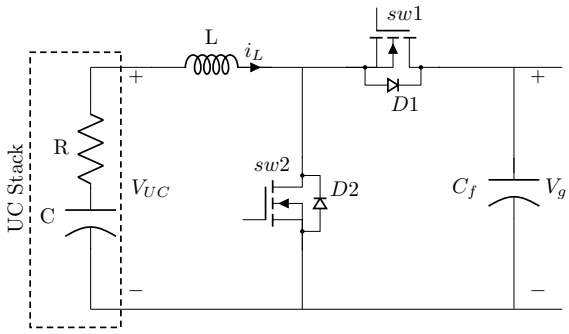


Fig. 1: Ultracapacitor based bidirectional converter

data sheet of UC [4].

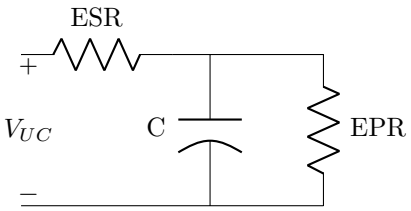


Fig. 2: Classical equivalent circuit of UC

To start with, the procedure for design of passive elements in the UC based DC/DC converter is outlined. Subsequently, the behavior of the DC/DC converter in various modes of operation is presented.

A. Design of Passive components of the converter

The UC based bidirectional converter has two passive components i.e. the UC stack and the filter inductor. The typical specifications involved in designing of the UC stack are the UC stack voltage and the discharge time period of UC stack [5]. The filter inductor on the other hand, is designed based on the maximum allowable ripple in the inductor current.

1) UC Stack Design: The capacitance value required for designing the UC stack can be computed based on the power rating of converter P_0 and the minimum ($V_{uc,min}$) and rated (V_{ucn}) voltages of the UC stack. Due to design considerations, the UC stack is usually allowed to discharge up to 50% of its rated value i.e.

$$V_{uc,min} = \frac{V_{ucn}}{2} \tag{1}$$

The maximum (I_{max}) and minimum (I_{min}) possible value of the current flowing through the UC stack (while discharging) can be computed as

$$\begin{aligned} I_{max} &= \frac{P_o}{V_{uc,min}} = \frac{2P_o}{V_{ucn}} \\ I_{min} &= \frac{P_o}{V_{ucn}} \end{aligned} \tag{2}$$

Accordingly, the average value I_{avg} of discharge current through the UC stack is given by

$$I_{avg} = \frac{1}{2}[I_{max} + I_{min}] = \frac{3P_0}{2V_{ucn}} \tag{3}$$

The minimum capacitance required for the UC stack can be computed based on the average discharge current and the maximum duration of discharge (Δt) as

$$C_{uc,min} = \frac{I_{avg}}{\Delta V}\Delta t = \frac{3P_o\Delta t}{V_{ucn}^2} \tag{4}$$

If V_{ucc} is the voltage of each UC (usually around 2.5 V), then, the number of UC cells to be connected in series to meet UC stack voltage is computed as,

$$n = \frac{V_{ucn}}{V_{ucc}} \tag{5}$$

The number of parallel branches (p) is determined based on the power rating of the converter and the current rating of the individual UC. The capacitance of the individual UC (C_{ucc}) is determined such that the the resulting capacitance (given by 6) is higher than the minimum value of stack capacitance (given by (4)).

$$C_{uc} = \frac{C_{ucc}\ p}{n} \tag{6}$$

2) Inductor Design: During the charging mode, the average value of current flowing through the inductor is equal to the average value of current through the UC stack and is given by (3). If the maximum allowable ripple (design parameter) is x (expressed as a percentage of average inductor current), then the value of inductance during charging mode can be computed using volt-second balance as

$$L_c = \frac{DT_s\left(V_g - DV_g\right)}{xI_{avg}} = \frac{V_g^2T_s}{xP_o}\frac{2D(1-D)}{3} \tag{7}$$

where T_s is the switching time period. The maximum value of inductance that will ensure that the ripple is below x for every operating duty ratio can be computed by setting $\frac{dL_c}{dD} = 0$. The maximum value of inductance during charging can be computed as

$$L_{c,max} = \frac{1}{6}\frac{V_g^2T_s}{xP_o} \tag{8}$$

During the discharging mode, the current through the inductor can be computed as

$$I_{L,dis} = \frac{P_o}{V_{uc}} = \frac{P_o}{V_g(1-D)} \tag{9}$$

The inductance needed during discharging mode (as a function of duty ratio) can be computed using volt-second balance as

$$L_d = \frac{V_g^2T_s}{xP_o}D(1-D)^2 \tag{10}$$

and the maximum value of allowable inductance that will ensure that the ripple criterion is satisfied for any operating duty ratio is

$$L_{d,max} = \frac{4}{27}\frac{V_g^2T_s}{xP_o} \tag{11}$$

Since the designed inductance must be suitable for both charging and discharging modes, the inductance can be chosen as

$$L_{max} = \frac{1}{6}\frac{V_g^2T_s}{xP_o} \tag{12}$$

B. Modes of operation of DC/DC converter

The bidirectional converter operates in three modes [6] namely, charging, discharging, and pulse width modulation (PWM) blocking modes. During charging mode, the converter behaves as a buck converter with switch $sw1$ operated in controlled manner and switch $sw2$ blocked. During discharging mode, the converter behaves as a boost converter with switch $sw2$ operated in a controlled manner and switch $sw1$ blocked. During the transition between charging and discharging modes or vice-versa, the converter operates in PWM blocking mode during which, both the switches $sw1$ and $sw2$ are blocked/turned OFF. In an independent control of charging and discharging loops, transition delay is important to block the switch pulses. The transport delay depends on the magnitude of inductor current and UC stack voltage. The PWM blocking period, Δt is given by:

$$\Delta t = L\frac{diL}{V_{uc}(i)} \tag{13}$$

where, $V_{uc}(i)$ is the UC stack voltage at the instant of transition. The state diagram and the transition between various states is shown in figure 3. The description of each state is mentioned in table. I.

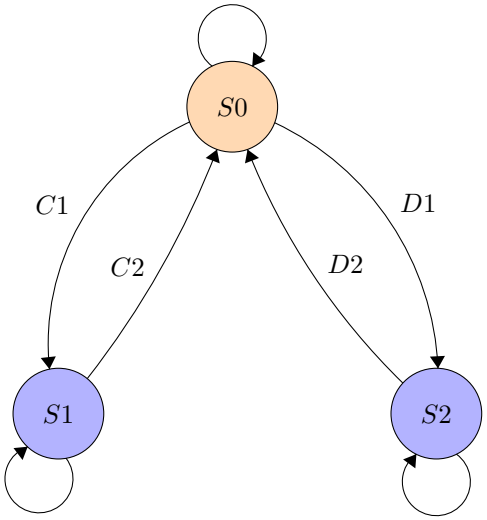


Fig. 3: control state diagram

TABLE I: state description

states	
S0	PWM blocking
S1	Charging
S2	discharging

The edges of the state transition diagram indicated the transition between the states. Edge C_1 indicates the transition from PWM blocking to charging mode and edge D_1 indicates the transition from PWM blocking state to discharging mode. As mentioned earlier the transition from charging to discharging mode happens via the PWM blocking state (as described by the edges C_2 and D_1) and similarly, the transition from discharging to charging state happens through PWM blocking state (as described by the edges D_2 and C_1).

III. Design of current controller

The control structure of the bidirectional DC/DC converter depends entirely on the intended application. In applications such as back up support [6], the overall control involves two control loops namely the inner current control loop and the outer voltage control loop. On the other hand, in applications such as microgrid and electric vehicle applications, the voltage support comes from the primary source/grid and the overall control involves only the current control. In both kind of applications, the current control loop is present and in this paper, we investigate the impact of non-linearities on the performance of DC/DC converters by considering only the current control loop. Furthermore, even in backup support applications, the effect of non-idealities appear only in the inner current control loop. The control structure of the current control loop is shown in Fig. 4.

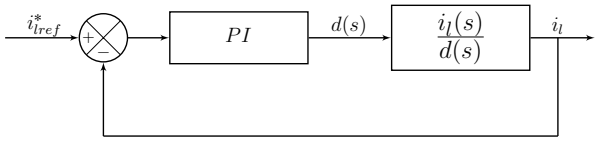
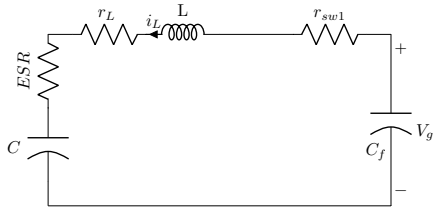


Fig. 4: current control block diagram

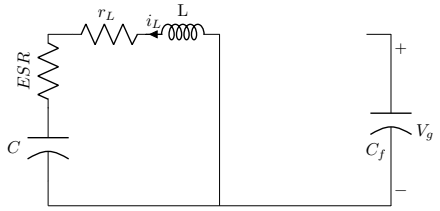
The required transfer function $\frac{i_l(s)}{d(s)}$, can be computed using the state space averaging approach.

A. Transfer function $\frac{i_l(s)}{d(s)}$ during charging mode

The equations describing the states of DC/DC converter (i.e. the inductor current and capacitor voltage) during charging mode with switch sw_1 turned ON (equivalent circuit shown in Fig. 5(a)) are given by



(a) Switch ON



(b) Switch OFF

Fig. 5: Equivalent circuits of the converter during charging

$$\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}(V_g - V_{uc} - V_{sw1} - (r + r_{sw1})i_L)\\ \frac{dv_{uc}}{dt} &= \frac{i_L}{C_{uc}}\end{aligned} \tag{14}$$

where r_{sw1} is the ON state resistance of the switch $sw1$. Similarly, when switch $sw1$ is OFF (equivalent circuit shown in Fig. 5(b)), the state equations of the DC/DC converter are given by

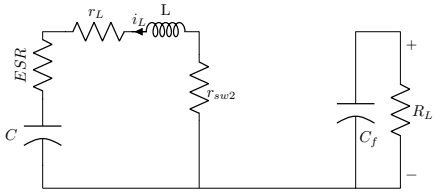
$$\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}(-ri_L - V_{uc} - V_{d2})\\ \frac{dv_c}{dt} &= \frac{i_L}{C_{uc}}\end{aligned} \tag{15}$$

where V_{d2} is the voltage drop of the diode associated with switch $sw2$. Using state space averaging, the transfer function $\frac{i_l(s)}{d(s)}$ for the DC/DC converter operating in charging mode can be computed as

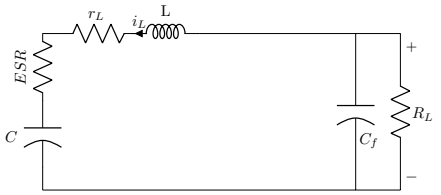
$$\frac{\widehat{i_L}(s)}{\widehat{d}(s)} = \frac{s(V_g - r_{sw1}iL)C_{uc}}{LCs^2 + (r + Dr_{sw1})C_{uc}s + 1} \tag{16}$$

B. Transfer function $\frac{i_l(s)}{d(s)}$ during charging mode

The equivalent circuits of the DC/DC converter when it is operating in discharging mode with switch $sw2$ being ON and OFF is shown in Fig. 6(a) and Fig. 6(b) respectively. When



(a) Switch ON



(b) Switch OFF

Fig. 6: Equivalent circuits of the converter during discharging

the converter switch $sw2$ is ON, the equations describing the sates of the converter are given by

$$\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}(V_{uc} - V_{sw2} - (r + r_{sw2})i_L)\\ \frac{dv_c}{dt} &= \frac{1}{C_f}\Big(\frac{-V_c}{R_L}\Big)\end{aligned} \tag{17}$$

where r_{sw2} is the ON state resistance of the switch $sw2$. Similarly, when switch $sw2$ is OFF (equivalent circuit shown in Fig. 6(b)), the state equations of the DC/DC converter are given by

$$\begin{aligned}\frac{di_L}{dt} &= \frac{1}{L}(V_{uc} - v_c - V_{d1} - ri_L)\\ \frac{dv_c}{dt} &= \frac{1}{C_f}\Big(i_L - \frac{V_c}{R_L}\Big)\end{aligned} \tag{18}$$

where V_{d1} is the voltage drop of the diode associated with switch $sw1$. Using state space averaging, the transfer function $\frac{i_l(s)}{d(s)}$ for the DC/DC converter operating in discharging mode can be evaluated as given by (19).

It is interesting to note that from (19), that the transfer function during discharging mode of operation can have zeros on the right hand side which can lead to an unstable response. The condition under which a right hand zero occurs is given by the relation

$$\frac{r_{sw2}LC_f}{2(1-D)} > R_L > \frac{r_{sw2}}{(1-D)} \tag{20}$$

If the load resistance (R_L) is in the range given by (20), the converter transfer function has right hand zero (RHZ). Therefore, the care should be taken while designing the converter.

On the contrary if the ON state resistance of the switch is neglected (as reported in [6]), the transfer function during charging and discharging mode are given by (21) and (22) respectively. It it to be noted that, while deriving the transfer functions given by (21) and (22) the ESR and the resistance of the inductance is considered.

$$\frac{\widehat{i_L}(s)}{\widehat{d}(s)} = \frac{sV_gC}{LCs^2 + RCs + 1} \tag{21}$$

$$\frac{\widehat{i_L}(s)}{\widehat{d}(s)} = \frac{V_c}{R_L(1-D)^2}\frac{[sR_LC_f + 2]}{\frac{LC_f}{(1-D)^2}s^2 + \frac{L}{(1-D)^2R_L}s + 1} \tag{22}$$

It can be observed that if the ON state resistance of the MOSFET is neglected, the right hand zero that is existing in the actual system cannot be detected.

C. Design of PI controllers

In this work, the PI controllers are designed using the approach reported in [7], [8]. Since the main objective of this work is to indicate the effect of non-idealities on the performance of the DC/DC converter, the tuning is carried out based on transfer functions given by (21) and (22). The design considerations adopted while tuning the controller are the system stability, bandwidth and steady state error and the design is carried out using frequency domain approach.

IV. Simulation and Experimental Analysis

In this section, simulation studies carried out on a 250 W UC based bidirectional DC/DC converter (whose specifications are given in Table II) are reported with an objective to demonstrate the effect of non-idealities. The impact of ON

TABLE II: Converter specifications

Parameters		
Converter rating P_{max}	250	W
UC stack capacitance	15	F
UC stack ESR	0.14	Ω
Filter inductor (L)	2	mH
Filter capacitor (C_f)	2200	μF
switching frequency (f_s)	10	kHz

$$\frac{\widehat{i}_L(s)}{\widehat{d}(s)} = \frac{V_c}{R_L} \frac{s(R_L C_f - \frac{r_{sw2C_f}}{(1-D)}) + 2 - \frac{r_{sw2}}{R_L(1-D)}}{LC_f s^2 + s(rC_f + Dr_{sw2}C_f + \frac{L}{R_L}) + \frac{r+Dr_{sw2}}{R_L} + (1-D)^2} \tag{19}$$

state resistance of the MOSFET on the frequency response of the DC/DC converter, when operated in charging and discharging mode is shown in Fig. 7 and Fig. 8 respectively. It can be observed from the frequency response plots that,

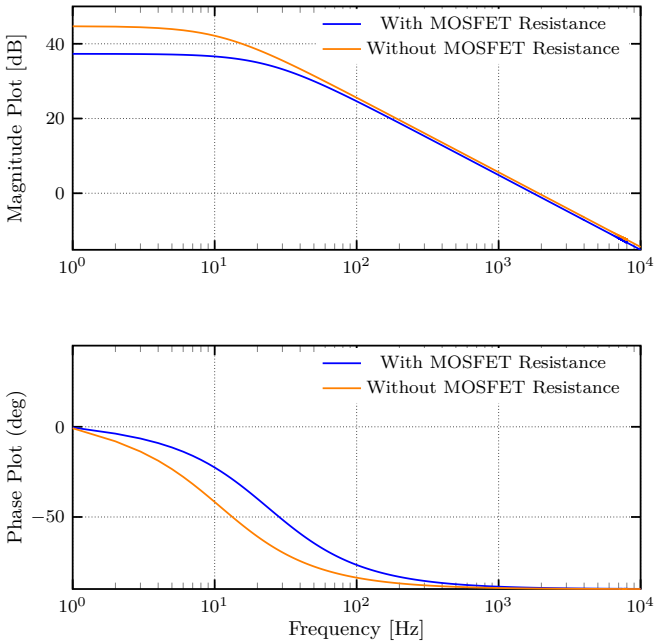


Fig. 7: Frequency response of the converter operating in charging mode

the ON state resistance reduces the gain (in both the charging and discharging modes of operation) of the DC/DC converter and the reduction is more pronounced at lower frequencies. If the switching frequency is quite high, then designing of converter neglecting the ON state resistance will have very little impact. However, in applications requiring fast control, designing the controller based on transfer function considering ON state resistance would be more efficient. The transfer function of the PI controller designed based on the transfer function neglecting the ON state resistance (using the approach presented in [7], [8]) for charging and discharging modes of operation is given by (23).

$$K_p + \frac{K_i}{s} = 0.573\left(1 + \frac{10}{s}\right) \tag{23}$$

In order to test the performance of the converter in the absence of right hand zero, the simulation is carried out by choosing the reference value of current while charging and discharging to be 10A. The response (i.e. inductor current, voltage across the UC stack and the switching pulses) of the converter during charing and discharging modes is shown in Fig. 9(a) and Fig. 9(c). In order to validate the designed controller, a laboratory based hardware setup comprising of

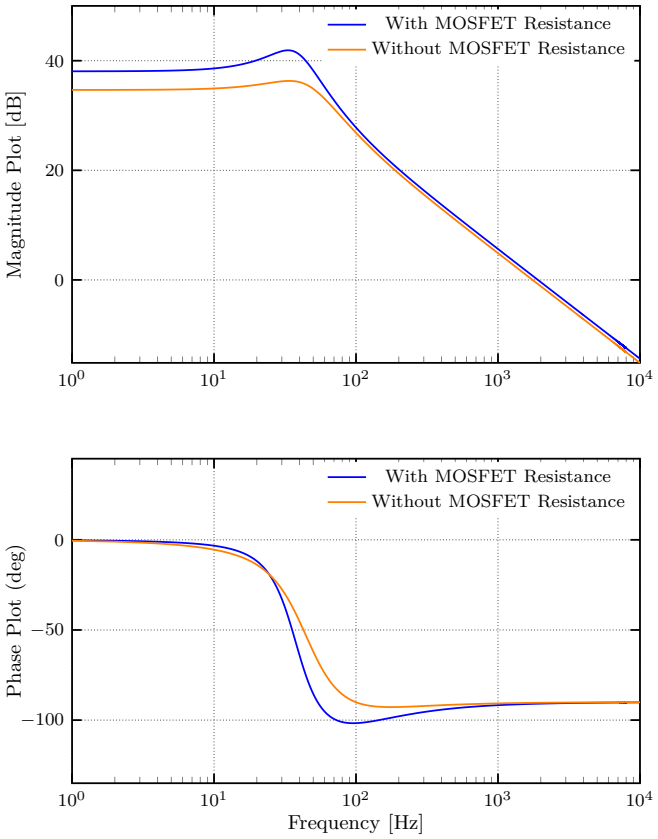
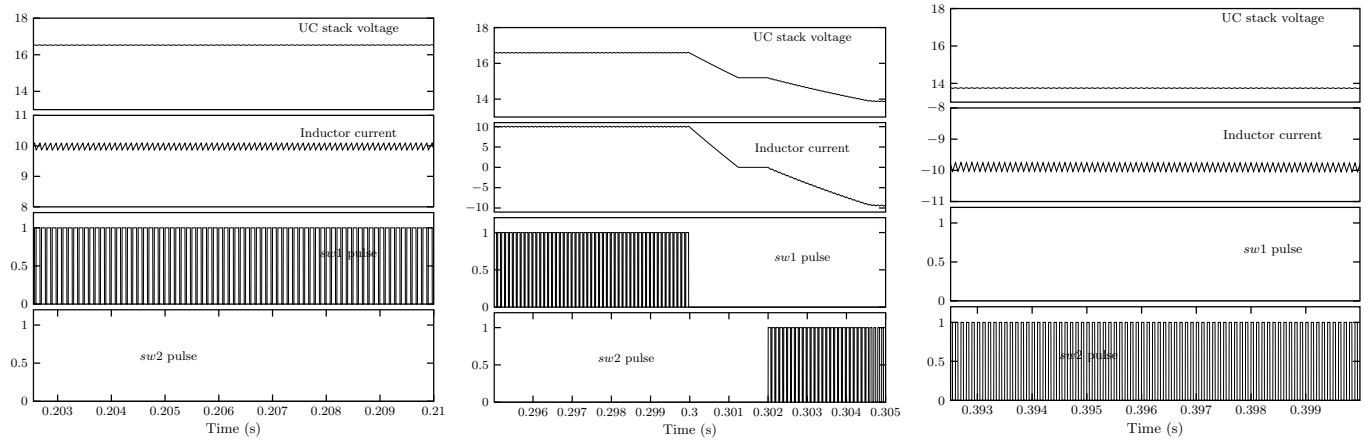


Fig. 8: Frequency response of the converter operating in discharging mode

the UC sack, bidirectional DC/DC converter and a battery is designed. The battery acts a source during charging of UC stack and also acts as a sink during discharging of UC stack. However, in the experimental evaluation, the reference values for charging and discharging current is chosen to be 1 A. The response of the converter during charging and discharging is shown in shown in Fig. 10(a) and Fig. 10(c) respectively.

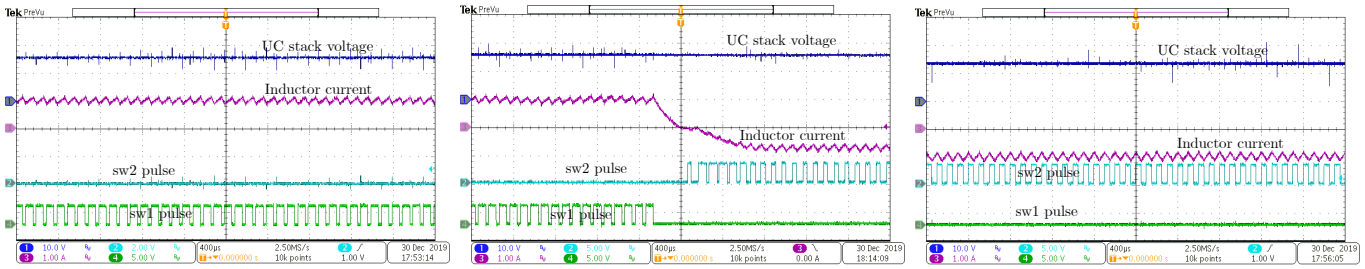
During the transition from charging to discharging, the converter goes through the blocking state where in the PWM pulses to both the switches are blocked (see Fig. 9(b) and Fig. 10(b)). For the simulation case study, the PWM blocking period calculated based on (13) (which is around $2ms$ with $V_{uc}(i) = 10V$) is is constant with that obtained using simulation.

In order to study the impact of non-idealities, the value of load resistance for which a right hand zero can occur is computed using (20). For the converter under consideration, our observation is that, the zero on the right hand side occurs when the load resistance is very small i.e. $R_L = 0.13\Omega$. The response of the converter transfer function (in discharging mode of operation) under this operating condition is shown in Fig. 11.



(a) Charging period (b) Transition period (c) Discharging period

Fig. 9: Bidirectional DC/DC converter simulation results



(a) Charging period (b) Transition period (c) Discharging period

Fig. 10: Bidirectional DC/DC converter hardware results

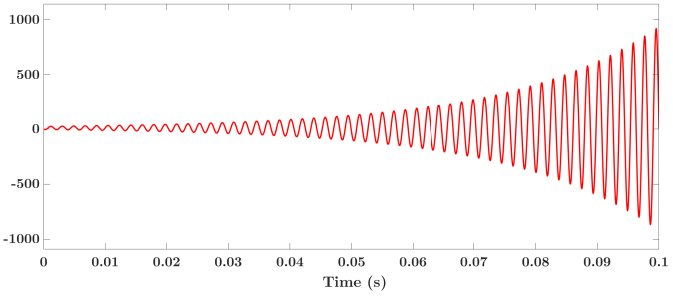


Fig. 11: The system response with RHZ

V. Conclusion

This paper investigates the effect of non-idealities on the performance of bidirectional DC/DC converter. Among the various non-idealities present in the circuit, it is observed that only the ON state resistance of the switches have an impact on the performance. The presence of ON state resistance creates a RHZ in the transfer function which can result in an unstable response under certain operating conditions. An analytical expression for identifying the operating conditions under which a RHZ can occur is derived. Our observation is that an unstable response due to non-idealities can occur when the load resistance is very low and for most of the grid connected applications (where the load resistance is typically high), the non-idealities do not have a significant impact.

References

[1] M. C. Joshi, S. Samanta, and G. Srungavarapu, "Frequency sharing based control of batteryultracapacitor hybrid energy system in the presence of delay," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 11, pp. 10 571–10 584, Nov 2019.

[2] M. C. Joshi and S. Samanta, "Modified ultracapacitor voltage control loop for batteryuc hess," in *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec 2018, pp. 1–5.

[3] R. L. Spyker and R. M. Nelms, "Classical equivalent circuit parameters for a double-layer capacitor," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 36, no. 3, pp. 829–836, July 2000.

[4] Amal S., R. V. Chacko, Sreedevi M.L, Mineeshma G.R, and Vishnu V., "Modelling of ultracapacitor and power management strategy for the parallel operation of ultracapacitor and battery in electric vehicle configuration," in *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec 2016, pp. 1–6.

[5] K. Saichand and V. John, "Generalized design of passive components for ultracapacitor based bidirectional dc-dc converters," in *2016 IEEE Annual India Conference (INDICON)*, Dec 2016, pp. 1–6.

[6] K. saichand and V. John, "Pwm block method for control of an ultracapacitor-based bidirectional dc–dc backup system," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4126–4134, Sep. 2016.

[7] M. C. Joshi and S. Samanta, "Average current mode control of batteryultracapacitor hybrid energy system its microcontroller based implementation," in *2018 IEEMA Engineer Infinite Conference (eTechNxT)*, March 2018, pp. 1–6.

[8] F. Pellitteri, V. Castiglia, P. Livreri, and R. Miceli, "Analysis and design of bi-directional dc-dc converters for ultracapacitors management in evs," in *2018 Thirteenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, April 2018, pp. 1–6.