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Low-frequency Noise in Vertical InAs/InGaAs Gate-all-around MOSFETs at 15 K for Cryogenic Applications

Mamidala Saketh Ram, Johannes Svensson, Sebastian Skog, Sofie Johannesson, and Lars-Erik Wernersson

***Abstract*— Low-frequency noise (LFN), or 1/*f*-noise, can be used effectively to evaluate device reliability which is a major concern in analog as well as digital circuits. In this work, we present 1/*f*-noise characterization of vertical InAs/InGaAs gate-all-around (GAA) MOSFETs with a 70-nm gate length (L_G) measured at cryogenic temperatures down to 15 K. The measurements at cryogenic temperatures reveal that the physical mechanism of 1/*f*-noise changes from carrier number fluctuations at 300 K to mobility fluctuations at 15 K. We conclude that the channel conduction at 15 K is dominated by the nanowire core instead of the nanowire surface due to the effect of the border and interface traps freezing out. Vertical InAs/InGaAs GAA MOSFETs at 15 K, due to reduced surface scattering, exhibit a low value of Hooge parameter, $\alpha_H \sim 5 \times 10^{-6}$ and also have a low input-referred gate voltage noise spectral density, $S_{VG} = 4.3\ \mu V^2\ \mu m^2\ Hz^{-1}$ that are important for reliable cryogenic circuit applications.**

***Index Terms*— Low-frequency noise, 1/*f*-noise, III-V, cryogenic, InAs/InGaAs, gate-all-around MOSFET, vertical nanowire.**

I. Introduction

Low frequency noise (LFN) is a dominant source of noise in modern electronic circuits including qubits for quantum computing [1-2]. Similarly, at extremely scaled nodes, MOSFETs are also affected by 1/*f*-noise due to charge trapping and de-trapping at the channel/high-*k* interface [3, 4].

The recent International roadmap for devices and systems (IRDS) identified the gate-all-around (GAA) MOSFETs as a promising candidate to extend Moore's law beyond the currently used finFETs [5]. The vertical GAA MOSFET provides more room for ohmic contacts and spacer layers, due to its vertical geometry, while reducing the power consumption by 10-15 % in the 7-nm technology node [6].

The favorable transport properties of III-V materials such as high mobility enables supply voltage scaling beyond that of Si [7-9]. A lower supply voltage combined with reduced OFF-state leakage currents is highly beneficial for cryogenic applications where the cooling power is limited. It also provides an opportunity to move some of the circuits inside the cryostat to manage the exponential increase in input/output cables. Recently, a lateral nanowire InGaAs MOSFET network based demultiplexer for qubit biasing was demonstrated at cryogenic temperatures [10]. Therefore, for future cryogenic applications, it is important to evaluate the noise properties of III-V GAA MOSFETs at low temperatures.

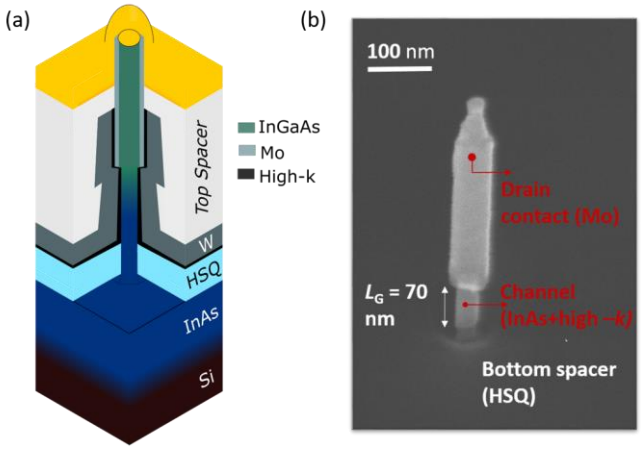

Fig. 1. (a) Cross-sectional illustration of a vertical InAs/InGaAs GAA MOSFET showing the different contacts and separation layers (b) A SEM image of the InAs/InGaAs vertical GAA MOSFET with L_G = 70-nm and W_{NW} = 27-nm post gate dielectric deposition.

LFN is widely used as a technology quality metric for transistors to evaluate material quality as well as transport properties. To address the lack of LFN characterization at cryogenic temperatures, recently, cryogenic 1/*f* characterization for fully-depleted silicon-on-insulator (FDSOI) MOSFETs was reported [11]. There have been reports on LFN for III-V nanowire MOSFETs at room temperature, but to the best of our knowledge, none yet at cryogenic temperatures [4, 13-16]. In this work, we present low-frequency noise characterization at temperatures down to 15 K where we demonstrate that the dominant mechanism of 1/*f*-noise in vertical InAs/InGaAs GAA MOSFETs changes from border and interface trap induced number fluctuations to mobility fluctuations originating from the nanowire core.

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M.S. Ram, J. Svensson, S. Skog, S. Johannesson, and L.-E. Wernersson are with the Department of Electrical and Information Technology, Lund University, 221 00 Lund, Sweden (e-mail: saketh_ram.mamidala@eit.lth.se).

II. DEVICE FABRICATION

A cross-sectional illustration and a scanning-electron-microscope (SEM) image of the fabricated III-V vertical GAA MOSFET with gate length (L_G) of 70-nm and gate width (W_{NW}) of 27-nm is shown in Fig. 1. The process starts by first growing a 300-nm-thick InAs buffer layer on a Si substrate. The vertical nanowires are then grown by Vapor-Liquid-Solid (VLS) growth where electron beam lithography (EBL) patterned Au seed particles are used as nanowire nucleation sites. A similar growth scheme was implemented in ref. [17]. The drain top metal-contact height is defined by first spin coating a hydrogen silsesquioxane (HSQ) film and then by using EBL. The drain contact is made up of 20-nm-thick Mo and 1.5-nm-thick TiN that are anisotropically etched away on the horizontal surface using reactive-ion-etching (RIE) so that the metal only remains on the vertical nanowire sidewalls. The HSQ layer is then etched away using a buffered-oxide-etch (BOE) solution.

A gate length of 70-nm is defined using a gate-last process [18]. The doped shell around the channel is removed using a digital etch process in which the shell is oxidized using ozone and then etched in a HCl:IPA solution. For the gate dielectric, an Al_2O_3/HfO_2 bilayer was deposited using ALD which resulted in an EOT of 1.5-nm. The gate-metal comprising of a 2-nm-thick TiN and 60-nm-thick W is deposited using ALD and sputtering. The 2-nm-thick TiN is used for better step coverage. The fabrication is then completed by depositing a top spacer layer, etching vias to contacts and final metallization using Ni/Au contacts (10-nm/100-nm).

III. ELECTRICAL CHARACTERIZATION AND ANALYSIS

DC characterization of the vertical InAs/InGaAs GAA MOSFETs was performed with an Agilent B1500 parameter analyzer. The output characteristics at room temperature for the vertical InAs/InGaAs GAA MOSFET is shown in Fig. 2(a). It can be noted that there are kinks in the drain-to-source current (I_{DS}) for instance when the gate-to-source voltage, V_{GS} = 0.4 V and drain-to-source voltage, V_{DS} > 0.4 V. For vertical MOSFETs without implementing a field-plate and using InGaAs on the drain side, a destructive breakdown in the OFF-state (V_{GS} = - 0.2 V) typically occurs at V_{DS} = 0.7 V [17, 18]. The kinks in I_{DS} observed in Fig. 2(a), when V_{DS} > 0.4 V are signs of increasing impact-ionization and band-to-band-tunneling (BTBT). It has also been shown that the onset of impact-ionization and BTBT can be extended beyond 1.0 V by introducing a vertical field-plate on the drain side [18]. Fig. 2(b) show the transfer characteristics with temperatures ranging from 300 K to 15 K, respectively, for the vertical InAs/InGaAs GAA MOSFET. A V_{DS} of 50 mV to measure the transfer characteristics was chosen as it is a typical bias for low-frequency noise measurements [11, 14, 15]. With decreasing T, the absolute value of the threshold voltage (V_{TH}) shifts towards higher values by ≈ 0.5 mV/K (Fig. 2(c)) which is comparable to Si n-channel MOSFETs and an improvement over previously reported InAs/HfO_2 nanowire MOSFETs [11-13]. Fig. 2(d) shows the inverse subthreshold slope (SS), $\partial V_{GS}/\partial(\log I_{DS})$ as a function of I_{DS} for four temperatures. It can be noted that the SS decreases to 36 mV/dec at 15 K at which the LFN characterization is performed.

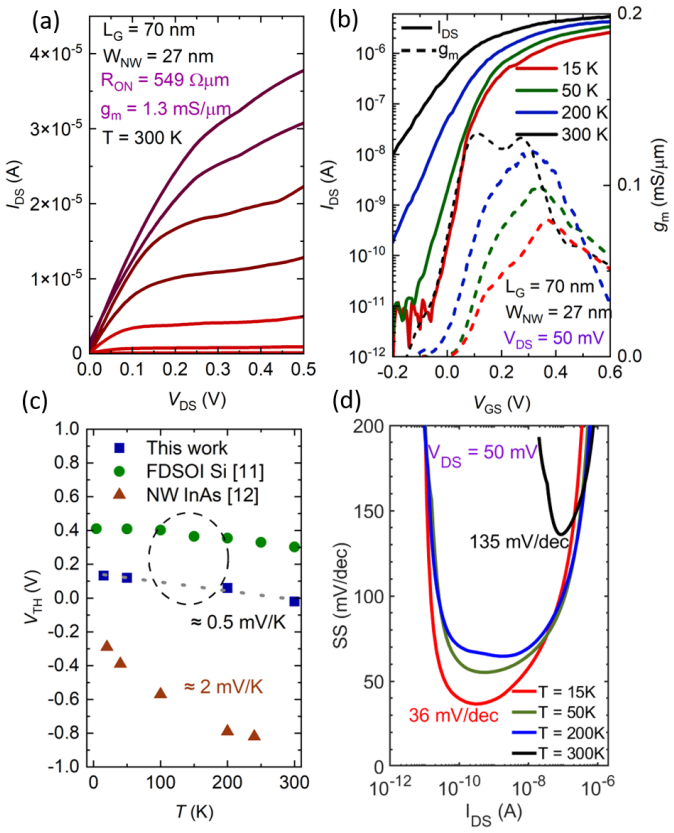

Fig. 2. (a) Output characteristics (-0.2 V < V_{GS} < 0.6 V, ΔV_{GS}= 0.1 V) at 300 K for a vertical InAs/InGaAs GAA MOSFET with R_{ON} = 549 Ωμm and measured g_m = 1.3 mS/μm at V_{DS} = 0.5 V and (b) Transfer characteristics measured at different temperatures with V_{DS} = 50 mV (c) V_{TH} versus T and (d) Inverse subthreshold slope versus T at V_{DS} = 50 mV for an InAs/InGaAs NW MOSFET.

For the LFN measurements, a low-noise preamplifier was used to supply a constant V_{DS} = 50 mV and the current noise power spectral density (PSD) was measured using a lock-in amplifier. A similar setup was used in our previous LFN reports [4, 14, 15]. The frequency was swept between 1 Hz

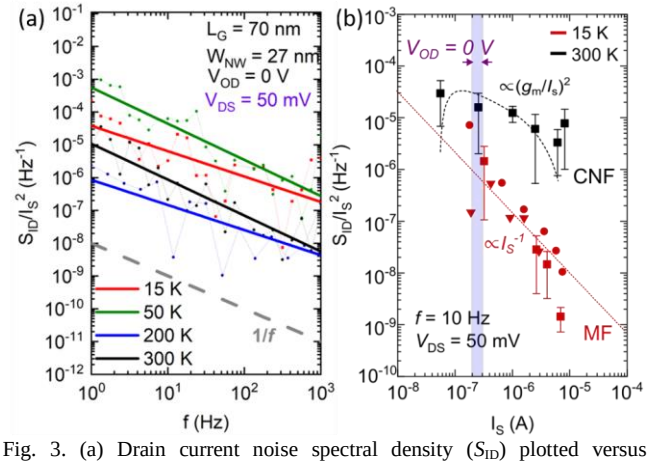

Fig. 3. (a) Drain current noise spectral density (S_{ID}) plotted versus frequency at different temperatures for a InAs/InGaAs vertical GAA MOSFET (b) S_{ID}/I_S^2 measured at a fixed frequency of 10 Hz at T= 300 K and T = 15 K. Three different devices indicated by circle, square and triangle markers were measured at 15 K.

and 1 KHz and the temperature was varied from 300 K to 15 K. At every temperature point, a gate voltage (V_{GS}) was applied so that the overdrive voltage ($V_{OD} = V_{GS} - V_{TH}$) was zero [11].

The $1/f^{\gamma}$ -noise behavior where $\gamma = -\partial \ln S_{ID}/\partial \ln f$ for different temperatures are shown in Fig. 3(a). It can be confirmed that the measured drain current noise spectral density (S_{ID}) has a typical $1/f^{\gamma}$ dependency at all measured temperatures with γ ranging from 0.8 to 1.1. A gamma value typically in the obtained range ~ 1 indicates a distribution of traps in the oxide which is uniform in depth [19, 20]. However, no strong dependence of LFN magnitude on temperature was observed in the $1/f$-noise characteristics when biased at $V_G = V_{OD} = 0$ V. This can be explained from Fig. 3(b), where S_{ID} when biased at $V_{OD} = 0$ V, is similar for both temperatures. Whereas, when biased at $V_{OD} > 0$ V, a clear reduction in S_{ID} at $T = 15$ K can be noted from Fig. 3(b).

The two mechanisms that generally explain the LFN in MOSFETs are carrier number fluctuations (CNF) and mobility fluctuations (MF). CNF arise from border traps present in the gate dielectric, whereas MF are caused due to electron-phonon scattering within the channel often described with the material dependent Hooge model. The mechanisms can be identified by measuring the current noise spectral density (S_{ID}) as a function of source current (I_S). When S_{ID}/I_S^2 is proportional to $1/I_S$, the LFN is expected to originate from MF. Instead, when S_{ID}/I_S^2 is proportional to the transconductance squared (g_m^2/I_S^2), the LFN is expected to arise from CNF [21]. To identify the noise mechanism in InAs/InGaAs vertical GAA MOSFETs, extended measurements where each data point is the average of 50 measurements repeated 5 times, were carried out at a frequency of 10 Hz. Interestingly, it can be noted from Fig. 3(b) , that the mechanism of LFN in InAs/InGaAs vertical GAA MOSFETs changes from carrier number fluctuations to mobility fluctuations when the temperature is reduced from 300 K to 15 K. This can be attributed to the current conduction being dominant at the nanowire surface at 300 K where the transport is more sensitive to charge trapping/de-trapping. On the other hand, when the temperature is reduced to 15 K, the conduction is mainly through the nanowire core due to the freezing out of the border traps. Notably, surface and core conduction modes were also previously observed at room temperature where the III-V vertical GAA MOSFET showed core conduction when biased below V_{TH} and surface conduction above V_{TH} [16].

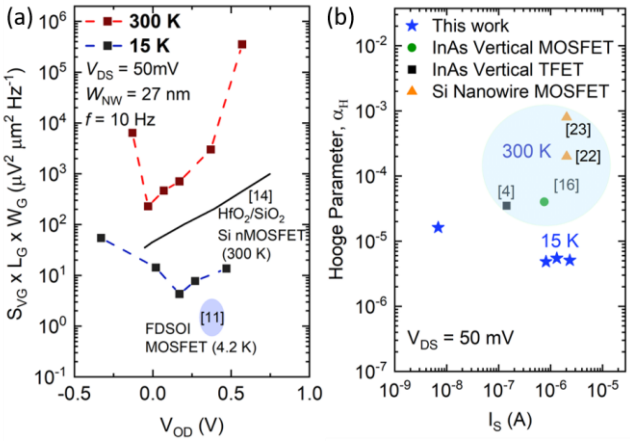

Fig. 4. (a) Input referred voltage noise power spectral density (S_{VG}) normalized with the gate area for an InAs/InGaAs NW MOSFET (b) Calculated Hooge parameter for InAs/InGaAs vertical GAA MOSFET at 15 K and other nanowire technologies at 300 K.

Fig. 4 (a) shows the input-referred gate voltage noise spectral density (S_{VG}). It is a commonly used metric that represents the minimum signal amplitude that can be amplified by the transistor [14]. At cryogenic temperatures, when compared to 1–µm-long FDSOI MOSFETs measured at 4.2 K, the InAs/InGaAs vertical GAA MOSFETs have comparable S_{VG}. The Hooge parameter (α_H) at 15 K for the InAs/InGaAs vertical GAA MOSFETs having a gate width, W_{NW} = 27-nm was calculated using (1) to be 5×10^{-6},

$$S_{ID}/I_S^2 = q\mu_{eff}\alpha_H V_{DS}/L_G^2 f I_S \qquad (1)$$

where q is the elemental charge, μ_{eff} the effective channel mobility, and f the frequency. The effective mobility (μ_{eff}) at 300 K was extracted from the virtual source (VS) model to be 1300 cm^2/Vs [24]. From Fig. 4 (b), it can be noted that the Hooge Parameter at 15 K improves by at least a factor of 10 when compared to previously reported α_H values for various nanowire FET technologies at room temperature. The presence of occupied trap sites close to the III-V/High-k interface result in increased surface scattering [25]. The lowering of α_H indicates a reduction in surface scattering caused by occupied trap sites due to freezing out of border traps close to the nanowire surface which is advantageous for cryogenic applications. It is also known that the III-V/ High-k interface is improved when a bilayer gate dielectric (Al_2O_3/HfO_2) is used to passivate the III-V surface [14]. The minimum border trap density (N_{bt}) for the InAs/InGaAs vertical GAA MOSFET was determined as in ref. [16] to be 2×10^{19} cm^{-3} eV^{-1} which is not too far away from previously reported N_{bt} values for planar Si MOSFETs with HfO_2 gate oxides and a SiO_2 interface layer [14]. Our results indicate the InAs/InGaAs vertical GAA MOSFETs to be an attractive option to be used in emerging III-V cryogenic circuits.

IV. CONCLUSION

In this work, we report cryogenic $1/f$-noise behavior in a InAs/InGaAs vertical GAA MOSFET. We have observed at 300 K that carrier number fluctuations are the dominant source of LFN resulting from the dielectric border traps. Whereas, at 15 K, the conduction is less surface sensitive and the LFN is dominated by mobility fluctuations having a low $\alpha_H = 5 \times 10^{-6}$. Our experimental findings contribute to III-V vertical nanowire MOSFET design aimed towards low temperature applications.

REFERNCES

[1] M. Kamada, A. Laitinen, W. Zeng, M. Will, J. Sarkar, K. Tappura, H. Seppa, P. Hakonen, "Electrical Low-Frequency 1/f$^{\gamma}$ Noise Due to Surface Diffusion of Scatterers on an Ultra-low-Noise Graphene Platform", *Nano Letters*, vol. 21, no. 18, pp. 7637-7643, 2021. Available: 10.1021/acs.nanolett.1c02325.

[2] S. Anton, C. Nugroho, J. Birenbaum, S. O'Kelley, V. Orlyanchik, A. Dove, G. Olson, Z. Yoscovits, J. Eckstein, D. Harlingen, J. Clarke , "Low-frequency critical current noise in Josephson junctions induced

by temperature fluctuations", *Applied Physics Letters*, vol. 101, no. 9, p. 092601, 2012. Available: 10.1063/1.4749282.

[3] H. Zhu, B. Ye, C. Tang, X. Li, Q. Sun and D. W. Zhang, "Improving Low-Frequency Noise in 14-nm FinFET by Optimized High-k/Metal Gate Thermal Processing," in *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1112-1115, Aug. 2021, doi: 10.1109/LED.2021.3091488.

[4] M. Hellenbrand, E. Memišević, M. Berg, O. Kilpi, J. Svensson and L. -E. Wernersson, "Low-Frequency Noise in III–V Nanowire TFETs and MOSFETs," in *IEEE Electron Device Letters*, vol. 38, no. 11, pp. 1520-1523, Nov. 2017, doi: 10.1109/LED.2017.2757538.

[5] *International Roadmap for Devices and Systems (IRDS)–More Moore*, *IEEE* Standard 27, 2022.

[6] D. Yakimets, G. Eneman, P. Schuddinck, T. Huynh Bao, M. G. Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A. Voon-Yew Thean, and K. De Meyer, "Vertical GAAFETs for the ultimate CMOS scaling, "*IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1433–1439, May 2015, doi: 10.1109/ted.2015.2414924.

[7] O. Kilpi, M. Hellenbrand, J. Svensson, A. Persson, R. Lind, and L. -E. Wernersson, "High-performance vertical III-V nanowire MOSFETs on Si with gm > 3 mS/μm," *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1161–1164, Aug. 2020, doi: 10.1109/led.2020.3004716.

[8] M.S. Ram, K. -M. Persson, A. Irish, A. Jönsson, R. Timm and L. –E. Wernersson, "High-density logic-in-memory devices using vertical indium arsenide nanowires on silicon", *Nature Electronics*, vol. 4, no. 12, pp. 914-920, 2021. Available: 10.1038/s41928-021-00688-5.

[9] X. Zhao, C. Heidelberger, E. A. Fitzgerald, W. Lu, A. Vardi and J. A. del Alamo, "Sub-10-nm-Diameter InGaAs Vertical Nanowire MOSFETs: Ni Versus Mo Contacts," in *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3762-3768, Sept. 2018, doi: 10.1109/TED.2018.2859202.

[10] L. Södergren, P. Olausson and E. Lind, "Low-Temperature Characteristics of Nanowire Network Demultiplexer for Qubit Biasing", *Nano Letters*, vol. 22, no. 10, pp. 3884-3888, 2022. Available: 10.1021/acs.nanolett.1c04971.

[11] B. Cardoso Paz, M. Cassé , C. Theodorou, G. Ghibaudo , T. Kammler, L. Pirro, M. Vinet, S. Franceschi, T. Meunier, F. Gaillard, "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.

[12] H. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlström and L.-E. Wernersson, "Temperature dependent properties of InSb and InAs nanowire field-effect transistors", *Applied Physics Letters*, vol. 96, no. 15, p. 153505, 2010. Available: 10.1063/1.3402760.

[13] G. Holloway, C. Haapamaki, P. Kuyanov, R. LaPierre and J. Baugh, "Electrical characterization of chemical and dielectric passivation of InAs nanowires", *Semiconductor Science and Technology*, vol. 31, no. 11, p. 114004, 2016. Available: 10.1088/0268-1242/31/11/114004.

[14] M. Hellenbrand, O. Kilpi, J. Svensson, E. Lind and L. -E. Wernersson, "Low-frequency noise in nanowire and planar III-V MOSFETs", *Microelectronic Engineering*, vol. 215, p. 110986, 2019. Available: 10.1016/j.mee.2019.110986.

[15] K. -M. Persson, E. Lind, A. W. Dey, C. Thelander, H. Sjöland and L. -E. Wernersson, "Low-Frequency Noise in Vertical InAs Nanowire FETs," in *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 428-430, May 2010, doi: 10.1109/LED.2010.2043637.

[16] K. -M. Persson, B. Malm and L. -E. Wernersson, "Surface and core contribution to 1/f-noise in InAs nanowire metal-oxide-semiconductor field-effect transistors", *Applied Physics Letters*, vol. 103, no. 3, p. 033508, 2013. Available: 10.1063/1.4813850.

[17] O.-P. Kilpi, J. Svensson, J. Wu, A. Persson, R. Wallenberg, E. Lind, and L.-E. Wernersson, "Vertical InAs/InAs/InGaAs heterostructure metal–oxide– semiconductor field-effect transistors on Si," *Nano Lett.*, vol. 17, no. 10, pp. 6006–6010, 2017, doi: 10.1021/acs.nanolett.7b02251.

[18] O. –P. Kilpi, S. Andric, J. Svensson, M. S. Ram, E. Lind and L. –E. Wernersson, "Increased Breakdown Voltage in Vertical Heterostructure III-V Nanowire MOSFETs With a Field Plate", IEEE Electron Device Letters, vol. 42, no. 11, pp. 1596-1598, 2021. Available: 10.1109/led.2021.3115022.

[19] W. Shin, J. –H. Bae, S. Kim, K. Lee, D. Kwon, B. –G. Park, D. Kwon, J. –H. Lee , "Effects of High-Pressure Annealing on the Low-Frequency Noise Characteristics in Ferroelectric FET", *IEEE Electron Device Letters*, vol. 43, no. 1, pp. 13-16, 2022. Available: 10.1109/led.2021.3127175.

[20] M. Haartman and M. Östling, *Low-Frequency Noise In Advanced Mos Devices*, Dordrecht, The Netherlands: Springer, 2007.

[21] J. Kim, M. -G. Kim, A. Facchetti and S. K. Park, "Analysis of Low-Frequency Noise in Quantum Dot/Metal-Oxide Phototransistors with Metal Chalcogenide Interfaces," in *IEEE Electron Device Letters*, 2022, doi: 10.1109/LED.2022.3189605.

[22] J. Li, S. Vitusevich, M. Petrychuk, S. Pud, A. Offenhäusser and B. Danilchenko, "Advanced performance and scalability of Si nanowire field-effect transistors analyzed using noise spectroscopy and gamma radiation techniques", *Journal of Applied Physics*, vol. 114, no. 20, p. 203704, 2013. Available: 10.1063/1.4833567.

[23] T. Moh, M. Nie, G. Pandraud, L. Smet, E. Sudholter, Q. Huang, P.M. Sarro, "Effect of silicon nanowire etching on signal-to-noise ratio of SiNW FETs for (bio)sensor applications", *Electronics Letters*, vol. 49, no. 13, pp. 782-784, 2013. Available: 10.1049/el.2013.1397.

[24] A. Khakifirooz, O. Nayfeh and D. Antoniadis, "A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters", *IEEE Transactions on Electron Devices*, vol. 56, no. 8, pp. 1674-1680, 2009. Available: 10.1109/ted.2009.2024022.

[25] I. Jayawardhena, R. P. Ramamurthy, D. Morisette, A.C. Ahyi, R. Thorpe, M. A. Kuroda, L. C. Feldman and S. Dhar, "Effect of surface treatments on ALD Al2O3/4H-SiC metal–oxide–semiconductor field-effect transistors", *Journal of Applied Physics*, vol. 129, no. 7, p. 075702, 2021. Available: 10.1063/5.0040586