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A nearest level control technique for an asymmetric source configuration of multi-level inverter topology

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Abstract

In this paper, an asymmetric source configuration of Multilevel Inverter (MLI) topology has been proposed. It consists of eight unidirectional switches, two bidirectional switches and four isolated DC sources. By considering 1:5 and 1:4 source configurations, the inverter produces 25-level and 21-level outputs respectively with the same switching action. For producing negative voltage levels, there is no requirement of separate backend H-bridge and inherently produces both positive and negative voltage levels. The main advantage of this topology is that in every state, only four switches are in ON mode and else are in OFF state. It also gives less per unit Total Standing Voltage (TSV) and thereby cost requirement of semiconductor devices can become decreases. For generating gate pulses, the simple Nearest Level Control (NLC) has been used by considering the round function. This technique is basically a fundamental switching frequency technique thereby switching losses are greatly reduces as compared with high switching frequency Pulse Width Modulation (PWM) techniques and it is particularly suitable for large number of levels. With this control technique, there is no inrush current has been developed at the input of DC sources. Finally, with step change in Modulation Index (MI) values the proposed topology with two different source configurations have been validated through MATLAB/Simulink platform.

Keywords: Multilevel Inverter, Pulse Width Modulation, Nearest Level Control, Total Standing Voltage, Modulation Index

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1. Introduction

In recent years in the view of current research trend of medium voltage and high-power energy control, the multilevel inverter technology has been used very extensively as an important alternative (Rodriguez et al., 2002). The most widely used multi-level inverters are Diode clamped, Capacitor clamped and Cascaded H-bridge MLIs described in Rodriguez et al. (2002). Generally, in all multilevel inverters, the major losses are switching losses and the cost of the inverter depends on number of switching components. Hence it is a challenging task to the researchers to reduce the component count (Gupta et al., 2016). The Multi-level inverters with reduced switch count can also be used in the application of renewable energy integration to the grid and drives application. The recent topologies developed for these applications are described in Bana et al. (2019). Many different topologies of multilevel inverters exist but it is to be noted that some submodules (SMs) exist very commonly in all the topologies (Vijeh et al., 2019). In the present research trend of reducing number of switches in a multi-level inverter, even if one switch is reduced, the gate driver and few assembly parts are eliminated which reduce the cost of equipment. A newer version of multi-level inverter with a DC link MLDCL inverter described in Su (2005), which reduces almost half the number of switches. There are many Pulse width modulation techniques which are introduced for the switching control strategy of multi-level inverters such as PD (Phase disposition), UPD (Uni-polar phase disposition) and sinusoidal. The UPD PWM technique for a 7 level MLDCL inverter is described in Kumar et al. (2021) with %THD as 19.31%. Generally, an LCL filter is used to reduce the %THD below 5% according to IEEE standards. A switched capacitor based MLI using UPD technique is described in Bhanuchandar and Murthy (2021), which uses LCL filter for connecting MLI to the grid.

The other technique called Nearest level Control (NLC) technique is most widely used in multilevel inverters for high levels. The NLC technique is not preferred for low level MLIs as they generate lower order harmonics. In Meshram and Borghate (2015), the nearest level control (NLC) voltage balancing method is applied to modular multilevel converter. The new topology consisting of Multilevel modules and full bridge converter generating 125 level output is proposed in Ebrahimi et al. (2012). Multilevel inverters can be classified as Symmetrical, Asymmetrical and Modified MLIs. Generally, cascaded H-bridge (CHB) multilevel inverter gives better result with less %THD, but requires many DC sources and generates only positive voltage levels. In Pereda and Dixon (2012), an asymmetrical CHB MLI is proposed which uses only one DC source and can be applied in Electric vehicle applications. A crisscross MLI with reduced number of components is proposed in Khosroshahi (2014), which has very advanced features. A cascaded MLI with added H-Bridge in series connection can generate all voltage levels (Babaei et al., 2015). An attempt to reduce the number of individual DC sources for cascaded MLI has been done in Babaei et al. (2014). A new 53 level multilevel converter is proposed in Babaei (2008), which includes reduction in switches, losses and installation area using 22 IGBTs. A new cross connected sources (CCS) based MLI is proposed in Gupta and Jain (2014) and analyzed for both asymmetrical and symmetrical source configurations. A new topology called switch-ladder and stacked multicell converter topology for MLI has been proposed in Alishah et al. (2017), Hosseinzadeh et al. (2012) and Sharma and Kapoor (2016) for power quality applications. In this paper a new topology of an asymmetrical MLI is proposed using NLC technique with 1:5 and 1:4 source configurations with a slight change in modulation index.

In this paper, Section-2 describes proposed asymmetrical MLI topology. In Section-3, the NLC scheme is described. In Section-4 the simulation results are discussed and finally Section-5 gives conclusion.

2. Proposed Asymmetrical MLI Topology

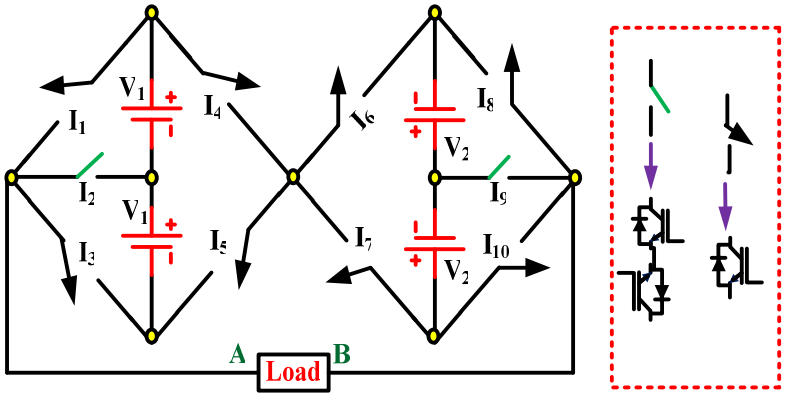

Figure 1. Proposed Asymmetrical MLI topology

The proposed asymmetrical MLI topology is shown in Figure 1. The proposed circuit consists of eight uni-directional switches and two bi-directional switches with four DC sources. With source configuration of 1:5, the peak voltage obtained as $+12V_{dc}$ and

with source configuration of 1:4, the peak voltage obtained is $+10V_{dc}$. The switching table for all the voltage levels is shown in Table 1.

The proposed topology is simulated in MATLAB/SIMULINK platform and 25-level output has been generated with 1:5 source configuration. Similarly, using the source configuration as 1:4 with same switching action, the 21-level output can be generated. To generate peak output voltage of $+12V_{dc}$ in 1:5 source configuration topology (i.e $V_1= V_{dc}$ and $V_2= 5V_1$) the switches I_1, I_5, I_7, I_8 are turned ON and remaining switches are OFF, which includes all the DC sources. Similarly, to generate the voltage level of $+6V_{dc}$ in 1:5 source configuration topology (i.e $V_1= V_{dc}$ and $V_2= 5V_1$) the switches I_2, I_5, I_7, I_9 are turned ON and remaining switches are OFF, which includes only two DC sources. The entire switching action is shown in Table 1, which includes all the voltage levels positive and negative levels from $+12V_{DC}$ to $-12V_{DC}$.

Table 1. Switching Table 1:5 source configuration

S. No	ON State Switches	Output Voltage
1	$I_2 – I_5 – I_7 – I_{10}$	$1V_{dc}$
2	$I_1 – I_5 – I_7 – I_{10}$	$2 V_{dc}$
3	$I_3 – I_4 – I_7 – I_9$	$3 V_{dc}$
4	$I_2 – I_4 – I_7 – I_9$	$4 V_{dc}$
5	$I_1 – I_4 – I_7 – I_9$	$5 V_{dc}$
6	$I_2 – I_5 – I_7 – I_9$	$6 V_{dc}$
7	$I_1 – I_5 – I_7 – I_9$	$7 V_{dc}$
8	$I_3 – I_4 – I_7 – I_8$	$8 V_{dc}$
9	$I_2 – I_4 – I_7 – I_8$	$9 V_{dc}$
10	$I_1 – I_4 – I_7 – I_8$	$10 V_{dc}$
11	$I_2 – I_5 – I_7 – I_8$	$11 V_{dc}$
12	$I_1 – I_5 – I_7 – I_8$	$12 V_{dc}$
13	$I_1 – I_4 – I_6 – I_8$	$0 V_{dc}$
14	$I_2 – I_4 – I_6 – I_8$	$-1 V_{dc}$
15	$I_3 – I_4 – I_6 – I_8$	$-2 V_{dc}$
16	$I_1 – I_5 – I_6 – I_9$	$-3 V_{dc}$
17	$I_2 – I_5 – I_6 – I_9$	$-4 V_{dc}$
18	$I_1 – I_4 – I_6 – I_9$	$-5 V_{dc}$
19	$I_2 – I_4 – I_6 – I_9$	$-6 V_{dc}$
20	$I_3 – I_4 – I_6 – I_9$	$-7 V_{dc}$
21	$I_1 – I_5 – I_6 – I_{10}$	$-8 V_{dc}$
22	$I_2 – I_5 – I_6 – I_{10}$	$-9 V_{dc}$
23	$I_1 – I_4 – I_6 – I_{10}$	$-10 V_{dc}$
24	$I_2 – I_4 – I_6 – I_{10}$	$-11 V_{dc}$
25	$I_3 – I_4 – I_6 – I_{10}$	$-12 V_{dc}$

3. NLC scheme

Generally, in any inverter the control scheme plays a vital role and these schemes control the gating signals of the switches. In this paper, the technique called Nearest level Control technique (NLC) is used to generate an output voltage of 25-levels. The scheme is explained with the control diagram and waveform synthesis shown in Figure 2. From the control diagram, it is clear that the reference signal V_{ref} (Sinusoidal) is given to the gain block of the value $V_{dc.}$ The ratio V_{ref} / V_{dc} is given to the round function which determines the nearest voltage level from which the switching logic of the inverter is derived and given as gating signals to switches. A nearest level control technique is one of important technique preferably used for high level inverters. If the NLC technique is used for low level inverters then it generates lower order harmonics which are quite difficult to eliminate. The waveform synthesis proves that the reference voltage cuts exactly at the midpoint of the staircase waveform as the $round_{0.5}$ {} function is applied.

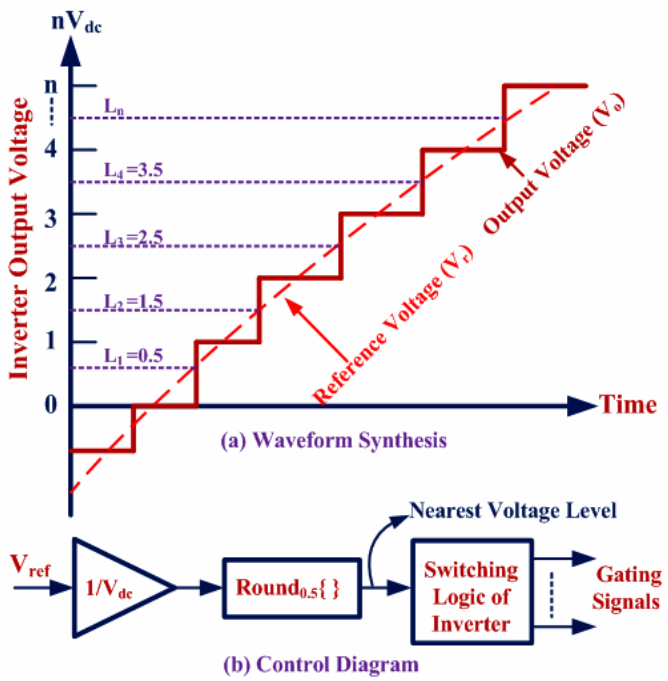

Figure 2. NLC Scheme

4. Simulation Results

Figure 3 shows the inverter input DC source currents with 1:5 source configuration. The peak value of the current is reduced suddenly if the modulation index is shifted at 0.06s. It is clear from the figure 3 that there are no huge inrush currents at the input of the inverter. Figure 4 shows the inverter output voltage and current. The generated 25- level output with peak value as $12V_{dc}$ (with V_{dc} = 20V) = 240V is shown in figure 4. After the modulation index has been shifted from 1 to 0.4 the inverter generates 11-level output with peak value as $5V_{dc}$ = 100V. The peak inverter output current at modulation index as unity is 2.398 A and at 0.06s the peak value has been reduced to 0.9953 A. The voltage and current stresses of all switches for 1:5 source configuration is shown in figure 5. The 21-level output voltage of the inverter with 1:4 source configuration is shown in figure 6. The peak voltage value of the inverter is +10 V_{dc} = 200V at modulation index as unity. The output levels of the same inverter configuration are reduced to 9 levels at 0.06s when the modulation index is shifted to 0.4 from unity. Now, the peak voltage value of the inverter is $+4V_{dc}$ = 80 V. Similarly, by referring to the inverter output current waveform from the figure 6, the peak value of the current before 0.06s is 1.996A and after 0.06s the peak current is reduced to 0.7986 A as modulation index is reduced to 0.4. The Simulation parameters are given in Table 3.

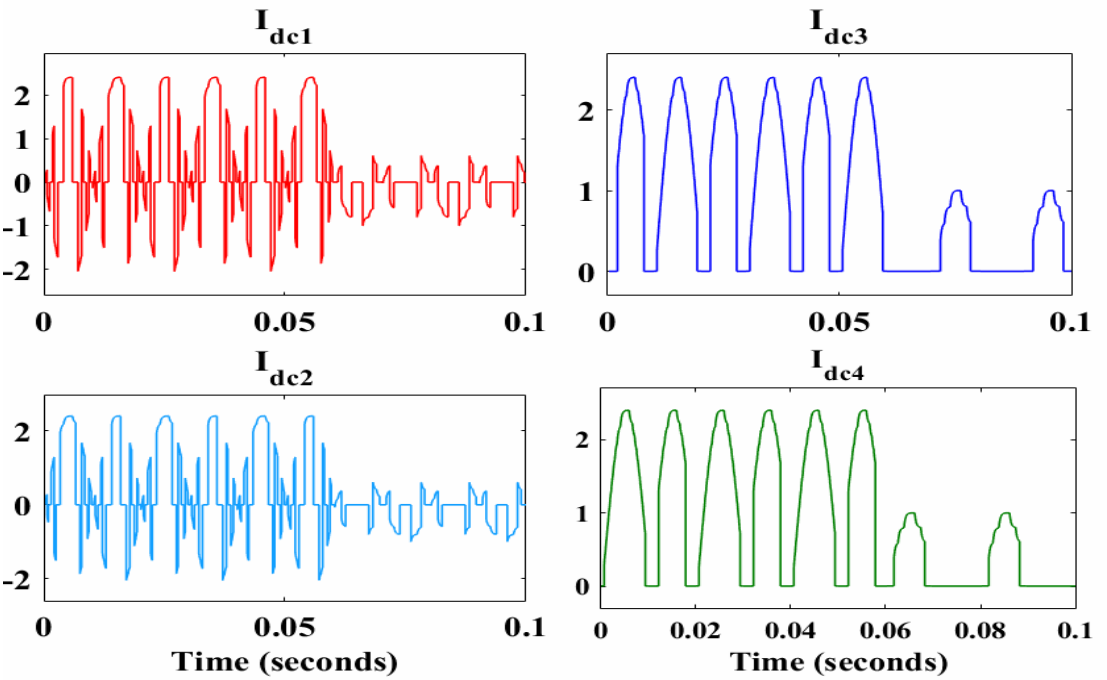

Figure 3. Inverter Input DC source currents for 1:5 source configuration with modulation index shifted from 1 to 0.4 at 0.06s

The Comparison of different asymmetrical MLI topologies is shown in Table 2, where 'p' indicates, number of levels. In Hosseinzadeh et al. (2012), the number of IGBTs required is $10\log_{17}^{p}$ where 'p' is considered as 17 levels only. The harmonic analysis is shown in figure 7, here at the fundamental frequency the inverter peak output voltage is 240.6V and %THD is 3.26% then it finally meets the IEEE1547 standards

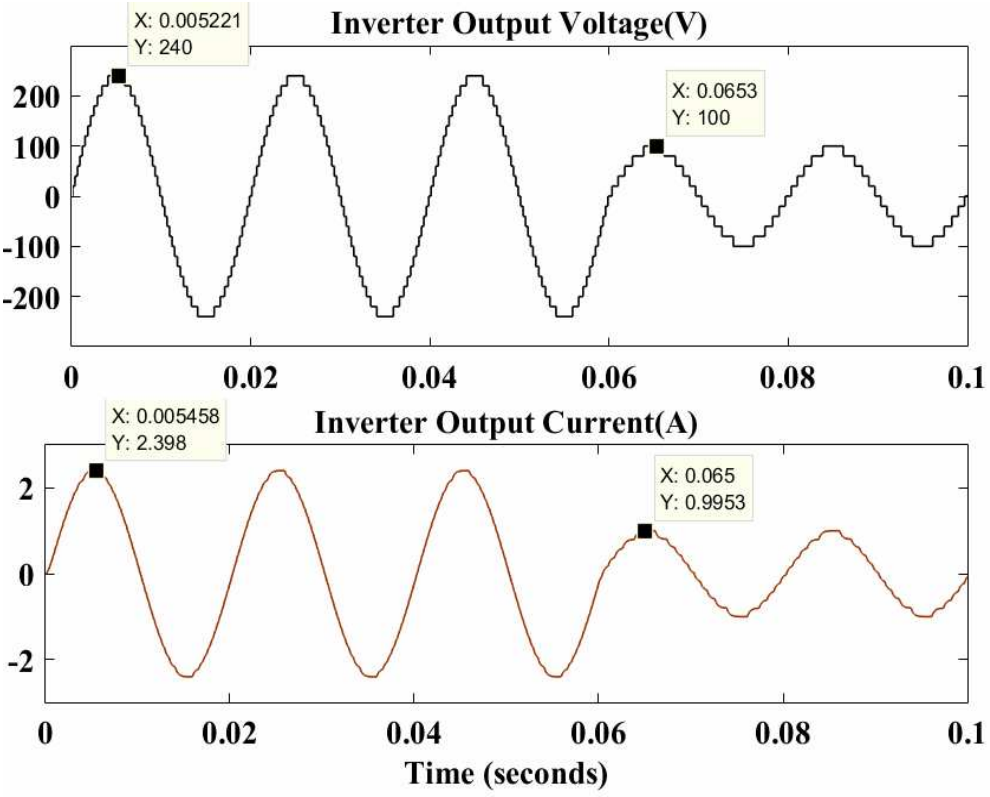

Figure 4. Inverter Output voltage and Inverter output current for 1:5 source configuration with modulation index shifted from 1 to 0.4 at 0.06s

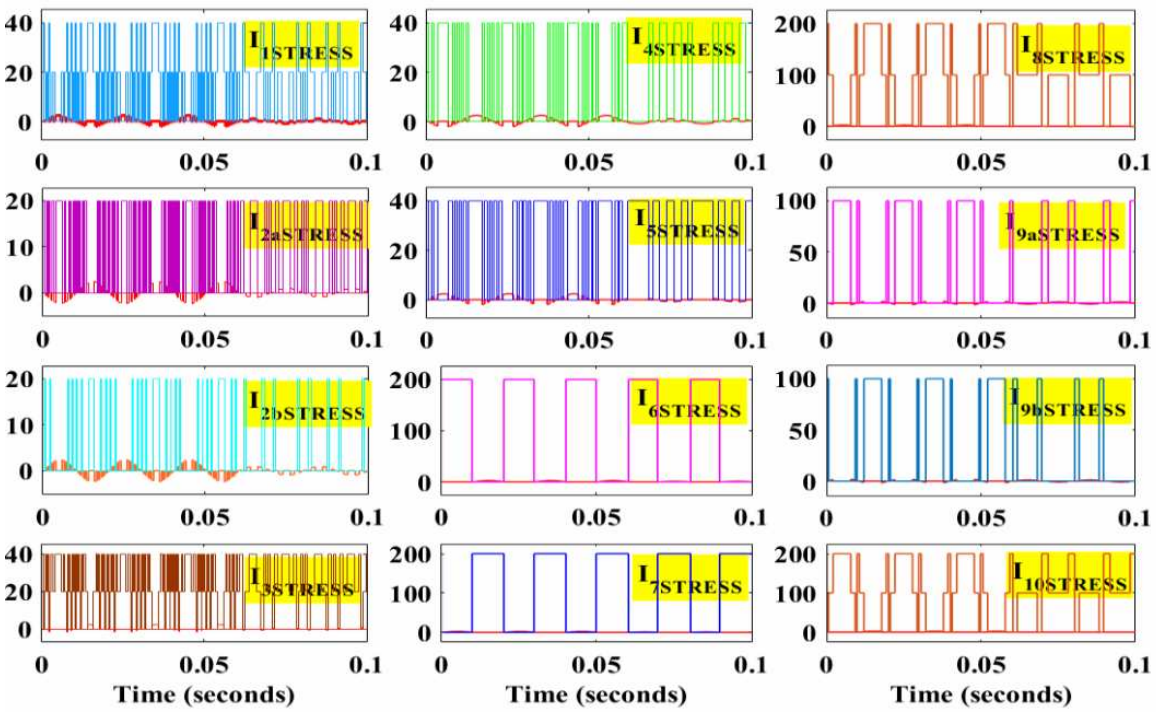

Figure 5. Voltage and current stresses of all power semiconductor switches for 1:5 source configuration.

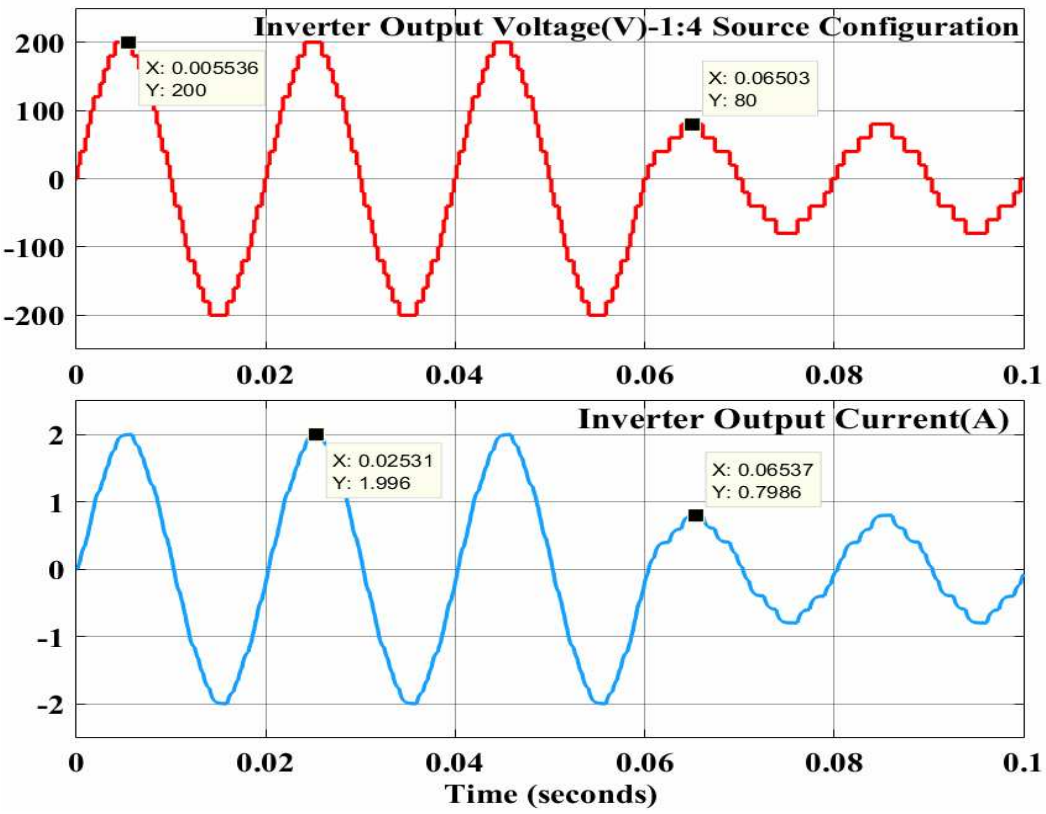

Figure 6. Inverter output voltage and Inverter output current for 1:4 source configuration with modulation index shifted from 1 to 0.4 at 0.06sec

Table 2. Comparison of different asymmetrical MLI topologies: Generalized Equations

Topologies	N_{IGBT}	N_{Driver}	$N_{sources}$	TSV*(V_{DC})	Negative Levels
Ebrahimi et al. (2012)	$8\log_5^P$	$6\log_5^P$	$2\log_5^P$	2.75(P-1)	With H-Bridge
Khosroshahi (2014)	$3\log_2^{P+1}+1$	$2(\log_2^{P+1}+1)$	$\log_2^{P+1}-1$	3.667(P-1)	With H-Bridge
Babaei et al. (2015)	$5\log_2^{P+5}$-9	$5\log_2^{P+5}$-9	$3\log_2^{P+5}$-8	(3.5P-4.5)	With H-Bridge
Babaei et al. (2014)	$4\left(\log_3^{\left(p+\frac{1}{2}\right)}+1\right)$	$4\left(\log_3^{\left(p+\frac{1}{2}\right)}+1\right)$	$2\log_3^{\left(p+\frac{1}{2}\right)}$	3(P-1)	With H-Bridge
Babaei (2008)	$6\log_3^{\left(p+\frac{1}{2}\right)}+4$	$3\log_3^{\left(p+\frac{1}{2}\right)}+4$	$2\log_3^{\left(p+\frac{1}{2}\right)}$	4.5(P-1)	With H-Bridge
Gupta and Jain (2014)	$\sqrt{4P-3}+1$	$\sqrt{4P-3}+1$	$0.5\left(\sqrt{4P-3}-1\right)$	2(P-1)	Inherent
Alishah et al. (2017)	$10\log_{17}^P$	$8\log_{17}^P$	$4\log_{17}^P$	2.5(P-1)	With H-Bridge
Hosseinzadeh et al. (2012)	$10\log_{17}^P$	$8\log_{17}^P$	$4\log_{17}^P$	2.5(P-1)	With H-Bridge
Sharma and Kapoor (2016)	$10\log_{17}^P$	$8\log_{17}^P$	$4\log_{17}^P$	2.5(P-1)	With H-Bridge
Proposed	$5\log_5^P$	$5\log_5^P$	$2\log_5^P$	2.5(P-1)	Inherent

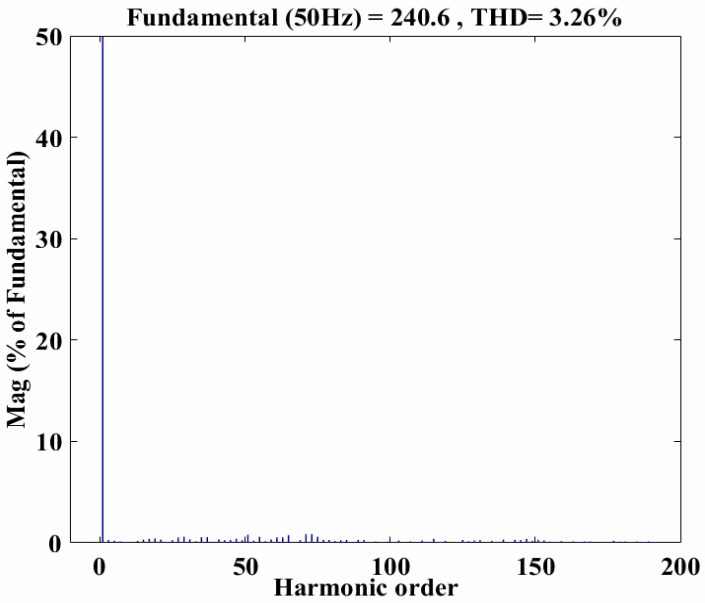

Figure 7. Harmonic Spectrum of Inverter Output Voltage-25 level output with 1:5 Source Configuration**:** MI=1.0

Table 3. Simulation Parameters

S. No	Description	Value
1	V_{DC}	20V
2	R	100 ohms
3	L	30mH
4	Output Frequency	50Hz
5	Voltage gain	1.0
6	Source Configurations	1:5 and 1:4
7	Modulation Index	1 to 0.4
8	TSV (p.u)	5.0

5. Conclusion

In this paper, a new asymmetrical MLI topology with two types of source configurations has been proposed and which requires less switch count when compared with other conventional topologies. The cost requirement of the switching devices can become reduces since less per unit TSV value is obtained. Basically, the reduction of switch count indicates that the respective reduction in gate drive circuits, heat sink and protection circuits. The NLC technique is used to provide the gate pulses to the switches which reduces switching losses and %THD value greatly reduces as compared with other conventional PWM control techniques. The change in peak value of the inverter output voltage and output current is observed with the step change of modulation index values from 1 to 0.4. The %THD value obtained for 25-level inverter output voltage with 1:5 source configuration is 3.26% and finally it meets the requirement of IEEE standards. The drawback of this topology is that it does not provide any boosting ability since voltage gain as unity. This topology is well suitable for grid connected applications.

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