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Differential Protection Scheme for A Micro Grid with Inverter-Type Sources Based On Positive Sequence Fault Currents

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Abstract: The microgrid (MG) is a coordinated collection of different distributed generation (DG) types that supply local demand through a distribution network. MG may operate in two different modes: grid-connected (GC), and islanded (IS) modes. The fault current value varies significantly between the GC and IS mode for a MG with inverter-based distributed generators (IBDGs). The fault currents are minimal in the IS mode owing to the power electronics equipment have a limited current carrying capacity. Therefore, the coordination of traditional overcurrent (OC) protection is difficult for these two operation modes. Therefore, a comprehensive MG protection scheme should be established to safeguard MG against all kinds of faults. The main protection strategy proposed in this paper is a positive sequence differential current protection scheme. The envisioned concept can overcome the protective device coordination problems, and all fault types can be detected during both operation modes of MG for radial and loop configurations. The validation of the proposed design is performed using PSCAD/EMTDC software. The results indicate that the maximum fault clearing time for the main protection in GC mode and IS mode is of 31.5 ms and 34 ms respectively. Compared with other schemes, the proposed scheme has a faster clearing time and is less expensive.

Keywords: Distributed Generation (DG), microgrid, protection, renewable energy sources

1. Introduction

The term "microgrid" (MG) has evolved to refer to distribution networks that use traditional distributed generation. (DGs), renewable energy sources (RES), or both. The RES including photovoltaic, wind power, hydro, gas turbine, diesel generator, microturbine, fuel cells, and battery storage [1]. The MG is more reliable and less expensive compared to conventional power system because of its ability to serve in both modes, islanded (IS) and grid-connected (GC).

Most DGs are inverter-based DGs (IBDGs) which produce DC power and convert it to AC by power electronic inverters. The fault currents are minimal in the IS mode, Due to the restricted current-carrying capacity of inverters, fault currents are limited when the MG operates independently of the main grid. The short circuit current is indeed 1.2–3 times the rated current in the case of IBDGs [4]–[6], while synchronous generators, in GC mode, can generate a fault current that is 4–10 times greater than IBDGs [7]. Thus, the coordination of traditional overcurrent (OC) protection is difficult for these two operation modes.

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Various solutions have been proposed to establish a reliable protective scheme for MG. It includes adaptive protection schemes [8]–[10], signal processing based on Fourier transform [11]–[13], signal processing based on wavelet transform [14]–[16], OC protection [17], [18] and differential protection (DP) [7], [20]–[25].

Adaptive schemes suffer from computation complexity due to changes in MG mode, loads, and transients during DG unit connection or disconnection. While a signal processing scheme requires accurate signal synchronization with a high sampling frequency. Furthermore, the scheme has a large computing overhead, resulting in slower response times.

The direction of power flow and coordination time have no effect on the DP so, the DP schemes have been acknowledged as one of the most effective types for this purpose because of its good sensitivity, high selectivity, and fast tripping as well as it is a unit protection type that does not require to coordinate with other protective devices [1]. As communication technology improves, pilot communication links become more dependable, making DP schemes the best option for MGs[19].

The researchers of [20] highlighted two major challenges related to MG operation: protection and control. A traditional differential relay was used for protection, and two control systems have been presented: a local system for each DG and the other is a central system. Because all system equipment must be connected to the control centre, this scheme is quite expensive for a large system. The scheme shows that the DP is suitable to the MG. The Italian distribution network was highlighted in [21] to develop innovative protection measures with the lowest implementation costs. The placement of differential relays on network line feeders is the foundation of the proposed protection solution. Although this scheme was used to protect MG with both IBDGs and synchronous DG sources, loop configuration, GC mode, two phase, and two phase-to-ground faults were not regarded.

Moreover, the authors of [22] present current DP to overcome the challenges of meshed MG protection. As the suggested method works with a number of parameters (i.e., three-phase currents (I_a, I_b and I_c), negative, and zero currents), it necessitates the use of extra links and adds to the computing burden. The authors also failed to account for variations in fault current magnitude caused by MG modes, fault kinds, and unbalanced loads, resulting in protection blindness or false tripping. A DP strategy relying on current frequency component fluctuations was proposed in the study [23] to isolate and identify faults in the IS mode. For the IS MG, the authors of [7] developed a differing scheme under symmetrical components alongside a central communication system. A fuzzy method was combined with the Hilbert space-based power theory in [24]. The scheme ignored the IS mode and did not consider the GC MG. Also, [25] employed the differential current protection and neglected the single-line fault and discarded the IS mode.

After a thorough review of the available protection strategies in the studies, it has been determined that different action plans are a good way for protecting a MG. This is as a result of the initiatives' ability to resolve the challenges of coordinating a vast group of sequential protection devices while supplying low fault current extracted from inverted-based DGs.

Nevertheless, several issues arise with this approach, including fault current magnitude differences because of changing operation modes, fault kinds, or unbalanced loads, resulting in protection blindness or false tripping. Additionally, a traditional DP often uses three units to accommodate all types of fault, necessitating extra links and adding to the computation complexity. Furthermore, the methods mentioned above have not been tested for other expected disturbances; as a result, they may fail to function properly during non-fault situations. Finally, several prior methods used a protection centre, which added to the expense by requiring multi-link to connect all protection devices. As a result, an appropriate protection solution capable of resolving these issues must be found. This paper provides a positive sequence differential current protection scheme as the primary protection. The suggested concept can overcome the protective device coordination problems, and all fault types can be detected during both operation modes of MG, IS, and GC for loop and radial configuration. PSCAD/EMTDC has been used of a case study validates the efficacy of the suggested approach. The following are the scheme's key contributions:

This scheme is established on positive sequence currents instead of the three-phase currents to reduce the differential calculation.

- The use of positive sequence currents reduces the number of communications links that are used to transmit the signal between both line sides.
- The proposed scheme can detect the low fault currents during IS operation mode as a result of using IBDG.
- Determination of the fault's current direction does not require.
- The scheme has the advantage of high sensitivity, more reliability, sufficient selectivity, and high-speed tripping.

The paper is organized as follows. Section 2 elaborates the background of varied protection. Next, the suggested positive sequence current protection method is explaining in Section 3. Then, the simulation findings and test system are mentioned in section 4. In the end, in Section 5, the study's main conclusions are reported.

2. Pilot DP

The DP approach is often used as an electrical unit's primary protection, for example, a bus, generator, power line, or transformer following its excellent performance. Pilot protection uses to protect a power line where a communication link is necessary to transfer data between the two-line ends. This technique is the most sensitive and robust method of offering fault protection For GC and IS modes [1]. DP is a simple concept related to the fact that any failure inside the

equipment causes the current entering and departing the apparatus to differ. The two currents can thus be compared, if the difference is greater than a certain threshold, a trip output can be generated. For an example of a unit in Fig. 1, The current accessing CT1 from one end must be the same as the current departing CT2 from the other. When a fault arises between the two ends, the two currents do not remain equal. Alternatively, the two currents entering the shielded apparatus might be summed together algebraically.

Differential current should have a zero magnitude during normal operation, but in practice, it has a low value because of the current transformer (CT) ratio mismatch, line charging current, or CT error [22]. Because of the distances involved, the DP approach was rarely used for line protection until recently. Six communication links are obligated for a three-phase line: one for each phase, one for the neutral, and two for tripping the circuit breakers (CBs). Line current DP has grown common as computers have been more widely utilized and communication has improved [23]. To prevent protective blindness or false tripping, the usage of current DP to MG lines necessitates consideration of difficulties associated with this system, such as the magnitude difference in fault current. The positive (+ve) sequence differential current protection scheme (PSDCPS) for both feeder sides is presented in this work as a modified differential current protection.

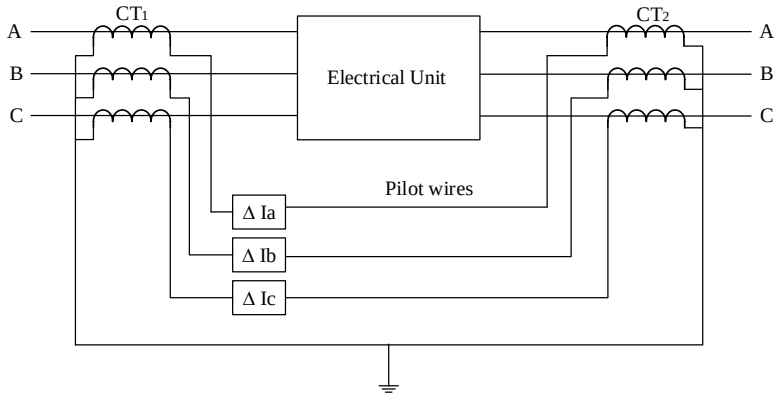

Fig. 1 - Three-phase differential protection

3. The Proposed PSDCPS

The approach proposed for PSDCPS has several procedures, including signal measurements, symmetrical components conversion, fault detection and fault isolation. The sections that follow provide a full description of these parts. This paper proposes a complete protection mechanism that can safeguard any type of MG in any configuration against a variety of faults. PSDCPS employed a sequence analyser in bias protection to overcome the problems associated with the pilot DP.

3.1 The +Ve Sequence Index

A sequence analyser is employed to transform the three phase values (abc) into +ve, -ve, and zero sequences in order to decrease computation complexity and communication links. As indicated in Table 1, an only +ve sequence is used since it is accessible in all kinds of faults. From three-phase systems, the +ve sequence component may be separated based on the symmetrical components method developed by C. L. Fortescue. A three-phase system with three unbalanced phasors can be converted into three balanced phasor system, where the system decomposes into three sequence networks as shown in Fig. 2.

Table 1 - Sequence components related with fault types

Fault Type	Sequence Component
Single-line-to-ground (SLG)	Positive + Negative + Zero
Line-to-line (LL)	Positive + Negative
Line-to-line-to-ground (LLG)	Positive + Negative + Zero
Three-phases (LLL)	Positive

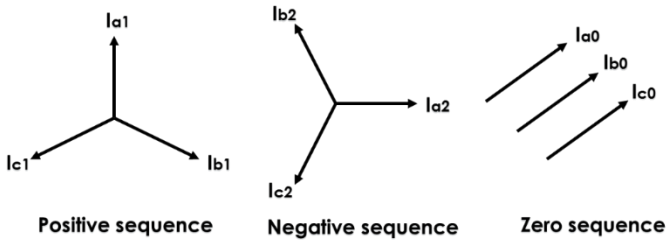

Fig. Error! No text of specified style in document. **- Currents sequence components**

Each phase contains the three-sequence component:

$$I_a = I_{a1} + I_{a2} + I_{a0} \quad (1)$$

$$I_b = I_{b1} + I_{b2} + I_{b0} \quad (2)$$

$$I_c = I_{c1} + I_{c2} + I_{c0} \quad (3)$$

where, I_{a1} , I_{a2} and I_{a0} are the +ve, -ve and zero current sequences of phase a; respectively; I_{b1} , I_{b2} and I_{b0} are the +ve, -ve and zero current sequences of phase b; respectively; I_{c1} , I_{c2} and I_{c0} are the +ve, -ve and zero current sequences of phase c; respectively and I_a , I_b and $I_c k = \frac{N_r}{N_o}$ are the three-phases currents. Let operator *a* be defined as $a = 1\angle 120°$. By referring to Fig. 3, the following relations are verified:

$$\begin{aligned} I_{b1} &= a^2 I_{a1} & I_{c1} &= aI_{a1} \\ I_{b2} &= aI_{a2} & I_{c2} &= a^2 I_{a2} \\ I_{b0} &= I_{a0} & I_{c0} &= I_{a0} \end{aligned} \quad (2)$$

Repeating (1) and substituting (4) in (2) and (3) yield

$$I_a = I_{a0} + I_{a1} + I_{a2} \quad (3)$$

$$I_b = I_{a0} + a^2 I_{a1} + aI_{a2} \quad (4)$$

$$I_c = I_{a0} + aI_{a1} + a^2 I_{a2} \quad (5)$$

The three-phase currents have the following sequence components in matrix form:

$$\begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{pmatrix} \begin{pmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{pmatrix} \quad (6)$$

$$\begin{pmatrix} I_{a0} \\ I_{a1} \\ I_{a2} \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{pmatrix} \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} \quad (7)$$

From (9), the +ve sequence current can be calculated as in (10)

$$I_{a1} = \frac{1}{3}\left(I_a + aI_b + a^2 I_c\right) \quad (8)$$

Consider the system demonstrated in Fig. 4, the three-phase currents that enter the first side (I_1) and leaving the second side (I_2) pass through a sequence analyser to extract the +ve sequence index that was named I_{A1} and I_{A2} respectively:

$$I_{A1} = \frac{1}{3}\left(I_{a(1)} + aI_{b(1)} + a^2 I_{c(1)}\right) \quad (9)$$

$$I_{A2} = \frac{1}{3}\left(I_{a(2)} + aI_{b(2)} + a^2 I_{c(2)}\right) \quad (10)$$

3.2 Fault Identification

The PSDCPS has two coils, an operation coil and a restraint coil, as seen in Fig. 3. The three-phase currents (A, B, C) flow through current transformer CT on both electric unit sides. The number of turns in restraint coil (N_r) divided into two sides while the operation coil has a number of turns N_o. The current flow in operation coil, I_o is

$$I_o = \left(I_{A1} - I_{A2}\right)N_o \quad (11)$$

The current flow in restraint coil, I_{res} is

$$I_{res} = \left(I_{A1} + I_{A2}\right)N_r \quad (12)$$

The relay will operate when $I_o > I_{res}$

$$\left(I_{A1} - I_{A2}\right)N_o > \left(I_{A1} + I_{A2}\right)N_r$$

$$I_{A1} - I_{A2} > \left(I_{A1} + I_{A2}\right)\frac{N_r}{N_o}$$

$$I_{op} > kI_r \quad \text{or} \quad \frac{I_{op}}{I_r} > k \quad \frac{I_{op}}{I_r} > k \quad (13)$$

where, $I_{op} = I_{A1} - I_{A2}$, $I_r = I_{A1} + I_{A2}$ and $k = \frac{N_r}{N_o}$ is called slope or bias which is usually expressed as a ratio value.

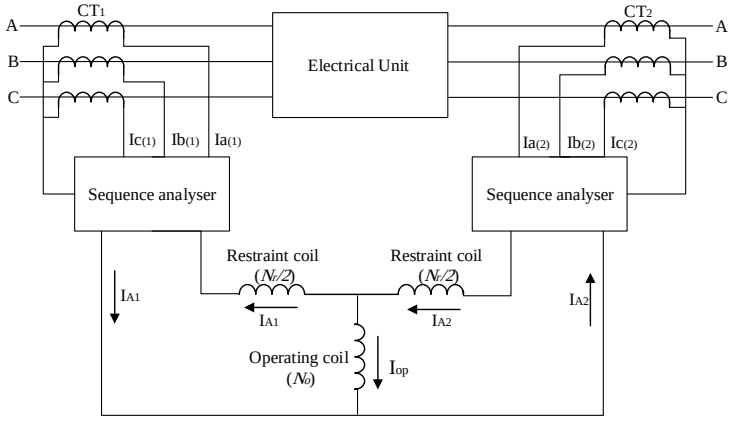

Fig. 3 - +ve sequence differential current protection principle

The procedures of the proposed main protection are detailed in the flowchart in Fig. 4. where the current is measured at two sides of the protected-line then the +ve sequence current is extracted, these values will be used to calculate the I_{op} and I_r. $\frac{I_{op}}{I_r}$ is compared with threshold value K, when it exceeds K the trip signal is generated.

To find the threshold value k of the proposed scheme for the protected line, the fault study will determine the minimum +ve current of the both ends of the protected line I_{A1} and I_{A2}. Minimum fault currents can be computed by applying the fault at the line end. The value of k is calculated by PSCAD recording to the fault analysis. The analysis shows that the minimum value of k is 0.36, so 0.3 is set to ensure that all faults for all cases are detected

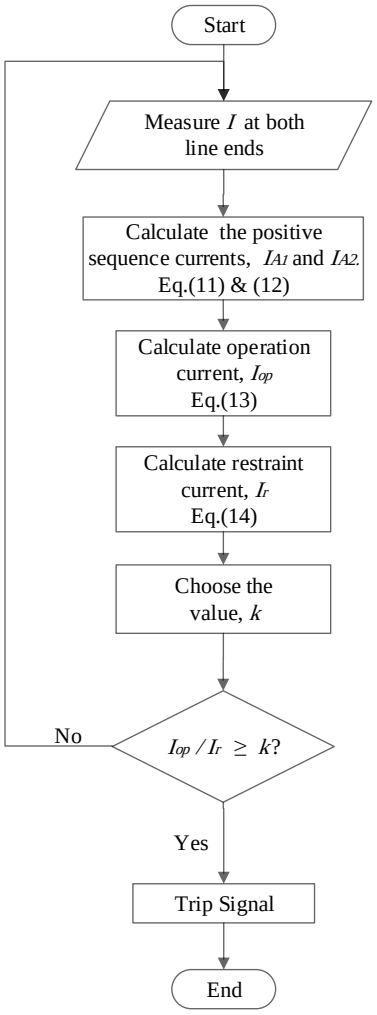

Fig. 4 - Flowchart of the proposed PSDCPS

4. Results and Discussion

Several simulations have been run to examines the suggested method by using the PSCAD/EMTDC. The MG test system is depicted in Fig. 6 as a single-line diagram. The reason for choosing this MG test system is because it has been used in many types of research, such as [26], [27], [28]. Furthermore, it is a medium voltage system that can be easily switched from radial to loop configuration. The investigated system's voltage level was 24.9 kV, with a 50 Hz operating frequency.

The MG operates in such a manner that it functions in the GC mode under normal conditions. However, in any event of the main grid disruption, it smoothly disengages from the main grid and continues to run in IS mode. A 69 kV/24.9 kV Dyn transformer connects the MG to the main grid, as illustrated in this diagram.

In addition to one synchronous generator (300 MVA), it has one wind turbine (500 KVA) and two photovoltaic systems (640 KVA) that are linked to the grid via an inverter circuit. A 0.4/24.9 kV transformer connects each DG source to the rest of the system. When the CBs on L7 are closed or opened, radial and loop configurations can be obtained.

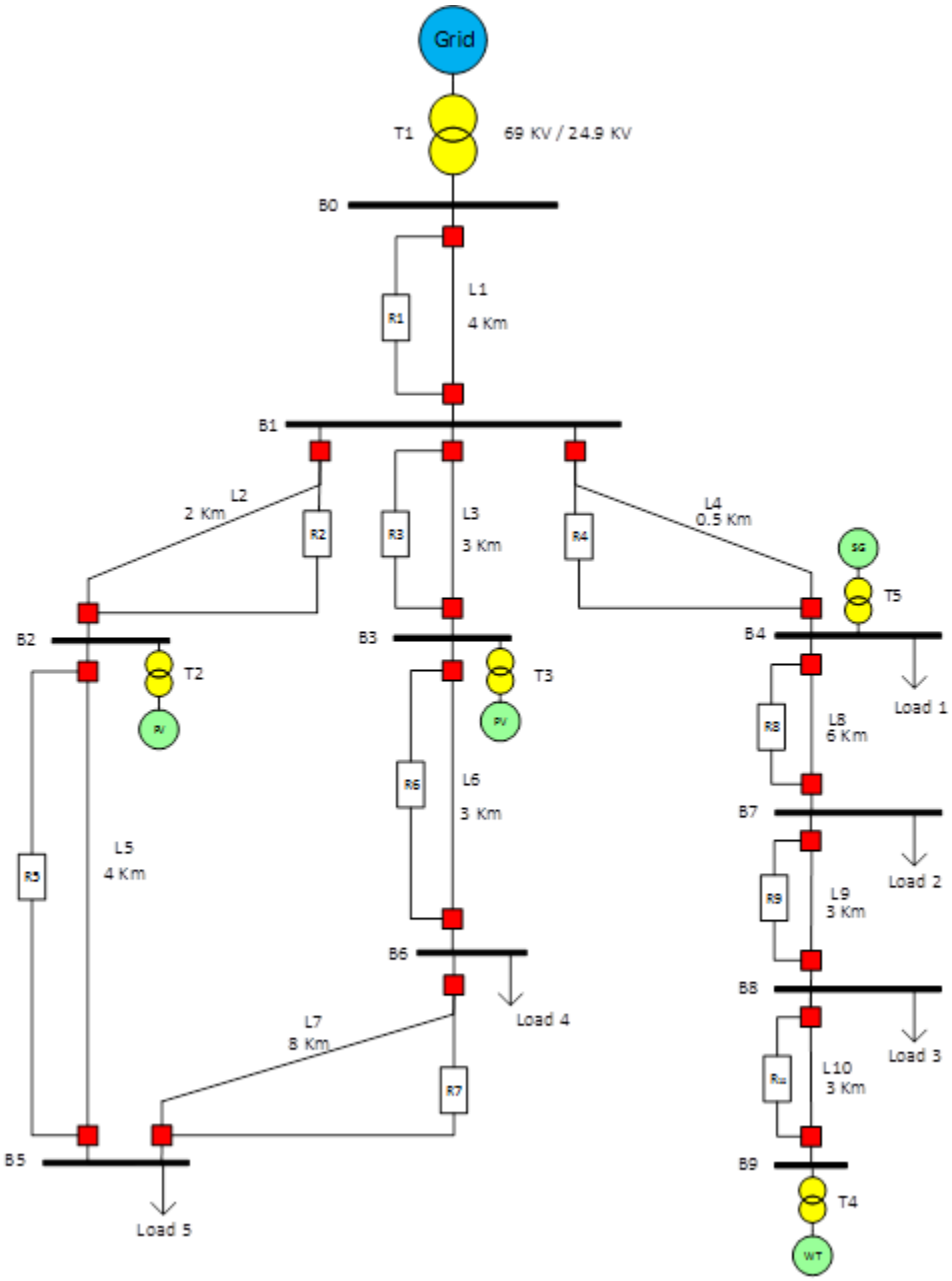

Fig. 6 - MG test system

Table 2 - The DG capacity and transformer ratio

DG type	Capacity	Transformer
PV1	(640 KVA)	0.4/24.9 kV
PV2	(640 KVA)	0.4/24.9 kV
WT	(500 KVA)	0.4/24.9 kV
SG	(300 MVA)	0.4/24.9 kV

4.1 Case Study1: GC Operation Mode

The case study's objective is to determine the efficacy of the planned main protection strategy in the course of the GC operation mode for radial and loop configurations of the MG. All faults are detected by the protection relays, which transmit a trip signal to the reasonable CBs, isolating the faulty portion from the other MGs as shown in Table 3. The simulation results of the primary protection mechanism during various types of faults are shown in the subsections below for different locations inside the MG.

Table 3 - The performance results of the protection scheme during different fault types for GC operation mode

Configuration	Fault type	Line involved	Ifa (A)	$\frac{I_{op}}{I_r}$		Main relay involved in the protection	Clearing time (ms)
				Internal fault	External fault		
Radial	SLG	L5 (phase 'a')	190	0.99	0.04	R5	31.5
	LL	L6 (phase 'a', 'b')	382	0.97	0.04	R6	30.5
	LLG	L9 (phase 'a', 'b')	414	0.96	0.01	R9	31.5
	LLLG	L8	656	0.98	0.01	R8	28
Loop	LLLG	L7	517	0.41	0.01	R7	28.5

For instance, an SLG fault was assumed to occur on line L5. As a result of this fault, the positive sequence of the fault current is the summation of these two ends current which is greatly increased up the normal condition. It is due to the MG connected to the main grid, which reaches 190 A as portrayed in Fig. 7.

Fig. 8 demonstrates the percentage value of (I_{op} / I_r) during an SLG fault (on phase a) on Line L5 with a fault resistance of 10 at 0.2 s simulation time, this fault is within the responsibility of relay R5 (internal fault). While the external fault can occur anywhere in the system, line L2 has been chosen for comparison, as seen from the Fig. that (I_{op} / I_r) raised during internal fault while it remained below 0.3 during external fault.

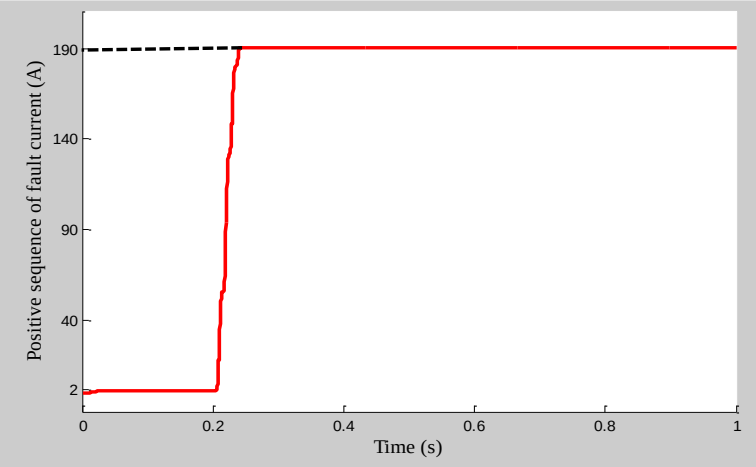

Fig. 7 - Positive sequence current magnitude when SLG fault occurs on L5 for GC mode

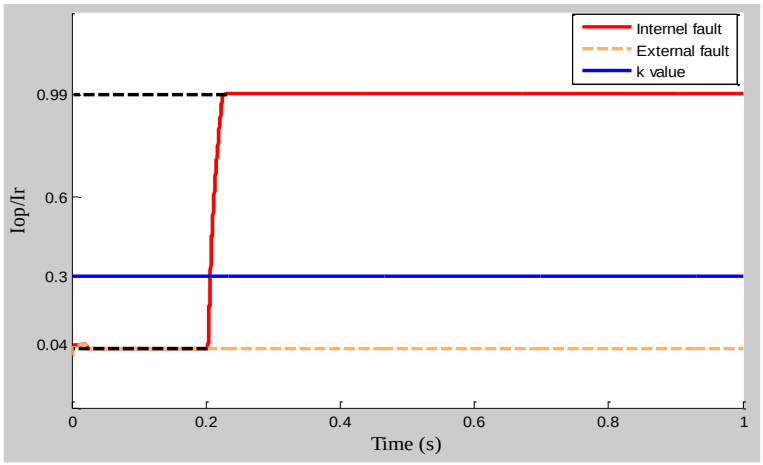

Fig. 8 - Iop / Ir for an internal fault (inside L5) and external fault (inside L2) for GC mode

Therefore, R5 sent a trip signal to the certain CBs for internal fault only, as the device's response was fast, as shown in Fig. 9. The Fig. can be referred to verify that trip time is shorter than 26 ms after the fault incident at time 0.2 s. The total clearing time is 31.5 ms, as shown in Fig. 10, which includes operating times of the relay, communication delay time, and CB opening time. This Fig. shows the fault initiated and cleared on the faulted phase (phase a) voltages waveforms.

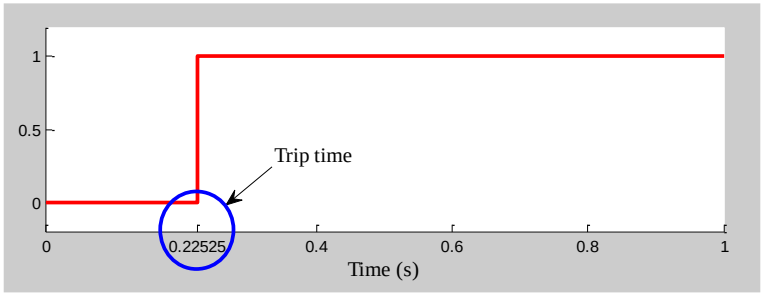

Fig. 9 - Trip signal of R5 for internal SLG fault for GC mode

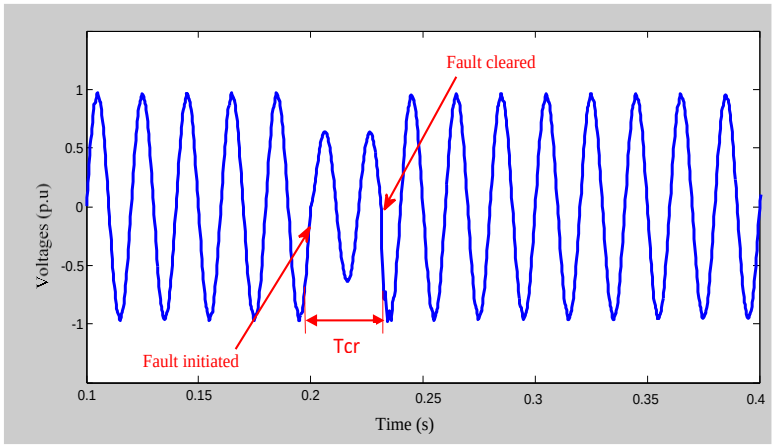

Fig. 10 - Voltage of phase a at bus two during SLG fault at L5 for grid-connected

In summary, this section presents the findings of the main protection scheme. The results showed the efficiency of this scheme for all types of fault during the GC operation mode for radial and loop configurations of the MG with balance and unbalanced load. The results also showed that the scheme is characterized by high reliability, accuracy, and fast operation speed of less than 32 ms.

4.2 Case Study2: IS Operation Mode

The case study's objective is to ensure that the suggested main protection solution is effective during the IS operation mode for radial and loop configurations of the MG as shown in Table 4.

Table 4 - The performance results of the protection scheme during different fault types for IS operation mode

Configuration	Fault type	Line involved	Ifa (A)	$\frac{I_{op}}{I_r}$		Main relay involved in the protection	Clearing time (ms)
				Internal fault	External fault		
Radial	SLG	L5 (phase 'a')	14.2	0.9	0.03	R5	32
	LL	L6 (phase 'a', 'b')	23	0.98	0.03	R6	31
	LLG	L9 (phase 'a', 'b')	26	0.36	0.01	R9	33
	LLLG	L8	33	0.44	0.01	R8	34
Loop	LLLG	L7	33	0.41	0.02	R7	34

As a result of the grid's disconnection, the fault current level fell considerably in this instance, and the only source of generation present is DGs. IS mode is obtained when the CB of L1 is opened, leading to disconnecting the MG from the main grid.

In the MG, the protection mechanism has detected all types of faults and suitable CBs receive the trip signal to separate the faulty section from the remaining portion of the MG. The simulation results of the primary protection mechanism during numerous faults are shown in the subsections below for different locations inside the MG.

An SLG fault was assumed to occur on line L5 (internal fault) with fault resistance is 10 Ω at a simulation time is 0.2 s. The positive sequence of the fault current increased slightly above the normal condition due to the MG be disconnected from the main grid where it reaches 14.2 A, as shown in Fig. 11.

The internal SLG fault was assumed on line L5, and the external fault can occur anywhere in the system. Line L2 has been chosen for comparison, as can be seen from Fig. 12 that (I_{op} / I_r) raised during internal fault while it remained below 0.3 during external fault.

Therefore, R5 sent a trip signal to the certain CBs for internal fault only, as the device's response was fast, as shown in Fig. 13. It is observable in the Fig. that the trip time takes less than 26 ms after the fault incident at time 0.2 s. The total clearing time is 32 ms, as shown in Fig. 14, which includes operating times of the relay, communication delay time, and CB opening time. This Fig. shows the fault initiated and cleared on the faulted phase (phase a) voltages waveforms.

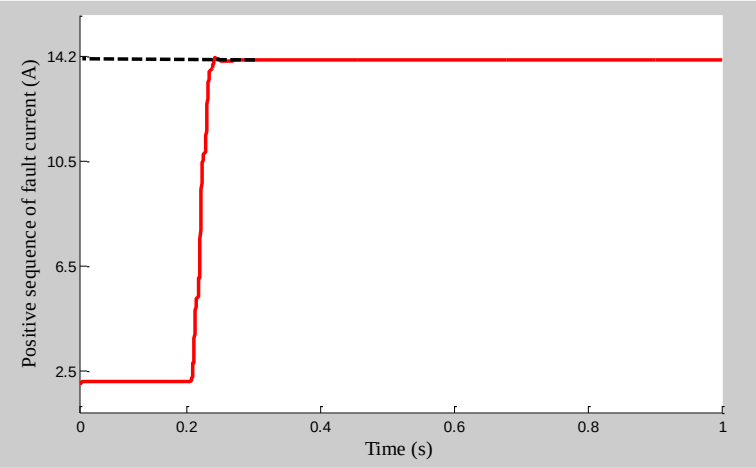

Fig. 11 - Positive sequence current magnitude when SLG fault occurs on L5 for IS mode

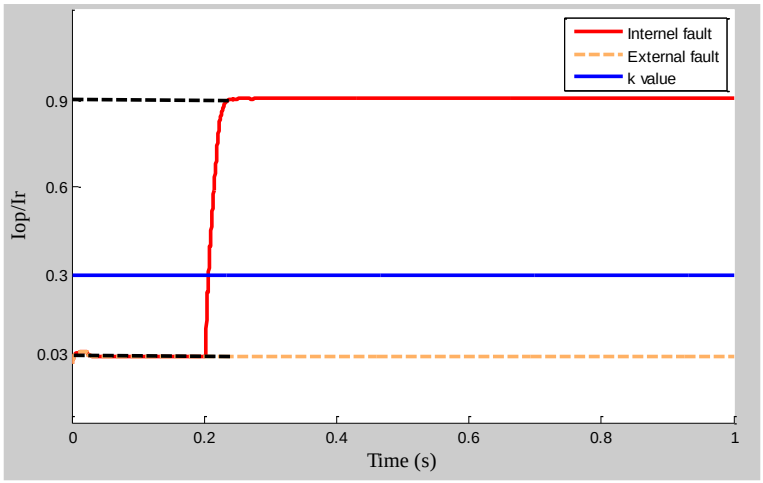

Fig. 12 - Iop / Ir for an internal fault (inside L5) and external fault (inside L2) for IS mode

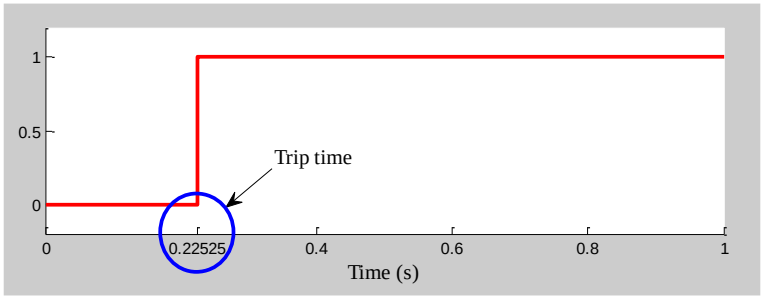

Fig. 13 - Trip signal of R5 for internal SLG fault for IS mode

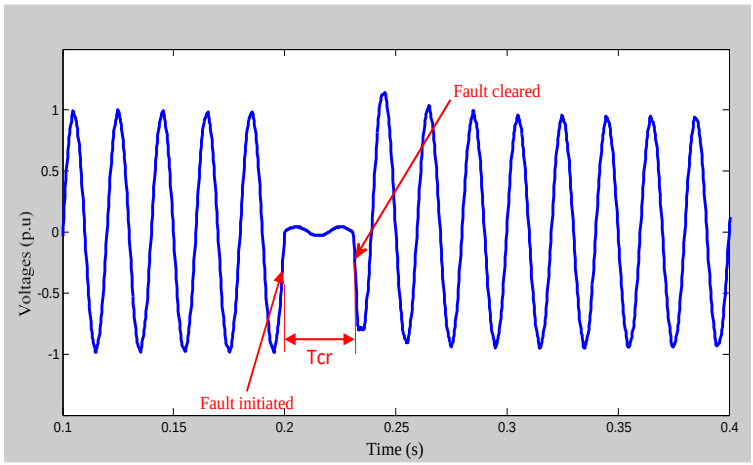

Fig. 14 - Voltage of phase a at bus two during SLG fault at L5 for IS mode

In summary, this section presents the results of the main protection scheme for IS mode. The results showed the efficiency of this scheme for all types of fault during the IS operation mode for radial and loop configurations of the MG with balance and unbalanced load. The results also showed that the scheme is characterized by high reliability and accuracy, in addition to fast operation speed that was less than 34 ms.

4.3 Validity of The Proposed Scheme

In order to validate the performance of the proposed scheme, it is compared with adaptive scheme [29], SP scheme [26], OC scheme [17] and DP scheme [30] in terms of the operation speed of protection scheme, as presented in Table 3. It clearly shows that the +ve sequence differential method achieved a higher isolation speed than the other methods.

The proposed scheme can detect all fault types correctly in grid-GC and IS modes for radial and looped systems. The results show that its maximum clearing time for the main protection in GC mode is 31.5 ms and 34 ms for IS mode.

Table 3 - Comparison of the proposed method with other methods

Method	Adaptive [29]	SP [26]	OC [17]	DP [30]	Proposed method
Operation mode	GC + IS	GC + IS	GC + IS	GC	GC + IS
DG type	SG	SG + IBDG	SG + IBDG	SG + IBDG	SG + IBDG
Configuration	Radial + Loop	Radial + Loop	Radial	Radial	Radial + Loop
Fault type	LL, SLG	All	All	All	All
Unbalance load	No	No	No	No	Yes
Max. OT (ms) GC	572	73.2	141	122	31.5
Max. OT (ms) IS	572	73.3	528	-	34

5. Conclusion

MG protection has been an issue as increasing prevalence of DGs, particularly inverter-based DGs. As a result, traditional protection techniques are ineffective in the MG system. This necessitates the development of alternate protection to isolate the network's faulty zone in the shortest amount of time possible.

This research aims to develop an all-inclusive protection method for an inverter-based MG. This approach can protect the MG against all types of faults for both GC and IS mode for loop and radial configuration. To achieve the aim of this research, first, an index based on positive sequence fault current was put forward to differentiate between fault on the protected line and fault at other lines.

This index was applied for the DP scheme for MG with multi-sources. The plan is suitable for GC and IS modes of operations.

The suggested scheme achieved the selectivity where only the faulty zone is isolated when a fault occurs. Also, the speed of the protection scheme was demonstrated since the main protection scheme tripped CBs did not exceed 34 ms during the GC and IS modes, while the backup scheme tripped CBs in less than 130 ms with delay time. Furthermore, the proposed scheme reliability for the GC and IS mode was validated, where the main and backup protection tripped and did not trip as expected in all cases. Finally, the proposed scheme was compared to the other schemes, the comparison with shows that the proposed scheme has a faster clearing time and is less expensive.

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