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FEASIBILITY INVESTIGATION OF FAULT DIAGNOSIS USING ELECTROMAGNETIC ANALYSIS OF PLANAR STRUCTURES

by

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FEASIBILITY INVESTIGATION OF FAULT DIAGNOSIS USING ELECTROMAGNETIC ANALYSIS OF PLANAR STRUCTURES

By

SOEUNG SOCHEATRA

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DECLARATION OF THESIS

Title of thesis | FEASIBILITY INVESTIGATION OF FAULT DIAGNOSIS USING ELECTROMAGNETIC ANALYSIS OF PLANAR STRUCTURES

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DEDICATION

To my beloved Dad and Mum;

To my sister;

To my two brothers;

To my dearest friend.

ACKNOWLEDGEMENTS

First of all, I would like to thank my supervisors Dr. Noohul Basheer Zain Ali and Dr. Mohd Haris Md Khir for their valuable guidance and support throughout my study in Universiti Teknologi PETRONAS. Thank them for everything that they have shared and taught me. When I find myself not be able to move on, they are there to encourage and guide me back to the right track. I have learned a lot from both of them.

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I would like to thank to my dearest friends for being always there for me all the time and in the time I need the most. I really appreciate their respectful, faithful, kind, and true friendship that they share with me. I am really thankful to the sharing of knowledge and experiences which have made me understand and see myself as who I really am. And I would like to thank V5 committees for their support and companionship throughout my study life in the University.

Lastly, I would like to thank the lab technicians and other friends who have assisted me in accomplishing this project successfully.

ABSTRACT

Nowadays, circuit design technologies have progressively advanced to cope with the high performance of the electronic components. With the circuit design advancement, the technology for IC fabrication has moved to deep submicron era. As the circuit sizes continue to scale down to nanoscale, the number of transistors and interconnects on the circuits tends to grow as well. This challenges the circuit testing by introducing high number of possible faults on the circuit. Consequently, the product quality control has become more challenging. The product quality could drop significantly if the circuits are not designed to be testable. Testing is a very important phase in the production of electronic products to ensure the correct performance of both integrated circuits (ICs) and circuit board such as printed circuit board (PCB). The major causes of fault in electrical circuits can be categorized into two types: shorts and opens. Besides that, the sum of a small current pulse from each transistor causes a high current flow in the circuit. This high current pulse induces electromagnetic field around the circuit. Due to the relationship between the current and electromagnetic field on the circuit, the thesis exploits the dynamic magnetic field behavior in inspecting the short and open faults on PCB conductive interconnect. The dynamic magnetic field is detected and investigated by the eddy current testing (ECT) probe. This work involves in conducting two main tasks: simulation and experiment on PCB models. The PCB models are simulated in Computer System Technology (CST) Microwave Studio to observe the magnetic field intensities strength of the models. Having simulated the magnetic field intensity, the PCB models and ECT sensor are designed and fabricated on flame retardant 4 (FR4) board. Prior to PCB fault inspection, each circuit and component has been calibrated and characterized. The faulty PCB interconnect is identified by observing the difference between the ECT probe induced voltages of the fault free and faulty boards. The PCB fault inspection result patterns can be used as the initial investigation to generate a fast and reliable testing method for nanoscale circuits by using the ECT probe.

ABSTRAK

Sejak kebelakangan ini, teknologi rekabentuk litar semakin canggih bagi menampung keperluan komponen elektronik berprestasi tinggi. Seiring dengan perkembangan rekabentuk litar, teknologi fabrikasi litar bersepadu telah menjangkau lapangan penerapan sub-mikron. Dengan saiz litar yang terus mengecut ke tahap skala nano, bilangan transistor dan litar sambungan turut meningkat. Ini memberi cabaran kepada usaha ujian litar kerana kebarangkalian untuk kerosakan di dalam litar berlipat ganda. Justeru, kawalan kualiti produk menjadi semakin sukar. Kualiti produk boleh jatuh dengan mendadak sekiranya kerosakan litar tidak dapat disaring uji secara berkesan. Saringan uji merupakan fasa yang penting dalam pengeluaran produk elektronik untuk memastikan prestasi yang betul bagi kedua-dua litar bersepadu (IC) dan papan litar seperti papan litar bercetak (PCB). Punca utama kerosakan dalam litar elektrik boleh dikategorikan kepada dua jenis: pintas dan terbuka. Selain itu, jumlah arus nadi kecil dari setiap transistor boleh menyebabkan aliran arus yang tinggi dalam litar. Nadi arus tinggi memberi kesan medan elektromagnet di sekitar litar. Berpandukan hubungan arus dan kesan elektromagnet dalam litar, tesis ini mengeksploitasi ciri medan magnet dinamik dalam memeriksa kerosakan pintas dan terbuka pada litar sambungan PCB. Medan magnet dinamik dikesan dan disiasat oleh Ujian Arus Eddy (ECT). Kerja penyelidikan ini melibatkan dua tugas utama iaitu simulasi dan eksperimen pada model PCB. Model PCB disimulasikan dengan menggunakan perisian Computer Simulation Technology (CST) Microwave Studio bagi melihat tahap kekuatan medan magnet. Setelah tamat simulasi, model PCB dan pengesan ECT direka dan difabrikasi pada lapisan FR4. Sebelum pemeriksaan kerosakan PCB, setiap litar dan komponen diselaras dan ciri-ciri diselidiki. Litar sambungan PCB yang rosak dikenalpasti dengan memerhatikan perbezaan antara voltan teraruh prob ECT papan litar yang berfungsi baik dan papan litar yang mengandungi kerosakan. Corak keputusan ujian saringan PCB boleh digunakan sebagai siasatan awal merangkap kaedah ujian yang pantas dan cekap untuk litar berskala nano dengan menggunakan prob ECT.

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LIST OF ABBREVIATION

AC	Alternating current
BPF	Band pass filter
DC	Direct current
ECT	Eddy current testing
EM	Electromagnetic
FFT	Fast fourier transform
FR4	Flame retardant 4
IC	Integrated circuit
PCB	Printed circuit board

NOMENCLATURE

CMOS	Complementary metal oxide semiconductor
Iddq	Quiescent supply current
Iddt	Transient current
GMR	Giant magnetoresistant
PML	Perfect matched layer
RTL	Register-transfer level
S_{12}	Reverse transmission coefficient
SQUID	Superconducting quantum interference device

CHAPTER 1

INTRODUCTION

1.1 Project Background

In the modern day, electronics testing has a long history of existence since the beginning of the commercial manufacturing of integrated circuits (ICs), which was first introduced in the early 1960s [1]. Today, semiconductors and IC technologies lie at the heart of the ongoing advances across the electronics industry, research and development world [1]. The advancement of circuit design technologies has an ever growing impact on human modernization and life transformation. With these technologies, electronic devices have become smaller and smarter with much improved performance and reliability. However, the new technologies pose new challenges. The product quality could drop significantly if the ICs are not designed to be testable. In the semiconductor industry, testing is a very important process to ensure the correct performance of a circuit. Testing an IC can be performed at any circuit abstraction level by applying the appropriate testing methods [2-3]. Once these ICs have successfully passed the testing stage, these chips will be packaged and be ready for commercialization. Testing is not only a crucial process for ICs but it is also important for printed circuit boards (PCBs). Before mounting the electronics component, the PCB traces need to be inspected. The possible defects on PCB traces could be short, open, or metal erosion. The PCB fault inspection can avoid electronic circuits and components from being damaged and it ensures that the system functions according to its design and specification.

1.2 The Effects of Advancement of Circuit Design on Fault Modeling

According to Moore's law, the performance of an IC, including the components on it, doubles every 18-24 months with the same chip price [1]. Today, technology for IC fabrication has moved to the deep submicron era and the increased integration capacity has resulted in more complex structures and chips [4]. The advancement of the IC design technology has forced dramatic changes in the design geometry and manufacturing methodologies for ICs. The reduction of the circuit geometry has led to gradually increase in the number of possible faults between the interconnects and the logic lines not only inside the ICs but also on the PCBs [5]. This has resulted in time consuming, extremely costly and complex IC testing techniques. IC tests could be performed by either using voltage tests [6-7] or current tests [8-9]. Each of these tests measures different circuit behaviors that could possibly be affected by any faults. The faulty behaviors of ICs can be represented by several fault models, such as the stuck-at fault model, bridging fault model and delay fault model [10].

Fault modeling is used to represent physical faults and to assist in generating fault testing methods and simulating faults. Even though there are many fault models that have been proposed, but no single fault model accurately reflects the behavior of all possible faults that occur [3]. A trade-off between a fault model's accuracy in representing the physical defects and the speed of the fault simulation can be achieved by choosing an appropriate level of abstraction [2]. The test generation time is less when the fault modeling is done at higher level of abstraction. However, the less accurate it will be [2-3, 11]. Structural fault models have become popular in IC test generation as it allows test engineers to generate algorithms to represent a logic gate and interconnect netlist faults in a circuit [12]. The most widely used structural fault model in the industry is the single stuck-at fault which assumes that one line or node in the IC is stuck at logic high or low. It can detect the majority of realistic physical defects up to 80-85% of the defects are detected [13].

The stuck-at-fault model does not guarantee to cover all of the possible faults in the ICs for a high number of input or output lines [1-2]. With n lines of input or output, a circuit might have single stuck-at-faults of 2^n and multiple stuck-at-faults of 3^n-1 [1]. As a result, the testing algorithm has become more complex and testing is

both much more costly and time consuming. Besides the stuck-at-fault model, the supplementary current testing, such as Iddq testing and Iddt testing which are known as the static current based test and dynamic current based test (transient) respectively, have been used as current monitoring to detect possible faults in CMOS technology. However, the effectiveness of these current testing techniques is reduced in deep sub-micron technology as the leakage current increases to the range of hundreds milliamps [2, 14-17].

1.3 Electromagnetic Emission from Interconnects

Electromagnetic emission commonly occurs from cables, connectors, wiring patterns and from integrated circuits themselves [18-19]. As the integrated circuit feature sizes continue to scale down to nanoscale and the number of transistors increases to millions, the amount of interconnects among the devices tends to grow as well. As a result, ICs consist of numerous metallization layers and conductors. Moreover, the switching of every transistor in an IC generates a small current pulse which flows mainly on the supply lines and interconnects. The sum of these small current pulses causes enormous current flows within the chip, close to ampere range. Due to these dynamic switching currents, the electromagnetic field will be induced around the ICs supply lines or interconnects [19-21]. Therefore, there is a meaningful correlation between the current flowing through the interconnects and its electromagnetic emission.

1.4 Non-Contact Probe for Nanoscale Circuit Fault Testing

Since the advancement of the circuit design technologies have gradually introduced the large number of possible faults in ICs, the conventional fault models and supplementary tests do not manage any longer to cover all of the possible faults. Besides that, it has been proved the existence of the electromagnetic field induced by the dynamic switching current flowing through ICs and interconnects. Therefore, a feasibility study on fault testing in nanoscale ICs by exploiting the electromagnetic field has been proposed. The difference between the magnetic fields from a fault free

circuit and a faulty circuit is compared and analyzed. These fields are detected by a non-contact probe of a micro array-coil sensor with the coil dimensions in micro scale. The array sensor is fabricated on a silicon die. The sensor probe is placed in close proximity to the chip surface as shown in Figure 1.1. By using this array-coil sensor, the EMF detection can be performed during the chip fabrication lines before or after packaging in order to test and locate the potential faults.

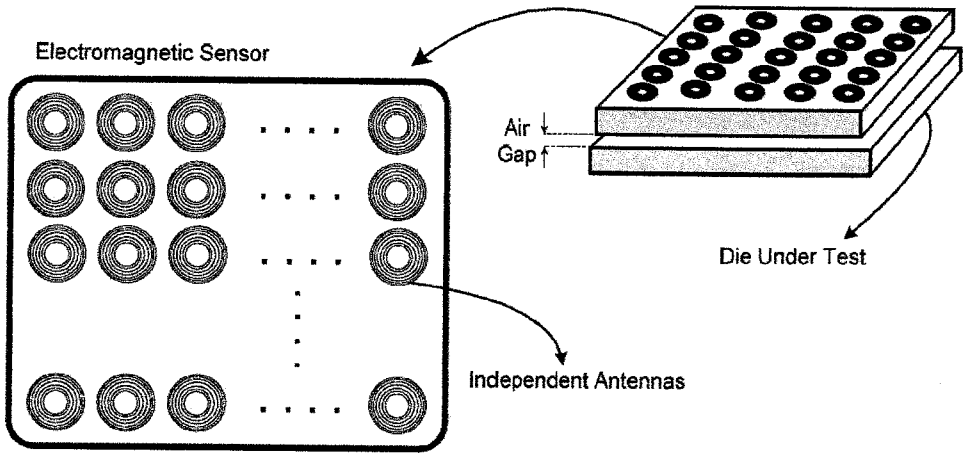


Figure 1.1: A suggested micro array-coil sensor for EMF detection and analysis

1.4.1 Research Constraint

Open and short faults on interconnects have been the main focus of the proposed non-contact probe for the nanoscale circuit fault testing project. Instead of fabricating and conducting the investigation on the nanoscale IC fault detection on silicon die, the die under test and micro array-coil sensor are modeled and fabricated on flame retardant 4 (FR4) PCB. This is due to the simplicity of PCB circuit prototypes. With the PCB fabrication, the prototypes can be fabricated many times compared to the nanoscale IC fabrication which can be performed only twice per year. In addition to the ease of PCB fabrication, the fault injection of the short and open faults can be performed instantaneously on the PCB interconnect prototype. Another advantage is the magnetic field characteristics of the faulty and fault free conductive lines are simply detected and observed by multi-meter and oscilloscope compared to the CMOS IC which requires high resolution equipments. The findings on the PCB interconnect

fault testing can be related to and used as the initial understandings for further investigation of fault testing in nanoscale IC interconnects.

1.5 Research Objective and Scope

The objective of this research is to conduct a feasibility investigation of fault inspection by exploiting the magnetic fields induced from PCB interconnects. The planar array-coil sensor as the sensor probe is designed to detect the induced magnetic field. The scopes of the project are:

- To simulate and observe the behavior and intensity of the magnetic field induced by the PCB conductive line models in the presence of short fault, open fault and fault free. For this purpose, Computer System Technology (CST) Microwave Studio is used. Understanding the strength of the magnetic field provides a beneficial knowledge in selecting the magnetic sensor and setting up the optimum fault inspecting system.
- To develop a contactless fault testing system. This is carried out by calibrating and characterizing a single coil sensor of the different number of turns, each circuit and component to obtain the optimum performance. The aim of this fault testing system is to investigate and inspect the PCB interconnects by utilizing the array-coil sensor to detect the induced magnetic fields of PCB interconnects. The advantages of the testing result patterns are to differentiate between the faulty and fault free PCBs and to locate the faults on the PCB interconnects.

This work starts by simulating the magnetic field intensity strengths induced by the PCB trace model in CST under the conditions of normal, short and open lines. The magnetic field intensities are detected above and along the conductive lines. Having observed and realized the strength of the magnetic field, the proposed PCB traces, single coil sensors and array-coil sensor layouts are designed in ADS (Advanced Design System) for fabrication. The PCB traces are designed under three conditions: normal, short and open lines. Prior to the array-coil sensor design, several single coil

sensors, an amplifier circuit, an active band pass filter and a pair of Helmholtz coils are calibrated and characterized. The optimum sensor is used as the element of the array-coil sensor in the PCB fault inspection. In order to obtain an optimum testing system, all of the electronic components and circuits are calibrated and characterized before being mounted on the testing system. Once the component characterization has been completed, the electronic components, such as connectors and jumpers are fixed during the PCB fault inspection. The array-coil sensor is used to detect the magnetic fields induced from the faulty and fault free PCB interconnects. Eventually, the obtained results are analyzed to differentiate the faulty and fault free behavior of the PCB conductive traces and to locate the potential faults on the lines.

1.6 Thesis Outlines

This thesis consists of four main chapters. These chapters are organized as follow:

Chapter 2 discusses the overview of the most common faults on both IC and PCB. The literature review of the PCB fault inspection methods is briefly highlighted. This chapter also discusses the concept of the eddy current testing principle and its application in the PCB fault inspection.

Chapter 3 presents the research methodology, experimental setup and sensor characterization. In this chapter, the instrumentation circuit, a pair of Helmholtz coils, a filter circuit, and single coil and array-coil sensors are calibrated and characterized before being mounted together for the PCB fault inspection.

Chapter 4 focuses on the PCB fault inspection results in the case of short and open faults. In this chapter, the inspections of PCB lines and eddy current behaviors are simulated in CST. This chapter also discusses the PCB fault inspection experimental results. These result patterns will be analyzed and discussed to differentiate between the faulty and fault free PCBs.

Chapter 5 concludes the thesis by summarizing the significant contributions of the project work and highlighting some future directions.

1.7 Thesis Contribution

This thesis presents a feasible method of detecting faults on circuit interconnects by analyzing the magnetic field properties of the faulty and fault free interconnects. In this work, the contactless probe sensor which is known as the array-coil sensor is proposed and designed to detect the induced magnetic fields of the PCB interconnects. The research work in this thesis has been presented in the formal proceedings of the following conferences and journal articles:

- S. Soeung, N. B. Z. Ali, G. A. Ellis, and A. Ahmadi. "**Feasibility investigation of fault diagnosis using electromagnetic analysis of planar structures**", *National Postgraduate Conference (NPC), 2011*, pp. 1-4. IEEE, 2011.
- S. Soeung, N. B. Ali, and M. H. Khir. "**CST simulation of magnetic field for PCB fault investigation**", *Intelligent and Advanced Systems (ICIAS), 2012 4th International Conference on*, vol. 1, pp. 407-411. IEEE, 2012.
- S. Soeung, N. B. Ali, and M. H. Khir. "**3D electromagnetic simulation on interconnect fault inspection based on magnetic field behavior**", *Regional Symposium on Micro & Nanoelectronics*, IEEE, 2013. (Accepted)
- S. Soeung, N. B. Ali, and M. H. Khir. **"PCB Fault Inspection Based On ECT With Planar Array-Coil Sensor"**, *Progress In Electromagnetics Research journal*, 2013. (Submitted)

CHAPTER 2
LITERATURE REVIEW

This chapter discusses the relevant literature review of the project on the circuit faults and the correlation between the induced magnetic field and the PCB interconnects with regards to the fault models and PCB inspection techniques. Starting with Section 2.1 briefly discusses the common faults occurring in a circuit. Section 2.2 describes the fault models and their drawbacks. The relationship between the magnetic field and the conductive interconnects is discussed in Section 2.3. Next, Section 2.4 introduces the printed circuit board (PCB) overview followed by Section 2.5 which describes the PCB fault inspection techniques. The following Section 2.6 introduces the induced eddy current on a conductive interconnect. In Section 2.7, the eddy current testing principle is discussed. Section 2.8 discusses the recent works on the eddy current testing with the different types of the magnetic sensor in the PCB inspection. The last section summarizes the chapter.

2.1 Circuit Faults

A fault is a representation of a defect, reflecting a physical condition that causes a circuit to fail to perform in a required manner [22]. In general, faults are categorized according to the level of the abstraction [2]. The causes of ICs and electronic circuits failing are many but they have been lumped into two broad categories: shorts and opens [13].

Shorts can be caused by extra conducting material or by a missing insulating material where an undesired conduction occurs. It can be the result of a photolithographic printing error, incomplete etch, incomplete metal polish or a crack in the insulator [13]. The short can occur between two elements such as transistor terminals or interconnects between transistors and gates. These elements are shorted

either to power or ground. When the two signal interconnections are shorted together, the shorted nets are modeled as a logical AND or OR of the values on the shorted lines. The wired-AND means the net signal of the shorted wire will take on a logic 0 if either shorted line is at logic 0. While the wired-OR means the net signal of the shorted wire will take on a logic 1 if either shorted line is at logic 1 [1].

Opens can be caused by missing conducting material or extra insulating material where the desired conduction does not occur. It can be the result of the manufacturing process step error, photolithographic printing error, incompletely filled via or an incomplete via etch [1]. An open fault can be said to be a weak or resistive open if the break does not completely disconnect the nodes resulting in a circuit that operates slower than expected. It is called fully open if it totally disconnects the interconnections of the conducting path resulting in a node that is electrically isolated from its surroundings [1, 23].

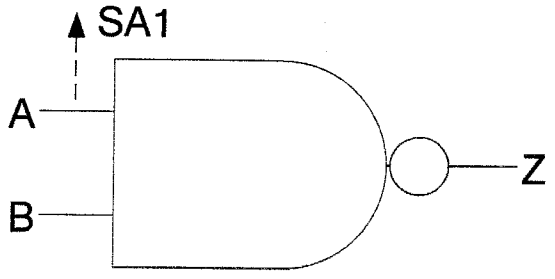
2.2 Fault Models

A fault model is used to represent the physical faults and to assist in generating fault testing methods and simulating faults. Many fault models have been proposed in [3, 13] but no single fault model accurately reflects the behavior of all possible faults. As a result, a combination of different fault models is used in generating algorithms and testing approaches for an IC. Being able to model many different types of physical faults under the logical fault model can make the fault analysis become less complicated [3]. The accuracy in representing the physical defects increases for the low level of abstraction; however, it will take a longer time in fault simulating. The advantages of a gate-level description which is also known as structural level description are its functionality and tractability in detecting faults. Since it lies between the register-transfer level (RTL) and the physical level (switch-level description and geometric description), there is a tradeoff between accuracy and the speed of the fault simulation [1]. Several fault models have been developed and applied in fault modeling, such as the stuck-at-fault model, stuck-open fault model, bridging fault model and delay fault model. Other supplementary fault testing methods are Iddq, Iddt, and thermal testing [1-2, 13].

2.2.1 Stuck-at-Fault Model

The stuck-at-fault model is the most commonly used logic level fault model due to its simplicity which is derived from the logical behavior of a circuit [11, 24]. Stuck-at-faults are referred to faults on interconnects or nets between logic gates where the lines are shorted to ground or a power line. Thus, they are also referred to as stuck-at-1 and stuck-at-0 faults. Under the faulty condition, stuck-at-0 or stuck-at-1, the affected line is assumed to have a stuck-at logic value of low or high, respectively [2].

Fig 2.1 shows a structure of a stuck-at-1 fault and the truth table of faulty and the fault-free NAND gate [11]. The input signal line A is being shorted to logic 1. A stuck-at-1 fault can be detected by a faulty NAND gate response when lines A and B are at logic 0 and 1, respectively. From the truth table the expected output Z differs from the actual output Z^*; as a result there is a fault on line A which can be detected.



A	B	Z	Z^*
0	0	1	1
0	1	1	0
1	0	1	1
1	1	0	0

Figure 2.1: A stuck-at-1 on the NAND gate and its fault-free and faulty truth table

The stuck-at-fault model can cover a single fault and multiple faults in a circuit. In a single fault assumption, there is at most one logic fault in a circuit [2-3]. It is defined as a single stuck-at-fault when a line has the following three properties [12]:

- Only one line is faulty
- The faulty line is set to logic 1 or 0
- The fault can be at the input or the output of a gate

If a circuit consists of n signal lines, it can have $2n$ possible single stuck-at-faults as there are two possibilities of the fault occurring on one signal line, or shorted to ground or a power line. In the same circuit of n signal line, there are 3^n -1 possible multiple stuck-at-faults as there are 3 possibilities for each line, stuck-at-0 or stuck-at-1 or fault free [2]. Testing for all of multiple stuck-at-faults in a circuit is impossible

and tedious due to a huge number of possible faults in the circuit. A fault collapsing technique is required to reduce the number of faults in a circuit as shown in [3]. Despite its simplicity and universality, the stuck-at-fault model has drawbacks in representing defects in the CMOS technology. It can only represent the subset of the defects of which most of the faults occur on interconnects [24-32]. Thus, this fault model is not enough to guarantee the high quality of the circuit and the detection of all of the possible types of faults [26, 33-41].

2.2.2 Stuck-open Fault Model

Besides short faults, open faults are also a cause of concern and are also the most common type of fault in most IC processes. In some cases the open faults can cause a circuit to function normally but at a slower speed. In another case, the open fault can cause a defected line to float or fix to a stable voltage level. The well-known model to cover the open faults is the stuck-open fault model [13, 42].

In the presence of the stuck-open fault, the defected transistor fails to transmit a logic value from its source to drain. The transistor can be treated as an opened switch despite all of the possible input logics to the transistor's gate. Figure 2.2 shows an example of a 2 input NOR gate in the presence of a stuck-open fault which causes an open connection in the gate. This fault prevents Q1 from conducting and resulting in a stuck-open fault in Q1.

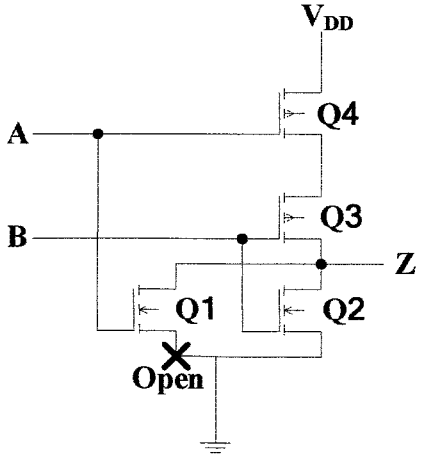


Figure 2.2: Two input NOR gate with Stuck-open

This gate consists of two nMOS (Q1 and Q2) and pMOS (Q3 and Q4). An nMOS transistor conducts when logic 1 is fed into its input, while pMOS conducts when logic 0 is fed into its input. In this NOR gate, the nMOS connected to input A is permanently off. At first, a pair of inputs, A = 0 and B = 0, sets the output Z to logic 1. With a pair of inputs, A = 1, B = 0, the output Z is expected to be at logic 0. However, the open fault has caused the transistor Q1 to remain open and the output Z to remain in logic 1 from the previous pair of inputs [2, 13]. A failure to set the output Z to logic 0 indicates the presence of a stuck-open fault in the NOR gate.

The test pattern for the stuck-open fault model can be ineffective if the patterns are not carefully selected [11]. The stuck-open fault model is a fault model targeted at open defects; however, it is not sufficient enough to represent many actual defects in CMOS circuits since predicting the behavior of open faults is quite challenging and erring-prone [13, 35, 43-47].

2.2.3 Supplementary Fault Testing

Besides voltage monitoring, the current testing is being used as a quality improving supplement to conventional testing. The supplementary testing methods are the Iddq testing and Iddt testing.

The current testing known as the Iddq test is used to detect defects in ICs through the use of supply current monitoring. It is suitable for CMOS circuits in which the quiescent supply current is normally low. A detect-free MOS transistor has a high input impedance; thus, there should be no current between the gate and the source, the gate and the drain or the gate and the substrate. However, some defects will cause a leakage current between the gate and other terminals of the transistor [11]. As a result, an abnormally high leakage current indicates the presence of defect.

The advancement of the semiconductor technology to a smaller geometry has reduced the effectiveness of the Iddq testing. At the same time, the number of transistors in a circuit can go up to millions. Each transistor in a circuit contributes a small leakage current to the conductive paths. This sum of all of the transistor leakage currents forms the total Iddq which keeps increasing significantly [2]. In the presence

of defects in an IC, the leakage currents are added up to several hundred micro amps flowing through the IC [16, 48]. The faulty leakage current is at most equal to the sum of all small transistors' currents. As a result, Iddq testing is inefficient and quite challenging to cover defects in deep submicron circuits [13].

Another current testing known as the dynamic current testing has been used to detect defects in ICs. Iddt testing is referred to as a transient or dynamic current testing which depends on switching activities during state transitions. By observing the average transient current, the Iddt testing can improve the real defect detection in an integrated circuit [2]. Figure 2.3 shows the voltage and current waveforms during the transition. When the inputs change from logic 1 (0) to logic 0 (1), the power supply current varies with the current pulses before all of the gate outputs are stabilized. In the case of any defects, the transient current increases or decreases significantly. A defect can be detected by the Iddt testing when the total amount of the charge flowing through a circuit is outside the transition margins of the circuit range.

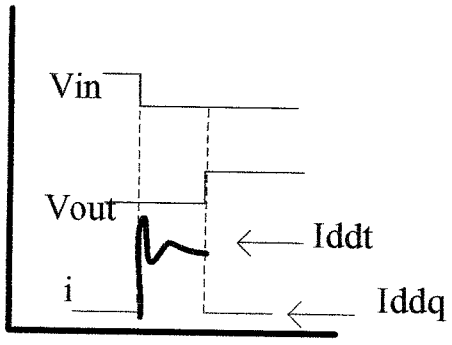


Figure 2.3: Voltage and current waveforms during the transition

However, the calculation of the dynamic current based on the logical transition is quite challenging to achieve as there are possibly many state transitions, which are caused by different path delays and possible hazards of the circuit, at the gate for a given input [14]. Moreover, it is not possible to monitor the current of each and every gate in a sub micron circuit. Another fact is when the amount of dynamic currents is very large, it is difficult to observe the variation of transient current caused by the defects [14, 49]. These facts have caused the Iddt testing not guaranteed to cover all of the possible defects in the latest high performance ICs.

2.3 Magnetic Field and Conductive Interconnection

As the integrated circuit feature sizes continue to be scaled down to nanoscale and the number of transistors increases to the millions, the number of interconnections among the devices grows as well. With this advanced technology, there are higher chances of possible faults occurrence on interconnects and logic lines [4-5, 20]. It has been shown that the electromagnetic radiation occurs from cables, connectors, wiring patterns and from the integrated circuit itself [18, 21]. In a faulty circuit, power consumption and switching activities in digital circuits can be affected by the presence of faults [10]. This affect introduces changes of the electromagnetic field during the normal switching compared to a fault free circuit. Besides the dynamic switching, currents on the supply lines of a silicon die are responsible for electromagnetic emissions [19]. Therefore, there is a meaningful correlation between the current flowing through a conductive interconnect and its electromagnetic emission.

2.4 Printed Circuit Board Overview

A PCB is a planar circuit board used to mechanically support and electrically connect electronic components using conductive pathways, tracks or signal traces etched from thin copper sheets which are on a non-conductive substrate. A printed circuit board consists of a thin copper clad board of a few micro meters thickness and non-conductive substrate made of materials, such as silicon, silicon dioxide, aluminum dioxide, sapphire, germanium, gallium arsenide, indium phosphide, an alloy of silicon and germanium [50]. In order to fabricate a circuit on a PCB, an electrical circuit layout must be initially designed and generated which will be used as a mask in the etching process to remove unwanted copper from the board.

The circuit board is required to pass through the board test once it is fabricated. This test will cover the possible faults, such as copper erosion, shorts, and opens [50]. Today, the number of electronic components mounted on a PCB is becoming denser. Consequently, the number of interconnections is also increasing and becoming crowded [4-5]. As a result, the geometry of the electrical components along with the

interconnects are scaled down to be fixed onto the small area of the board. This leads to an increase in the number of possible faults, such as shorts and opens among interconnects or signal lines. Thus, the quality control processes have become very critical during the fabrication of PCBs to ensure the fault free PCBs [51]. In order to avoid electronic components or systems from being damaged, an inspection of the PCB circuit must be provided before the components are installed. There are several PCB testing methods that have been proposed but they are either time consuming or inefficient in the era of the modern circuit design technology [52].

2.5 Conventional PCB Fault Inspection Methods

Any defects on a PCB may cause an error in an electronic system performance. It is noticed that the major causes of circuit failures are from short and open faults as discussed in Section 2.1. Since the PCB is an important key in an electronic mounting system, the reliability of the circuit boards is necessary to be inspected in order to assure the reliability of the electronic devices on which they are mounted. There are several conventional inspection methods such as visual inspection and magnetic image analysis that have been used to inspect faults on PCBs. However, these methods have their own disadvantages.

Hara *et al.* [53] successfully investigated the possibility of detecting fault patterns (short and open) by illuminating a PCB with ultraviolet rays. The PCB pattern could be detected by using fluorescent light emitted by a glass-polyimide. It was found that the pattern could be detected clearly by selecting an optical filter that could separate the emitted fluorescent light from the illumination, and using a high-sensitivity TV camera to produce an image in which the base material is bright and the pattern is dark. Fluorescent light from the corresponding parts of two PCB patterns was detected by a pair of TV cameras. These images were converted to digital images and compared to each other. The differences between the two patterns revealed the defects. However, the visual inspection or reflected light inspection method has the advantages over the detected image which is easily affected by the surface state of the pattern and required a special care to keep the pattern surface clean. It is difficult to detect defects where the image surface is dirty or blackened [51]. Moreover, the

quality of the PCB image is blurred over the edge where the vertical line area is dense [54]. In addition to image inspection methods, PCB pattern inspection machines, a Surface Mounted Device (SMD) mounter with visual positioning, soldering inspection machines and the assembled PCB visual inspection has been introduced into almost every level of PCB manufacturing to improve the PCB fault detection [55]. This visual inspection method, nevertheless, is not sufficient to cover all defects as the rapid development in the circuit design technologies is making the component density on the PCB surface become higher and higher [54-56].

In the response to the modern electronic development, a PCB fault detector based on magnetic image analysis was introduced for fast detection of a PCB [57]. The vector of the amplitude and direction of the magnetic field can be found by exciting the electrical current to the PCB. As the circuit current is flowing through the board, it couples with the conducting path and other magnetic fields emitting from the surrounding environment; the PCB will have a certain magnetic field on the board surface. The field strength depends on the size of the conducting path and the current. As a result, any defect on the PCB will cause a change in the current distribution and lead to changes in magnetic field on the PCB. The defect can be detected and located by the comparing of the normal magnetic field image pattern to the magnetic field image of the defect. However, this testing method has its own limitation in inspecting PCB faults due to high density of the conductive paths on PCBs. Besides that, this system is meant only for fast scanning purposes. In order to detect and locate PCB faults, the improvement of this method is required for further study.

2.6 Eddy Current Induced on Interconnections

When a conductive material is placed close to an alternating magnetic field, there will be an oscillating electrical current induced in the conductive material due to electromagnetic induction. These currents are defined as eddy currents [58]. Figure 2.4 shows how the eddy current can be generated. An alternating current flows through a coil producing an alternating magnetic field around it. The coil with the alternating magnetic field is brought close to a conductive material surface. Eddy currents are induced on a conductive material surface as a result of an alternating

magnetic field induction. These induced eddy currents will produce an alternating magnetic field which is in the opposite direction of the original alternating magnetic field [58]. These induced eddy currents will flow through the conductor if a closed path is provided which the currents can circulate over, due to Faraday's law of induction [59]. The presence of any discontinuity or defect in the material will disturb the eddy current flow; hence, the opposite magnetic field will be disturbed. This opposite magnetic field can be detected as a voltage across a second coil. It has been shown that the advancement of the circuit design has introduced numerous metallization layers and conductors. Therefore, eddy currents can be produced along any interconnection in a circuit when it is exposed to an alternating magnetic field. The next section will discuss the application of eddy current principle in the testing technique.

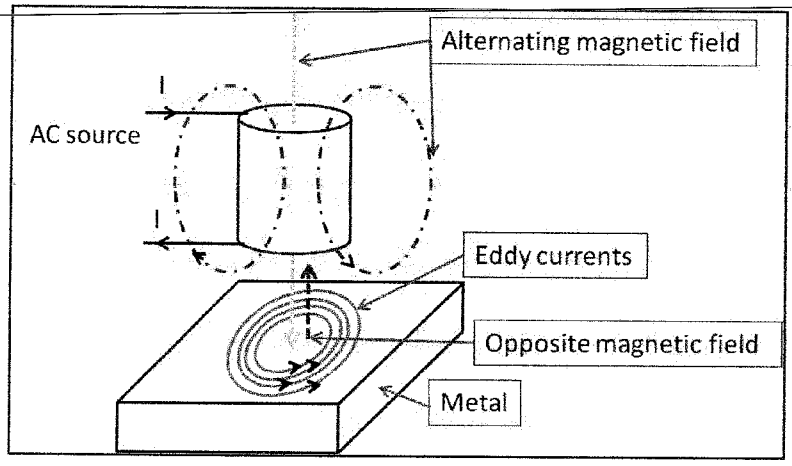


Figure 2.4: Induced eddy currents on the metal surface

2.7 Eddy Current Testing Technique

The eddy current testing (ECT) technique is the well-known method of the nondestructive evaluation (NDE) technique that is applied to evaluate the material flaws without changing or altering of the testing material [60]. A nondestructive evaluation is used to determine the discontinuities that may have an effect on the usefulness of the object. NDE may also be carried out to measure the characteristics of the test objects, such as size, dimension, configuration, and structure. The ECT method has the advantage of high sensitivity to material conductivity which depends

on many variables, such material thickness and crack. Along with a variety of methods that include dye penetrants, x-ray, and ultrasonic, ECT is also commonly used for detecting defects such as fatigue cracks in conductive materials [61]. In addition, it has been used to detect dangerous cracks on aircraft, and jet engines [62-63]. In recent researches, the ECT sensor has been applied successfully and developed to detect microdefects on microconductors of bare PCB [64-71].

In order to detect the eddy current behavior, various types of magnetic sensors have been implemented in the ECT probe. Several types of magnetic induction sensors have been described and reviewed in [72]. Among the magnetic induction sensors, a pick-up coil sensor which is also known as a coil sensor is sensitive to the rate of the change of the magnetic field over a period of time. Its output signal can be obtained by applying the Faraday's law of induction:

$$V = -nA\frac{dB}{dt}, \tag{2.1}$$

where B is the magnetic density passing through a coil with an area A and number of turns n. The above Equation (2.1) can be optimized by adjusting the dimensions of the coil, such as the size, the number of turns and the magnetic field cutting through the coil [73]. A planar coil sensor is one type of planar type electromagnetic sensors which is a flat solenoid with a minimum length. Its advantages include the flexibility of attachment to a complex surface, high sensitivity and easy construction [74]. In recent years, the planar coil sensor has become an area of interest in many researches including analytical modeling of various sensor dimension designs [74-76] and magnetic field detection applications [77-79]. It has been reported that planar coil sensors have been successfully implemented in the ECT technique to inspect the PCBs [60, 80-82].

2.8 Solenoid and Magnetoresistance as ECT's Pick-up Sensors for the PCB Open Fault Inspection

In ECT, a high sensitivity pick-up sensor is placed in the middle of the exciting coil [64-71]. There are three major criteria in choosing the most suitable magnetic sensor

to be used in the ECT technique: low field operating range, wide operating frequency, and small dimensions, in order to obtain a high spatial resolution.

Kacprzak *et al.* [67] introduced an eddy current sensor consists of a meander-exciting coil and three solenoid pick-up coils. Figure 2.5 shows the eddy current sensor with the three pick-up coils.

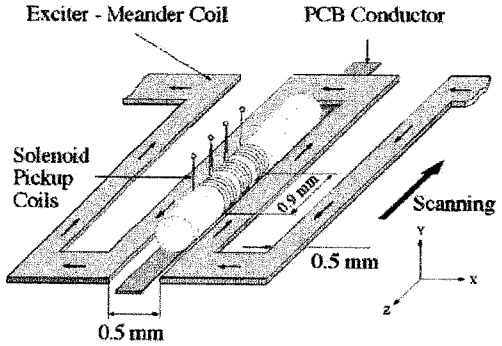


Figure 2.5: Eddy current test sensor with solenoid pick-up coils [67]

In Figure 2.5, the meander-exciting coil is said to be a long conductor with an exciting current flowing through it. The meander-exciting coil is used to excite the magnetic field onto the PCB conductor under test which is placed beneath. With this induced magnetic field, the eddy currents are generated in the PCB conductor under test. Any cut or open occurring on the tested PCB will cause a disturbance to the eddy current flow path and its distributions along the conductor [83]. The changes in the eddy current distribution lead to changes in the magnetic field density in the z direction along the tested PCB. The three pick-up coils are installed on the meander-exciting coil to detect the changes in the magnetic field in z-axis which is produced by the eddy currents on the tested PCB. It has been proved that open defects are always located between two peak values; high and low, which are obtained from the amplitude characteristic graph of the pick-up coils.

A planar magnetic sensor which is known as a Giant Magnetoresistance (GMR) has been successfully introduced in eddy current testing for surface and near-surface defect detection in conductive metals [84]. It was used to detect short surface-breaking cracks in metal and PCB fault inspection [64, 66, 69-70]. Magnetoresistance sensors can be fabricated on ICs in small sizes and a low cost. They have small dimensions, high sensitivity and low noise [85]. The eddy current probes comprise

either a large cylindrical coil or a flat spiral coil in which the GMR sensor is located on the coil axis [84-85]. Figure 2.6 shows the cross section view of the basic ECT probe consisting of a GMR sensor in the middle of a cylindrical coil.

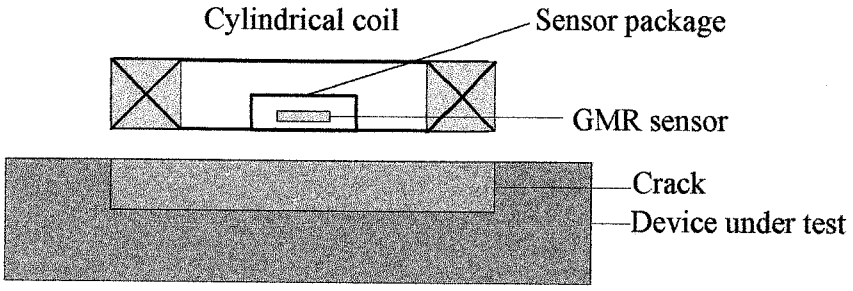


Figure 2.6: GMR sensor implanted in the middle of a cylindrical coil of the ECT probe

Yamada *et al.* [69] demonstrated the use of a spin-valve type giant magnetoresistance (SV-GMR) sensor as a magnetic sensor in the ECT technique to detect magnetic fields occurring from conductive microbeads. The ECT probe consists of a planar meander coil to which the alternating exciting current is fed and the GMR sensor is mounted on the meander coil. The exciting current generates a magnetic field surrounding the meander coil and induces eddy currents flowing in the conductive microbeads. The probe was used to scan through the conductive microbeads. The detection of a conductive microbead has shown that the determinations of the microbead diameter and its position can be obtained by observing the peak value of the ECT signal waveform which is about 60 μV peak to peak. Furthermore, the improvement on the ECT using GMR sensor in detecting cuts on PCB has been achieved by a multi sensor type GMR [64, 70]. The ECT probe consists of a meander exciting coil and a multi sensor type GMR sensor which is mounted on the axis of the meander coil. Figure 2.7 shows the multi sensor type GMR. The multi sensor type GMR consisted of 4 strips; each strip dimension was 100 μm in length and 18 μm in width. The study showed that it had a high sensitivity in the sensing axis (*z*-axis) but low sensitivity in the x- and y- axis. This multi sensor type was mounted on the middle of the meander coil.

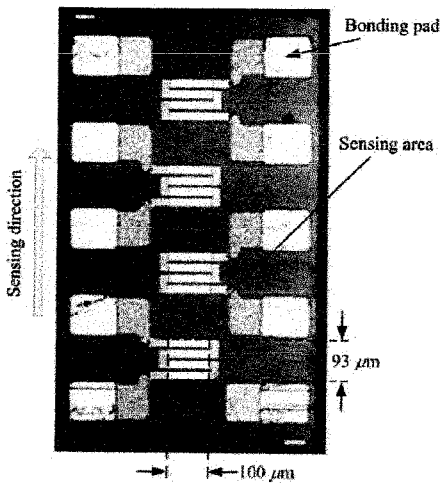


Figure 2.7: Multi sensor type in array [66]

Figure 2.8 shows the ECT probe using the above multi sensor type GMR. It has been shown that the open defect can be noticed by considering the peak values on the ECT signal. The ECT amplitude variation depends on the PCB conductor width, defect length and defect type. An additional observation is the signal to noise ratio increased gradually when the PCB conductor became wider [66].

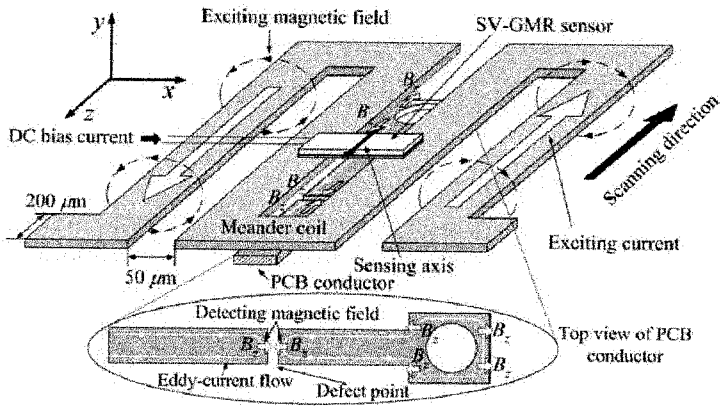


Figure 2.8: The proposed SV-GMR sensor ECT probe [66]

The ECT technique with solenoid and magnetoresistance sensor that has been discussed is used only to inspect the presence of microbead characteristic and cuts on the bare PCBs. The open defect on a bare PCB can be identified by observing the two peak values of the amplitude characteristic obtained from the pick-up sensor of the ECT. While the size and microdefect on a microbead on the PCB is identified by the

observing the peak value of the amplitude characteristic obtained from the pick-up sensor of the ECT.

2.9 Concluding Remarks

The advancement in circuit design technologies has led to a high density of electronic components and interconnects on both ICs and PCBs. As a result, the geometry of the electrical components along with the interconnects have been scaled down to be fixed onto the small area of the board. This makes the interconnections become dense not only in the ICs but also on the PCBs and leads to an increase in the number of possible faults, such as shorts and opens, among the interconnects or signal lines. Conventional fault models and supplementary fault testing cannot manage to cover all of the possible faults in the ICs. The same goes for the PCBs; in order to control the quality of the electronic systems, circuit boards are required to go through fault inspection. Many PCB fault inspection methods, such as visual inspection and magnetic image analysis have been developed. However, these inspection methods are not sufficient to cover all of the possible defects on PCBs due to the challenges of cleanliness state of the image surface and high density of conductive paths. Recently, the research on the application of detecting eddy current to inspect the metal thickness and crack has been developed. The ECT is a well-known method of a nondestructive evaluation technique. This technique has been developed further to inspect the presence of the conductive microbead characteristic and cut or open on bare PCBs. In the ECT inspection method, non-contact probes are in the form of a meander exciting coil and magnetic sensors as pick-up coils. Throughout the researches on the ECT, solenoid and magnetoresistance as ECT's Pick-up Sensors which have been successfully developed and applied in PCB open defect inspection have been presented.

CHAPTER 3
EXPERIMENTAL SETUP AND SENSOR CALIBRATION

This chapter focuses on experimental procedure and sensor calibration for PCB fault testing. It is important to characterize and calibrate each electronic component and circuit prior to full device characterization to avoid measurement errors in fault inspection. Starting with Section 3.1, this section discusses the research methodology and the process flow of the project. Next, Section 3.2 elaborates the experimental setup for devices characterization followed by Section 3.3 which demonstrates the inspection system assembling prior to experimental measurement. The following Section 3.4 discusses on the single coil and array-coil sensor characterization. In the last section, the calibration results of the circuit used in this research is discussed.

3.1 Proposed Research Methodology

In Chapter 2 under literature review, ECT principle has been applied in detecting metal properties. Few types of magnetic sensors such as superconducting quantum interference device (SQUID) sensor, coil sensor, Hall effect sensor, and GMR sensor have been successfully used in eddy current testing (ECT) in detecting metal crack [84]. Recently, the extended research on planar magnetic sensors has been conducted and applied in ECT technique for PCB fault inspection [60].

In this research, a new design of ECT probe is constructed and used in detecting short and open defects on the PCB. The probe consists of a pair of Helmholtz coils, and a planar array-coil sensor. The planar array-coil sensor is fabricated on flame retardant 4 (FR4) board of thickness 1.6 mm on which the copper-clad of thickness 32 μm is used. This sensor is placed 1.6 mm above the PCB trace and in the middle of a pair of Helmholtz coils. The sensor and the board under test are separated by FR4 substrate which acts as an insulator. The alternating magnetic field is generated by the pair of Helmholtz coils will cut through the PCB trace and induce eddy currents on

the surface of the trace. The established eddy currents will circulate on the trace surface which further induces an alternating magnetic field perpendicular to the traces axis. The vertical magnetic field will cut through the axis of each element of the array-coil sensor. From the law of induction, when a magnetic field cuts a conductor, an electrical current will flow through the conductor. Thus the voltage is induced across each coil. The induced voltage of each coil will be amplified and filtered by the band pass filter. The filtered output will be recorded and used in fault inspection analysis to differentiate the faulty and non-faulty conductive lines. Figure 3.1 shows the front view of the proposed ECT probe used in PCB fault inspection.

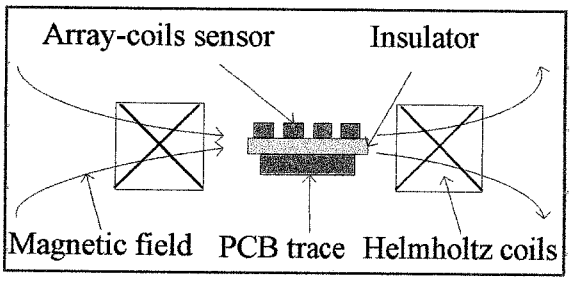


Figure 3.1: Front view of the proposed ECT probe

Figure 3.2 illustrates how the PCB fault inspection method is successfully accomplished in this project. Firstly, PCB lines is modeled and simulated in CST Microwave Studio to observe the magnetic field intensity behavior along the lines. The magnetic intensity field strengths are observed at the position of 3 mm above the lines. Once the result from simulation is fully analyzed meeting the research objectives, next the PCB traces and coil sensors are designed in ADS for layout generation and PCB fabrication. Upon completing the layouts, the PCB traces, coil sensors and array-coil sensors are fabricated on single-sided PCB. Prior to components assembling on the fault testing system, each component and circuit is separately characterized and calibrated. The complete testing system consists of PCB traces, array-coil sensors, a pair of Helmholtz coils, instrumentation amplifier circuit, active band pass filter, function generator, oscilloscope, dual power supplies, and 6 ½ digit multi-meter. All of these components' performances are tested and calibrated in order to gain optimized system performance. If the results obtained from experimental measurement are in agreement with the results obtained from CST simulation, the next stage is to analyze the experimental results of the magnetic field behavior of the faulty and non-faulty lines. Otherwise, the equipment setup stage needs to be

recalibrated and characterized. This PCB fault testing is carried out until the optimal experimental result patterns are obtained.

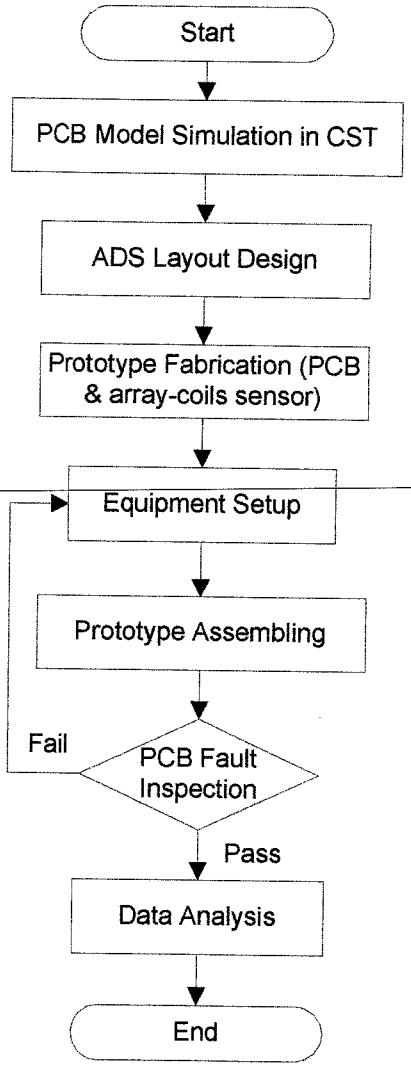


Figure 3.2: The process flow of the project

3.2 Experiment Setup

This section discusses the equipment calibration and characterization prior to fault testing. It is important to characterize each component at earlier stage before mounting all the components on the testing system. Component and circuit

characterization provide beneficial understanding of each component operation and improvement on testing results.

3.2.1 Instrumentation Amplifier Setup

An instrumentation amplifier is a type of differential amplifier composing of input buffers which are used to provide electrical impedance transformation from one circuit to another circuit. These input buffers eliminate the need for input impedance matching and thus makes the amplifier particularly suitable to be used in measurement and test equipment. It has low DC offset, low drift, low noise, and high open-loop gain. The instrumentation amplifier internally consists of three operational amplifiers as shown in Figure 3.3. Its voltage gain, A_v can be set by adjusting the value of R_{gain}. The maximum gain of this amplifier is 10,000 with R_{gain} equals to 4.94 Ω.

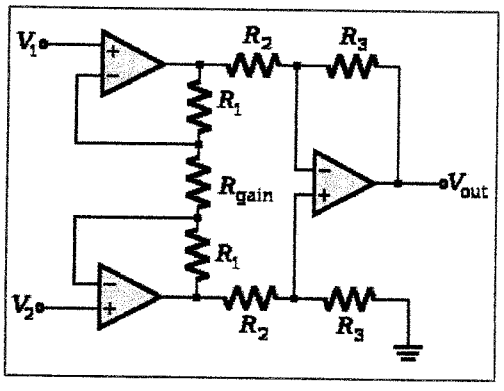


Figure 3.3: Instrumentation amplifier

In this work the instrumentation amplifier, INA129 from Texas Instrument is selected due to its high voltage gain, low power and good accuracy. The amplifier is calibrated and characterized for linearity observation in both DC and AC inputs. The small input signals in microvolt ranges, DC and AC, are used in this characterization process to emulate the actual signal from the sensor and to avoid amplifier signal distortion. The block diagram of the characterization process is shown in Figure 3.4. The amplified output voltages are measured by multi-meter and oscilloscope.

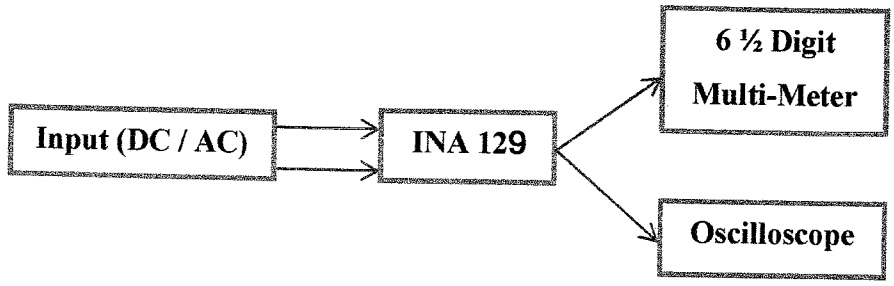


Figure 3.4: Amplifier configuration block diagram

Figure 3.5 shows the instrumentation amplifier basic connection. The gain of the instrumentation amplifier can be obtained by substituting the values of gain resistor, R_G into the following formula

$$G = 1 + \frac{49.4k\Omega}{R_G} \tag{3.1}$$

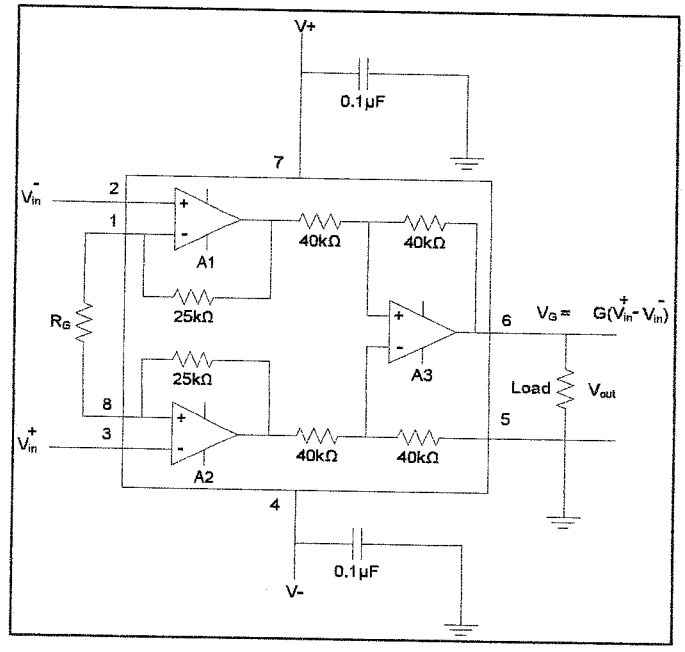


Figure 3.5: INA129 circuit for basic connection

The amplifier can be operated on power supplies ranging from ±2.25 V to ±18 V. Within this range the amplifier performance remains in good operation. In this work, the power supply voltages of ±15 V are chosen in order to obtain wider input linear range and bandwidth. At the highest gain of 10,000, its operation frequency bandwidth is 1 kHz. At the lowest gain of 1 the operation frequency bandwidth of

amplifier can go up to 500 kHz. The input frequency is chosen to be 800 Hz to make sure the input voltage is within the operation frequency range. Table 3.1 shows the amplifier gains obtained by using Equation (3.1) with the measured gain resistors.

Table 3.1: R_G and amplifier gain

Gain resistor (R_G)	Measured gain resistor	Amplifier gain
Open loop	Open loop	1
500 Ω	489.5 Ω	102
51 Ω	51 Ω	970
5.1 Ω	5.42 Ω	9115.4

Under amplifier configuration, in order to achieve low output voltage in the range of microvolt, a simple voltage divider circuit is used. A voltage divider commonly known as potential divider or resistive divider is a linear circuit used to produce an output voltage as a fraction of its input voltage. The voltage divider circuit is shown in Figure 3.6. The output voltage V_{out} can be defined as

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in}. \tag{3.2}$$

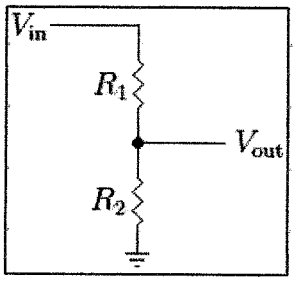


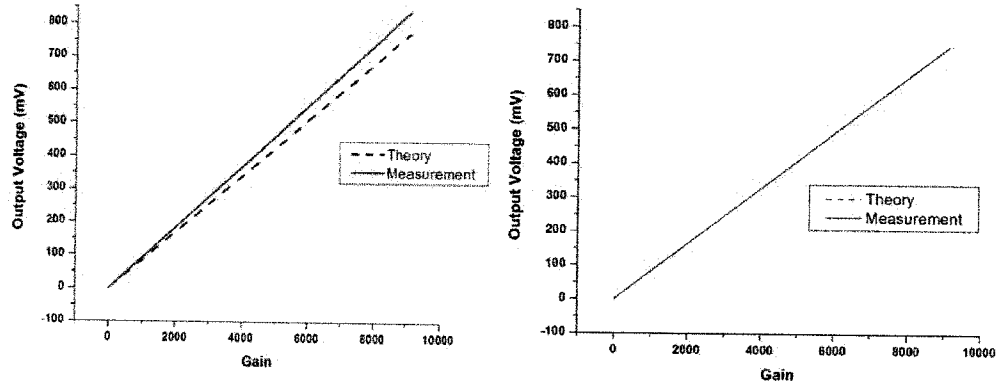
Figure 3.6: Voltage divider circuit

The voltage divider circuit produces the output voltage V_{0ut} equal to 2.10^{-4} of the input voltage V_{in}. The minimum DC input from power supply is 0.424 V and the minimum AC input from function generator is 0.412 V with the frequency range from 1 Hz to 1 kHz. From Equation (3.2), the microvolt output voltages from these two inputs are equal to 84 μV and 82.4 μV for DC and AC inputs respectively.

The output voltages of the voltage divider are supplied to the input pin 2 of the amplifier while the input pin 3 is connected to ground to produce the positive amplified output. The input voltages are amplified from the lowest to highest gains. These amplified output voltages are recorded in Table 3.2. The graphs in Figure 3.7 describe the instrumentation amplifier characteristic for DC and AC responses.

Table 3.2: Amplifier output for DC and AC inputs

	Amplifier's output (DC input)		Amplifier's output (AC input)	
Gain	Theory (mV)	Measurement (mV)	Theory (mV)	Measurement (mV)
1	0.085	0.01	0.082	0.149
102	8.67	8.835	8.36	8.38
969.6	82.42	89.52	79.5	79.9
9115.4	774.8	840	747.4	746



(a) (b)

Figure 3.7: Amplifier output responses, (a) DC output and (b) AC output

Figure 3.7 shows the linearity of the amplifier output responses for both AC and DC inputs. It can be concluded that the amplifier is capable to amplify the voltage of microvolt range precisely for both DC and AC inputs. Moreover from Figure 3.7b, the AC output responses obtained by measurement and calculation with overlapping responses and are linearly in agreement to each other. Therefore, it is suitable to integrate this amplifier circuit into the fault testing system to amplify the microvolt output signals from the magnetic planar coil sensors.

3.2.2 Helmholtz Coils Setup

A Helmholtz coil is a wire-wound device that produces nearly uniform magnetic field. A pair of Helmholtz coils consists of two identical magnetic coils placed symmetrically on each side of the experimental area facing each other along the common axis. The two coils of radius r are separated by the distance h equal to the radius r of each coil as shown in Figure 3.8. Each coil drives the equal amount of current in the same direction [59].

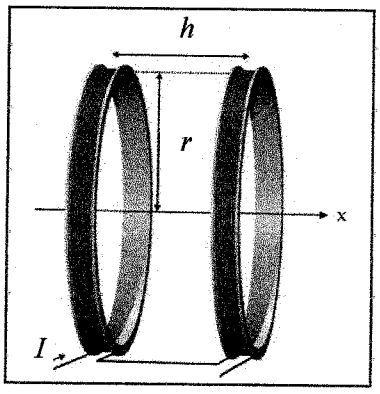


Figure 3.8: Helmholtz coil

The magnetic field produced from a pair of Helmholtz coils can be obtained by using the following formula

$$B = (\frac{4}{5})^{\frac{3}{2}} \mu_0 \frac{nI}{r}, \tag{3.3}$$

where $\mu_0 = 4\pi \times 10-7$ T·m/A (permeability of free space), n is the number of turns in each coil, I is the current flows through each coil, r is the radius of the coil. The resistance of each coil can be obtained by

$$R = \rho \frac{l}{A}, \tag{3.4}$$

where $\rho = 17.2 \times 10\text{-}9$ Ωm is the resistivity of copper, l is the length of wire, A is a cross section area of the wire. Table 3.3 describes the specification of each Helmholtz coil used in this work.

Table 3.3: Each Helmholtz coil parameters

Parameters	Values
Maximum current	2 A
Diameter of the wire	0.71 mm
Number of turns	320
Length of wire in one loop	0.478 m
Resistance (R)	6.64 Ω
Radius (r)	76 mm

Equation (3.3) can be expressed in relation to input voltage as

$$B = (\frac{4}{5})^{\frac{3}{2}} \mu_0 \frac{nV}{rR}. \quad (3.5)$$

Equation (3.5) can be obtained by applying Ohm's law for the current flowing through each coil of a resistor R with voltage supply of V. The AC input voltage signal in millivolt at 800 Hz from function generator is applied to each coil to generate the uniform magnetic field density in the middle of both coils. The magnetometer with sensitivity up to ±300 μT is used to measure the magnetic field induced in between both coils. The magnetometer is interfaced with the Magnetic Range Data Acquisition System (DAS). The Helmholtz coils input voltage is set from 100 mV to 500 mV. The millivolt range voltages can be obtained by setting the resistor R_1 to 1 kΩ and R_2 to 110 Ω in voltage divider circuit. Both the calculated and measured magnetic field densities are recorded in Table 3.4.

Table 3.4: Calculated and measured magnetic field densities induced in between both coils

Input voltage(mV)	Calculated field (μT)	Measured field (μT)
0	0	0
100	57	60.2
150	85.5	92
200	114	120.5
250	142.5	152
300	171	180
350	199.5	212
400	228	240.8
450	256.5	272
500	285	301

Figure 3.9 shows the graphs of the calculated and measured magnetic field induced in the middle of the Helmholtz coils. The two graphs are linearly in agreement to each other. However, the measured and calculated magnetic fields diverge from each other as the input voltage is increased. This error occurs due to magnetization of surrounding electrically conductive materials such as metal stand, connectors, and jumpers. Reduction of magnetic interference from the surrounding materials can be achieved by placing the Helmholtz coils in a magnetic field shielded chamber to improve the experimental data.

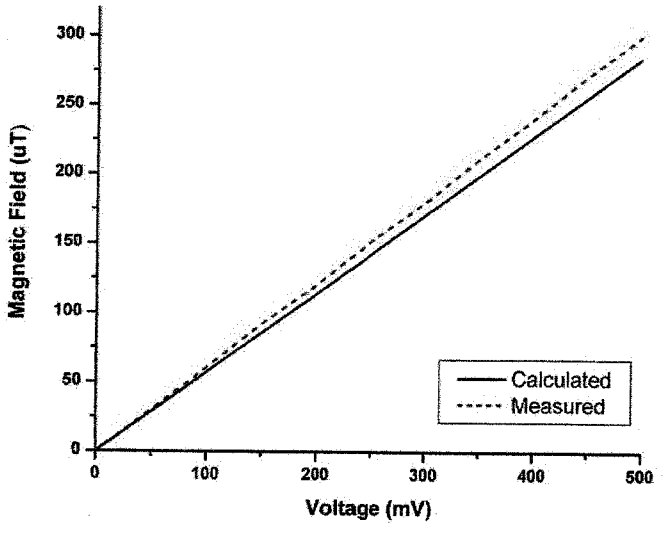


Figure 3.9: Graph of calculated versus measured magnetic field induced from Helmholtz coils

3.2.3 Active Band Pass Filter Setup

A Band pass filter (BPF) is a two-port network filter having the ability to pass all frequencies over a specified band. In addition to passive band pass filter, active band pass filter is a frequency selective filter circuit used to separate a signal or a range of signals that lies within a certain band of frequency from signals at all other frequencies. A band of frequencies is set between two cut-off frequencies known as lower frequency and higher frequency while attenuating any signals outside these two cut-off points.

Active band pass filter is a cascade of a single high pass filter and a single low pass filter with the amplifier circuit in between as shown in Figure 3.10. The low pass filter is used to discriminate the signals above and below its cut-off frequency which is at point of 70.7 % or -3 dB [86]. The signal that can be passed through the network called pass band signal whose range of frequency is below the cut-off frequency. The high pass filter is used to discriminate the signals above and below its cut-off frequency. It is the exact opposite to the low pass filter. Any frequency range below its cut-off frequency (of point 70.7% or -3 dB) cannot pass through and is known as stop band. In active filter design, the amplification circuit is used to introduce gain and provide isolation between stages of filter [87].

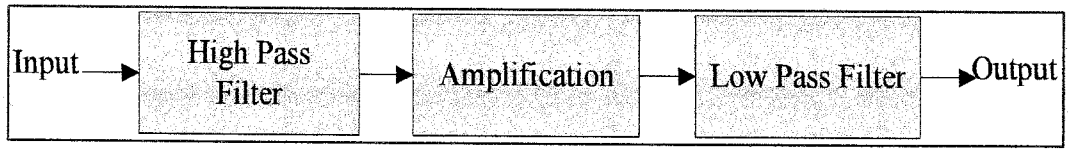


Figure 3.10: Bandpass filter circuit

Under filter setup, the RC components of the band pass filter are calculated and its circuit is designed and simulated in PSpice. The band pass filter is designed with the center frequency of 800 Hz, and voltage gain, $Av = 1$. The following formulas are used to calculate the gain, Q-factors, and center frequency of the band pass filter [88-89]

$$Av = -\frac{R_2}{2R_1} = -2Q^2 \tag{3.6}$$

$$Q = \frac{1}{2}\sqrt{\frac{R_2}{R_1}} \tag{3.7}$$

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{3.8}$$

From (3.6), $Q = \sqrt{\frac{1}{2}} = 0.7071$, and $R_2 = 2R_1$. The resistors R_1 and R_2 are selected to be 10 kΩ and 20 kΩ respectively. The capacitor values can be achieved by assuming $C_1 = C_2 = C$. From (3.8), the capacitor values of the band pass filter circuit are $C_1 = C_2$ = 14 nF. The PSpice simulation result of band pass filter is shown in Figure 3.11.

Figure 3.11 shows that the band-pass filter at -3 dB has the lower frequency at 420.6 Hz and the higher frequency at 1.572 kHz. The center frequency located at 804.129 Hz has the loss of 4.25 dBm. The multiple feedback band pass filter is designed with the low Q factor to get wide bandwidth in order to pass wide range of the input frequency from the instrumentation amplifier.

LM 358N operational amplifier is selected as the main component for the filter prototype. With the low power and wide bandwidth, this amplifier is suitable for multiple feedback active band pass filter design. The active band pass filter circuit configuration is realized as shown in Figure 3.12. The multiple feedback band pass filter topology allows the designer to be able to adjust the Q factor, and gain based on the values of resistors R_1 and R_2. Resistor R_3 in this design is used to adjust the center frequency without affecting the bandwidth and gain. However, for the low Q factor the band pass filter can work without the resistor R_3. From the LM 358N configuration the resistor R_3 can be selected as high input impedance of 10 kΩ and the output capacitor is selected to be $10C$ equal to 140 nF to obtain a smooth filter output. The parameters for this active band pass filter configuration setup are listed in Table 3.5.

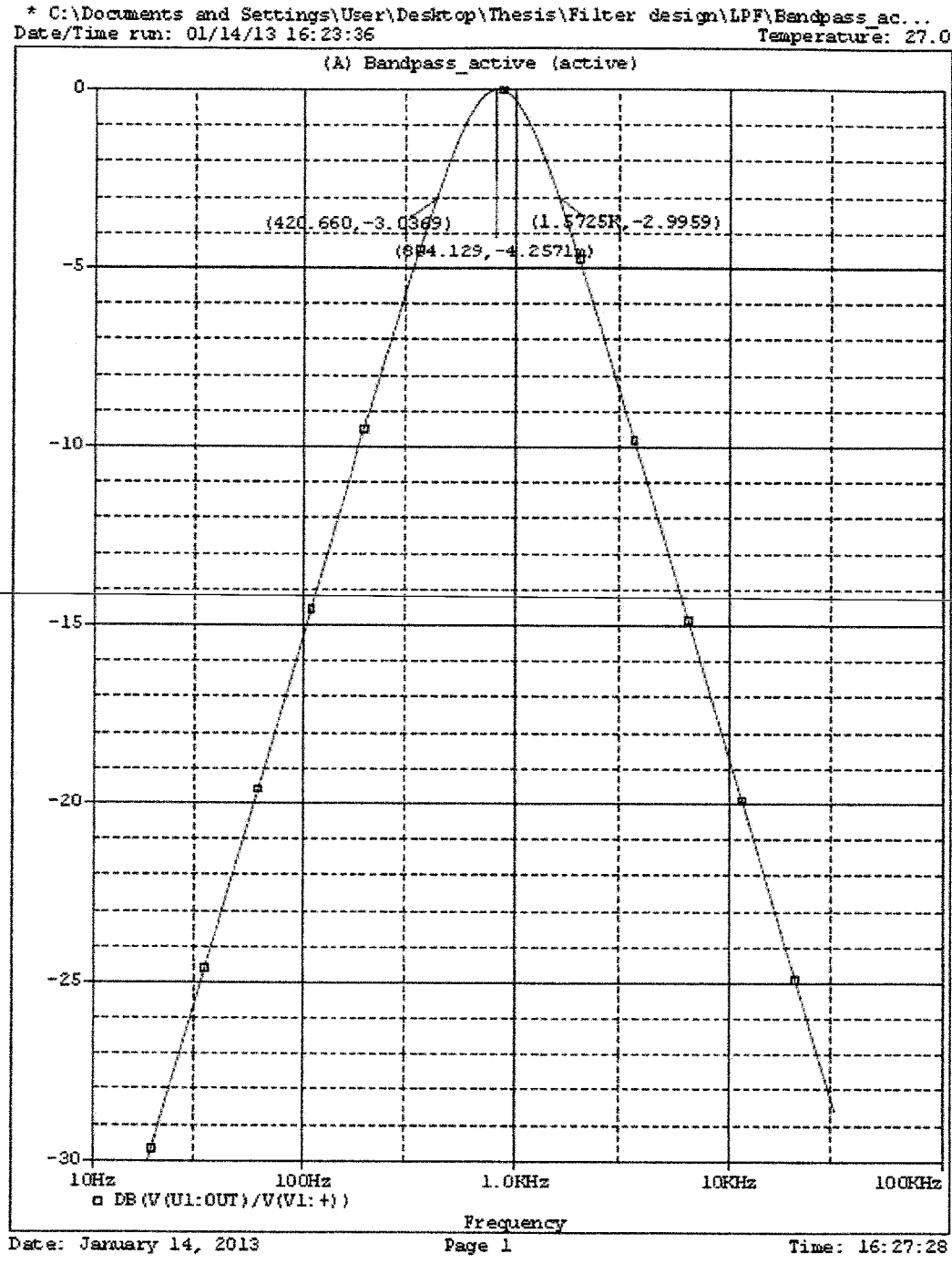


Figure 3.11: Band pass filter output response

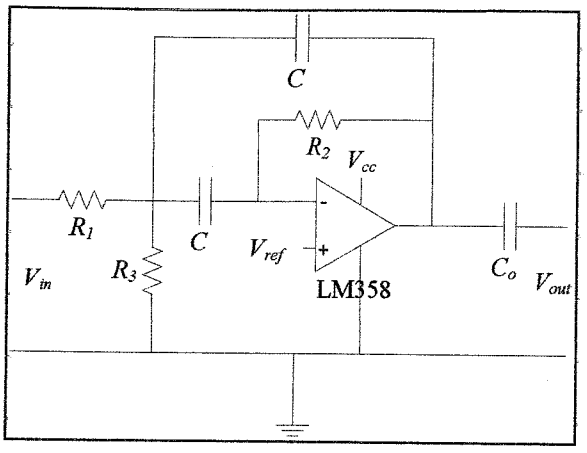


Figure 3.12: Active band pass filter configuration

Table 3.5: Active band pass filter parameters

Parameters	Values
R_1	10 kΩ
R_2	20 kΩ
R_3	10 kΩ
C	14 nF
C_0	140 nF
V_{cc}	15 V
V_{ref}	7.5 V

Figure 3.13 shows the active band pass filter circuit assembled on the veroboard. The filter is experimented with the input signal of 1 V at frequency of 800 Hz. The fast fourier transform (FFT) is used to analyze the filter's response. Figure 3.14 shows the FFT response of the filter. From the FFT graph obtained, most of the power is obtained at the frequency of 800 Hz while the power is suppressed when the frequency is higher than 800 Hz.

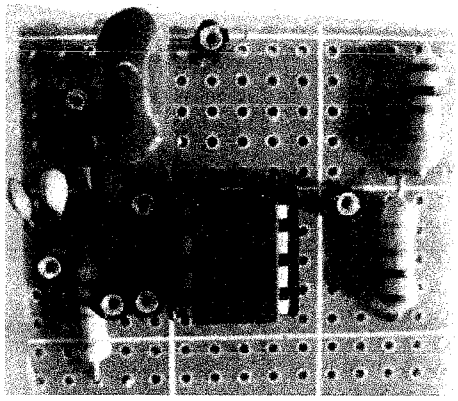


Figure 3.13: Active band pass filter on stripboard

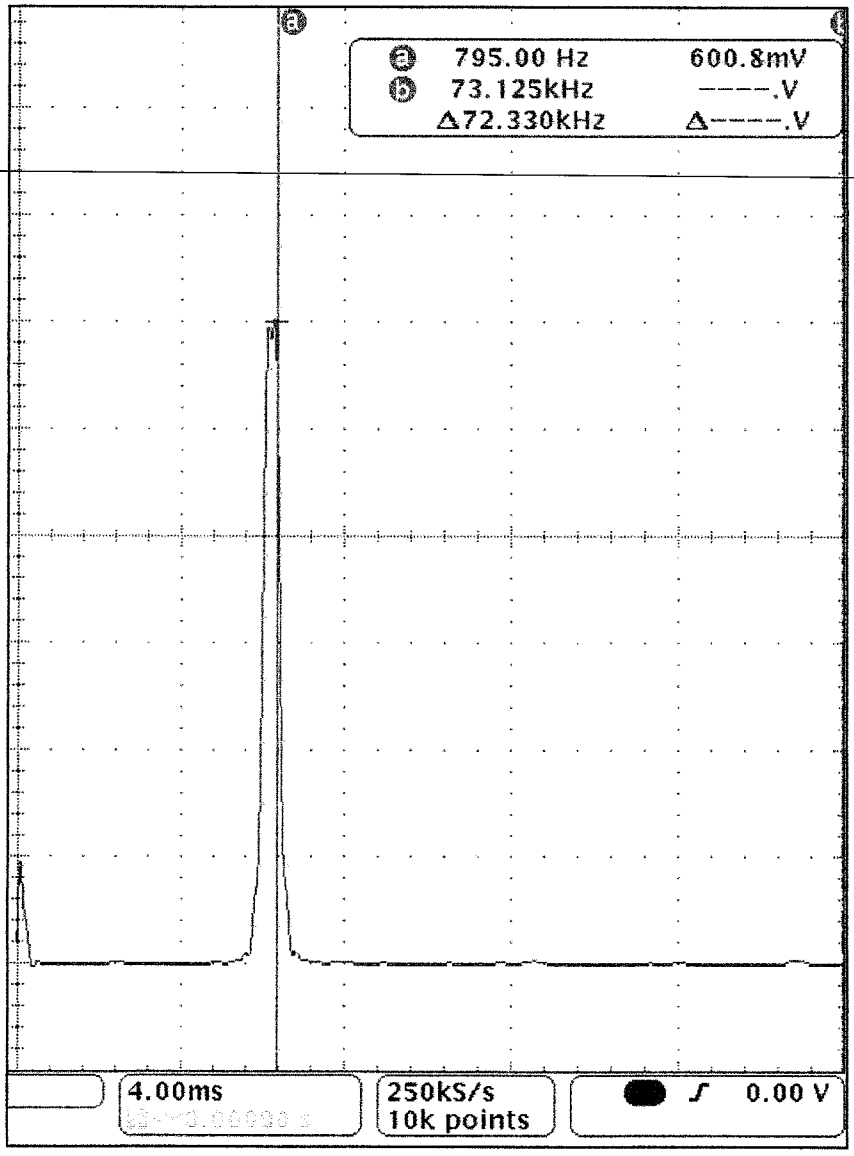


Figure 3.14: Fast fourier transform of the filtered output

3.2.4 Magnetic Field Chamber

Figure 3.15 shows a box covered by aluminum foil used as the magnetic field chamber. The chamber is designed and built to have a shielded room for equipment that generates magnetic fields and for equipment susceptible to the noise of magnetic fields. For this work, the box is covered by aluminum foil and properly grounded. This is to make sure the leakage electromagnetic field generated by the pair of Helmholtz coils inside the chamber can be reduced. Furthermore, the penetration of outside electromagnetic (EM) field can be suppressed. Theoretically, the magnetic field can only propagate in the dielectric material but not in case of a very good conductor [59]. However, if the conductor is not perfect conductor, practically the amount of the field can still penetrate in with the depth defined as skin depth [90]. The effect of the magnetic shielded box on the experiment results will be discussed in Section 3.5 of this chapter.

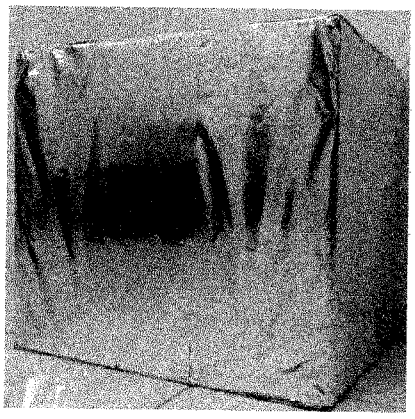


Figure 3.15: Magnetic Field Chamber

3.3 Prototype Assembling

Figure 3.16 shows the block diagram of overall testing system. In this diagram there are function generator, the pair of Helmholtz coils, devices (PCB and sensors), amplifier circuit, filter circuit, and multi-meter. All the circuits are placed inside the magnetic chamber except the function generator and multi-meter. The pair of Helmholtz coils gets the sinusoidal signal supplied by function generator at frequency of 800 Hz. The eddy current sensors and PCB lines under test are placed in the middle of the pair of Helmholtz coils. The induced output voltage from sensors will be

amplified by the instrumentation amplifier circuit. The circuit comes after the amplifier is the active band pass filter circuit which is used to filter signals from amplifier's output terminal. The filtered signals will be measured in root mean square (RMS) value in millivolts. The detail view of the fault inspection system setup is shown in Figure 3.17.

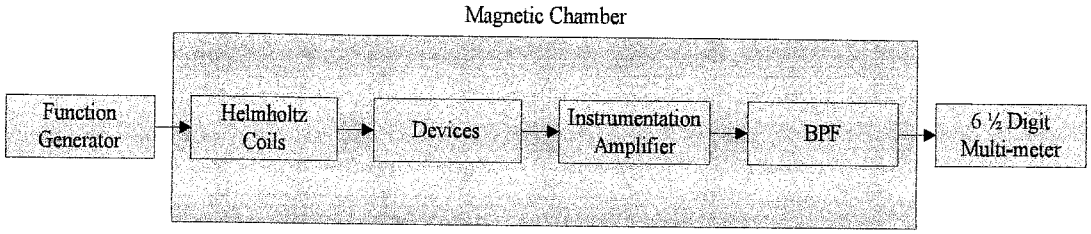


Figure 3.16: Testing system block diagram

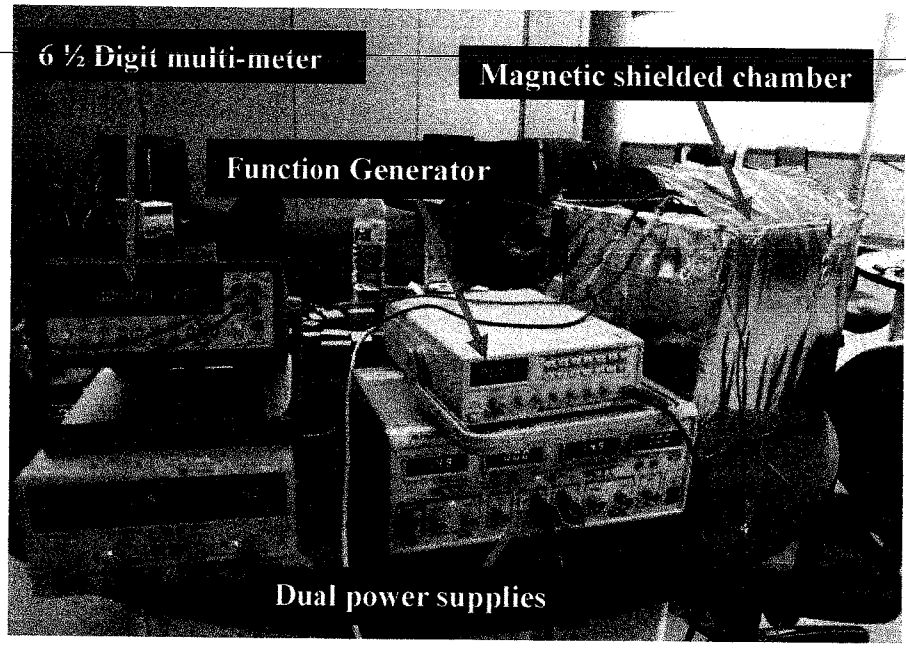


Figure 3.17: Overall system setup

In the box, there are the pair of Helmholtz coils, eddy current sensor, device under test, amplifier circuit, and active band pass filter circuit. Figure 3.18 shows the inside view of the shielded box.

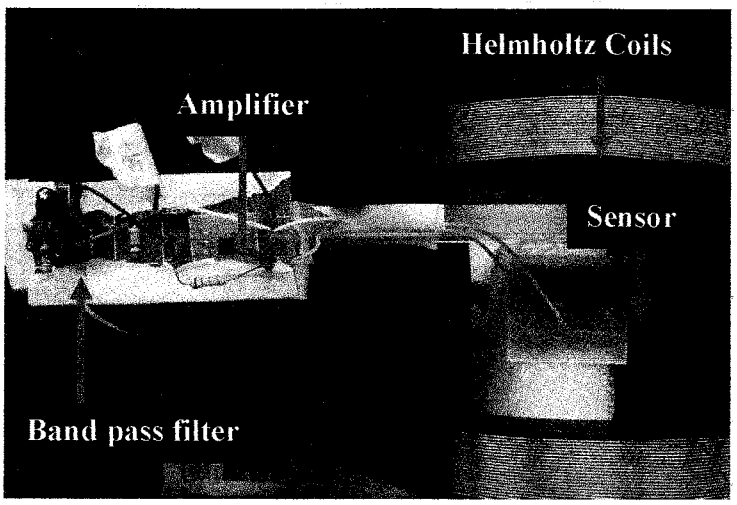


Figure 3.18: Inside view of shielded box

3.4 Planar Coil Sensors Characterization

Planar coil sensors are designed in ADS to generate the layout files for fabrication on FR4 boards. Each coil sensor is characterized in the presence of an alternating magnetic field generated by the pair of Helmholtz coils. The characterization is carried out in the environment with and without magnetic field shielded box. One of the coil sensors is selected to form the array-coil sensor for PCB fault inspection. The selection is based on the optimal sensitivity, number of turns and dimension of the coil sensor. Example of five-turn coil fabricated on FR4 board is shown in Figure 3.19. Table 3.6 shows a list of each coil sensor properties.

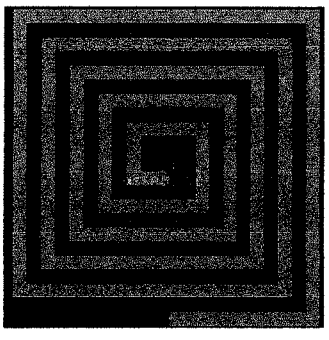


Figure 3.19: Five-turn coil sensor

Table 3.6: Coil sensor properties

Number of turns	Length (mm)	Resistance (ohm)	Area (mm^2)
3	35.1	0.063	31.23
4	56.4	0.101	61.20
5	82.5	0.148	105.75
6	113.4	0.203	167.76
7	149.1	0.267	250.11
8	189.6	0.304	355.68

3.4.1 Shielded and Unshielded Testing Conditions

This section focuses on the investigation of the effect of shielded and unshielded box to the sensor performance. Each single coil sensor is placed in the middle of the pair of Helmholtz coils. The maximum alternating magnetic field is generated by the maximum input from function generator at frequency of 800 Hz flowing through each Helmholtz coil. The magnetic flux cuts through each coil sensor inducing microvolt range voltage across the coil sensor terminals. These induced voltages are required to amplify by the instrumentation amplifier. Consequently, the amplified signals are filtered by the band pass filter. The filter's output voltages are measured and divided by 10,000. Table 3.7 shows the record of sensor characterization for unshielded and shielded testing conditions.

Table 3.7: Shielded and unshielded cases for sensor characterization

Number of turns	Shielded(μV)	Unshielded(μV)
3	53.3	1042
4	64.1	1141
5	87.1	9433
6	101	800
7	131.7	713
8	135.1	833

Due to the Faraday's law of induction, the induced voltage on a coil sensor is proportional to its number of turns. From the results obtained in Table 3.7, in the shielded condition, the induced voltage increases proportionally to the number of turns. This shows that the results obtained in the shielded case are in the agreement with the law of induction. However, in the unshielded condition, the induced voltage values are varied and high compared to the results obtained in shielded condition. This is due to the strength of external leakage magnetic field inducing extra voltage to the sensor output. As the result, the coil sensor outputs are interfered. Therefore, the experiment should be conducted in the shielded room in order to achieve optimal results.

3.4.2 Single Sensitivity of The Single Coil Sensor

In the presence of an alternating magnetic field generated from the pair of Helmholtz coils, the induced voltage from a coil sensor can be calculated by

$$V = -N\frac{d\Phi}{dt} = -NA\frac{dB}{dt}, \tag{3.9}$$

where N is the number of turns, A is the cross sectional area of the loop and Φ is the magnetic flux. In this single coil characterization, the experiment is carried out in the magnetic shielded box. The induced voltage in each coil sensor is experimented in two cases. Case one, each sensor output is measured directly without amplification. Case two, each sensor output is amplified by intrumentation amplifier. The amplified outputs are divided by 10,000 before recording in the Table. Table 3.8 presents the theoretical and measured induced voltage in each coil sensor. These induced voltages versus number of turns are plotted in Figure 3.20.

From the plot, the experimental results obtained from the sensors do agree with the theoretical results up to number of turn equal to 7. The experimental results diverge from the theoretical values when the number of turns increased beyond 7 turns. In the case without amplification, the induced voltage rises when the number of turns increased. This is due to the effect of the long multi-meter probes which are connected directly from the coil sensor to the multi-meter. The two long probes create

an extra loop through which magnetic field cuts. Thus, the high voltage is induced across the loop.

However, in the case with amplification, the induced voltage tends to slowly rise when the number of turns increased which is due to the linearity of the amplifier. The measurement results started to be constant when number of turns increased beyond 7 turns. This is due to the constant length of short jumpers connected from the coil sensor to the amplifier circuit. From Table 3.8, the sensor's output is less interfered once the sensor is connected to amplifier circuit. As a result, an improvement on reading sensor's induced voltage is achieved by implementing the amplifier circuit to the coil sensor.

Table 3.8: Induced voltage V_{rms} of each sensor

Number of turns	Theory (μV)	Measurement (μV)	
		Without Op-Am	With Op-Am
3	0.39	1.05	0.33
4	1.02	1.65	1.41
5	2.20	2.35	3.17
6	4.17	4.70	5.10
7	7.26	10.75	8.17
8	11.79	36.90	8.50

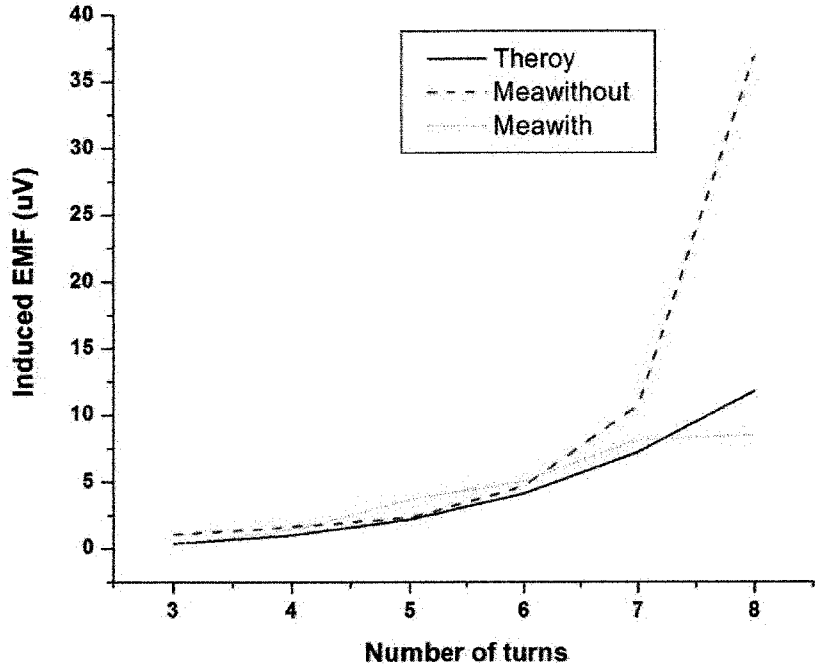


Figure 3.20: Induced voltage versus sensor's number of turns

According to the above induced voltage results from Table 3.8, the sensivity of each coil sensor can be calculated by dividing the induced voltages to the magnitude of magnetic field generated by the pair of Helmholtz coils. Table 3.9 shows the calculated coil sensors' sensitivity.

Table 3.9: Coil sensor sensitivity

Number of turns	Sensor Sensitivity (μV/mT)		
	Theory	Without Op Am	With Op Am
3	0.093	0.25	0.056
4	0.24	0.4	0.34
5	0.54	0.56	0.76
6	1	1.13	1.23
7	1.75	2.59	1.96
8	2.84	8.9	2.05

The coil sensors with number of turns from 1 to 7 have provided a good matching operation with the amplifier circuit. The single coil sensor of 5 turns is chosen to be an element of the array-coil sensor for inspecting PCB lines. Among all the coil

sensors, it has the optimum sensitivity of 0.76 μV/mT which is sufficient to detect the magnetic field of the Helmholtz coil. Furthermore, its output voltage is in the input linear range of amplifier. With the optimum area of 105.75 mm^2, the single coil sensor of 5 turns can be used to form an optimum size of 4 by 4 matrix sensor to cover the device under test.

3.4.3 Array-coil Sensor Characterization

This section focuses on the characterization of each element of the whole array sensor. The array-coil sensor is designed and fabricated on FR4 board. Figure 3.21 shows the array-coil sensor prototype of matrix 4 by 4.

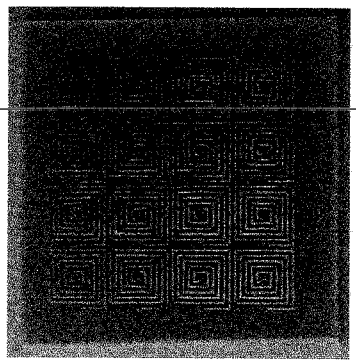


Figure 3.21: Array-coil sensor of 4 by 4

The array-coil sensor characterization is conducted in the magnetic shielded box as shown in Figure 3.22. The amplifier and filter circuits are used to amplifier and filter each element's induced voltage respectively. The sensitivities of each element of array-coil sensor are recorded in Table 3.10.

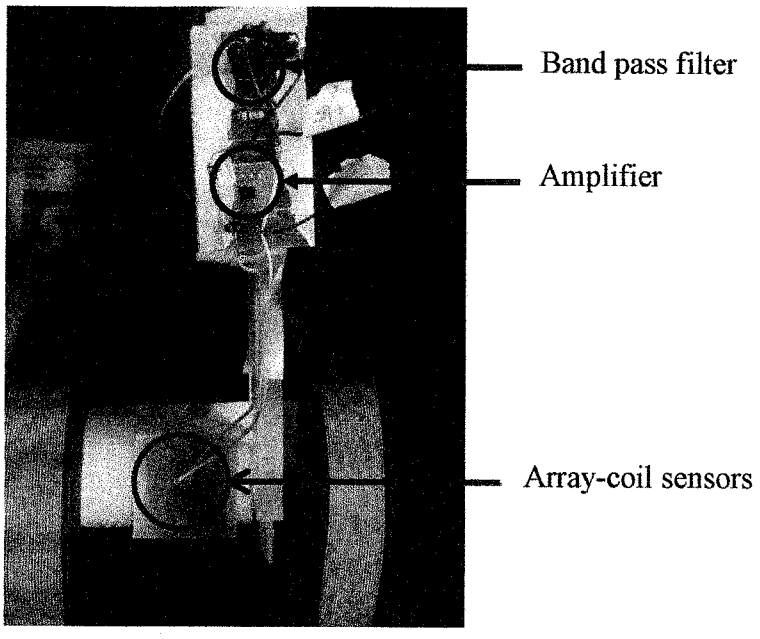


Figure 3.22: Array-coil sensors inside magnetic shielding box

Table 3.10: Array-coil sensitivity (μV/mT)

4 x 4 Array coils sensor with N = 5 turns			
0.74	0.72	0.76	0.81
0.62	0.61	0.57	0.62
0.52	0.57	0.61	0.51
0.41	0.41	0.48	0.42

Each row and column from Table 3.10 represents each element of the matrix sensor. From Table 3.10, each element's sensitivity in the same row is approximately close to each other. However, the sensitivity of the array-coil sensor drops from the 1st to the 4th row. This is due to the arrangement of array-coil sensor position, extra length of connectors or jumpers, and additional magnetizing conductive material on the board. The change in sensitivity may be due to the changes in area and shape of the jumpers which are connected from each element to the amplifier. It can be concluded that the sensitivity of the sensor is easily affected by the additional area created by external conductive wires or jumpers. Therefore, all the component parameters used in the array-coil sensor characterization are fixed in order to obtain optimal PCB fault inspection results.

3.5 Concluding Remarks

This section concludes the calibration and characterization of the components or circuits used in this work. Starting with the experimental setup, the components such as instrumentation amplifier, the pair of Helmholtz coils, active band pass filter, and magnetic shielded box configurations are realized and calibrated. The instrumentation amplifier has a maximum gain of 10,000 and is biased with DC sources of ±15 V in order to obtain wide input range. Besides that, the pair of Helmholtz coils is supplied by 10.2 V AC input of 800 Hz to produce the maximum dynamic magnetic field in the position between the two coils. The third component configuration is the active band pass filter. The filter of the center frequency at 804 Hz is designed and calibrated. It is used to filter the coil sensor's output. Next, the system is properly assembled and mounted in the magnetic shielded box prior to conducting experiment on single coil and array-coil sensors characterization. The optimum single coil of 5 turns of 0.76 μV/mT is chosen to form the array-coil sensor matrix. The sensor matrix prototype is realized and characterized prior to inspecting fault on PCB lines.

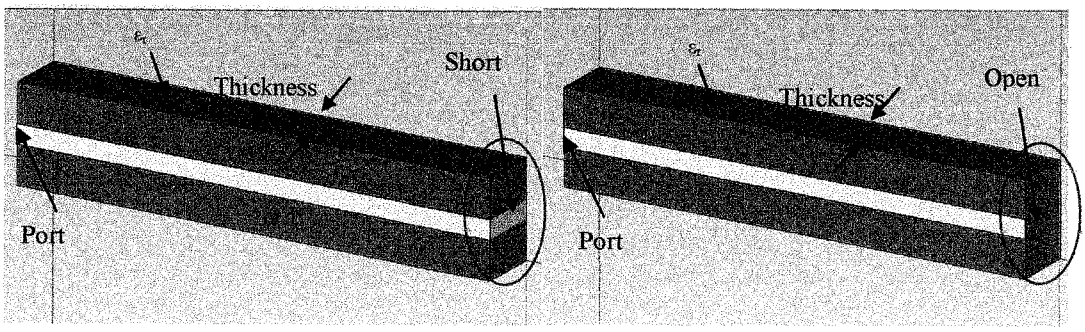
CHAPTER 4
RESULT AND DISCUSSION

This chapter discusses the simulation and experimental results of the PCB fault inspection. Section 4.1 discusses the first design of the open and short conductive line models. Section 4.2 demonstrates the second generation model design and simulation for the real PCB prototype. The following Section 4.3 focuses on the eddy current sensor modeling and 3D simulation followed by Section 4.4 which discusses the experimental setup and fault inspection of the PCB conductive lines. Finally the last section, the PCB fault inspection results are discussed and analyzed to differentiate between the faulty and fault free PCB traces.

4.1 Narrow Width Interconnect Modeling and Simulation

This section discusses the initial observation of the magnetic field intensity strength induced from the short and open circuits of the interconnect models. The short and open interconnects of an IC have been modeled in Computer Simulation Technology (CST) Microwave Studio for the purpose of observing the induced magnetic field intensity above the lines. These models have been simulated for two conditions, short and open. A very high frequency of 25 GHz is used to excite the narrow line in order to observe the resulting electromagnetic field strength surrounding the lines for both short and open conditions. This signal has the wavelength of 12 mm. A lossless narrow copper line with the length of 18 mm is modeled in CST in order to allow the signal to propagate one cycle of wavelength over the line. The line is mounted on a silicon substrate of the thickness of 65 μm and dielectric constant of $\varepsilon_r = 9.8$. The conduction line has a width of 10 μm. In the short condition, one end of the line is shorted to the substrate's ground plane. While in the open condition, the line is terminated by the open load. The models are excited by the discrete port of 1 V. The virtual probes are placed along the line at the position of 100 μm above the line. In the

simulation, the magnetic field intensities are detected by the virtual probes at different locations. Figure 4.1 shows the lines modeled in CST for the short and open conditions.



(a) (b)

Figure 4.1: Line modeling in CST: (a) short and (b) open model

At high frequency, a conductive line can be treated as a piece of transmission line as the physical dimensions of the line is approximately equal to the electrical wavelength of the signal [59]. A piece of transmission line is a distributed-parameter network, where voltages and currents can vary in magnitude and phase over its length. Such transmission lines included a coaxial cable, microstrip printed on circuit boards, wave guides etc. From the transmission line equivalent circuit model, Kirchhoff's voltage and current laws can be used to develop wave equations derived in a form of a second-order differential equation as [91]

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0, \tag{4.1}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0, \tag{4.2}$$

where $\gamma = j\beta = j\frac{2\pi}{\lambda}$ for the lossless transmission line and λ is the wavelength of the signal. The wave equations have travelling wave solutions of the following form

$$V(z) = V_0^+ e^{-j\beta z} + V_0^- e^{j\beta z}, \tag{4.3a}$$

$$I(z) = I_0^+ e^{-j\beta z} - I_0^- e^{j\beta z} \tag{4.3b}$$

The wave amplitudes (V_0^+, I_0^+) represent the $+z$ propagation wave and (V_0^-, I_0^-) of the $-z$ propagation wave. Note that the characteristic impedance Z_0 and the reflection coefficient Γ of the line is defined by [91]

$$Z_0 = \frac{V_0^+}{I_0^+}, \tag{4.4}$$

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{4.5}$$

where Z_L is the impedance of the load connected to a transmission line. Hence, (4.3) can be rewritten as

$$V(z) = V_0^+[e^{-j\beta z} + \Gamma e^{j\beta z}], \tag{4.6a}$$

$$I(z) = I_0^+[e^{-j\beta z} - \Gamma e^{j\beta z}] = \frac{V_0^+}{Z_0}[e^{-j\beta z} - \Gamma e^{j\beta z}]. \tag{4.6b}$$

Consider a transmission line terminated at a location of $z = l$ with a short circuit load i.e. $Z_L = 0$. From (4.6), it is seen that the reflection coefficient for a short circuit load is $\Gamma = -1$; it then follows from (4.5b) that the current on the line is

$$I(z) = \frac{V_0^+}{Z_0}[e^{-j\beta z} + e^{j\beta z}] = \frac{2V_0^+}{Z_0}\cos\beta l. \tag{4.7}$$

Similarly, for an open circuit load $Z_L = \infty$, Equation (4.5) gives $\Gamma = 1$. Hence, from (4.6b), the current on the line is defined as

$$I(z) = \frac{V_0^+}{Z_0}[e^{-j\beta z} - e^{j\beta z}] = \frac{-2jV_0^+}{Z_0}\sin\beta l. \tag{4.8}$$

Now, a magnitude of the magnetic field intensity, H, of a linear conductor of the length l carries a current, I, along the z-axis and is defined by [59]

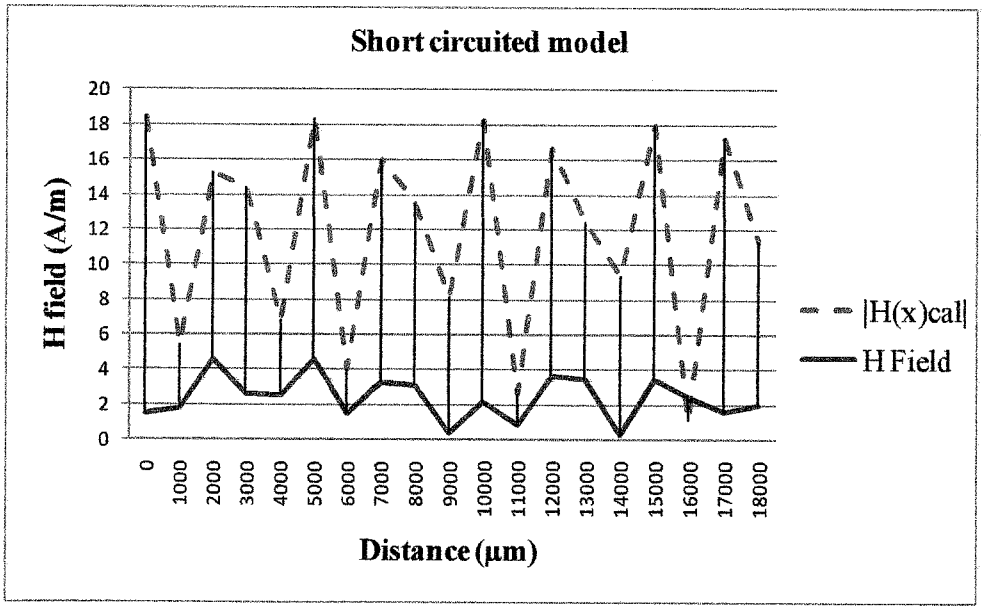
$$H = \frac{Il}{2\pi d\sqrt{l^2 + 4d^2}}, \tag{4.9}$$

where d is the distance from the line to the point of observation. If the length of the line l is much greater than the distance d, (practically 10 times bigger), Equation (4.9) becomes

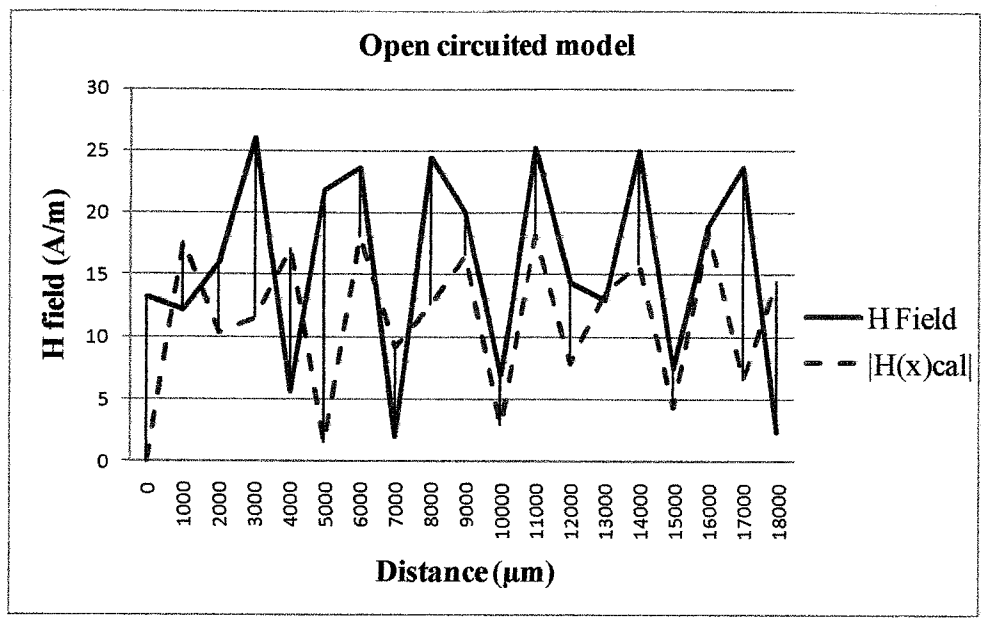
$$H = \frac{I}{2\pi d}. \tag{4.10}$$

From CST simulation, the obtained characteristic impedance of the interconnect models is Z_0 = 97.6 Ω. By using (4.7), (4.8) and (4.10) the approximate absolute magnetic field intensity, H, can be calculated. The H fields are detected by the virtual probes along the x-axis for both the short and open lines. Graphs of the H field simulation versus the absolute value of the calculated H field of both short and open

models are shown in Figure 4.2 (a) and Figure 4.2 (b), respectively. These results show that when a signal flows through a conductive line, the magnetic field intensity, *H*, is circularly induced along the lines. Both short and open models induced high ratios of the maximum over the minimum peak magnetic field intensity. In Figure 4.2 (a), the magnetic field intensity amplitudes of the short model obtained from simulation and calculation are highly different. This may be due to the effect of the image current which is induced symmetrically to the excitation current by the ground plane. In addition to the image current effect, the fringing effect may contribute to the calculation error. However, the open model shows a close agreement between the simulation and calculation magnetic field intensity. The simulation of magnetic field intensity in CST has shown the feasibility detection of the magnetic field induced from the short and open circuit models. In the next section, these models are designed and fabricated on FR4 boards in millimeter scale to obtain a strong emission of electromagnetic field which is measured by the Agilent Network Analyzer model E8363C. The strengths of the electromagnetic signal of these prototypes are detected by the array of single coil sensors.



(a)



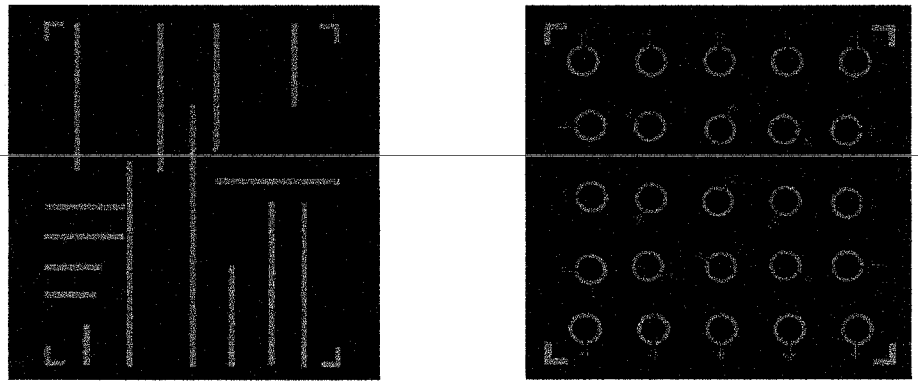
(b)

Figure 4.2: Simulation and calculated results of the H field intensity: (a) short and (b) open models

4.2 PCB Conductive Line Prototypes

The CST simulation has shown that there is a significant magnetic field intensity emitting along the micro-range lines which is illustrated in Figure 4.2. This time the PCB lines and an array-coil sensor of one turn are designed in hundred of millimeter scale to obtain a strong emission of the electromagnetic signal from the models which is detected and measured by the single coil sensor and Network Analyzer, respectively. With this large scale, one cycle of the signal of wavelength less than 500 mm can fully propagate over the lines. The layouts are designed and generated by ADS. Two types of PCB traces are identically designed for two purposes: one is short end lines and the other one is open end lines. Figure 4.3 shows the PCB layout designs in ADS, which consists of two layouts; one is random PCB lines and the other one is the array-coil sensor. These art works are fabricated on FR4 boards. The Network Analyzer is used to measure the reverse transmission coefficient (S_{12}) from a PCB line to the corresponding element of the array sensor above the lines. Insertion loss can be used to describe the reduction of a signal strength when it passes through a medium from a source to a load [92]. With this coefficient, the output of the coil

sensor can be analyzed. Figure 4.4 displays the arrangement of the array-coil sensor and PCB lines. While the PCB dimension is in hundreds of millimeter scale, the interconnects are excited by the input signal of 1 V at frequency of 1 GHz from the Network Analyzer input line. This signal has wavelength of 300 mm. The array of single coil board is placed on top of the interconnect prototype separated by FR4 substrate of 1.5 mm. The output end of the Network Analyzer is connected to the single coil sensor. The touch tone files of S_{12} are generated and obtained by the Network Analyzer at different locations; near the excitation port and near the end of the line for both the short and open conditions.



(a) (b)

Figure 4.3: PCB layouts; (a) conductive lines and (b) array-coil sensor

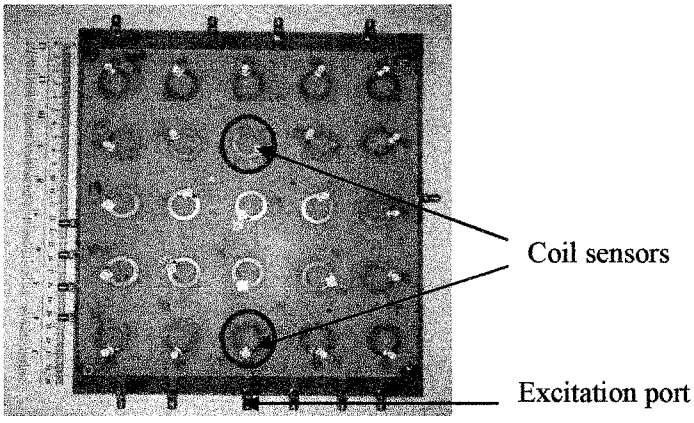
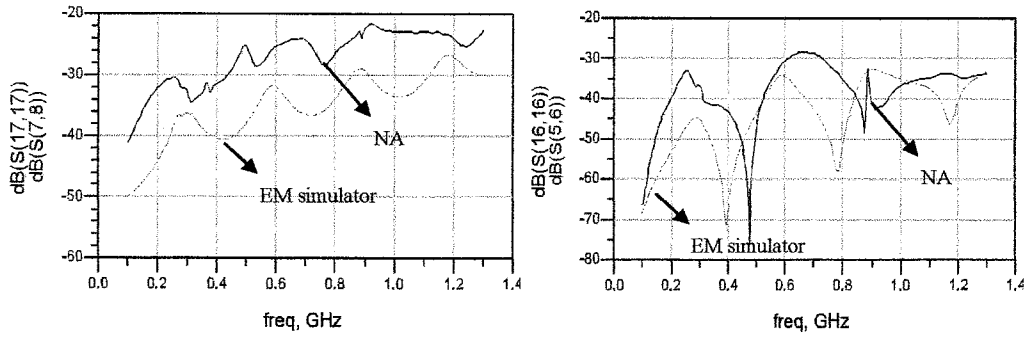


Figure 4.4: PCB prototype with array-coil sensor

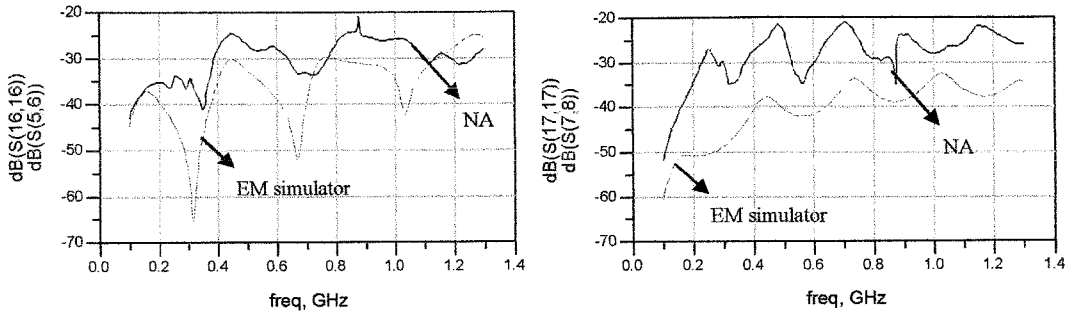
At the same time, the layouts of the prototypes are imported to the EM Simulator (SONNET) to simulate the S_{12} from the line to the coil sensors. Both touch tone files of S_{12} obtained from the EM Simulator and Network Analyzer are imported and plotted in the ADS software. Figure 4.5 shows the graphs of the S_{12} between the

conductive line and the coil sensors in the short condition. Figure 4.5 (a) and Figure 4.5 (b) show the S_{12} graphs at the location near the excitation port and at the end of the short line, respectively. The results for the open load condition are shown in Figure 4.6. Figure 4.6 (a) and Figure 4.6 (b) show the insertion loss plots of the loops near the excitation port and at the end of the open line, respectively. When a high frequency signal flows through a line, an electromagnetic field will be induced around the line. This field will cut through the coil sensors. The transmitted electromagnetic signal coefficients from the line to the coil sensor are simulated and measured by SONNET and Network Analyzer, respectively. At 1 GHz, both the simulation and measurement results have shown the high insertion loss patterns for both the short and open cases. Near the excitation port, more signals can be observed compared to the position far from the excitation port. Both SONNET and the Network Analyzer provided closed result patterns. The loss of the signal is higher than 20 dB in both cases. The mismatched of the system and low sensitivity of the single coil sensor of one turn have caused the high loss for the system. However, the Network Analyzer has shown smaller insertion losses compared to SONNET. The environmental magnetic source interferences have the effect on the signals of the PCB lines and coil sensors during the measurement by the Network Analyzer. This phenomenon has introduced additional signal to the original signal which is resulted in lower loss compared to SONNET simulation.



(a) (b)

Figure 4.5: Reverse transmission coefficient from the short line to the sensors: (a) near the excitation port and (b) at the end of the line



(a) (b)

Figure 4.6: Reverse transmission coefficient from the open line to the sensors: (a) near the excitation port and (b) the end of the line

This section has shown that in the first observation of the magnetic field using either simulation and/or prototype testing yielded results which are not encouraging enough to generate the testing result patterns for the short and open conditions. Both the Network Analyzer and EM simulator have shown that the S_{12} for the short and open copper lines to the coil sensor have a minimum power loss of at least 20 dB. It means that very small signal can be detected and observed at the sensor's side which is quite challenging to measure. These high loss signals detected by the low sensitivity single loop coil sensor of one turn can be categorized as noises arising from the magnetic surrounding environment. However, these obtained results provides an understanding for further improvement in modeling the PCBs and designing the array-coil sensor to inspect the PCB interconnect fault. The new model and prototype designs of the PCB lines and array-coil sensor are developed in the next section to achieve optimum PCB testing results.

4.3 PCB interconnect Model Simulation in CST Microwave Studio

In this section, the PCB interconnects on the FR4 are modeled in CST for the purpose to inspect the magnetic field behavior of the normal, short, and open interconnects. The structure configuration of the PCB lines used for the inspection of the magnetic field is shown in Figure 4.7. The model consists of four conductor lines mounted on lossy FR4 substrate with the ground plane and four voltage excitation ports. The thickness, the width and the length of the board are 1.6 mm, 30 mm and 50 mm

respectively. Each conductor line has the width of 300 μm, and thickness of 32 μm. The first two conductors at port 2 and port 3 from the left are treated as the short circuit model (high or low voltage level). The stuck-at-faults are located at 3 cm from the excitation port. The third line at port 1 is treated as the reference excitation conductor, and the line on the right most one at port 4 is treated as the open circuit model which is located at 2 cm from the excitation port.

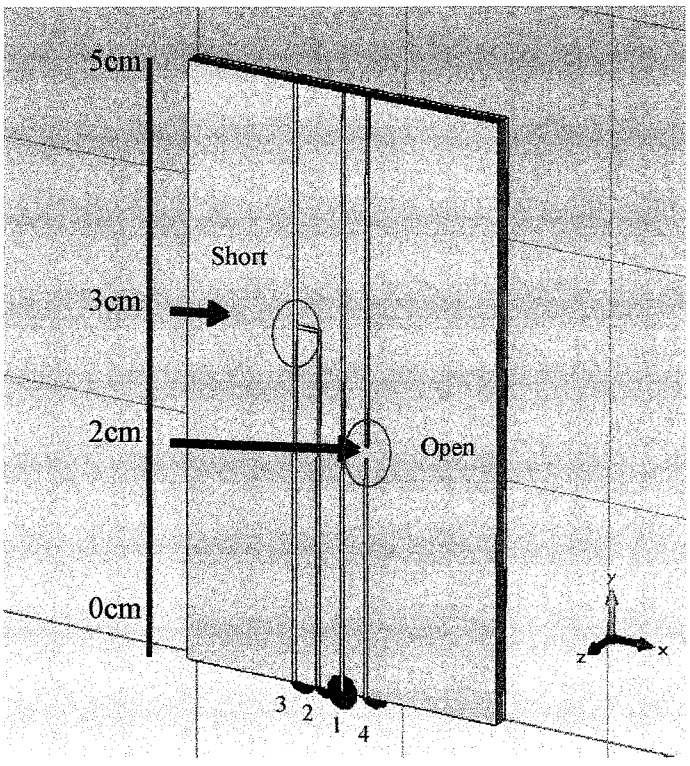


Figure 4.1: Microstrip model

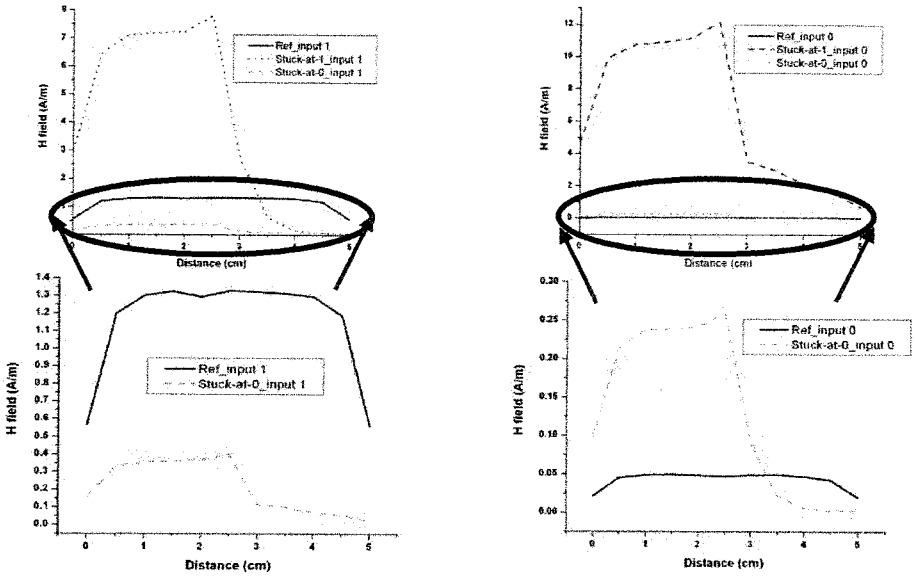
The characteristic of magnetic field intensity H in the +z-axis direction is obtained by CST simulation. The model is excited by the input signal of the frequency ranging from 0 Hz to 200 MHz in the boundary condition of the open perfect matched layer (PML) in all directions except the ground plane which is in the electric boundary. The high and low voltage levels of 3 V and 0.1 V, respectively, are excited by the discrete ports. Let P1, P2, P3, and P4, respectively, be denoted for port 1, port 2, port 3 and port 4. Several virtual probes are placed at distance of 3 mm above the first, third and fourth lines. These probes are used to detect the magnetic field intensity, H_Z, on the z-axis. The model has been simulated in five different cases. Table 4.1 summarizes the excitation input voltage level high (1) or low (0) in each case. Case one, the high input

line (P3) is shorted to the high input line (P2) and the opened line (P4) has a 10 μm cut. For case two, the high input line (P3) is shorted to the low input line (P2) and the opened line (P4) has a 100 μm cut. In case three, the low input line (P3) is shorted to the high input line (P2), and the opened line (P4) has a 120 μm cut. In case four, the low input line (P3) is shorted to the low input line (P2), and the cut on the opened line (P4) is 130 μm. In the last case, the opened line with a 130 μm cut is excited by the low voltage signal.

Table 4.1: Summary of excitation ports

Cases	Ports			
	1	2	3	4
1	1	1	1	1
2	1	0	1	1
3	0	1	0	1
4	0	0	0	1
5	x	x	x	0

The simulations have been performed on several conditions such as a normal reference line with inputs of high and low, shorted lines with inputs of high and low, and opened lines with different gaps on the line. The virtual probes at 3 mm above the lines in the $+z$ direction are used to detect the presence of the H field intensity at each specific location along the lines. Figure 4.8 illustrates the magnetic field intensity along the line in the condition of the normal and the shorted lines. Figure 4.9 illustrates the magnetic field intensity along the line in the condition of opened line when the open gap is less than 120 μm. And Figure 4.10 shows the magnetic field intensity along the line in the condition of the opened line when the open gap is greater than 130 μm.



(a) (b)

Figure 4.2: Magnetic field intensity behavior of the short and the reference line for the input (a) high and (b) low

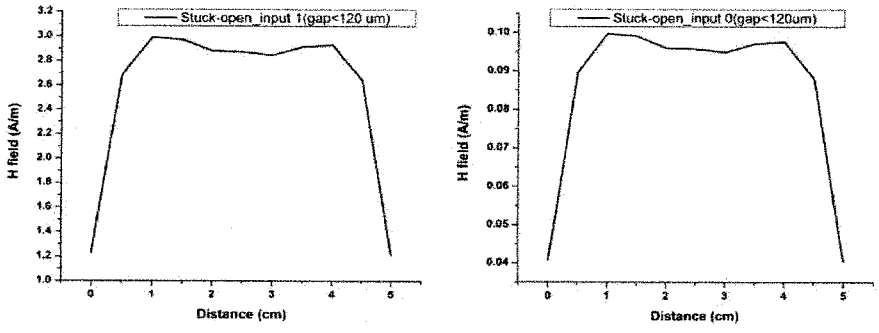


Figure 4.3: Magnetic field intensity behavior for an opened line (cut < 120 μm)

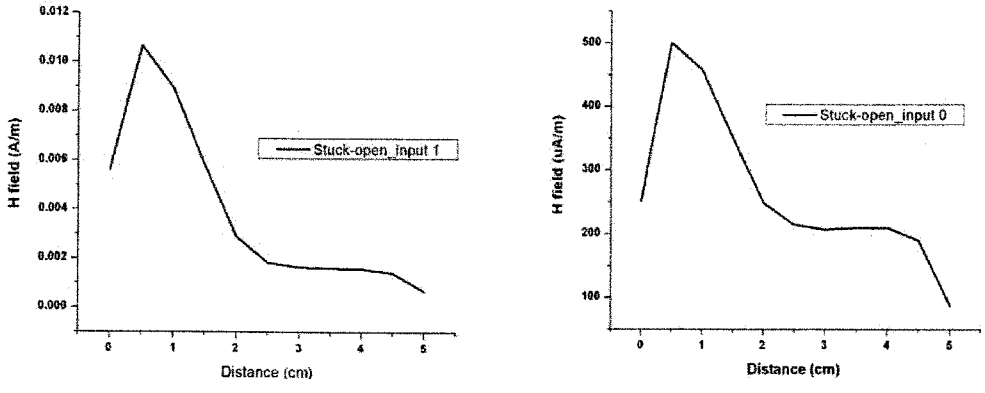


Figure 4.4: Magnetic field intensity behavior for an opened line (cut > 130 μm)

From the simulation results, normal line or reference line induces a constant magnetic field intensity *H* regardless of high or low excitation signal. The *H* field of the high input line which is shorted to the high (low) input line is greater (lower) than *H* field produced by the high input reference line. In the shorted condition, the shorted line induces peak and small magnetic field intensity near and after the short point at 3 cm as shown in Figure 4.8.

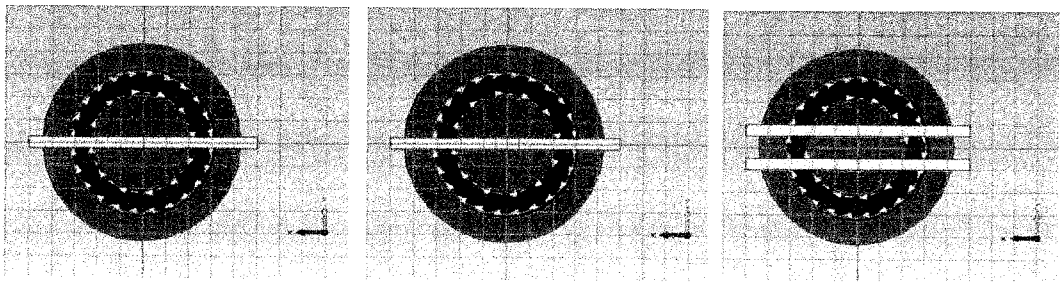
Simulations on opened lines (stuck-open) for case four and five have been carried out with different opened gap dimensions on the line at location 2 cm. From simulations when the gap is less than 120 um, the magnetic field intensity *H* has the same pattern compared to magnetic field intensity induced from the reference line for both high and low input. Since the gap is small, there is a coupling between the two pieces of broken lines. This is complex to differentiate whether the line has an open defect or not. Figure 4.9 shows the magnetic field intensity, *H*, graphs when the opened gap is less than 120 μm. However, other simulations on the opened line of the gap greater than 130 um provide a significant *H* field behavior. Figure 4.10 shows that the opened circuit line induces very small value of *H* field intensity compared to the reference line. In the presence of an opened gap bigger than 130 μm, the opened line induces peak and low magnetic field intensity near and after the opened gap at 2 cm.

Thus, these simulations have shown a significant behavior of a magnetic field intensity induction from the lines (reference, short and open). When there is a short or an opened gap along the PCB line, the difference between the peak values around the defect point position, maximum and minimum magnetic field intensity, can be observed with the comparison to the magnetic field intensity of the normal (reference) line which is constant along the line. The current path of the normal line is changed once there is a short between the normal lines. This change in current direction from y-axis to x-axis introduces the peaks in magnetic field intensity around the defect point compared to the normal line's magnetic field which is constant. In the open condition, the current path of the normal line is cut off. The two pieces of line couple to each other allow a small current to flow through the line when the cut is greater than 130 μm. The coupling effect introduces the peaks in magnetic field intensity compared to the normal line's magnetic field which is constant. The variation of the

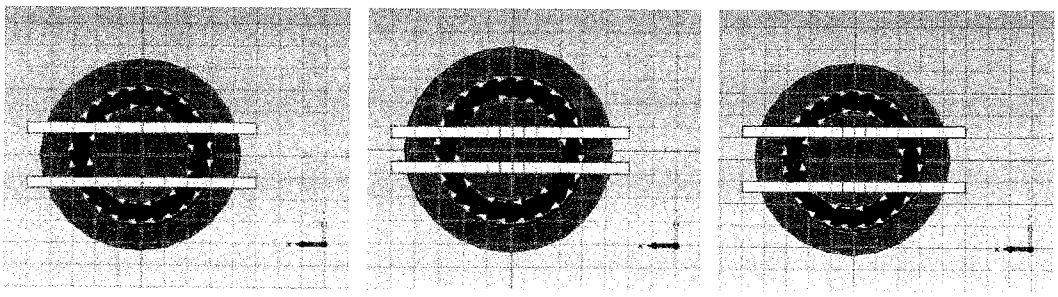
magnetic field intensity in the short and open conditions is detected by the magnetic sensor which is simulated and discussed in the next section.

4.4 Eddy Current Sensor Model in CST EM Studio

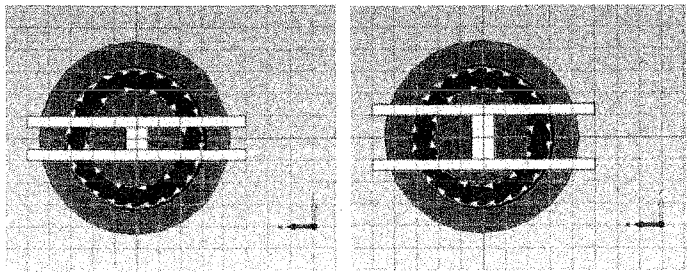
The eddy current sensor is modeled in CST as a multi-turn coil. The eddy current effects can be obtained by observing the polarity changes across the multi-turn coil placed above the non-defective and defective conductive lines. In this simulation, a single coil is placed at 1.5mm above a conductive line. The coil has the diameter of 4.4 mm with 1000 turns and the current flowing of 0.1 A at 800 Hz. This coil is designed to have a high number of turns in order to effectively study and detect the changes of the alternating magnetic field above the conductive lines. The conductive line is modeled with the dimensions of 500 μm width, 10 mm length and 1 mm thickness. The simulations are conducted for 8 cases: single normal line, single open line, two normal lines with a line spacing of 1 mm, two normal lines with a line spacing of 2 mm, two open lines with a line spacing of 1 mm, two open lines with a line spacing of 2 mm, a pair of short lines with a line spacing of 1 mm, and a pair of short lines with a line spacing of 2 mm. The models are shown in Figure 4.5.



(a) (b) (c)



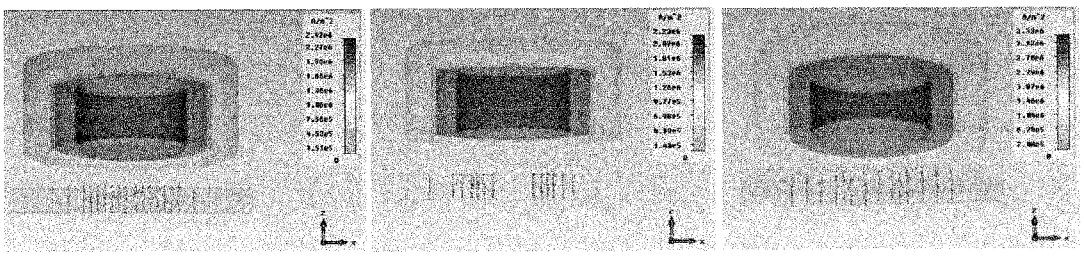
(d) (e) (f)



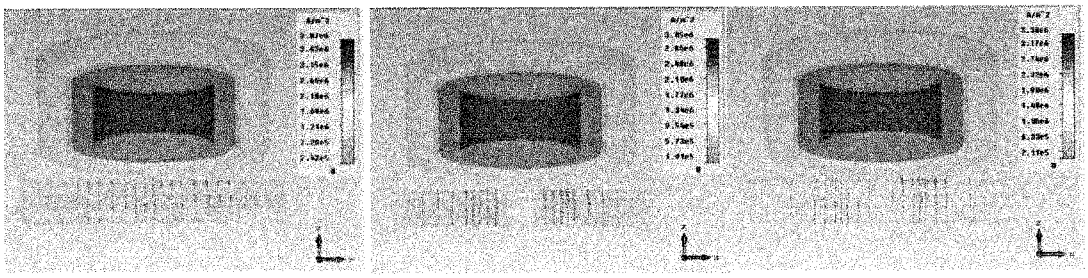
(g) (h)

Figure 4.5: Eddy current sensor for (a) one normal line, (b) one open line, (c) two normal lines of 1 mm spacing, (d) two normal lines of 2 mm spacing, (e) two open lines of 1 mm spacing, (f) two open lines of 2 mm spacing, (g) a pair of short lines of 1 mm spacing, and (h) a pair of short lines of 2 mm spacing

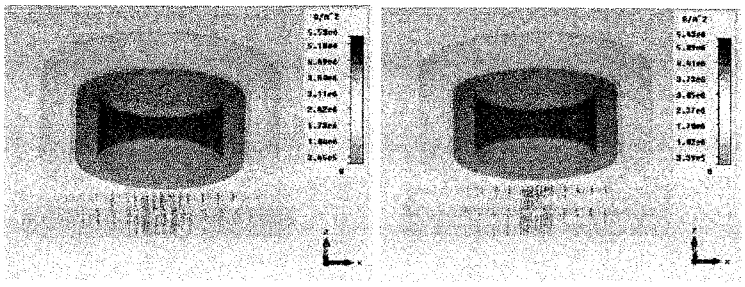
These models have been simulated in CST EM Studio in order to observe the density of the eddy currents being induced in the conductive lines and to record the voltage changes across the coil sensor. Figure 4.6 displays the 3D results of eddy current density for these 8 cases which have been extracted from CST EM Studio.



(a) (b) (c)



(d) (e) (f)



(g) (h)

Figure 4.6: 3D simulation results of eddy current behavior; (a) one normal line, (b) one open line, (c) two normal lines of 1 mm spacing, (d) two normal lines of 2 mm spacing, (e) two open lines of 1 mm spacing, (f) two open lines of 2 mm spacing, (g) a pair of short lines of 1 mm spacing, and (h) a pair of short lines of 2 mm spacing

From the above Figure 4.6, the density of the eddy currents on the continuous line (normal line) are distributed fairly on the parts of the line that are exposed to the magnetic field as shown in Figures 4.6 (a), 4.6 (c) and 4.6 (d). When there is a gap or discontinuity on the conductive line, the distribution of the eddy currents on the line are disturbed. In Figures 4.6 (b), 4.6 (e), 4.6 (f), more eddy currents arise around the gap. For the shorted line, the current density is high compared to other cases at the short point between the two normal lines.

Figure 4.6 shows that on the surface of the normal or continuous conductive lines, the density of the eddy currents is well distributed along the lines. While with any extra metal or discontinuity on the lines, the eddy current path is disturbed. The disturbance of the current's path causes changes in the coil voltage. The density of the eddy currents is high when there is a short (extra metal) between the lines. The density of the eddy currents is low when there is an open or discontinuity on the lines. A high density of eddy currents would induce a high voltage across the coil compared to the normal (continuous) lines. And a low density of eddy currents would induce a low voltage across the coil compared to the normal (continuous) lines. Table 4.2 shows the induced voltages for each condition. From Table 4.2, the induced voltage from the one normal line is lesser than from the two normal lines. The induced voltage is less for the case of the two lines having two cuts as compared to the two normal lines. Whereas, the shorted line induced a higher voltage values as compared to the normal and opened lines. Therefore, the difference between the induced

voltages from the normal lines and from the shorted lines is highly negative in the values at the point of the defect. Whereas, the difference between the induced voltages from the normal lines and the opened lines is highly positive in their values at the point of the defect.

Table 4.2: Induced coil voltages at frequency 800 Hz

Figure	Line condition	V_{rms} (mV)
4.12 (a)	One normal	0.292
4.12 (b)	One open	0.2
4.12 (c)	Two normal (1 mm)	0.708
4.12 (d)	Two normal (2 mm)	0.784
4.12 (e)	Two open (1 mm)	0.496
4.12 (f)	Two open (2 mm)	0.555
4.12 (g)	Shorted line (1 mm)	1.237
4.12 (h)	Shorted line (2 mm)	1.75

4.5 PCB Fault Inspection by ECT

In this section, the experiment on PCB fault inspection is setup and experimented. The single fault and two faults at a time inspection are observed and experimented. Prior to PCB fault inspection, the induced voltages of the reference or fault free boards are detected by the array-coil sensor matrix. The voltage matrices of the fault free boards are used as the ground truth values to compare with the induced voltage of the faulty boards.

4.5.1 PCB Inspection Setup

Having modeled and simulated the PCB lines and the eddy current sensor in CST, the PCB design layouts from the ADS are sent for fabrication on FR4 boards. Three sets of PCB lines have been fabricated for normal, open and short lines. These boards are passed through ECT to inspect the changing induced voltage patterns in the condition of faulty and fault-free conditions and to locate the potential fault on the PCB lines. Figure 4.7 and Figure 4.8 show the PCB normal line prototypes on the FR4 boards.

The PCB lines have been fabricated in two widths; 300 μm and 600 μm with different line spacing of 4 mm, 2 mm and 1 mm.

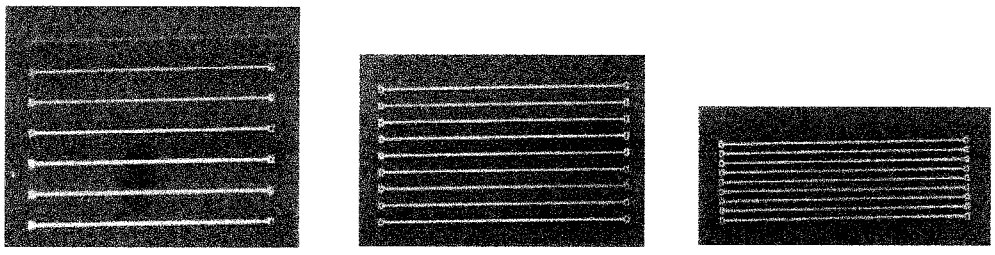


Figure 4.7: Line width=300 μm and the line to line distance of 4 mm, 2 mm and 1 mm respectively

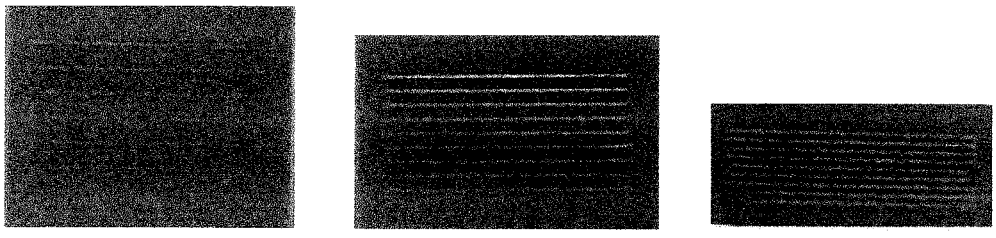
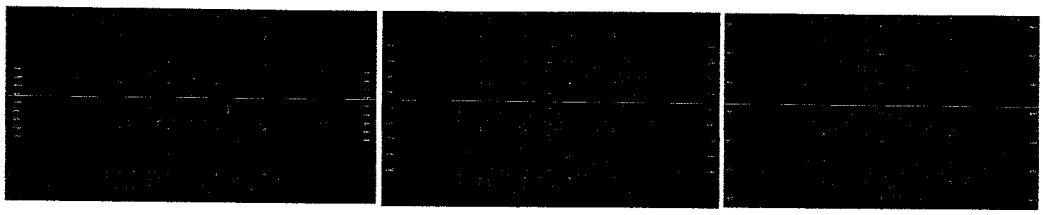
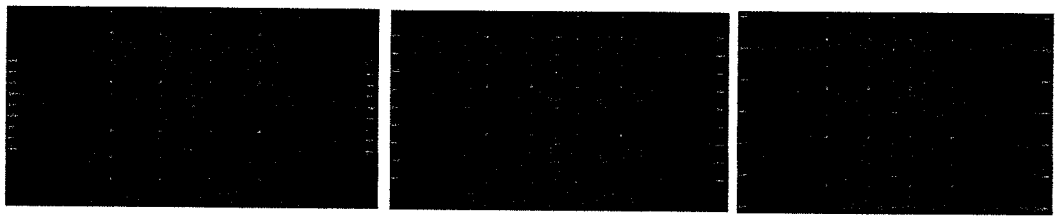


Figure 4.8: Line width=600 μm and the line to line distance of 4 mm, 2 mm and 1 mm respectively

The fabricated PCB lines which are shown in Figure 4.7 and Figure 4.8 have been inspected under three conditions: fault free, single fault at a time and two faults at a time. The array-coil sensor of 4 by 4, composed of single coil sensors of 5 turns, is placed on the top of each PCB. Figure 4.9 displays the six fault free boards with the array-coil sensor lying on top of each board. A single element of the array-coil sensor could cover at most 5 lines, 3 lines, and 2 lines for the line spacing of 1 mm, 2 mm, and 4 mm, respectively.



(a) Line width=300 μm and line to line distance of 1 mm, 2 mm and 4 mm respectively



(b) Line width=600 μm and line to line distance of 1 mm, 2 mm and 4 mm respectively

Figure 4.9: PCB line width of, (a) 300 μm, (b) 600 μm with array-coil sensor 4 by 4

A single fault at a time and two faults at a time are injected to the fault free PCB lines of Figure 4.9. The two types of fault are short and open. For a single fault at a time, it occurs on the third and fourth lines for the short fault and the third line for the open fault. In addition to a single fault at a time, two faults at a time has an extra fault located on the fifth and sixth lines for the short fault and the sixth line for the open fault. The PCB fault injection on the PCB lines is shown in Figure 4. 10.

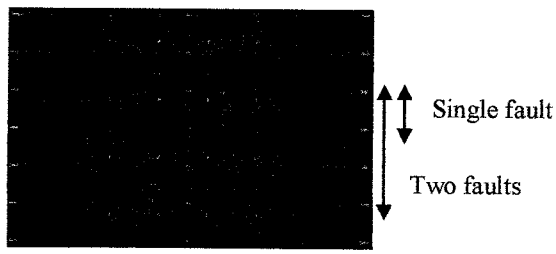


Figure 4.10: PCB fault injection on PCB lines for a single and two faults at a time

4.5.2 Experimental Results

Each of the above setup boards is placed in the middle of a pair of Helmholtz coils as discussed in Chapter 3, Section 3.4. The PCB lines are exposed to an alternating magnetic field generated by the pair of Helmholtz coils. In the presence of the

alternating magnetic field, eddy currents are induced on the conductive lines. These eddy currents induce an alternating magnetic field perpendicular to the PCB lines. This field cut through the axis of the array-coil sensor which is placed at 1.6 mm above the PCB lines. The induced voltage values from every element of the array-coil sensors is amplified and filtered before recording. The output signals are measured in RMS. In this experiment, each board along with the array-coil sensor produces a 4 by 4 induced voltage matrix. The six induced voltage matrices under the same testing condition are summarized in one table. The records of the induced voltages from all reference boards (fault free) are used as reference voltage values which are compared to the induced voltage values from the faulty (short and open) boards. Each board is tested for more than three times in order to get the average induced voltages. The average values of the induced voltages are displayed in tables and used throughout the fault analysis process.

Having been discussed in Section 4.5.1, the PCB lines have been fabricated in two widths; 300 μm and 600 μm with different line spacing of 1 mm, 2 mm, and 4 mm. The reference or the normal boards are assumed to be fault free boards. Firstly, the fault free boards are inspected and the output induced voltages are recorded. Secondly, the single fault inspection is conducted and the output induced voltages are recorded. Thirdly, the two faults at a time inspection is experimented and the output induced voltages are recorded. Lastly, these recorded output voltages are analyzed to generate patterns to differentiate between faulty and fault free boards and to locate the potential fault on the lines.

4.5.2.1 Ground Truth Data

The boards in Figure 4.7 and Figure 4.8 are used as the reference boards (fault free boards). The induced voltages from these boards are tested and recorded for several times until the results are stable before proceeding further for the PCB inspection. Once the calibration of the testing system is completed, the inspection of the fault free boards is conducted more than three times. The three stable induced voltage values from each board are recorded in three tables. These tables are used to generate the table of the average induced voltage values. The average induced voltage values of

each matrix from each board are used as the ground truth data or reference values in order to carry out fault analysis patterns. Table 4.3 provides the first, second, and third reference board testing results and the average induced voltages from the three testing results.

Table 4.3: Average induced voltages for reference (fault free) boards

First test

Line width	4 x 4 Array-coil sensor with N = 5 turns											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	150	230	218	161	154	142	190	184	126	162	187	175
	145	223	154	136	123	151	126	150	163	162	115	112
	126	113	167	122	126	138	137	121	134	131	177	131
	136	142	167	168	133	140	151	153	117	101	122	129
600 µm	201	234	226	232	165	244	237	227	161	355	233	248
	230	237	213	183	158	210	242	161	135	247	103	141
	109	132	220	134	116	164	236	159	134	126	226	177
	171	138	154	125	98	106	106	133	119	110	109	131

Second test

Line width	4 x 4 Array-coil sensor with N = 5 turns											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	180	215	196	210	212	207	216	199	150	192	195	202
	170	185	155	145	179	190	142	156	118	174	146	156
	126	145	175	123	142	165	145	136	129	176	152	164
	150	128	127	155	100	125	136	138	159	142	140	157
600 µm	168	214	210	196	187	194	218	198	191	178	153	189
	178	198	180	174	194	186	146	132	125	190	176	128
	150	145	150	121	150	140	155	120	125	150	142	120
	123	124	162	155	115	140	130	160	125	111	105	140

Third test

Line width	4 x 4 Array-coil sensor with N = 5 turns											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	174	194	186	191	179	185	200	178	132	186	200	195
	162	156	132	139	187	184	155	135	118	165	132	143
	132	132	168	127	134	165	138	124	142	176	160	140
	143	135	156	145	126	125	130	144	159	135	140	149
600 µm	189	212	215	205	191	204	199	220	182	178	184	208
	183	189	180	174	194	198	176	139	145	190	159	130
	140	152	155	123	148	134	170	156	125	150	142	126
	132	131	164	125	120	120	130	142	125	131	110	140

Average

Line width	4 x 4 Array-coil sensor with N = 5 turns (Reference)											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	162	213	200	172	163	178	202	187	136	165	194	175
	159	188	147	140	163	175	141	147	133	167	131	137
	128	130	170	124	134	156	140	127	135	161	163	145
	143	135	150	156	128	130	139	145	145	126	134	145
600 µm	186	220	217	211	181	214	218	215	178	237	190	215
	197	208	191	177	182	198	188	144	135	209	146	133
	133	143	175	126	138	146	187	145	128	142	170	141
	142	131	160	135	111	122	122	145	123	110	108	137

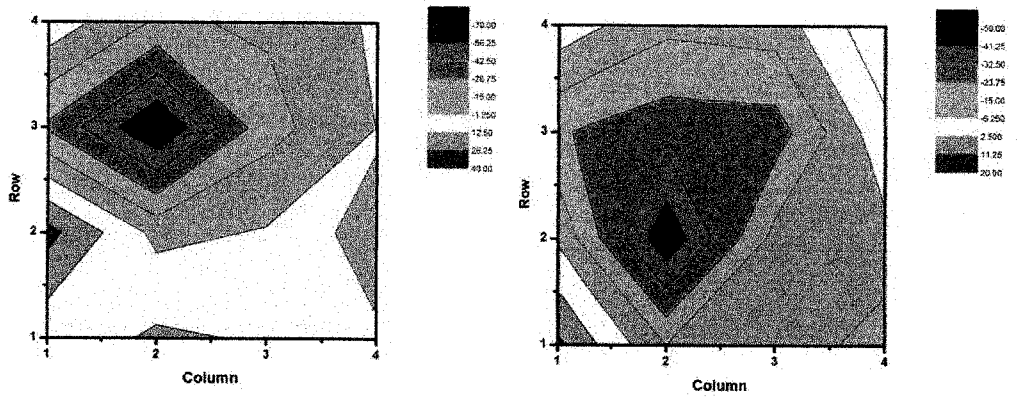
4.5.2.2 Single Fault at a Time

Table 4.4 presents the difference between the induced voltages detected by each element of the array-coil sensor from the fault free boards and single short fault boards.

Table 4.4: Difference of the induced voltages from the fault free and single short fault boards

Line width	4 x 4 Array-coil sensor with N = 5 turns (Ref- Short)											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	2	15	11	-1	13	-15	-8	-20	-1	0	-6	3
	31	-5	0	-2	-8	-48	-12	-9	-11	-27	-25	-9
	-31	-70	-20	-1	-23	-29	-28	0	-7	-41	-26	-16
	8	-17	-13	1	-1	-13	-11	10	9	-14	-16	6
600 µm	4	10	-8	-4	-1	-12	-5	-6	-19	7	-15	13
	-3	-20	1	-4	-12	4	-3	-16	-32	-3	-3	-4
	-27	-47	-36	-20	-19	-34	-35	0	-3	-30	-10	1
	2	-14	10	-12	-39	-31	-5	-16	2	-14	-6	-10

The highlighted elements have negative voltage values of higher than 30 mV. They are defined as the high resultant voltage values and a high potential location of a short fault occurrence on the lines which could be covered and observed by that element of the matrix. In the presence of a single short fault, higher induced voltages occur around the defect point compared to the fault free lines. This leads to a strong difference in the negative values in the matrix shown in the above Table 4.4. The matrices in Table 4.4 can be represented by the contour plots to clearly display and locate the defect point detected by the elements of the array-coil sensor. Figure 4.11 illustrates the contour plots of each matrix.



(a) (b)

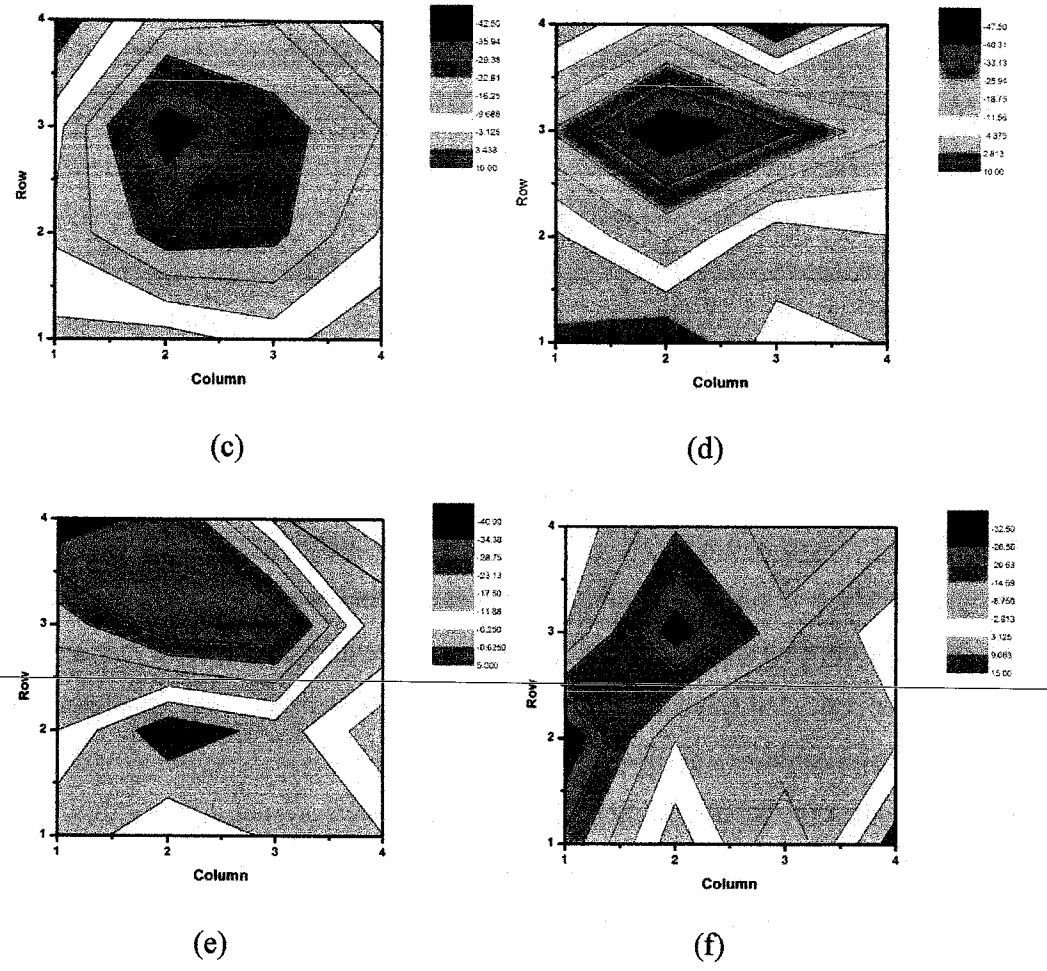


Figure 4.11: Contour map of the difference of the induced voltages between the fault free and single short fault boards: the lines of the width of 300 μm: (a) 1 mm, (b) 2 mm and (c) 4 mm line spaces and the lines of the width of 600 μm, (d) 1 mm, (e) 2 mm and (f) 4 mm line spaces

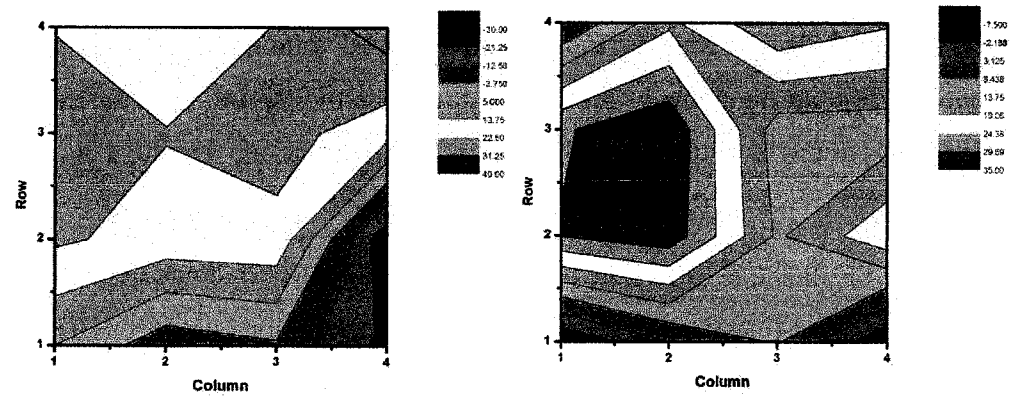
In Figure 4.11, the huge difference in the negatively induced voltage between the normal lines and short lines are displayed in the blue color regions. From these plots, the position of the single short fault can be clearly located at the abnormal voltage difference of the element of row 3, column 2.

The next observation is on the single open defect on the conductive lines. Table 4.5 shows the record of the difference between the induced voltages from the normal lines and the single open fault lines.

Table 4.5: Difference of the induced voltages from the fault free and single open fault boards

Line width	4 x 4 Array-coil sensor with N = 5 turns (Ref-Open)											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	5	-9	-5	-23	-7	3	9	-7	9	9	-16	4
	24	19	20	-28	30	33	13	23	11	36	21	12
	28	23	26	17	29	34	11	11	30	48	41	12
	22	15	23	36	3	18	29	25	18	4	-6	3
600 µm	-12	-5	2	28	5	-10	-8	-3	0	11	-16	-2
	17	26	45	26	52	53	43	14	-3	17	-5	-7
	19	19	25	21	20	38	56	35	18	37	35	18
	11	15	42	8	21	2	8	15	23	-8	3	15

From this table it can be seen that the single open defect induced a lower voltage as compared to the normal lines. As a result, the difference of the induced voltage varies from the fault free lines and a single open defect line is highly positive in its values. These highly positive values which are greater than 30 mV are highlighted in yellow. The first matrix from PCB line width of 300 µm with the line spacing of 1 mm shows the high positive values located on the middle elements. This means that there is a possible fault occurrence on the line which is covered by the 2nd and 3rd row of the sensor. The location of the single open fault can be located around those highlighted elements. These matrices have been translated in the contour plots to ease the single open fault observation as shown in Figure 4.12.



(a) (b)

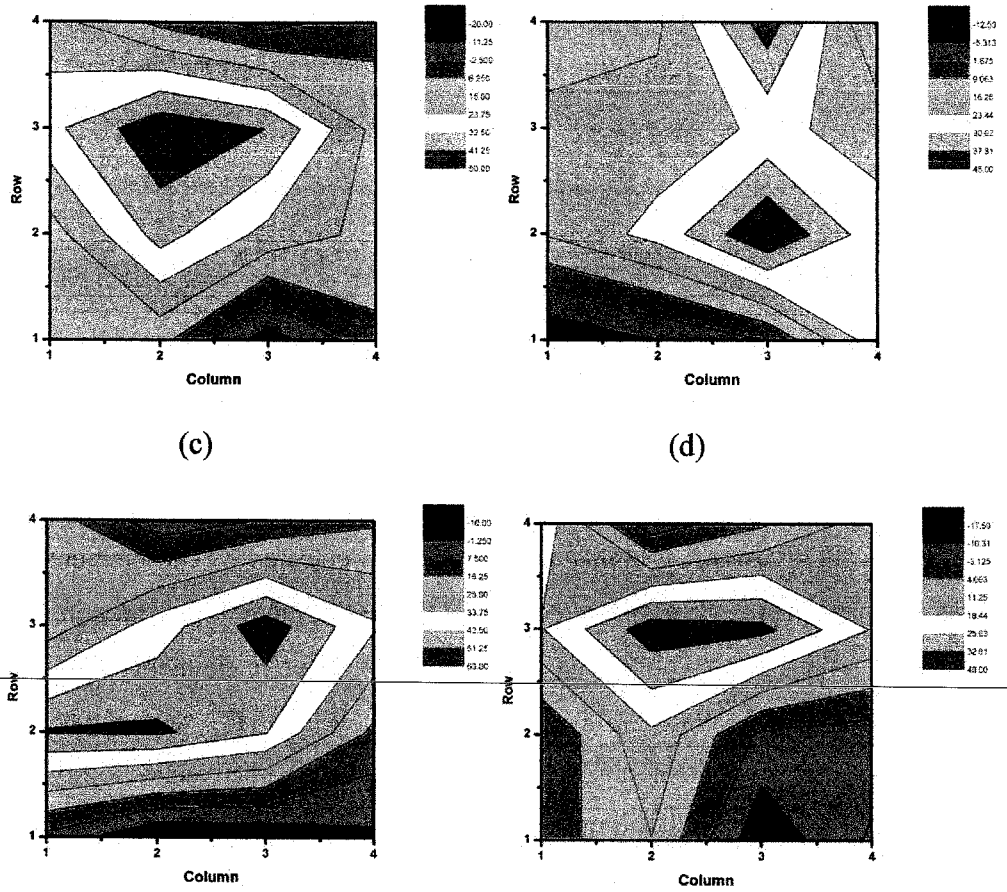


Figure 4.12: Contour map of the difference induced voltages between the fault free and single open fault boards: the lines of the width 300 μm, (a) 1 mm, (b) 2 mm and (c) 4 mm line spaces and the lines of the width 600 μm: (d) 1 mm, (e) 2 mm and (f) 4 mm line spaces

In Figure 4.12, the contour plots have shown the highly positive regions covered by the orange to red color. These maps demonstrate the high potential location of the single open fault which can be found on any matrix element lying in the highly positive regions.

4.5.2.3 Two Faults at a Time

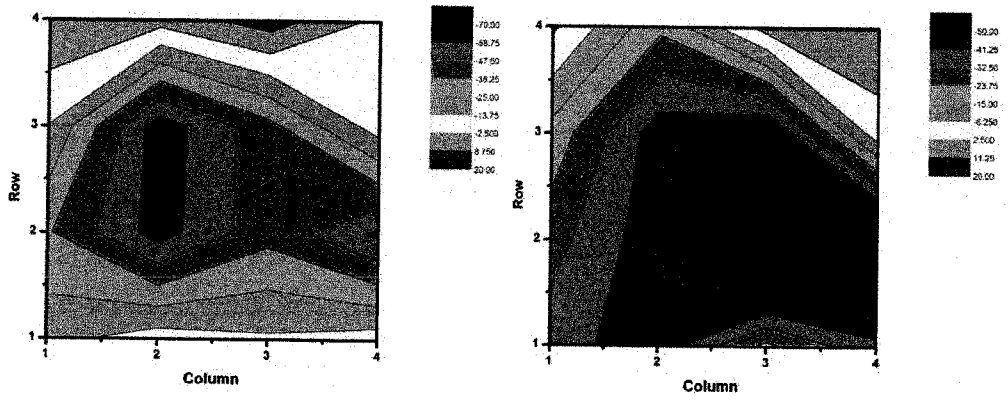
The experiment on two faults at a time has been conducted on the same PCB line patterns for the purpose to observe the changes in the induced voltage values from

each element of the array-coil sensor. Table 4.6 shows the difference between the induced voltages from the reference lines and the two short faults on the lines.

Table 4.6: Difference of the induced voltages from the fault free and the two short fault boards

Line width	4 x 4 Array-coil sensor with N = 5 turns (Ref- Short) for 2 short defects											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	-18	-8	-12	-8	-37	-47	-21	-39	-6	-4	-33	-31
	-35	-64	-40	-61	-29	-47	-95	-67	-9	-76	-74	-35
	-14	-65	-40	-9	-18	-46	-52	-2	-1	-53	-10	8
	8	2	14	-6	4	-22	6	10	15	-4	-15	-2
600 µm	-14	-10	-10	-27	-16	-39	-62	-58	-25	-40	-66	-15
	-12	-24	-59	4	0	-44	-35	-19	-30	-21	-46	-4
	-17	-37	-36	-4	-8	-46	-27	5	-26	-41	-43	-12
	-23	-20	10	-5	-8	-35	-23	7	-5	-20	-30	-13

In Table 4.6, there are many highly negative values detected by the elements of the array-coil sensor compared to the inspection of single fault at a time. The potential fault locations can be found by observing the highlighted negative elements of greater than 30 mV. The contour plots have been used to interpret the matrices in Table 4.6. Figure 4.13 shows the contour plots representing the difference between the induced voltages from the reference lines and the two short fault lines.



(a) (b)

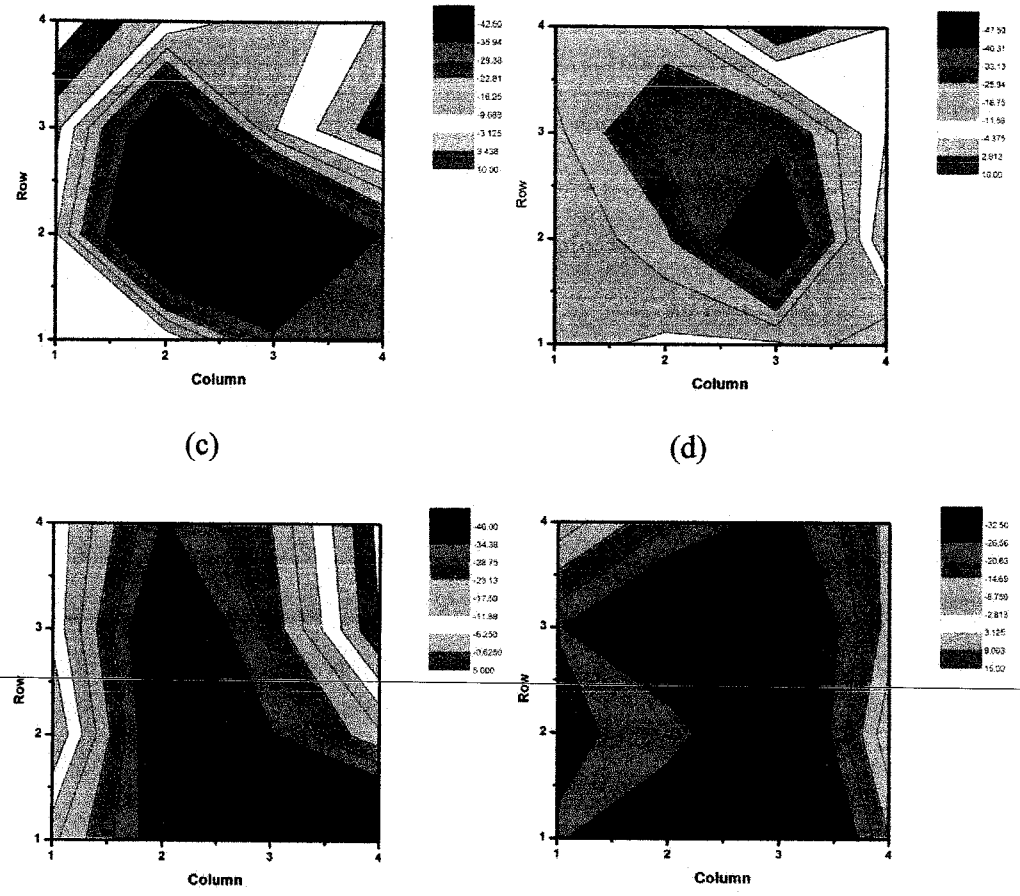


Figure 4.13: Contour map of the difference induced voltages between the fault free and two short faults boards: the lines of the width 300 μm: (a) 1 mm, (b) 2 mm and (c) 4 mm line spaces and the lines of the width 600 μm: (d) 1 mm, (e) 2 mm and (f) 4 mm line spaces

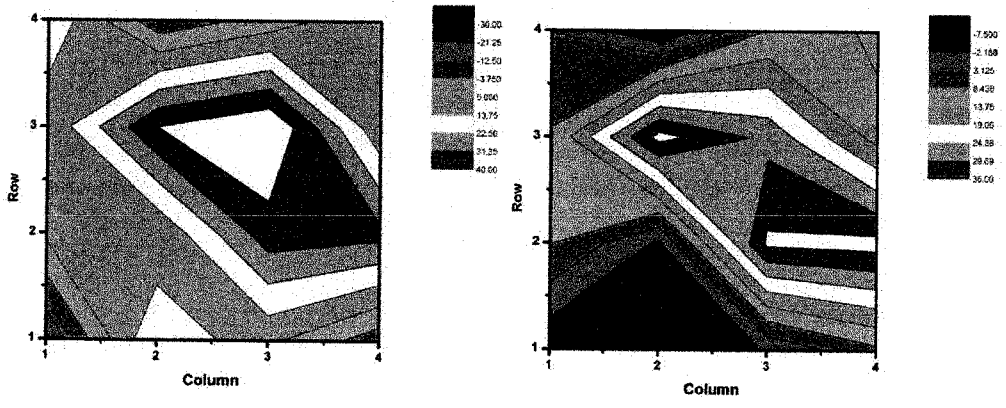
The highly negative regions have been represented by the ranges of color from blue to black. Since there are two short faults on each board, the wider regions of the highly negative values in the contour plots can be observed. These regions give the information about the locations of the two short faults which can be detected by the elements of the matrix. These results have shown that two faults at time provide a clear visualization to locate the potential faults on the PCB lines compare to single fault at time.

The last observation is to detect the two open faults on the lines of each board. Table 4.7 summarizes the difference between the induced voltages from the fault free lines and the two open faults on the lines.

Table 4.7: Difference of the induced voltages from the fault free and the two open fault boards

Line width	4 x 4 Array-coil sensor with N = 5 turns (Ref-Open) for 2 open defects											
	Line Space = 1 mm (mV)				Line Space = 2 mm (mV)				Line Space = 4 mm (mV)			
300 µm	-20	22	7	-9	-7	-5	-2	7	9	2	-16	11
	7	6	36	34	9	-3	36	37	-5	5	26	27
	7	40	49	7	9	37	28	12	14	45	44	19
	21	-10	0	14	3	-7	9	15	7	3	14	0
600 µm	8	15	-3	6	-14	-12	-15	-12	6	-9	10	29
	22	1	44	43	13	-3	41	26	2	11	23	33
	-3	37	30	4	15	29	50	10	-1	41	32	11
	4	-1	29	2	11	-8	9	5	11	-4	8	4

In the case of the two open faults at a time, the difference of the induced voltages between the fault free and the faulty boards are highly positive. The highly positive values occur around the potential defect points are highlighted. Figure 4.14 illustrates these values of the matrices in the form of contour plots. From the contour plots, the range of the highly positive regions is in the ranges of color from orange to red to white. These regions are the potential regions of the defect points.



(a) (b)

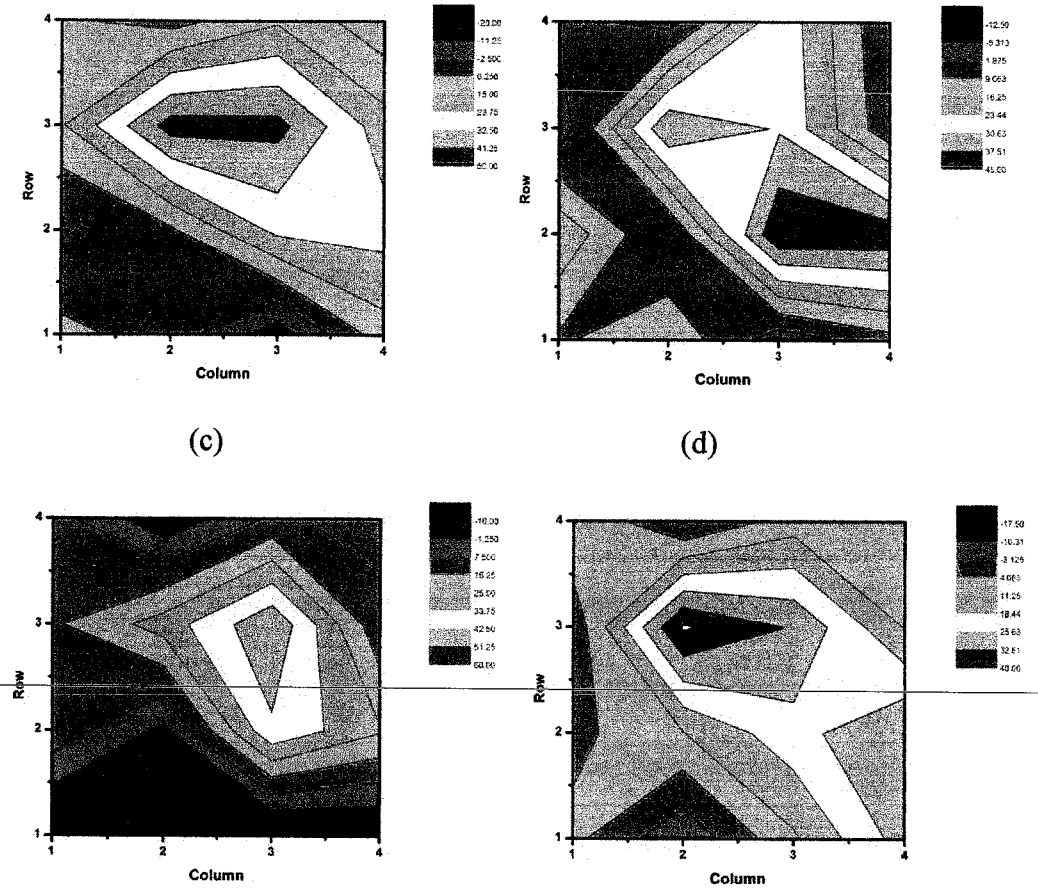


Figure 4.14: Contour map of the difference induced voltages between the fault free and two open faults boards: the lines of the width 300 μm: (a) 1 mm, (b) 2 mm and (c) 4 mm line spaces and the lines of the width 600 μm: (d) 1 mm, (e) 2 mm and (f) 4 mm line spaces

According to the above PCB testing for a single fault and two faults at a time, the faulty boards induce higher or lower induced voltages than the induced voltages from the normal lines which can be detected by the corresponding elements of the array-coil sensor matrix. The location of the faults can be identified by reading the contour plot color regions. From the observation, the PCB lines with the bigger line spacing of 4 mm produced a high difference between the induced voltages from the fault free boards and from the faulty boards. These differences have provided a clear observation to identify and locate the potential fault regions on the elements of the matrix as well as on the lines. Moreover, from the contour plots, two faults at a time

could be noticed by having the wider regions of the highly negative or positive color ranges than a single fault at a time.

4.6 Concluding Remarks

The CST simulation has shown that when there is a short or an open termination load on the conductive line, there will be a maximum and minimum magnetic field emitting along the line. In the presence of a short or discontinuity occurring on the middle of the line, the CST simulation has shown that there is an abnormal peak magnetic field intensity emitting around the PCB line. The shorted lines produce higher peak magnetic field intensity than the fault free line which has a magnetic field intensity that is constant. While the opened line produces lower peak magnetic field intensity than the fault free line having a constant magnetic field intensity, *H*. In addition to the magnetic field intensity simulation, the eddy current sensor has been modeled and simulated in the CST EM Studio to observe the changes in the coil voltages in the conditions of the fault free and faulty lines. It has shown that the short fault lines induce higher voltages as compared to the normal or fault free lines of the same dimensions. Another observation is that the open fault lines induce lower voltages than the normal or fault free lines of the same dimensions. In order to conduct the PCB fault inspection, the designed PCB and array-coil sensor layouts have been fabricated. The PCB lines consisted of two line widths: 300 μm and 600 μm. Each type consisted of three line spacing patterns of 1 mm, 2 mm, and 4 mm. The array-coil sensor is the matrix of 4 by 4. This sensor is placed on top of each board for further PCB fault inspection to differentiate the faulty and fault free lines.

Each board is exposed to the magnetic field generated by a pair of Helmholtz coils. In the presence of the alternating field, eddy currents are induced on the conductive PCB lines. These currents circulated and induced a perpendicular magnetic field to the line. The field generated by the eddy currents induced voltages on the array-coil sensors which could be measured by the multi-meter. The changes of the induced voltages could be used for the observation and location of the effect of any defects on the conductive PCB lines. In the presence of short faults, the eddy currents had a more conductive area to flow which caused a high induced voltage

around the area of the short lines. This led to highly negative voltage values different from the normal lines. While, in the presence of the open faults, the eddy current path is now disturbed and had a less conductive area to move in as compared to the normal ones. The different induced voltage values between the normal and open lines are highly positive in value. These induced voltage differences are recorded and translated into the contour plots. In the contour plots, the regions of the highly negative or positive values are presented in color patterns which are displayed on the color bar in each plot. These color regions provided the very important information about the abnormal difference of the induced voltage region occurrences at any elements of the matrix. The contour plots illustrated that the faulty boards of the two faults at a time produced the wider regions of highly negative or positive values than a single fault at a time. These color regions could be used to locate the potential faults on the PCB lines under testing.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

5.1 Conclusion

Printed circuit board (PCB) has played an important role as an electronic board to support and electrically connects the electrical components. With the advancement of the electronic circuit design technology, the reliability of the bare PCB on which the electronic components are mounted is very important to ensure a fully functioning system. The short and open faults which are the two common faults occur between the interconnects or signal lines. The PCB inspection methods, such as optical inspection, and magnetic image analysis have been used to inspect PCBs. However, these methods are not sufficient to fully cover all of the possible faults as the density of the PCB traces become higher. In this thesis, the feasibility investigation of fault inspection using the magnetic field properties of PCB interconnect is experimented. The non-contact probe which is known as eddy current testing (ECT) sensor is realized. The sensor consists of the array of single coil of 5 turns is used to detect the changes of the induced magnetic field. This thesis has highlighted the proposed ECT sensor probe, planar array-coil senor, to detect and locate the potential faults (short and open) on PCBs. The PCBs have been fabricated and tested for three cases: fault free (reference), short and open fault boards. Prior to PCB fault testing, computer system technology (CST) simulations were used to model and observe the magnetic field intensity patterns above PCB line models. It has shown that in the presence of short or open circuit, the magnetic field intensity is not constant and there are peak values occur around the fault position. In addition to the software simulation, the millimeter scale PCB prototypes were fabricated on FR4 boards in order to observe the insertion loss of a signal transmitted from PCB lines to single loop coil sensors. The obtained results have shown that the high environment noise interferences and

high loss signal are detected at the single coil sensor's output. As a result, the improvement of the testing system is required in order to obtain the optimum result. The PCB fault testing system should be conducted in the shielded box in order to enhance the experimental result. The effect of the shielded box to the experimental results has been demonstrated in the single coil characterization.

The experimental setup and components' characterization have been discussed in this work. The proposed feasibility study on PCB fault detection has been conducted in the magnetic shielded box. It has been shown that the short fault induces higher voltage levels around the fault area compared to the fault free lines. It leads to highly negative values of difference between fault free and short lines induced voltage values. In contrast to the short fault, the open fault induces lower voltage levels around the fault area compared to the fault free lines. Thus, the difference between fault free and open lines induced voltage is highly positive in values. The potential fault locations can be located and observed by the highly positive or highly negative region of the contour plots from each matrix sensor. From the contour plots the PCB lines of the bigger line spacing of 4 mm provide a better vision of highly positive or negative regions of potential faults. The experimental results have proved the feasibility investigation of short and open faults inspection by exploiting the magnetic field property of PCB interconnects which is detected by the non-contact probe ECT. The testing fault patterns have been generated and analyzed.

5.2 Future Direction

The goal of the research on PCB fault testing is to produce an effectively sensitive fault testing method with less time consuming and high accuracy to achieve high fault coverage and to locate faults on the PCB conductive lines. In this thesis the PCB fault inspection system using the proposed ECT probe has been realized. In addition, the system should be equipped with advanced and intelligent features such as image processing technique. However, this work focuses mainly on feasibility study on fault inspection on planar circuit using non-contact ECT probe.

Now a day, the advancement of IC design has caused dramatic changes in circuit geometry and fabrication process. With the development of circuit design, the integration capacity of the component has increased and resulted in more complex structures. It leads to gradually increase the number of possible faults between interconnects and logic lines not only inside ICs but also on PCBs. Thus following the work presented in this thesis, the future improvement in PCB fault detection using ECT may include:

- Fabricating array-coil sensor on silicon die with more number of turn in order to increase the sensitivity of the sensor and be able to cover and scan through a single PCB line in nanometer ranges.
- Setting up the experiment should be conducted in the well proper shielded magnetic room in order to improve fault detection experiment.
- Designing ECT probe with an improvement on configuration of the excitation coil and pick-up coil. The better perform and higher sensitivity of magnetic sensor should be explored.
- Improving in electronic components such as high resolution multi-meter and proper shielded connectors or jumpers.

Therefore, the extending research of the proposed work in this thesis on improving fault testing of ECT technique provides an important knowledge to apply on nanoscale circuit fault testing by implementing very sensitive magnetic field sensor.

REFERENCES

[1] L.-T. Wang, *et al.*, *VLSI Test Principles And Architectures Design For Testability*. San Francisco: Morgan Kaufmann Publishers, 2006.

[2] N. K. Jha and S. Gupta, *Testing of Digital Systems*: Cambridge University Press, 2003.

[3] M. Abramovici, *et al.*, *Digital systems tetsing and testable design*. New York: IEEE Press, 1990.

[4] L.-R. Zheng and H. Tenhunen, *Wires as Interconnects*. Stockholm: Royal institute of technology (KTH), 2004.

[5] M. Celik, *et al.*, *IC Interconnect Analysis*: Kluwer academic publishers, 2002.

[6] H. Hong and E. J. McCluskey, "Very-low-voltage testing for weak CMOS logic ICs," in *Test Conference, 1993. Proceedings., International*, 1993, pp. 275-284.

[7] L. Yuyun and D. M. H. Walker, "Optimal voltage testing for physically-based faults," in *VLSI Test Symposium, 1996., Proceedings of 14th*, 1996, pp. 344-353.

[8] H. T. Vierhaus, *et al.*, "CMOS bridges and resistive transistor faults: IDDQ versus delay effects," in *Test Conference, 1993. Proceedings., International*, 1993, pp. 83-91.

[9] M. Sachdev, "Deep sub-micron I_{DDQ} testing: issues and solutions," in *European Design and Test Conference, 1997. ED&TC 97. Proceedings*, 1997, pp. 271-278.

[10] N. B. Zain Ali, "An investigation of delay fault testing for multi voltage design," Doctoral, School of Electronics and Computer Science, University of Southampton, 2009.

[11] M. Sachdev and J. P. d. Gyvez, *Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits*, 2 ed. The Netherlands: Springer, 2007.

[12] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*: Kluwer Academic Publishers 2002.

[13] D. Gizopoulos, *Advances in Electronic Testing: Challenges and Methodologies*. The Netherlands: Springer, 2006.

[14] Y. Min and Z. Li, "IDDT Testing versus IDDQ Testing," *Journal of Electronic Testing*, vol. 13, pp. 51-55, 1998/08/01 1998.

[15] A. E. Gattiker and W. Maly, "Current signatures [VLSI circuit testing]," in *VLSI Test Symposium, 1996., Proceedings of 14th*, 1996, pp. 112-117.

[16] A. Keshavarzi, *et al.*, "Intrinsic leakage in low power deep submicron CMOS ICs," in *Test Conference, 1997. Proceedings., International*, 1997, pp. 146-155.

[17] C. Thibeault, "A novel probabilistic approach for IC diagnosis based on differential quiescent current signatures," in *VLSI Test Symposium, 1997., 15th IEEE*, 1997, pp. 80-85.

[18] T. Sudo, *et al.*, "Electromagnetic radiation and simultaneous switching noise in a CMOS device packaging," in *Electronic Components & Technology Conference, 2000. 2000 Proceedings. 50th*, 2000, pp. 781-785.

[19] T. Steinecke, *et al.*, "EMC modeling and simulation on chiplevel," in *Electromagnetic Compatibility, 2001. EMC. 2001 IEEE International Symposium on*, 2001, pp. 1191-1196 vol.2.

[20] B. Vrignon, *et al.*, "Characterization and modeling of parasitic emission in deep submicron CMOS," *Electromagnetic Compatibility, IEEE Transactions on*, vol. 47, pp. 382-387, 2005.

[21] S. Hayashi and M. Yamada, "EMI-noise analysis under ASIC design environment," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 19, pp. 1337-1346, 2000.

[22] P. K. Lala, *Digital Circuit Testing and Testability*. San Diego: Academic Press, 1997.

[23] D. Arumi, *et al.*, "Experimental characterization of CMOS interconnect open defects," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 27, pp. 123-136, 2008.

[24] H. Takahashi, *et al.*, "On diagnosing multiple stuck-at faults using multiple and single fault simulation in combinational circuits," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 21, pp. 362-368, 2002.

[25] X. Likun, *et al.*, "Automated Model Generation Algorithm for High-Level Fault Modeling," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 29, pp. 1140-1145, 2010.

[26] I. Pomeranz and S. M. Reddy, "Robust Fault Models Where Undetectable Faults Imply Logic Redundancy," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 18, pp. 1230-1234, 2010.

[27] S. B. Akers, "Universal Test Sets for Logic Networks," *Computers, IEEE Transactions on*, vol. C-22, pp. 835-839, 1973.

[28] G. Gupta and N. K. Jha, "A universal test set for CMOS circuits," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 7, pp. 590-597, 1988.

[29] F. N. Najm and I. N. Hajj, "The complexity of fault detection in MOS VLSI circuits," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 9, pp. 995-1001, 1990.

[30] E. M. Rudnick, *et al.*, "Diagnostic Fault Simulation of Sequential Circuits," in *Test Conference, 1992. Proceedings., International*, 1992, p. 178.

[31] J. A. Waicukauski and E. Lindbloom, "Failure diagnosis of structured VLSI," *Design & Test of Computers, IEEE,* vol. 6, pp. 49-60, 1989.

[32] M. Abramovici, "A Maximal Resolution Guided-Probe Testing Algorithm," in *Design Automation, 1981. 18th Conference on*, 1981, pp. 189-195.

[33] J. Galiay, *et al.*, "Physical Versus Logical Fault Models MOS LSI Circuits: Impact on Their Testability," *Computers, IEEE Transactions on,* vol. C-29, pp. 527-531, 1980.

[34] R. Rajsuman, *et al.*, "Limitations of switch level analysis for bridging faults," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 8, pp. 807-811, 1989.

[35] M. Favalli, *et al.*, "Modeling and simulation of broken connections in CMOS IC's," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 15, pp. 808-814, 1996.

[36] I. Pomeranz and S. M. Reddy, "A Bridging Fault Model Where Undetectable Faults Imply Logic Redundancy," in *Design, Automation and Test in Europe, 2008. DATE '08*, 2008, pp. 1166-1171.

[37] P. C. Maxwell and R. C. Aitken, "Biased voting: A method for simulating CMOS bridging faults in the presence of variable gate logic thresholds," in *Test Conference, 1993. Proceedings., International*, 1993, pp. 63-72.

[38] V. Krishnaswamy, *et al.*, "A study of bridging defect probabilities on a Pentium (TM) 4 CPU," in *Test Conference, 2001. Proceedings. International*, 2001, pp. 688-695.

[39] S. Ma, *et al.*, "A comparison of bridging fault simulation methods," in *Test Conference, 1999. Proceedings. International*, 1999, pp. 587-595.

[40] K. C. Y. Mei, "Bridging and Stuck-At Faults," *Computers, IEEE Transactions on,* vol. C-23, pp. 720-727, 1974.

[41] T. Yamada and T. Nanya, "Stuck-At Fault Tests in the Presence of Undetectable Bridging Faults," *Computers, IEEE Transactions on,* vol. C-33, pp. 758-761, 1984.

[42] R. Wadsack, "Fault modeling and logic simulation of CMOS and MOS integrated circuits," *AT T Technical Journal*, vol. 57, pp. 1449-1474, 1978.

[43] H. Xue, *et al.*, "Probability analysis for CMOS floating gate faults," in *European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings.*, 1994, pp. 443-448.

[44] Y. Sato, *et al.*, "A persistent diagnostic technique for unstable defects," in *Test Conference, 2002. Proceedings. International*, 2002, pp. 242-249.

[45] H. Konuk and F. J. Ferguson, "An unexpected factor in testing for CMOS opens: the die surface," in *VLSI Test Symposium, 1996., Proceedings of 14th*, 1996, pp. 422-429.

[46] S. M. Reddy, *et al.*, "On testing of interconnect open defects in combinational logic circuits with stems of large fanout," in *Test Conference, 2002. Proceedings. International*, 2002, pp. 83-89.

[47] V. H. Champac and A. Zenteno, "Detectability conditions for interconnection open defects," in *VLSI Test Symposium, 2000. Proceedings. 18th IEEE*, 2000, pp. 305-311.

[48] B. Kruseman, *et al.*, "Comparison of I_{DDQ} testing and very-low voltage testing," in *Test Conference, 2002. Proceedings. International*, 2002, pp. 964-973.

[49] F. N. Najm, "Transition density: a new measure of activity in digital circuits," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 12, pp. 310-323, 1993.

[50] R. S. Khandpur, *Printed Circuit Boards: Design, Fabrication, Assembly and Testing*. New York McGraw-Hill, 2006.

[51] Y. Hara, *et al.*, "Automatic Inspection System for Printed Circuit Boards," *Pattern Analysis and Machine Intelligence, IEEE Transactions on*, vol. PAMI-5, pp. 623-630, 1983.

[52] D. Enke and C. Dagli, "Automated misplaced component inspection for printed circuit boards," *Computers & Industrial Engineering*, vol. 33, pp. 373-376, 1997.

[53] Y. Hara, *et al.*, "A system for PCB automated inspection using fluorescent light," *Pattern Analysis and Machine Intelligence, IEEE Transactions on*, vol. 10, pp. 69-78, 1988.

[54] G. Shu-an and G. Fenglin, "A New Image Enhancement Algorithm for PCB Defect Detection," in *Intelligence Science and Information Engineering (ISIE), 2011 International Conference on*, 2011, pp. 454-456.

[55] L. Horng-Hai and L. Ming-Sing, "Printed circuit board inspection using image analysis," in *Industrial Automation and Control: Emerging Technologies, 1995., International IEEE/IAS Conference on*, 1995, pp. 673-677.

[56] Z. Ibrahim, *et al.*, "A noise elimination procedure for wavelet-based printed circuit board inspection system," in *Control Conference, 2004. 5th Asian*, 2004, pp. 875-880 Vol.2.

[57] B. Chen, *et al.*, "The Portable PCB Fault Detector Based on ARM and Magnetic Image," in *Computer Science and Software Engineering, 2008 International Conference on*, 2008, pp. 978-981.

[58] B. Raj, *et al.*, *Practical Non-destructive Testing*. UK: Alpha Science International Ltd, 2007.

[59] F. T. Ulaby, *Electromagnetics for Engineers*. Upper Saddle River, NJ: Pearson/Prentic Hall, 2005.

[60] S. Mukhopadhyay, "Novel Planar Electromagnetic Sensors: Modeling and Performance Evaluation," *Sensors*, vol. 5, pp. 546-579, 2005.

[61] M. Uesaka, *et al.*, "Micro eddy current testing by micro magnetic sensor array," *Magnetics, IEEE Transactions on*, vol. 31, pp. 870-876, 1995.

[62] T. Dogaru, *et al.*, "Deep Crack Detection around Fastener Holes in Airplane Multi-Layered Structures Using GMR-Based Eddy Current Probes," *AIP Conference Proceedings*, vol. 700, pp. 398-405, 2004.

[63] R. Grimberg, *et al.*, "A Novel Rotating Magnetic Field Eddy Current Transducer for the Examination of Fuel Channels in PHWR Nuclear Power Plants," *AIP Conference Proceedings*, vol. 760, pp. 471-478, 04/09/ 2005.

[64] S. Yamada, *et al.*, "Application of Giant Magnetoresistive Sensor for Nondestructive Evaluation," in *Sensors, 2006. 5th IEEE Conference on*, 2006, pp. 927-930.

[65] S. Yamada, *et al.*, "Eddy-current testing probe with spin-valve type GMR sensor for printed circuit board inspection," *Magnetics, IEEE Transactions on*, vol. 40, pp. 2676-2678, 2004.

[66] K. Chomsuwan, *et al.*, "Application of eddy-current testing technique for high-density double-Layer printed circuit board inspection," *Magnetics, IEEE Transactions on*, vol. 41, pp. 3619-3621, 2005.

[67] D. Kacprzak, *et al.*, "Novel eddy current testing sensor for the inspection of printed circuit boards," *Magnetics, IEEE Transactions on*, vol. 37, pp. 2010-2012, 2001.

[68] S. Yamada, *et al.*, "Application of ECT technique for inspection of bare PCB," *Magnetics, IEEE Transactions on*, vol. 39, pp. 3325-3327, 2003.

[69] S. Yamada, *et al.*, "Conductive micro-bead array detection by high-frequency eddy-current testing technique with SV-GMR sensor," in *Magnetics Conference, 2005. INTERMAG Asia 2005. Digests of the IEEE International*, 2005, pp. 419-420.

[70] K. Chomsuwan, *et al.*, "Improvement on Defect Detection Performance of PCB Inspection Based on ECT Technique With Multi-SV-GMR Sensor," *Magnetics, IEEE Transactions on*, vol. 43, pp. 2394-2396, 2007.

[71] K. Chomsuwan, *et al.*, "Bare PCB Inspection System With SV-GMR Sensor Eddy-Current Testing Probe," *Sensors Journal, IEEE*, vol. 7, pp. 890-896, 2007.

[72] S. Tumanski, "Induction coil sensors—a review," *Measurement Science and Technology*, vol. 18, p. R31, 2007.

[73] H. Xiaohui and Y. Wuqiang, "An imaging system with planar PCB-coil sensor array," in *Imaging Systems and Techniques, 2009. IST '09. IEEE International Workshop on*, 2009, pp. 26-31.

[74] R. J. Ditchburn and S. K. Burke, "Planar rectangular spiral coils in eddy-current non-destructive inspection," *NDT & E International*, vol. 38, pp. 690-700, 2005.

[75] Y. Sheiretov and M. Zahn, "Design and modeling of shaped-field magnetoquasistatic sensors," *Magnetics, IEEE Transactions on*, vol. 42, pp. 411-421, 2006.

[76] S. K. Burke and R. J. Ditchburn, "Mutual Impedance of Planar Eddy-Current Driver–pickup Spiral Coils," *Research in Nondestructive Evaluation*, vol. 19, pp. 1-19, 2008/01/15 2008.

[77] M. Uesaka, *et al.*, "Eddy-current testing by flexible microloop magnetic sensor array," *Magnetics, IEEE Transactions on*, vol. 34, pp. 2287-2297, 1998.

[78] D. J. Sadler and C. H. Ahn, "On-chip eddy current sensor for proximity sensing and crack detection," *Sensors and Actuators A: Physical*, vol. 91, pp. 340-345, 2001.

[79] N. Goldfine, *et al.*, "Conformable eddy-current sensors and arrays for fleetwide gas turbine component quality assessment," *Journal of Engineering for Gas Turbines and Power(Transactions of the ASME)*, vol. 124, pp. 904-909, 2002.

[80] S. Yamada, *et al.*, "Eddy current testing probe composed of planar coils," *Magnetics, IEEE Transactions on*, vol. 31, pp. 3185-3187, 1995.

[81] S. Yamada, *et al.*, "Defect images by planar ECT probe of meander-mesh coils," *Magnetics, IEEE Transactions on*, vol. 32, pp. 4956-4958, 1996.

[82] S. Yamada, *et al.*, "Investigation of Printed Wiring Board Testing By Using Planar Coil Type ECT Probe," in *Magnetics Conference, 1997. Digests of INTERMAG '97., 1997 IEEE International*, 1997, pp. GP-17-GP-17.

[83] D. Kacprzak, *et al.*, *Comparison of two types of pick-up coil for meander excitation*: IOS Press, 2000.

[84] T. Dogaru and S. T. Smith, "Giant magnetoresistance-based eddy-current sensor," *Magnetics, IEEE Transactions on*, vol. 37, pp. 3831-3838, 2001.

[85] P. Ripka, *Magnetic sensors and magnetometer* Boston: Artech House, 2001.

[86] D. Lancaster, *Active Filter Cookbook*. London: Newnes, 1996.

[87] I. C. Hunter, *Theory and Design of Microwave Filter*. London: The institution of electrical engineers, 2001.

[88] W.-K. Chen, *Passive, active and digital filters*. Boca Raton: Taylor & Francis, 2006.

[89] L. P. Huelsman, *Active and passive analog filter design : an introduction*. New York McGraw-Hill, 1993.

[90] A. Das and S. K. Das, *Microwave Engineering*. New Delhi: Tata McGraw Hill, 2009.

[91] D. M. Pozar, *Microwave Engineering*, 3 ed. New York: John Wiley & Sons, 2005.

[92] A. W. Scott, *Understanding Microwaves*. Hoboken, N.J.: Wiley-Interscience, 2005.