STATUS OF THESIS

Title of thesis | DESIGN AND CHARACTERIZATION OF AN ULTRA-LOW POWER INTERFACE CIRCUIT FOR OPTICAL SENSORS

I, ISRAEL YOHANNES BAYOU

hereby allow my thesis to be placed at the Information Resource Center (IRC) of Universiti Teknologi PETRONAS (UTP) with the following conditions:

1. The thesis becomes the property of UTP
2. The IRC of UTP may make copies of the thesis for academic purposes only.
3. This thesis is classified as

☐ Confidential

☑ Non-confidential

If this thesis is confidential, please state the reason:

The contents of the thesis will remain confidential for _____ years.

Remarks on disclosure:

Endorsed by

Signature of Author

Signature of Supervisor

Permanent address: Kebele 03,
Dire Dawa
Ethiopia

Name of Supervisor
Dr. Maher Assaad

Date : 14/3/2013

Date : 14/3/2013

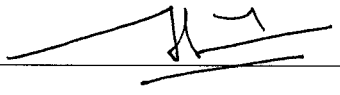
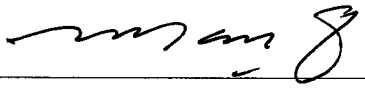
UNIVERSITI TEKNOLOGI PETRONAS

DISSERTATION TITLE: DESIGN AND CHARACTERIZATION OF AN ULTRA-LOW POWER INTERFACE CIRCUIT FOR OPTICAL SENSORS

by

ISRAEL YOHANNES BAYOU

The undersigned certify that they have read, and recommend to the Postgraduate Studies Programme for acceptance this thesis for the fulfillment of the requirements for the degree stated.

Signature:	
Main Supervisor:	Dr. Maher Assaad
Signature:	
Co-Supervisor:	A/P Dr. Nor Hisham Bin Hamid
Signature:	
Head of Department:	Dr. Rosdiazli B Ibrahim
Date:	Dr Ros... Head of Department Electrical & Electronic Engineering Department Universiti Teknologi PETRONAS 14-3-13

DESIGN AND CHARACTERIZATION OF AN ULTRA-LOW POWER INTERFACE CIRCUIT FOR OPTICAL SENSORS

by

ISRAEL YOHANNES

A Thesis

Submitted to the Postgraduate Studies Programme

as a Requirement for the Degree of

MASTER OF SCIENCE

ELECTICAL AND ELECTRONICS ENGINEERING DEPARTMENT

UNIVERSITI TEKNOLOGI PETRONAS

BANDAR SERI ISKANDAR,

PERAK

MARCH 2013

DECLARATION OF THESIS

Title of thesis | DESIGN AND CHARACTERIZATION OF AN ULTRA-LOW POWER INTERFACE CIRCUIT FOR OPTICAL SENSORS

I ISRAEL YOHANNES BAYOU

hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

Witnessed by

Signature of Author

Signature of Supervisor

Permanent address: Kebele 03,
Dire Dawa
Ethiopia

Name of Supervisor
Dr. Maher Assaad

Date : 14/3/2013

Date : 14/3/2013

DEDICATION

To my beloved family and friends

ACKNOWLEDGEMENTS

The greatest of all my appreciation goes to the almighty GOD, creator of the universe and everything that is in it. As I wouldn't be here, complete my project without his gracious will.

Next, I want to thank my supervisor Dr. Maher Assaad, for his constant help, guidance and encouragement throughout the MSc project. Thank you for making me work harder and teaching me so much. I would also like to extend my thanks to my co-supervisor Assoc. Prof. Dr Nor Hisham Bin Hamid, for helping, and consulting with me especially on the start of my MSc.

My appreciation goes to my parents and siblings especially to Birhan, Meron, Bisrat and Henock. Their love, care, and never ending support always helped me to face any ups and downs. I thank them for always believing in me and being by my side. Not to forget Mulluken Nega, whom I am deeply grateful for his constant encouragement, advice and inspiration.

I would also want to thank all my beloved friends in UTP who made my stay pleasant, and unforgettable. And to those who have directly or indirectly assisted me during this research, I wish you all success and the best of luck all the time.

ABSTRACT

Sensors are one of the most ubiquitous devices in our day to day life. The ever increasing demand for *insitu* environmental monitoring has created a continuing research endeavor to produce a low-cost, low power, fast sensor systems. Optical sensors are preferred for various applications due to their non-intrusive nature and are commonly used to monitor the environment. Dedicated interface electronics are needed to interpret the output of these sensors accurately into a usable form to a user or subsequent systems. In this work, an interface circuit architecture for optical sensor is proposed that is suitable for integration in a single chip. It is a mixed signal solution that directly interfaces with a light transducer (e.g. OPT301) and produces a digital output to a direct display such as LED. In contrast to conventional systems, the proposed design avoids the need for an ADC, DSP and memory units which leads to reduced power, reduced complexity and cost. Moreover, it is ideal to be used for simple autonomous and portable real-time monitoring applications. The proposed design has been implemented for 4, 8, and 32 levels of resolution (i.e. wavelength) with minor change in number of components.

This thesis contributes towards low power sensor development by proposing simple yet efficient; ultra-low power interface circuit that can be integrated. To that end, a single chip integrated circuit (IC) is designed and fabricated using commercially available 0.35 μm CMOS standard process. The design is validated via simulation and experimental results from discrete component implementation (i.e. PCB) as well as from fabricated prototype (i.e. IC).

ABSTRAK

Pengesan-pengesan merupakan satu alat-alat kebanyakan sentiasa ada dalam hidup hari ke hari kami. Permintaan yang sentiasa meningkat kerana pengawasan persekitaran insitu telah mewujudkan usaha penyelidikan berterusan pada hasil satu kos rendah, sistem-sistem pengesan cepat yang kuasa rendah. Pengesan-pengesan optik diutamakan untuk pelbagai kegunaan disebabkan mereka tidak mengganggu dan biasa digunakan untuk memantau persekitaran. Antara muka berdedikasi diperlukan untuk mentafsirkan output pengesan-pengesan ini dengan tepat ke dalam satu bentuk agar dapat digunakan bagi seorang pengguna atau sistem-sistem berikutnya. Dalam tugas ini, seni bina litar antara muka untuk pengesan optik ialah dicadangkan bahawa ada sesuai bagi integrasi dalam satu cip. Ia penyelesaian isyarat bercampur-campur yang secara terus berhubung kait dengan satu transduser ringan (misalnya OPT301) dan menghasilkan satu output digital bagi satu pameran langsung seperti LED. Berbeza dengan sistem-sistem konvensional, reka bentuk yang dicadangkan menghindari perlukan satu ADC, DSP dan unit-unit ingatan yang membawa ke kuasa yang berkurangan, keadaan kompleks berkurangan dan kos berkurangan. Tambahan pula, ia ideal digunakan untuk mudah berautonomi dan mudah alih masa nyata aplikasi pengawasan. Reka bentuk yang dicadangkan telah dilaksanakan untuk 4, 8 , dan 32 peringkat resolusi (iaitu panjang gelombang) dengan perubahan kecil dalam bilangan komponen.

Tesis ini menyumbang ke arah pengesan kuasa yang rendah dengan mencadangkan antar muka yang mudah tetapi berkesan; kuasa ultrarendah yang dapat diintegrasikan. Di penghujung, satu litar bersepadu cip tunggal (IC) direka bentuk dan dibina secara komersial 0.35 proses standard μm CMOS. Reka bentuk ini disahkan melalui simulasi dan hasil percubaan dari pelaksanaan komponen diskret (iaitu PCB) serta dari prototaip yang direka (iaitu IC).

TABLE OF CONTENT

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Sensors

A sensor converts one type of energy in to an electrical signal [1]. Sensors can be considered one of the most commonly used devices associated with our day to day life. They help us interact to our environment in a smart way. Sensors are found in common house hold commodities such as smoke detectors, refrigerators, washing machines; in personal equipment such as capacitive sensor in our smart phones, accelerometers in airbag release systems, motion/optical sensor in computer mouse and many others.

A typical sensor system is shown in Fig. 1.1. The sensor interacts with the environment and produces an electrical signal which will be conditioned to a suitable signal (amplified, sampled, filtered) by the signal conditioning block. Finally the signal is digitalized and either stored or further processed using the digital signal processing and delivered to the next system or to a display unit. Depending on the type of analyte involved, often exciting the environment/analyte might be necessary e.g. sending light to illuminate when optical sensor system is employed.

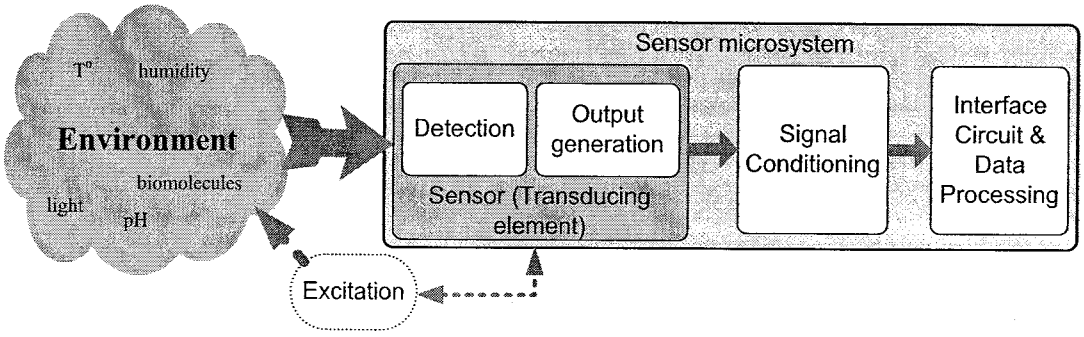


Figure 1.1: Typical sensor system

There are wide variety of sensors for variety of applications and types of stimulus involved [2] as shown in Fig. 1.2. Based on the type of signals they measure (measurand) sensors can be classified as radiant, thermal, magnetic, and so on [3-6]. They can also be classified according to the type of transduction principle they employ [3] e.g. capacitive sensors exhibits a change in their capacitance for a change in stimulus. Finally, sensors can also be classified as passive (self-generating) or active (modulating) sensors based on whether they draw their output energy from the input signal (measured phenomenon) or if they need an additional energy (excitation) source [4]. Further classification of sensors based on other parameters is found on various literatures.

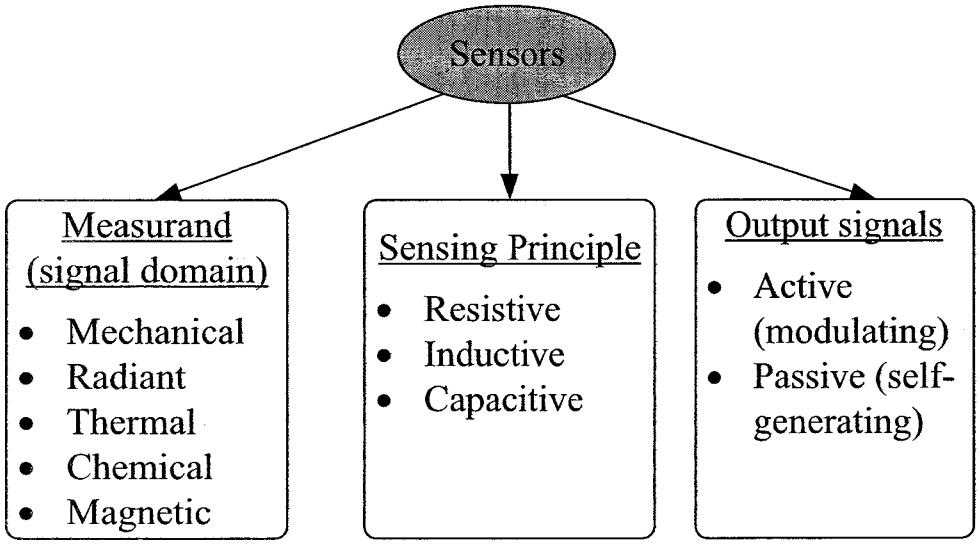


Figure 1.2: Sensor classification

1.2 Sensors and Environment

The environment is being contaminated continually by various human activities and industrial effluents. Maintaining the optimum balance of the environment (either soil or water bodies) is important to insure the continuity of proper flora and fauna life. In order to assess the impact and take actions, continuous environmental monitoring is necessary and hence demand for *insitu* environmental monitoring is a continuing research endeavor to produce a low-cost, low power, reliable sensor systems that can produce a fast result for preliminary analysis on the spot. While choosing the 'best'

sensor for a specific application, cost, size and portability, power consumption, applicability in distributive networks, packaging and biocompatibility play a major role.

In environmental monitoring portability and continuous on-site monitoring of a wide range of analytes is necessary. Basically, this goal can be achieved either by miniaturizing established analytical apparatus, or by developing miniaturized measuring devices optimized to interact with a specified analyte [7].

Commonly used categories of sensors based on the principal operating mechanism that are applied in environmental applications are: Chromatography and spectrometry, electrochemical sensors, mass sensors, and optical sensors [1]. Chromatography and spectroscopy are fairly expensive method for the separation of complex mixtures by percolation through a selectively adsorbing medium, with subsequent detection of compounds by analyzing using methods of spectroscopy. Electro-chemical sensors include sensors that detect signal changes (e.g., resistance) caused by an electrical current being passed through electrodes that interact with chemicals. Whereas mass sensors rely on disturbances and changes to the mass of the surface of the sensor during interaction with chemicals. Optical sensors on the other hand are becoming the preferred choices due to their distinct advantages [8].

1.2.1 Optical Sensors

Optical sensors fall under radiant type sensors which detect light waves. Photodetectors, fiberoptic sensors, infrared sensors, and interferometers are examples of optical sensors. Optical methods have been used for several years in various fields of analyses [9]. They can be used directly to analyze parameters such as proximity, color, intensity or indirectly to measure other variables such as concentration or identity of analyte. With the help indicator dyes, they are used in biomedical and environmental sensing applications such as level measurement for O2, CO2, blood pH; monitoring biological events [10-12] and determination of molecular concentration. Optical sensors are good candidates for monitoring variables due to their non-intrusive nature, suitability for in-line measurements, low cost and long term

usage without the need of frequent recalibrations [13, 14]. They are used actively to monitor environmental variables such as ammonia concentration in fish tank spoilage [15], phosphorous ions to determine eutrophication (change of body of water due to increase nutrient) [16], pH monitoring of the environment [14, 16], and other commonly occurring metal ions [17].

Nowadays, optical sensors are emerging as the preferred choice due to their advantages such as:

- Non- intrusive (non-contact) method for closed or toxic mediums [14]
- Compatible with CMOS technology hence suitable for miniaturization (may not require exotic processing steps or materials)
- Suitable for online integration for system control
- Considerable accuracy over other commonly known sensors [18, 19]
- Sensitivity, Low cost, non-destructive
- Do not require reference cell, as is the case in potentiometers /Electrochemical sensors [20]
- Not affected by electrical or electromagnetic interferences; more suited to sterilization techniques [21].

A typical optical sensor system is comprised of a light transducer a signal conditioning and a readout/interface circuit. The signal conditioning converts the photocurrent produced by light transducer to an amplified photovoltage and the readout/interface circuit processes the photovoltage converting it into digital form for further processing. An efficient readout circuit is highly important for overall enhanced functionality of the sensor electronics with a reduced cost, less power, smaller area or size, portability, reliability and faster signal processing.

1.3 Signal Conditioners and Interface Circuit

Sensors convert the measurand information from the environment in to an electrical domain for further processing [22]. However, it's rarely that signal from the transducer suitable to be processed and extract the information directly, hence the generated signal has to undergo some signal conditioning before it is suitable to process. This usually involves amplification, filtering depending on the sensor and the signal type. The specific form of the front end circuit is dependent on the form of the signal from the transducer and the process technology that is used to manufacture the circuit. The transducer element can output signals encoded as changes in charge, voltage or current. Low-level and high impedance signals must be amplified early in the circuit to minimize noise. [23].

A sensor interface is an electronic circuit which allows to readout the information coming from the signal generated by a sensor, providing a suitable output signal simple to display [24]. A sensor interface performs functions [25]: (i)Measurement/Reading of the appropriate sensor parameters, and (ii) Interpretation of the physical, chemical or biological phenomena to an output display or to a subsequent block.

There are varieties of interface circuits, as there are various sensors, to suit the application and working environment of the sensor system. Sensors System overall performance as well as cost can be improved significantly by integrating interfacing electronics along with sensors [26]. In this thesis, the interface circuit does not refer to the signal conditioning block but rather the interface from pre-amplification stage to the display unit or subsequent processing device.

Suitable interfaces circuits for a particular application are critical to the sensor development and applicability. Once the most promising sensing techniques are identified, it is necessary to determine input and output requirements, the major sensing device components, and the application requirements.

When developing an interface circuit for sensors, the designer has to take into account several aspects about not only the electronics itself, but also about the system

and the sensor characteristics as well as the environment where the sensor has to work. When deciding to use a particular interface circuitry, factors that come in to account are the overall cost; the volume productivity; the component availability; the sensor complexity; the tolerance of part-to-part variations; the compatibility with other system components; the reliability; the repeatability; the maintainability; the environmental constraints [27].

1.4 The role of CMOS technology

It is the CMOS technology that has made it possible to fabricate cheap integrated circuits (ICs) that are now an integral part of the world around us. The systems designed and developed using the chips produced by the CMOS technology also, in turn, help improve this technology, thereby creating a snowballing effect.

In CMOS (Complementary Metal-Oxide Semiconductor) technology, both N-type and P-type transistors are used to realize logic functions. Today, CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). CMOS technologies are superior in digital market due to low power dissipation, low area, low cost and fast technology scaling down than their bipolar counterparts. CMOS gates dissipate power only during switching. In order to benefit from low cost of fabrication, packaging and improving the overall performance, digital and analog components are included on the same chip. Even though CMOS transistors are noisier for analog applications compared to bipolar transistors [28], technology scaling down and speed improvement has enabled them to dominate the analog market as well.

Like many other fields, sensor systems technology owes a fair amount of its progress to the developments in the CMOS technology. Most importantly, it has enabled to produce cheap and flexible digital signal processing (DSP), memory on a single chip that gets denser and faster by each succeeding technology generation. When designing a complete sensor system, there are certain blocks that are not possible to implement in the digital domain and where analog circuits are required

since we dealing with the 'analog' world. Hence mixed-signal design and integration on the same chip is done.

1.5 Research Problem Statement

Multitudes of sensors are found in every application that involves interacting with our environment. Such sensors are not necessarily optimized in terms of power, complexity and cost to the application they are being used. A typical sensor system incorporates an ADC, memory and subsequent complex signal processing blocks or in some cases they may use a microcontroller to read and process their signal [29-31]. In such cases the power consumption easily shoots in to tens or hundreds of miliwatts. Moreover, overall system can get too bulky to be used for simple field monitoring application. In addition, there are many applications where a high accuracy in sensing is not essential; in such cases, a simple interface circuit can not only save the design time, but may also offer area and power advantages over the more complex circuits. Therefore, one of the main aims in this research has been to realize simple circuit topologies that may benefit such applications.

1.6 Objectives and Scope of Project

The scope of this research includes proposing an interface circuit suitable for integration on the same chip with optical sensors and validation of the interface circuit by simulation and experimental testing.

More specifically, the thesis has the following aims:

- To propose an ultra-low power and low cost interface circuit
- To verify the design via simulation and experimental analysis using discrete components as a proof of concept.

- To design and fabricate an integrated circuit (IC) design of the interface circuit using 0.35 μm standard CMOS technology and validate by conducting experimental testing on fabricated prototype.

In order to achieve its objectives, this work started by proposing a suitable interface circuit and validating the proposal by CAD (computer Aided Simulation i.e. PSpice, and Eagle PCB designer) and PCB fabrication for discrete experimental testing in the lab. After successful preliminary result, designing the integrated interface circuit in CMOS is done using Cadence Design system software. Experimental validation from the fabricated IC prototype is also carried out. Upon the need to further improve the resolution and efficiency of the proposed Interface circuit, pipelined (two-stage) is proposed and tested.

1.7 Significance/ Contribution of Thesis

This thesis focuses on the design of simple interface design suitable for integration in CMOS technologies. The main motivation being: to realize simple, low cost and low power frontends for optical sensors and microsystems for integration in field sensing applications, for example, in application where level of concentration or pH is required to conduct regulatory measures. In addition, there are many applications where a high accuracy in sensing is not essential; where a simple interface circuit is the best choice considering the cost, complexity and power consumption. Therefore, one of the purposes of this research has been to realize simple circuit topologies that may benefit such applications.

To this end two interface circuit designs have been designed and tested and an integrated circuit prototype has been fabricated. The interface circuit is low power, having less number of blocks and hence low cost making it suitable to field applications. The research work in this thesis has been presented in the formal proceedings of the following conferences and journal articles:

- Israel Yohannes, Maher Assaad, "Design and Modeling of Low Power and High Resolution Color Sensor Based Microsystem for Biochemical

Applications", **National Postgraduate Conference (NPC),** Seri Iskandar, 19-20 Sept. 2011.

- Maher Assaad and Israel Yohannes, "Design and Characterization of Multi-Color Sensor Circuit", **IEICE Electron. Express (ELEX) Journal**, Vol. 8, No. 24, pp.2093-2099, 2011.

- Israel Yohannes, and Maher Assaad, "A Four-Color Optical Detector Circuit" **International Journal of Electronics**, vol. 100(2), pp.196-204, 2012.

- Maher Assaad, Israel Yohannes, Amine Bermak "A 2-Stage Interface Circuit Design for a 32-Color Resolution Optical Sensor" **IEEE Sensors Journal**, vol.13, no.2, pp.610-617, 2012.

- Israel Yohannes, Maher Assaad, Nor Hisham B. Hamid "A CMOS Interface Circuit Design for a 32-level Resolution Light Sensor" **International Review on Simulation and Modeling (IREMOS)**, PWP, Italy, Aug. 2012.

- Israel Yohannes, Maher Assaad, Fabrice Meriaudeau, "A Low Power Interface Circuit Design for a CMOS Based Smart Optical Sensor" **International conference on circuit and systems (ICCAS)**, Kuala Lumpur, Oct 3-5, 2012.

- Maher Assaad, Israel Yohannes, Amine Bermak "A Low-Power CMOS Interface Circuit Design for Optical pH Sensor" **IEEE Sensors Journal**, 2012-2013. [under review]

1.8 Thesis Organization

In this chapter a brief overview with sensors and their application in environmental monitoring as well as interface circuit design is presented to provide motivation for the work. The next chapters in the thesis are organized as follows:

Chapter 2 presents the theoretical background of the optical sensor system including their applicability and other related research works that have implemented

optical sensors for similar applications are also discussed. The chapter further discusses the role of having efficient interface circuit in portable sensor microsystems. **Chapter 3** discusses the methodology or the step by step approach towards addressing the objective of the thesis. It also discusses the software used in the project. **Chapter 4** presents the proposed design and working principle as well as the preliminary validation using simulation in PSpice and experimental testing from discrete component implementation. **Chapter 5** discusses the main achievement of the thesis which is design of an integrated circuit (IC) and experimental testing of the fabricated prototype chip. **Chapter 6** discusses the architecture in comparison to other interface circuit and an ADC. The final chapter, **Chapter 7**, concludes the thesis by highlighting the significance of the work, the challenges and recommendations for future further implementation.

CHAPTER 2

LITERATURE REVIEW

The chapter presents a theoretical background of an optical sensor system and their building blocks. The chapter further discusses application example in set up of optical sensor for analysing environmental variable.

2.1 Optical Sensors and their Principle of Operation

Optical methods are one of the well-established techniques for sensing biochemical analytes [32]. By taking advantage of interaction of light with matter and electronic signal elaboration capability, environmental sensing procedures can be effectively miniaturized to autonomous and portable sensors.

Based on whether an indicator reagent is involved, optical chemical sensors can be categorized as direct sensors (label free) and reagent-mediated (labeled) sensors [33, 34]. Direct (label free) optical sensor makes use of the analyte's intrinsic optical property; while in reagent-mediated optical sensing systems; an intermediate agent is used to monitor analyte property. This latter technique is useful particularly in the case where the analyte has no convenient intrinsic optical property, which is the case for many analytes. In optical sensing, the most commonly employed methods are absorption, emission and reflection (fluorescence) and scattering of light (refractive index) [20, 35]. Although fluorescence and reflectance have gained increasing interest, absorbance (or transmittance) still remains the most employed optical principle [36].

Instrumentation for optical measurements generally consists of a light source (to generate a light beam), filters and waveguides (e.g. fiber optic cable - to direct light to

a modulating agent), a photodetector (for processing the modulated optical signal), the electronics for signal processing and, finally, a user interface unit for results visualization [32]. Although the actual implementation vary depending on the type of application intended and the materials involved, a general block diagram of a basic optical sensor setup can be represented as illustrated in Figure. 2.1. The modulating agent is the receptor molecule which brings a change in the optical parameter, e.g. color or intensity change, based on the physical property of the sample under test (SUT). The receptor identifies the parameter of interest and provides an optical signal proportional to the magnitude of this parameter, while the sensing element or photodetector produces a coresponding electrical response to be amplified, converted or other necessary manipulation by the signal processing unit. The focusing lens, absorption filters helps to focus the light to the active area of the sensor and filter out unwanted spectra respectively. Moreover optical fibers can be used in optochemical sensing to serve the purpose of guiding light to and from the SUT [37]. Finally the signal processor measures either photovoltage, photocurrent, life time or other electrical parameters and produces a suitable signal to a direct user or data storage unit. In this thesis, we are interested in photovoltage/photocurrent measurement and output a digital value that represents the sensed color (wavelength) or intensity information.

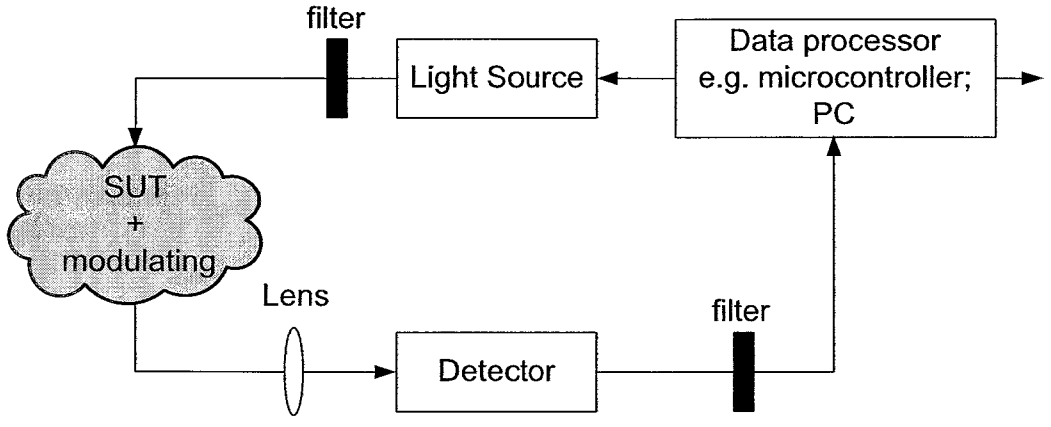


Figure 2.1: Typical Optical sensor setup

2.1.1 Light Source

Wide selections of light sources are available for optical sensor applications. These include: broad spectrum incandescent lamps e.g. tungsten halogen lamps; narrow-band LEDs and Laser diodes. The important requirements of light sources are generating a stable and intense radiation. Laser diodes have narrow band emission spectra (as low as 1 nm spectral bandwidth) and are good for highly selective applications but are rather expensive. In contrast, tungsten lamps are cheaper and can provide a broader range of wavelengths, higher intensity, better stability and long life span but require a sizable power supply and can cause heating problems [34]. In certain applications, e.g. in portable instrumentation, LEDs are chosen due to their significant advantages over other light sources. They consume lower power, are small and inexpensive, produce a narrow band with 25-50 nm spectral bandwidth and are easy to work with. Figure 2.2 illustrates some of the UV-visible spectral region covered by commercially available light emitting diodes. The maximum of absorbance or excitation of the selected modulating agent for a particular application has to be matched with the spectral bandwidth of the light source being used [34].

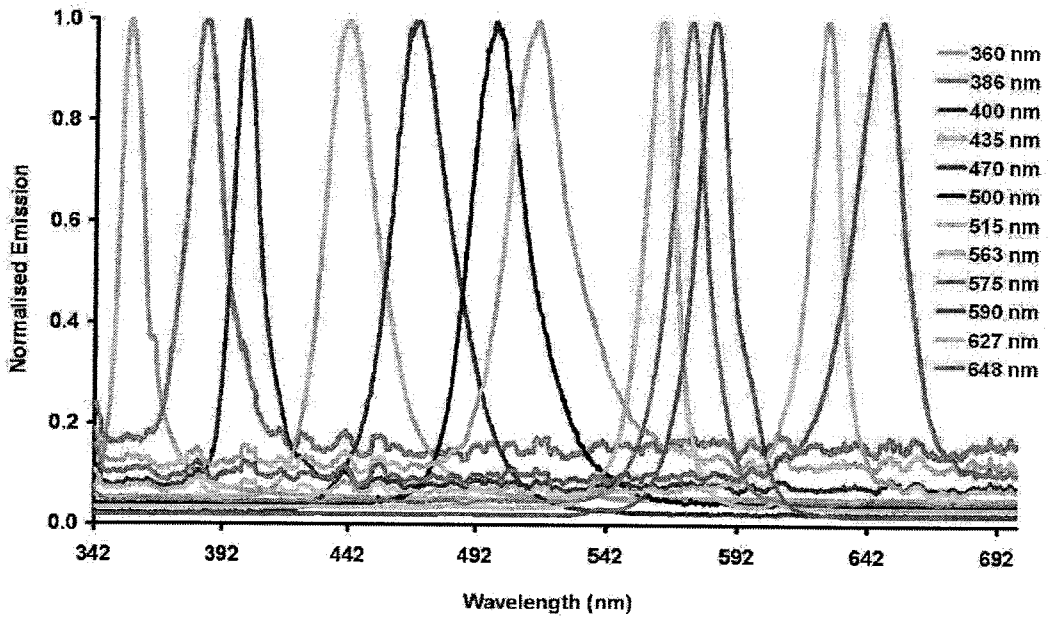


Figure 2.2: spectral range covered by a variety of commercially available LED [17]

2.1.2 Indicator Reagents

Indicators are synthetic dyes that can bring change in color upon interaction with chemical species as a result converting the analyte physical property in to a measurable optical signal [38].

2.1.2.1 Absorption Principle

The most commonly used analytical technique for the routine analysis of biochemical parameters of patient's physiological fluids is the colorimetric change detection that results from the interaction of a known reagent with a given parameter in those fluids [39]. These reagent–biochemical parameter mixtures have an absorption maximum at a specific wavelength. The absorbance value at this wavelength is directly proportional to the concentration of the biochemical parameter in the physiological fluid samples.

Absorption method is based on Beer- Lambert law [40] which dictates that a light beam passing through an absorbing homogenous solution a fraction of it is absorbed which is proportional to the type of material (its molar absorptivity) and the concentration of the analyte. It connects the expected decrease in transmitted light (absorbance) with the properties of the material. The law may be written in terms of the absorption A (shown in (1.1)) which is defined as the logarithmic relative decrease intensity: where Io and I are the light beam intensities before and after passing through the sample respectively. From the absorption we can determine either the concentration or the material type when the other parameters are known based on Equation (1.2). Where L is the optical path length, C is the concentration and $\varepsilon(\lambda)$ is the molar absorptivity [9].

$$A = \log\left(\frac{I_0}{I}\right) \qquad 1.1$$

$$A = \varepsilon(\lambda)LC \qquad 1.2$$

The spectral properties of such a receptor used should be compatible with the photodetector, and light source selection.

2.1.2.2 Fluorescence Principle

Fluorescence sensors use indicator dyes which can be excited by a particular wavelength of light and re-emit a lower wavelength light (different colour of light from the absorbed). Fluorescein is used commonly as indicator in fluorescence applications and has an excitation maxima of λ=490 nm and emission maxima λ=515 nm [41, 42]. Hence a an excitation source with peak wavelength at 490 nm and a photodiode of peak sensitivity at 515 nm can be used along with fluorescein for a detection application.

2.1.3 Photodetector

Photodetectors are the essential part of the sensor that interfaces the sensed information to electrical signal. Photodetectors can be broadly classified into two groups: thermal detectors and quantum detectors [43]. Thermal detectors absorb photons and causing warming of their bulk e.g. thermal radiation sensor. Such detectors wide operating range of wavelengths, but are relatively slow and have a low sensitivity. On the other hand, quantum detectors follow the principle of photoelectric effect where individual absorbed photons deliver enough energy to transit an electron from a lower energy state to a higher energy state as a result of the absorption of a photon overcome some threshold to release charge e.g. photodiode.

In choosing photodetectors for optical sensors, a number of factors must be considered are sensitivity, noise, spectral response, and response time. Accordingly a photodetector must possess a peak sensitivity at the measurement wavelength; must generate a minimal amount of noise and must respond rapidly to a variation in intensity of the incident light [35]. There are many types of photodetectors depending on the application requirement. A review of the commonly used photodetectors for biochemical sensing applications can be found in detail in [44]. Photodiodes are mostly the attractive choices for optical sensing because of their simplicity of application, low power consumption, compactness and easily integrated in commercial CMOS process.

2.1.3.1 Photodiode

Photodiodes are made up of p-n junction and produce photocurrent upon exposure to an electromagnetic spectrum in the visible region. Photocurrent is generated when the absorption of visible light in the silicon bulk induces electron and hole carriers across its depleted junction causing a drift current. The structure of a typical n/p-substrate photodiode and its equivalent circuit [1] is shown in fig. 2.3.

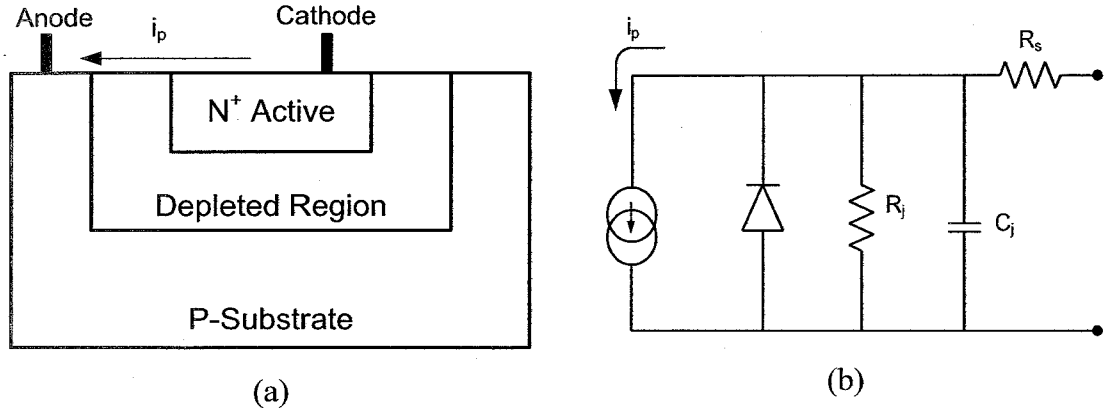


Figure 2.3: (a) n/p-substrate photodiode and (b) Its equivalent circuit

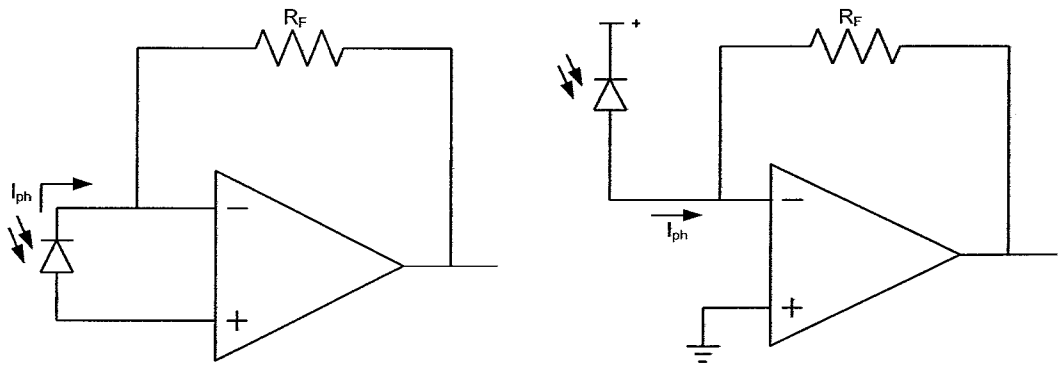
The maximum photo-current of a photodiode in the presence of a reflectivity coefficient and an absorption over a thickness can be given by (1.3) [45, 46]. Where R is the surface reflectivity of the photodiode; α is the absorption coefficient which is dependent on the material property(e.g. silicon or GaAs); d is depth from the silicon surface; q is electron charge; Pin is the power of incident light; h is Planck's constant ; and v is the frequency of incident light

$$I_{ph} = (1 - R) * \left(1 - e^{\alpha * d}\right) * q * \frac{P_{in}}{h\nu} \qquad 1.3$$

Photodiodes can be operated with a reverse bias voltage (photoconductive mode) or with zero bias (photovoltaic mode) depending on the application intended. Photoconductive mode improves linearity and speed of response while increasing noise and dark current whereas photovoltaic mode minimizes variation of response due to noise, temperature and is preferable for low speed and low light level applications.

a) CMOS photodiodes: Depending on the required application, photodiodes are fabricated with different processing in CMOS process to enhance their selectivity and spectral response e.g. TFD (transverse field detector) [47], BDJ (buried double junction) [48, 49]. Such photodiodes can be used for the simultaneous measurement of light intensity and color without using an optical filter [50] due to their monotonous response in the visible spectra.

b) Light-to-voltage converters: Light-to-voltage converters are made by combination of photodetectors that produces photocurrent and current to voltage converters [1]. Transimpedance amplifiers are usually employed to convert current to voltage and at the same time amplify the weak signal from the sensor. There are a number of commercially available monolithic light-to-voltage converters e.g. TSL257 (TAOS sensors) [51] , OPT integrate photodiode series [52]. Photovoltaic and photoconductive mode of biasing of photodiodes and amplifiers (Light to voltage converter) is shown in the Fig. 2.4.



(a) photovoltaic mode (b) photoconductive mode

Figure 2.4: photodiode modes of operation

2.2 Optical Sensor Application

Optical sensors can be applied in monitoring environmental and biochemical variables by measuring the intensity [53] or wavelength [39, 54, 55] of the solution

under test. Depending on the solution intrinsic character, an indicator reagent can be added to the solution to bring a measurable color change. Illustration of measurement setup can be seen in Fig 2.5. A light from a suitable source is used to excite the analyte-indicator solution. This light has to pass through an optical filter to remove the undesired wavelength from the emission spectra. Filtering is done due to undesirable spectrum such as infrared and noise involved in many light sources. The light passes through the analyte-indicator dye solution and coded by the color information of the solution. A focusing lens is can be used to maximize the amount or light rays falling on the active area of the photodiode. Finally analysis of the photodiode response is carried out.

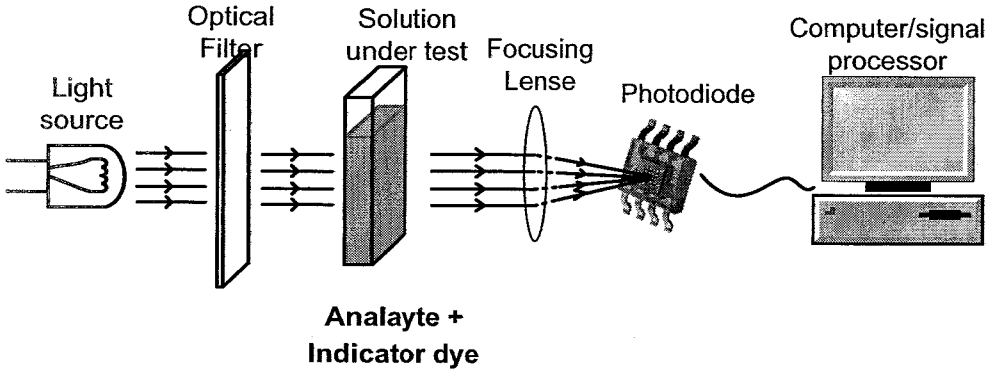


Figure 2.5: optical sensor analyte measuring arrangement (for illustration)

Many sensor systems make use of personal computers and or microcontrollers to interpret sensed data from the sensor and output a meaningful result [16, 42, 56, 57]. Such systems enable flexibility by the designer to manipulate the data and generate result. Although such process undeniably results in accurate interpretation of result, it also adds complexity, to the overall system and cannot be portable.

CHAPTER 3

METHODOLOGY

A low cost, low power and simple sensor architecture based on optical sensing methods to monitor environmental variables like pH and concentration of various ions is required. In this work the interface circuit which is a mixed signal solution and suitable to be integrated with the sensor microsystem is proposed and validated. In the current chapter the step by step approach from proposal to testing the final design as well as the main software used in the process are discussed briefly.

3.1 Step-by-Step Design Approach

Signal from the environment is detected by the optical transducer and the response is fed to the interface block for signal processing. Two interface circuit architectures are proposed and validated in this project - namely: One-stage and Two-stage (pipelined) interface circuit design. The approach towards designing and validating the proposed designs is shown in the flow diagram Fig 3.1.

As illustrated in the flow diagram, once the problem statement is identified, proposing a design solution follows. The design is formulated on paper and is simulated to test its functionality using PSpice. Rigorous transient, time domain analysis is carried out until desired response graph is found successfully. The reason for using PSpice is due to simplicity of implementation and availability of multitudes of library model files representing actual components ready for simulation. After successful simulation in PSpice, the same components that are used in simulation were bought from the respective supplier to conduct experimental testing using discrete components.

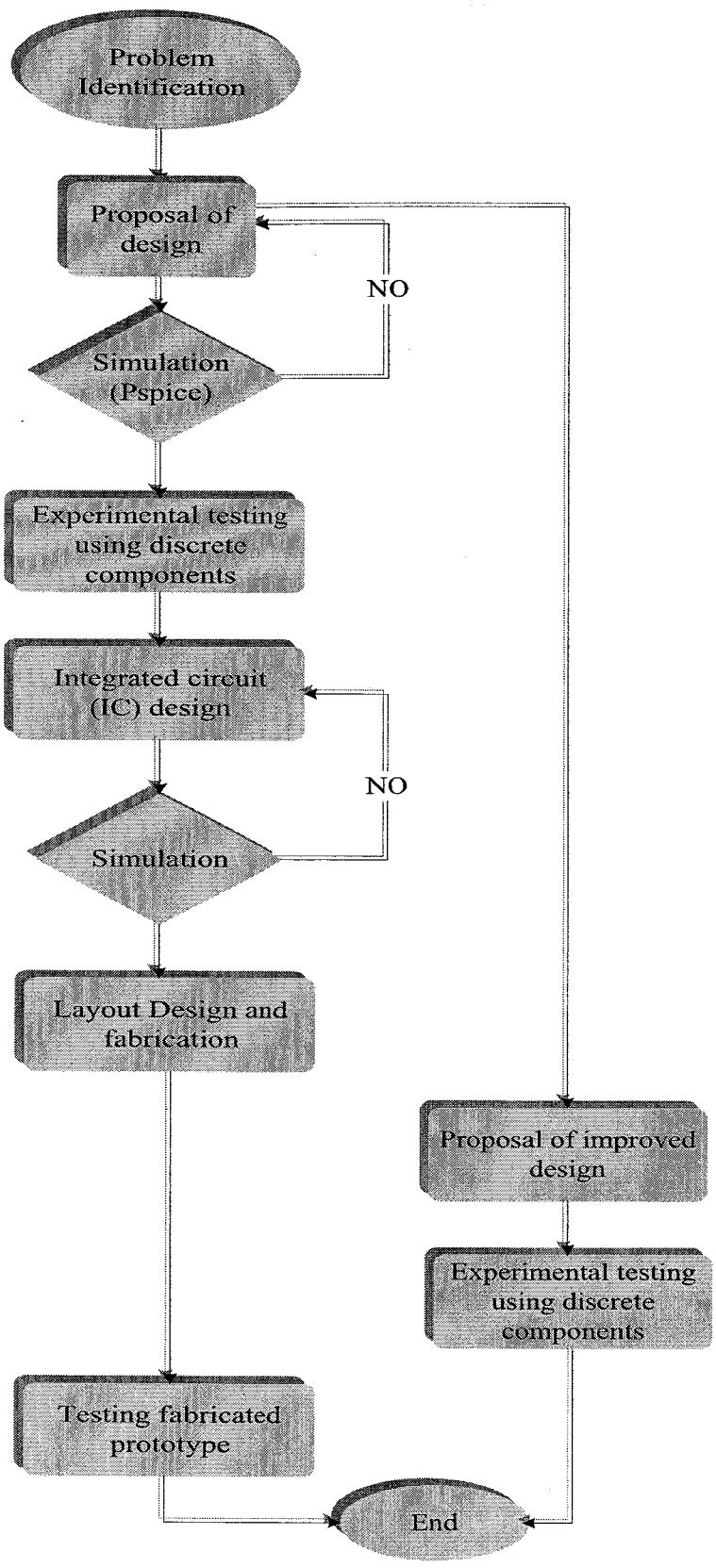


Figure 3.1: flow-chart illustrating step by step process towards completion of the M.Sc. thesis

After the proof of concept validation using discrete components is through, designing integrated circuit is carried out. Functionally equivalent and optimized integrated circuit (IC) blocks were designed and simulated in Cadence design system software using standard CMOS 0.35 μm Austria Microsystems technology. For the first design (one-stage), the process continued until designing layout, fabrication of the IC and experimental testing of the fabricated prototype. Characterization of the fabricated prototype is done by supplying various inputs and recording the result using data acquisition oscilloscopes.

The main highlight of this M.Sc work is the fabrication and testing of the Integrated Circuit (IC) which is a promising step towards an integrated single chip, portable, low power sensor microsystem.

Finally, while the tape-out of the first design is under fabrication, a more efficient and higher resolution design (two-stage design) is proposed and validated via simulation and experimental design.

3.2 PSPICE

PSpice is a personal computer version of SPICE (Simulation Program with Integrated Circuit Emphasis) program which is in the OrCAD product family. It is an industry-standard Spice-based simulator for system design simulating complex analog-only, mixed analog/digital, and digital-only circuit designs containing both analog and digital parts, and it supports a wide range of simulation models [58]. PSpice is chosen as the validation tool for preliminary designs due to its availability and user friendly interface combined with accuracy of analysis.

The version used is PSpice 9.2.3, a product of Cadence Design system, and it has functionalities of both analog and digital simulation (mixed signal design) with DC analysis, AC analysis, and transient analysis and so on. The software incorporates silicon based device models from variety of semiconductor device vendors hence

enabling near actual simulation validation of a design before hardware implementation with the actual components. PSpice is helpful due to:

1. Simplicity of implementation and multitude of available components supplied in library.
2. Evaluate different varieties of a design and with different building blocks
3. Assessing performance of design
4. Evaluate circuit performance with non-linear elements
5. provides opportunity to explore with more parameter
6. Optimize circuit design without actually having to build the design hence saving a great deal of cost and time.

3.3 Custom IC design Using Cadence

Cadence Design System (Cādence®) is electronic design automation (EDA) software that provides front to back design tools for semiconductor design. It serves as a platform for designing customized ICs by using different CMOS technologies. Based on the type of block cells involved, design flow in cadence can be [59]:

- All digital design flow using behavioral modeling (using HDL languages e.g. Verilog, Verilog-A) and a synthesizer. This option requires availability of fully functioning standard cells in the library.
- All analog design flow by drawing schematic and manually connecting the cells/blocks.
- Mixed signal design flow where using both aforementioned options (analog and digital design flow) is possible.

While designing a custom IC, two hierarchical design approaches can be followed [60]: bottom-up approach and top-down approach:

- Bottom-up approach: starting with the basic functional microcells and blocks which are next used to create more complex ones. This process continues until reaching the top-level structure of the design. In this case all blocks can be simulated and verified before incorporating in to the main design.

- Top-down approach: starting from top-level structure of the design defining the main functional blocks and connections between them. Then the contents of these main blocks will be defined using simpler modules. This process continues until reaching the bottom level, at which modules are built from primitive components.

In this project a mixed signal design interface circuit for the optical sensor is designed using the analog design flow in Cadence Spectre and by using bottom-up approach. A typical bottom up design flow using Cadence is summarized in the flow diagram [61-63] illustrated in Fig 3.2.

3.3.1 Design Specification

The first stage in any design is to formulate the detail specification from the application requirement e.g. power specification, expected outcome, response time, and input & output signal types. At this stage the general circuit topology and constituting blocks/cells are spelled out which may be subject to design trade-off to some extent during later stages.

In this project, the initial design specifications for the interface circuit, from the project objective as well as cost point of view, are:

- Technology: 0.35 μm CMOS

- Circuit area < 3 mm2

- Dynamic power dissipation (at VDD=3.3 V) < 100 μW

The selected process is 0.35μm AMS standard CMOS process with 4-Metal, 2-poly and a supply voltage of 3.3 V.

This technology allows integration of all basics components, as the MOS transistors, capacitors and resistors.

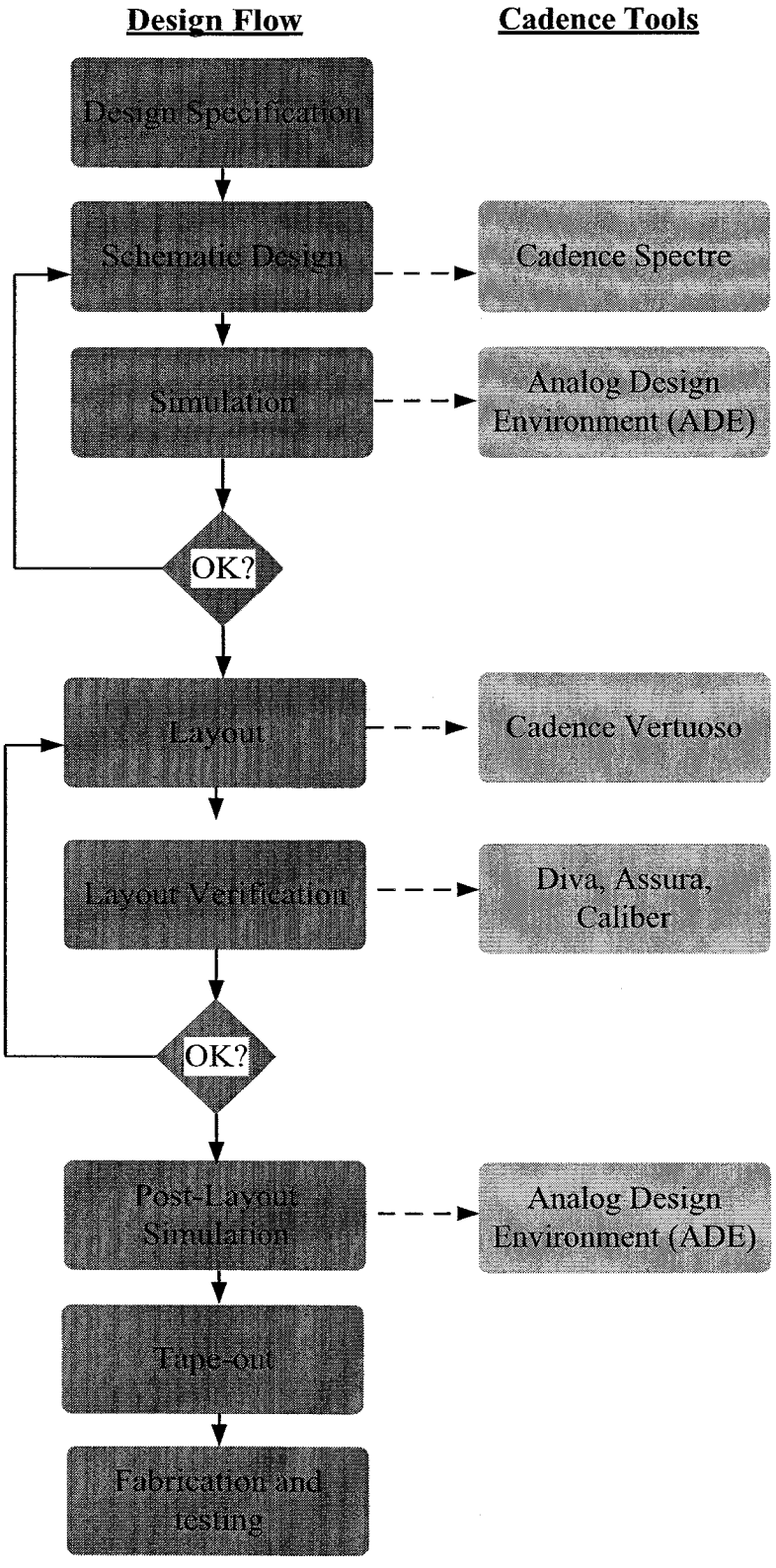


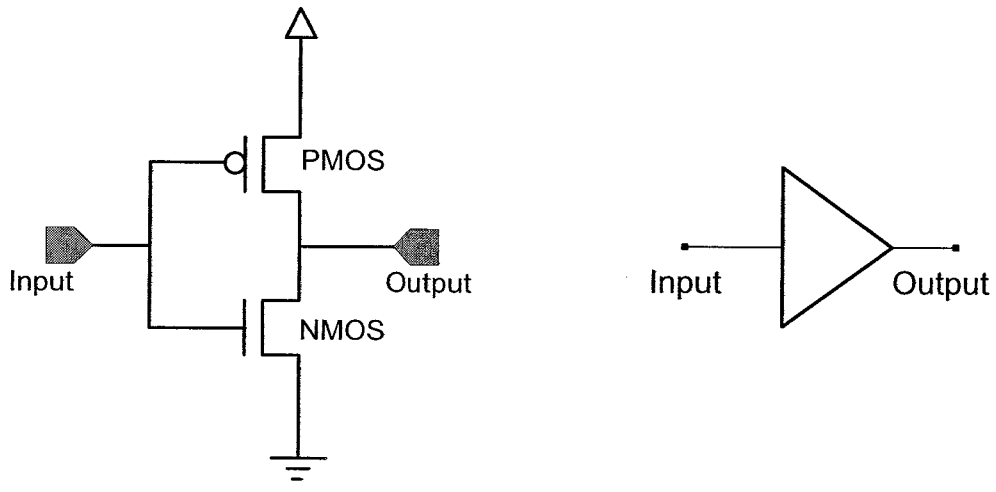
Figure 3.2 Custom IC design flow

3.3.2 Schematic Design

The generation of a complete circuit schematic is the first important step of the transistor-level design flow. This stage follows after setting the design specification and rough outline of the circuit topology, or in our case already simulated and validated beforehand. Cadence Spectre tool is used at this stage.

Spectre provides simple, intuitive means to draw, to place and to connect individual components that make up the design. The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections.

Also included in the schematic are the power supply and ground connections, as well as all "pins" for the input and output signal of the circuit. This information is crucial for generating the corresponding netlist, which is used in later stages of the design. For our design, involving bottom-up hierarchy, each block is designed and represented with a symbol. The symbol view of a circuit module is an icon that stands for the collection of all components within the module and can be used in simulation in block level simulation. Fig 3.3 below shows an example of a CMOS inverter circuit and its standard symbol view representation.



(a) schematic view (b) symbol view

Figure 3.3: A CMOS inverter

3.3.3 Simulation

It is done for each block and later after all the necessary blocks that make up the design are completed. After the transistor-level description of each block in the circuit is completed the electrical performance and the functionality of the circuit must be verified using a Simulation tool. This step serves as the first validation of the circuit operation and also detects design errors that may have been created during the schematic entry step such as unintended crossing of two signals and broken connections, name errors. Based on simulation results modification of some of the device properties (such as transistor width-to-length ratio) in order to optimize the performance hence, it is extremely important to complete this step before proceeding with the subsequent design optimization steps.

3.3.4 Layout

The creation of the layout is one of the most important steps in the full-custom (bottom-up) design flow, where the detailed geometries and the relative positioning of each mask layer to be used in actual fabrication is defined using a Layout Editor. Fig. 3.4 below shows a layout view of an inverter. Physical layout design is very linked to overall circuit performance (area, speed and power dissipation) since the physical structure determines the transconductances of the transistors, the parasitic capacitances and resistances, and obviously, the silicon area which is used to realize a certain function [64].

3.3.5 Layout Verification

This step is important in order to avoid fabrication defects. It includes Design Rule Check (DRC), Extraction and Layout Versus Schematic (LVS).

- Design Rule Check (DRC): checks if the design conforms to a complex set of design rules, such as geometry limitation (minimum width, spacing, extension, and enclosure), antenna effect. Design Rule Checker (built- in tool in the Layout Editor), is used to detect any design rule violations during and after the mask layout design. Errors markers displayed in the layout editor to locate the

error indicating which rules (specific to the technology involved or general rule) are violated.

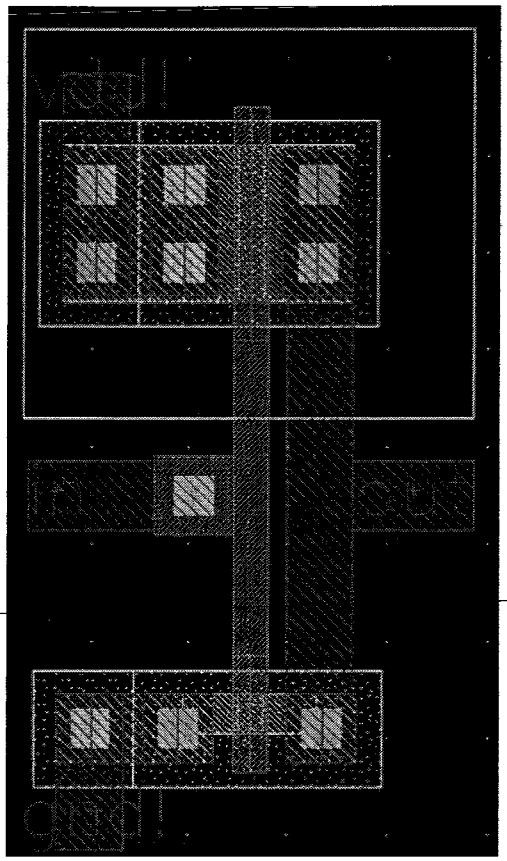


Figure 3.4: Layout view of an inverter.

- Extraction: creates a detailed netlist of the layout design providing a very accurate estimation of the actual device dimensions and device parasitic (parasitic, resistance, parasitic capacitance, diode, and so on) that ultimately determine the circuit performance.

- Layout versus Schematic (LVS): In order to confirm that the layout is a correct realization of the intended circuit topology, the extracted netlist is compared against the circuit netlist.

3.3.6 Post-Layout Simulation

The electrical performance of a full-custom design can be best analyzed by performing a post-layout simulation on the extracted circuit net-list. The detailed

(transistor-level) simulation performed using the extracted net-list will provide a clear assessment of the circuit speed, the influence of circuit parasitic (such as parasitic capacitances and resistances), and any glitches that may occur due to signal delay mismatches.

3.3.7 Tape-out

At this stage the core (which is the designed IC) is equipped with I/O peripherals that are compatible to the signal type (analog/digital/clock signals) and the maximum voltage or current they are capable of. And the final file that is to be sent to fabrication is generated in GDS II format.

3.3.8 Fabrication and Testing

Fabrication of the prototype IC is carried out at the foundry based on available commercial process. Packaging type is chosen carefully at the request of the customer. Plastic or ceramic type materials, SOC or DIP configuration or open-able or non-openable lid is decided based on the application and usage. Once the fabrication is done, experimental testing is carried out to verify whether the prototype meets expectation or not.

3.4 Summary

The current chapter discussed the step by step procedure of designing the proposed interface circuitry. Also discussed were two major software: PSpice and Cadence Virtuoso, which were used extensively throughout the project. In this work the interface circuit which is a mixed signal solution and suitable to be integrated with the sensor microsystem is proposed and validated. In the current chapter the step by step approach from proposal to testing the final design as well as the main software used in the process are discussed briefly.

CHAPTER 4

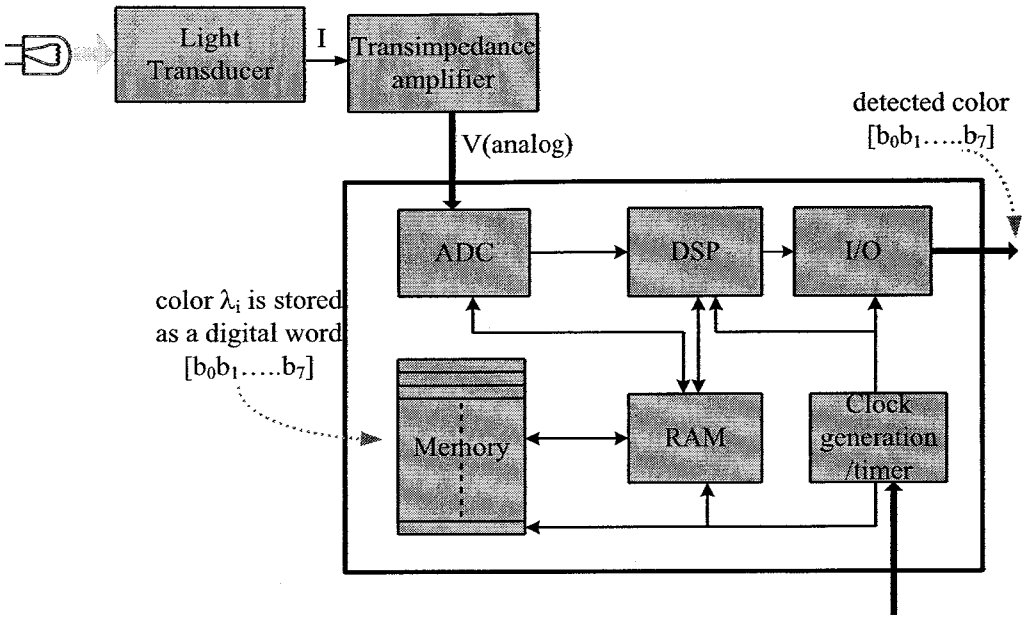
PROPOSED INTERFACE CIRCUIT DESIGN

The ever increasing application of sensors networks in various fields is increasing the demand for low cost, low power sensor systems for monitoring various physical variables in our environment. After the sensor output signal passes through signal conditioning block for amplification and possible signal conversion (e.g. current to voltage, frequency to voltage so on.), a typical low cost optical sensor system takes advantage of using microcontroller or a personal computer to process its signal which includes ADC , Memory and DSP units as shown in Fig. 4.1(a) below [42, 56, 57, 65]. Such system will have high power consumption (usually in tens of milliwats) and large size which affects their portability and in turn their field applicability. Moreover, they are not optimized enough since they are not using a dedicated processor

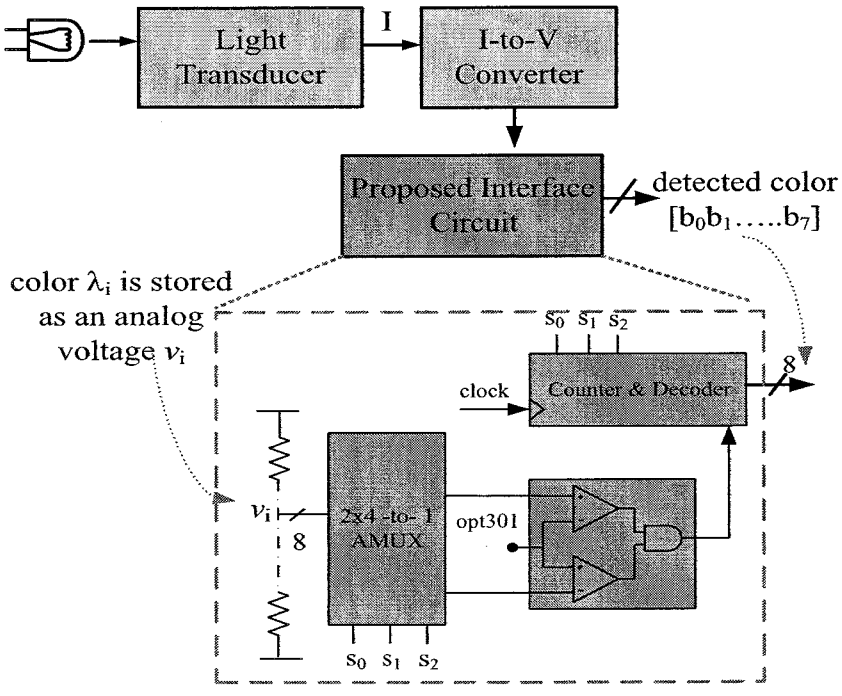
The interface circuit introduced in this work reads an analog input from a transducer and outputs a digital value corresponding to the detected light. The proposed system, shown in Fig. 4.1(b), uses an interface circuit which consists of two comparators, two multiplexers and a few logic gates and it avoids the use of further signal processing components. Fig 4.1 illustrates the distinctive feature of the proposed interface circuit with respect to conventional architecture of a typical optical sensor interface circuit. Typical optical sensor consists of:

a. An interface block to pre-amplify the signal and/or change the signal from current to voltage domain;

b. An ADC to convert the analog input to digital output for a fully digital processing; and



(a) Conventional optical sensor system



(b) Optical sensor system using the proposed interface circuit

Figure 4.1: Block diagram comparison of the of (a) Conventional optical sensor system; (b) Optical sensor system using the proposed interface circuit (mixed-signal interface circuit)

c. A DSP for further signal processing which may include a memory, digital comparator arrays, arithmetic units and so on depending on the application at hand.

The proposed interface circuit uses stored analog memory on a variable resolution resistor ladder, and directly does processing in analog domain while generating a digital result at the end. As will be explained in the subsequent sections, the interface circuit is able to output a user ready data to a display unit.

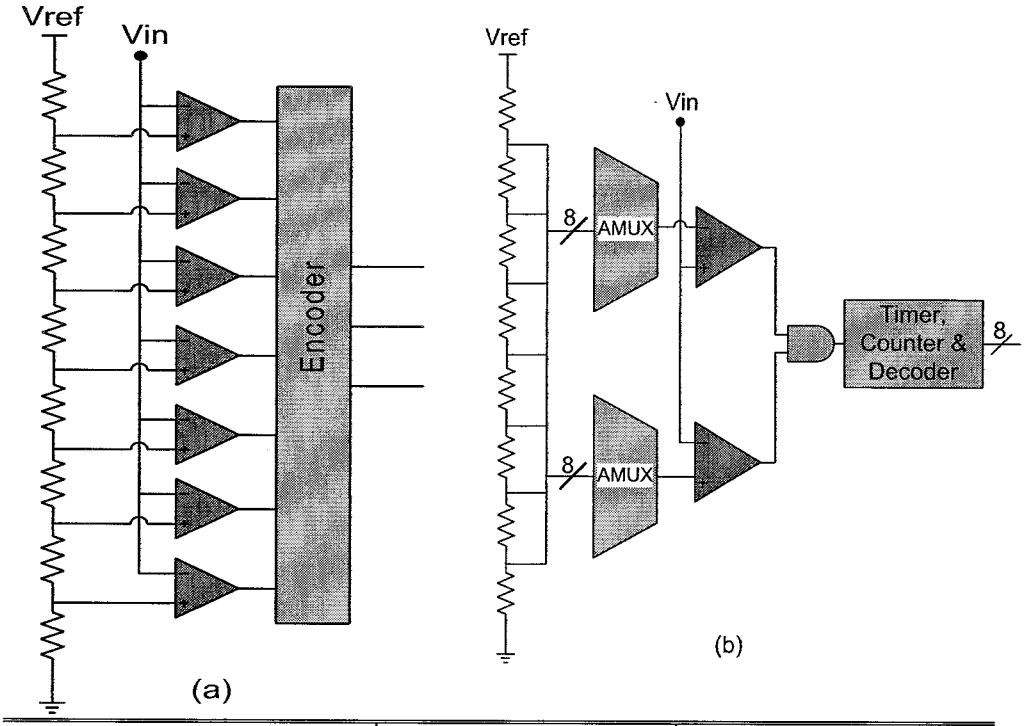
4.1 Comparison with Conventional Flash ADC

The proposed interface circuit has some analogy to a conventional flash ADC in terms of architecture but has key points that make it peculiar and advantageous. Fig. 4.2 illustrates comparison of a typical flash ADC and the simplified proposed interface circuit design graphically.

1. The first difference is about component count and as a result power and area consumption. The proposed interface circuit utilizes only two comparators per stage, i.e. One-stage and Two-stage designs utilize an overall 2 and 4 comparators respectively, regardless of the number of colors (number of output bits) being detected. Whereas a conventional flash ADC has $2^N - 1$ comparators, where N is the number of output bits. This number will shoot very high for higher resolution ADCs e.g 5 bit flash will have 32 comparators! While the proposed interface circuit maintains 2 or 4 comparator. By having less number of comparators the power consumption as well as the on-chip area can be greatly reduced with some trade-off with the speed of conversion.

2. The second difference or advantage of proposed circuit is in terms of resolution variability. Using variable resolution enhances the fitting to desired response better than using a typical ADC as sensor interface as illustrated in Fig. 4.3. Assume the response of an optical sensor is a curve as shown in dotted line. Since it has a flatter response at the top, more information is condensed there. With typical ADC this information will be lost but using the

proposed solution, we can adjust the resolution to fit to the desired response. The proposed design uses variable resistors to store analog memory that represents the light transducer response. Hence it serves the purpose of analog-to-digital conversion as well as outputting the final color information in digital form by comparing with the pre-stored color values (color representing voltage).



	(a)	(b)
Number of resistors	2^N $(2^3 = 8)$	2^N $(2^3 = 8)$
Number of Comparators	$2^N-1 = (2^3-1 = 7)$	2
Number of active bits at a time	1 to 3	only 1
Active bit duty cycle	100%	Controlled by timer (10-100%)

Figure 4.2: Comparison of (a) 3-bit flash ADC and (b) proposed interface circuit (3-bit implementation)

3. Finally, the last peculiarity is in terms of optimization to direct LED based data display. The interface circuit uses simple LEDs to display the output which can draw considerable power from the interface circuit, for such reason,

the output bits in the interface circuit are decoded to be only one bit "hot" ("1") at a time representing the corresponding color. Moreover, the duration of the active bit (duty cycle) is controlled by an optional timer block included in the design. Such efforts are done towards further reducing power consumption of the overall system during implementation.

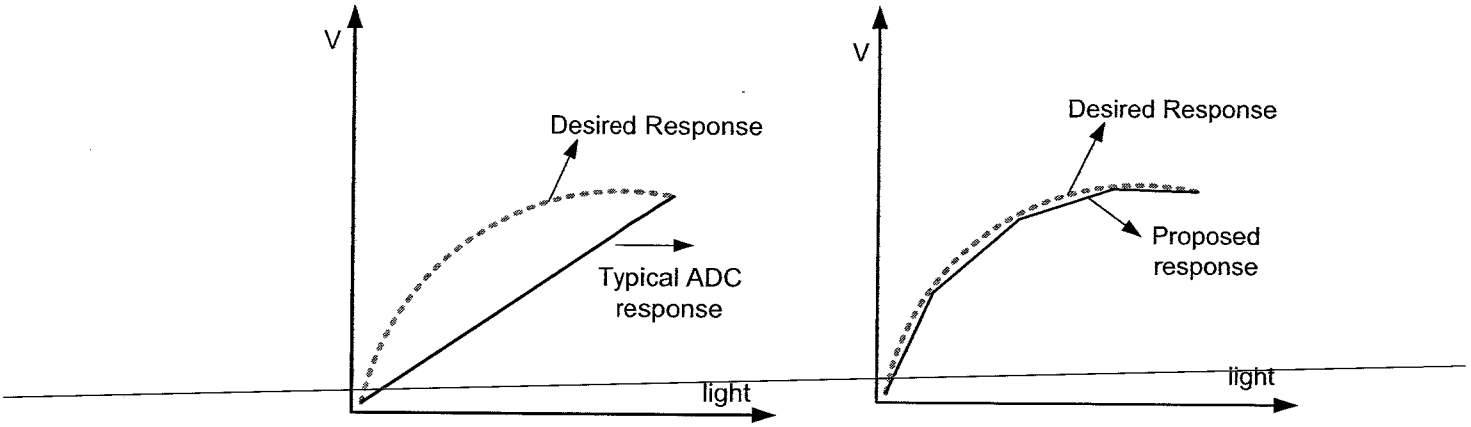


Figure 4.3: Typical ADC response and proposed interface circuit response

4.2 Complete Optical Sensor System

In this thesis we propose a dedicated mixed signal interface circuit interface circuit design for an optical sensor that consumes very low-power and suitable to be integrated on the same chip with the transducer and signal conditioning circuit. Since the proposed interface circuit design is based on a complete optical sensor system, a brief overview of the optical sensor system and its blocks is given before proceeding with the interface circuit design discussion.

The proposed complete optical sensor system consists of a light transducer, a preamplifier block and an interface circuit block. Such a light transducer and a preamplifier integrated are found in the market by few optical sensor suppliers. The OPT301 package includes an integrated photodiode and a transimpedance amplifier with a gain adjust options as desired by the designer.

4.2.1 OPT301

The proposed sensor microsystem requires a monotonic photodiode response (i.e. one to one mapping between wavelength and photocurrent) to achieve an accurate processing of the response in order to get a unique digital output. This becomes apparent after discussing the interface circuit section. OPT301 photodiode from Burr Brown [52] is chosen to be used as such element. The responsivity curve of a consumer photodiode (OPT301- Burr Brown), shown in Fig. 4.3., relates photo-voltage and photocurrent against wavelength normalized with the incident light radiant power (A/W). OPT301 integrated photodiode is suitable for the proposed sensor system due to its features such as low dark current, high responsivity, noise elimination and the required monotonic response in the visible electromagnetic spectra (380nm to 700nm) as shown in Fig. 4.3.

Apart from a linear response, the reason for choosing OPT301 is due to the already integrated in transimpedance amplifier. The purpose a transimpedance amplifier is to convert the photocurrent to a usable voltage amplifying it at the same time [66]. Signal amplification early in the system is important to minimize the signal to noise ratio performance of the overall circuit. Moreover it is also used to increase the resolution of the sensor output. In the OPT301, with the help of the integrated transimpedance amplifier, the current output of the photodiode is converted to an amplified voltage equal to IRF where RF is an internal feedback resistor laser trimmed to 1MΩ ±2%. OPT301 provides an option to connect an external resistor for feedback depending on the voltage amplification level and bandwidth needed.

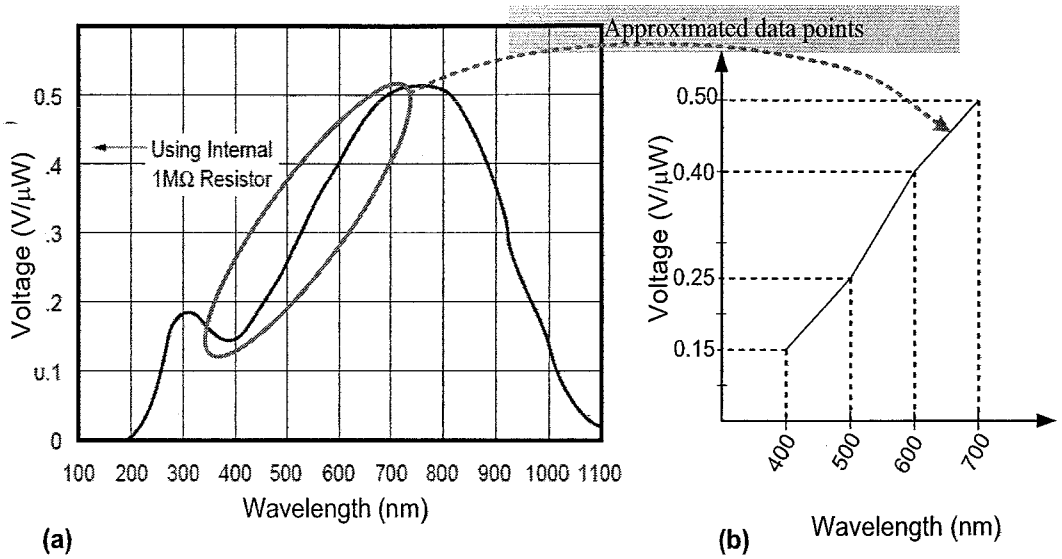


Figure 4.4: (a) Photodiode response. (b) Circled part is approximated as a linear region for simulation purpose [52].

4.3 Proposed Interface Circuit Design

Signal transformation by the interface circuit is to convert the output of the transducer to a suitable form e.g. current to voltage, analog voltage to frequency or digital form and so on. The proposed interface is a mixed signal solution containing both analog and digital blocks. It accepts analog input voltage from the optical transducer and produces a digital word that represents the sensed signal. The proposed interface circuit outputs a digital value (without the need for an ADC, DSP, and memory units) which can be directly used by a user in real time monitoring applications. Two related designs, namely One-stage design and Two-stage design, have been proposed as an interface circuit. These designs have been validated by simulations on PSPICE, Cadence design systems software and experimentally by discrete implementation and prototype testing on fabricated chip.

The proposed design constitutes few blocks keeping its simplicity and suitability for low power application. Moreover, its resolution can be extended for higher resolutions without major change to the architecture. The interface circuit continuously runs as long as there is a power supply and a clock input signal without requiring any interference from a user, making it ideal for continuous monitoring

applications. In the following sections the design and operating principle of the designs are discussed.

4.3.1 One-Stage Design

The one-stage design directly analyses the photovoltage input and outputs a digital value in just one stage process. Fig. 4.5 shows the block diagram of the design implemented for a resolution of 'n' levels. The interface circuit consists of a resistor ladder, two analog multiplexers, two comparators, three D type flip flops, a counter, a decoder and an optional timer. Each of the main constituting blocks of the proposed one-stage interface circuit is discussed briefly below.

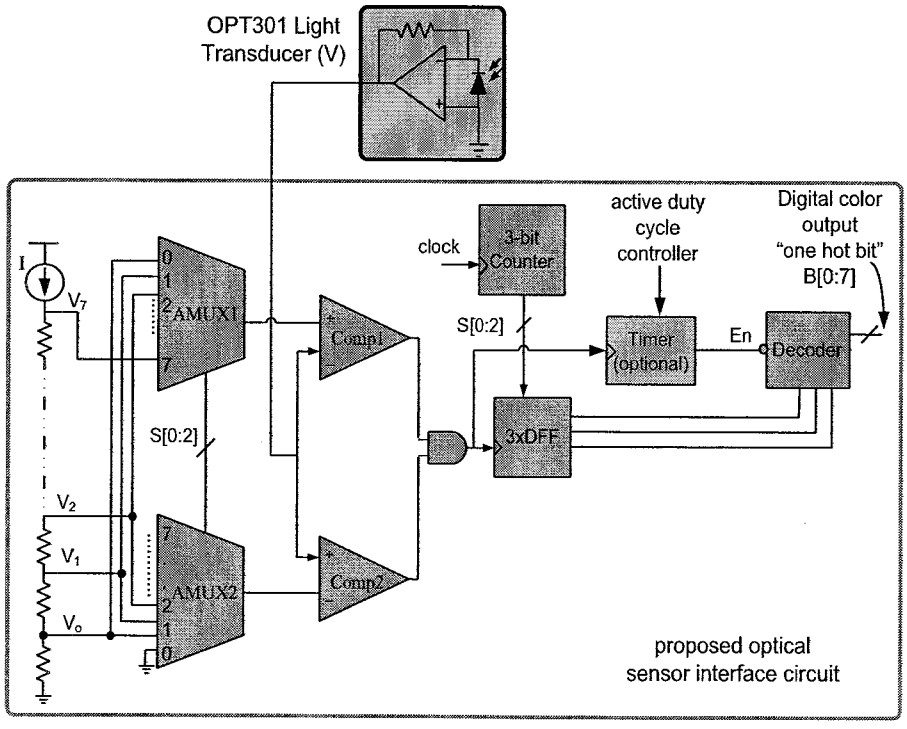


Figure 4.5: One-stage Interface circuit design.

a) Resistor Ladder

This ladder is a simple and fast way to store and read reference voltages. It consists of a string of resistors connected in series and successively drop the

reference voltage supplied (Vref = VrefN = Iref * (RN + ... + R2 + R1)) as illustrated in Fig. 4.6.

The stored reference voltages represent a predefined/pre-calibrated sampled voltage levels from the light transducer block upon exposure to various wavelength light and normalized with the incident power.

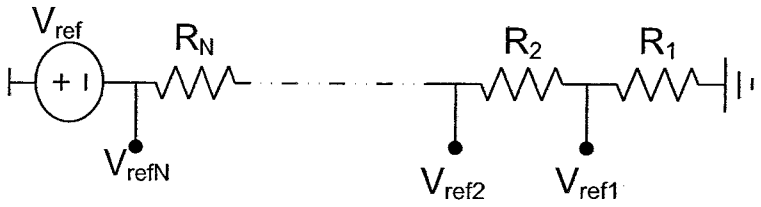


Figure 4.6: Resistor Ladder

b) Analog Multiplexer

Analog multiplexers (AMUXs), shown in Fig. 4.7, unlike digital multiplexers, transfer the analog voltage from input to output as controlled by the switching input ideally with no voltage drop. For the proposed circuit, two AMUXs were required for circuit proper function, thus at any time two consecutive reference voltages are selected and fed to the two comparators hence creating a closed interval for comparison with the photo-voltage.

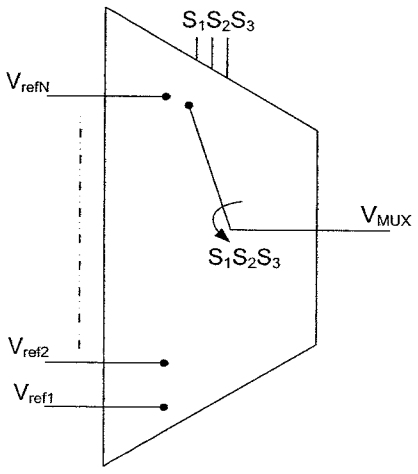


Figure 4.7: Analog Multiplexer

c) Analog Comparator

The comparators task is to compare the analog voltages issued from the light transducer block against the reference voltages selected from AMUX. Two comparators and two analog multiplexers are used to perform windowed comparison, as can be illustrated in Fig. 4.8, i.e. first comparator compares if the transducer response is lower than the upper reference value VMUX1 and the second comparator to compare if the transducer response is higher than the lower reference value VMUX2). When both comparators have a high digital output, it shows that the appropriate interval of reference voltage (color value) has been successfully found.

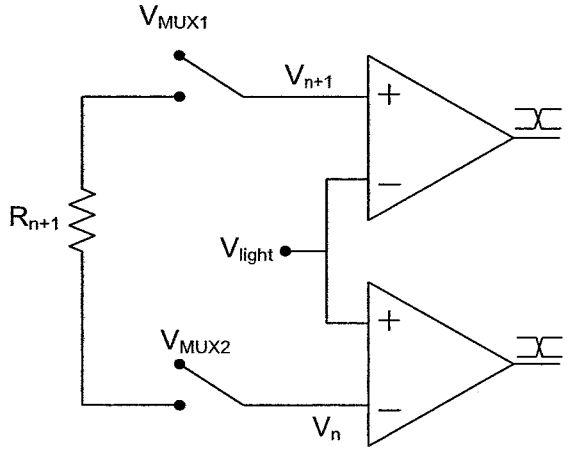


Figure 4.8: Windowed Comparison

d) Counter

The counter is a digital block serving two purposes: (i) To control the switching activity of the analog multiplexers (generates signals S1 S2 and S3 in Fig. 4.7); (ii) To serve as the final digital output when the right interval is found (which will be discussed shortly in the operation).

e) Decoder

The decoder is a fully digital block used as the final block of the interface circuit to decode the digital output to a 'one-active' bit at a time.

f) Timer (optional block)

The timer block is a mixed signal block that sets the duration of final output bits. The interface circuit prototype uses simple display units and in order to avoid continuous current draw from the output ports (which implies higher power dissipation), a timer block that controls the active bit duty cycle is proposed. This block is optional since it doesn't affect the basic functionality of the system rather the duty cycle for the displayed output bits.

4.3.1.1 Operating Principle

Having discussed the brief description of each constituting blocks in the proposed design, next we will discuss the operation.

The operating principle of the design is illustrated by Fig. 4.9. The analog multiplexers switch through the pre-calibrated reference voltages as controlled by the counter signal. Two multiplexers and two comparators are needed so that at any time two consecutive reference voltages are selected for windowed comparison. When the analog input from the light transducer block falls in the windowed interval, both comparators will go high simultaneously as can be seen in Fig. 4.9(b). At this point the signal from AND activates the D-flip flops to register counter state and then decoded to show in which interval/window the color response is found. The proposed interface circuit features a reasonable conversion speed with a significantly lower hardware overhead.

The main idea of the proposed sensor interface circuit is that it should transform a voltage input from sensing element to a digital form that is readily available for output interface (LED) without including Microcontroller or other components that increase complexity and hence cost and power consumption. For one-stage design the resolution of the output is directly linked to the number of reference storage resistors and the number of analog multiplexer inputs.

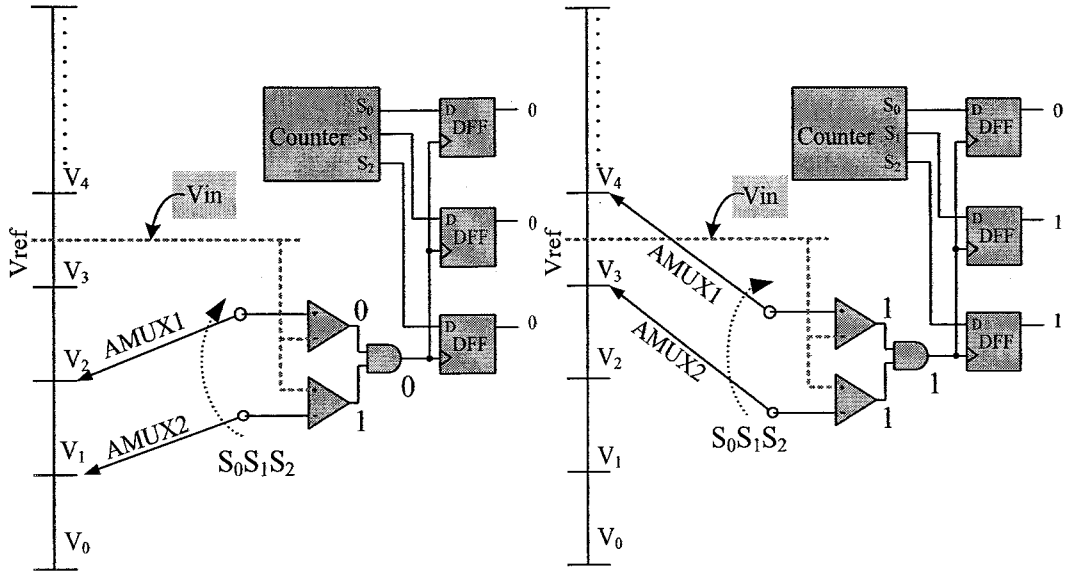


Figure 4.9: Conceptual diagram illustrating operation of the proposed ADC. (a)The AMUX's switch through the ladder voltage until both comparators fire, (b) both comparators fire indicating the right window interval is found.

4.3.1.2 Simulation Result

The proposed one-stage design, implemented for 2 bits (four color resolutions), is simulated first in PSpice for preliminary validation. The simulation result is as shown in Fig 4.9 (a) through (c). Since the reference voltages are a pre-stored representation of the transducer response, the output digital bits are referred as the respective color (refer OPT301 response curve in Fig. 4.4 and legend in Table 4.1).

Table 4.1. Reference windowed Voltage intervals used and their corresponding legend for colour outputs.

	C0	C1	C2	C3	Voltage intervals (in V)
Violet	0	1	1	1	(0.00-0.15]
Blue	1	0	1	1	(0.15-0.25]
Green	1	1	0	1	(0.25-0.40]
Red	1	1	1	0	(0.40-0.50]

Fig 4.10(c) represents the stair case signal as generated by the two multiplexers as they flip through the ladder reference voltages while forming a closed interval for comparison. Whereas (b) shows the two comparators output (Comp1 & Comp2). Comp1 gives a high output when Mux1 has a higher value than the transducer output. While comparator two (Comp2) gives high output when Mux2 has a value lesser than the transducer. As a result the two comparators will have both a high output simultaneously when the photovoltage is in between an interval of any two consecutive reference voltages (in the windowed interval). The final indicator outputs are designated as C0, C1, C2, and C3. Whenever both comparators have a high output the 'right' color is obtained and will be displayed at the indicator LED outputs which are shown as digital active-low values. As can be shown circled in the figure, C3 is 0 while the others are 1 indicating Red color is detected or in another words the supplied photovoltage value falls in the red color interval (0.4 V – 0.5 V).

The photovoltage input to the comparators is changed continuously to simulate real life color changes or instance continuous color changes in a pH solution or fluorescence emission phenomenon. As it can be seen from this simulation result the optical detector circuit is autonomous i.e. it can track the color change without any need of interference from a user.

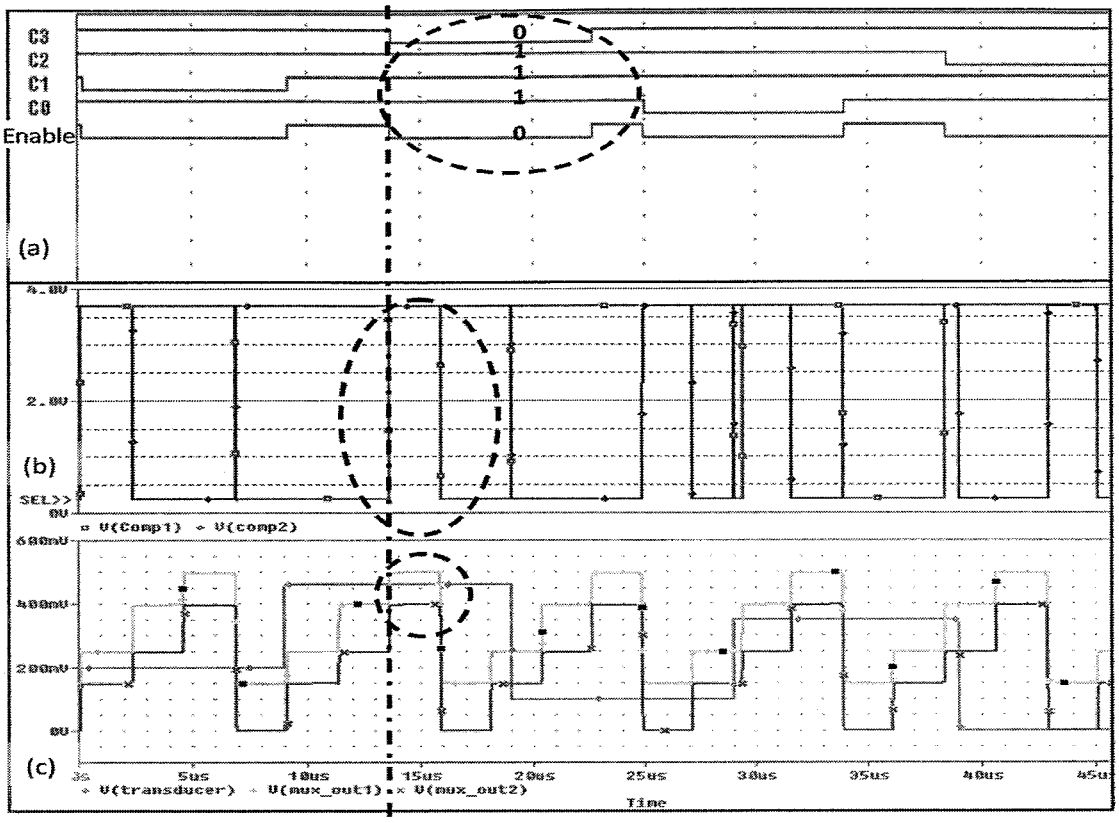


Figure 4.10: PSPICE simulation result (a) final digital outputs (C0, C1, C2, C3 outputs); (b) Comp1 and Comp2 outputs; (c) Photovoltage, AMux1 and AMux2 outputs (staircase like signal)

4.3.1.3 Experimental Results

The one-stage interface circuit design is further validated experimentally using discrete components to assert the simulation results. The same components used in the simulation were bought from the respective supplier and used in the discrete experimental testing. Instruments used in the setup are Instek voltage source, Tektronics frequency generator to generate the clock signal and Tektronics Digital phosphor oscilloscope to display the output signals. The discrete components used are listed in Table 4.2 and the experimental setup using breadboard is shown in Fig. 4.11.

Table 4.2: Discrete off-the shelf components used in experimental validation.

Part Number	Discrete off-the-shelf components	Producer
ADG409	Analog Multiplexer	Analog Devices
LT1016	Ultrafast Analog Comparator	Linear Technology
74161	4 bit Counter	Texas Instrument
74175	D-Flip-flop	Texas Instrument
74139	Decoder	Texas Instrument
74121	Timer (optional block)	Texas Instrument
7408	And gate	Texas Instrument

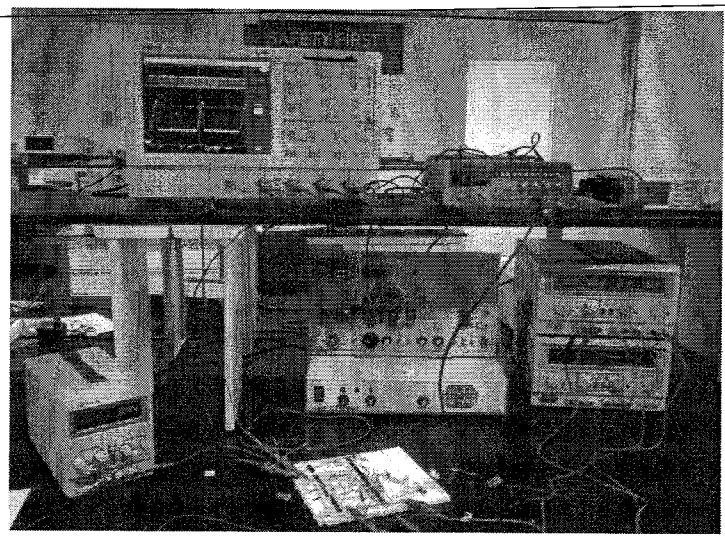
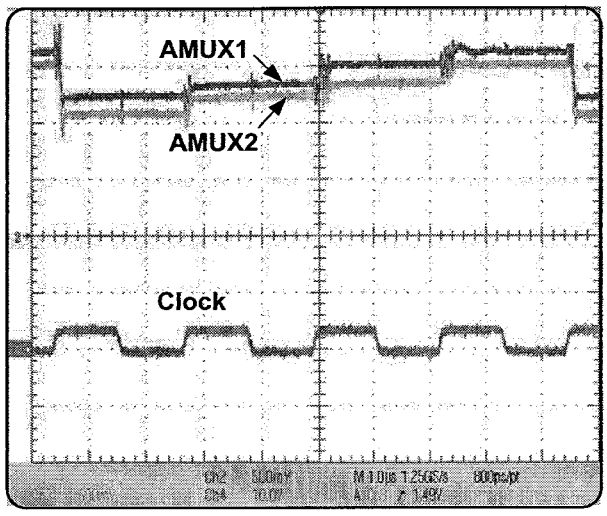


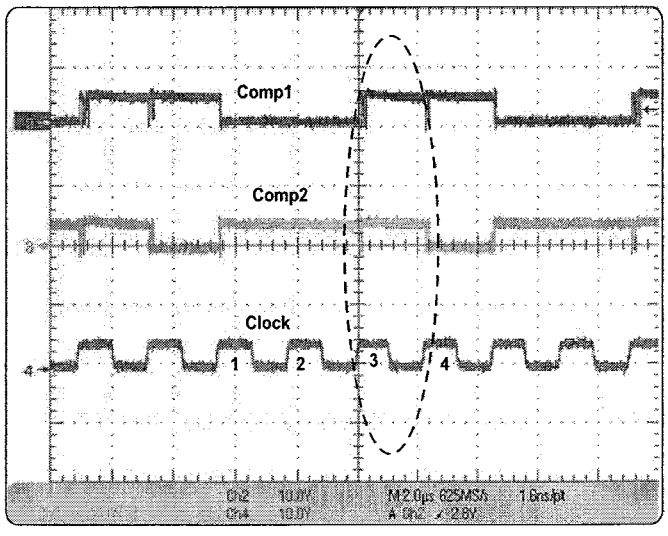
Figure 4.11: Experimental setup using discrete implementation of One-Stage Design

In the experiment, a sampled differential photovoltage is applied at the comparator and the corresponding digital output s observed. Fig. 4.12 (a) through (c) shows the result graphs generated from the experimental testing. Fig. 4.12(a) shows the analog multiplexers (AMUX1 & AMUX2) while they switch through the reference voltages at different clock cycles as controlled by the counter. The two comparator outputs for a selected photovoltage inputs is shown in Fig. 4.12(b). For instance, a photovoltage of Vph = 0.32 V that represents a Green colored incident

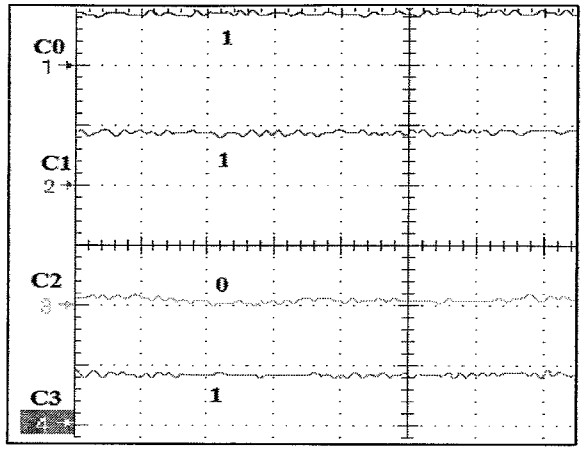
light (refer to Fig. 4.4); as a result Comp1 and Comp2 are high simultaneously only on the third clock cycle (shown circled in the Fig. 4.12(b)) and the corresponding digital output indicated C2 is detected successfully showing the correct color.



(a) Clock input and AMux1 & AMux2 voltages outputs as they switch through the reference voltages.



(b) Comparator1 and Comparator2 output for a selected photovoltage input (at V_{ph}=0.32V)



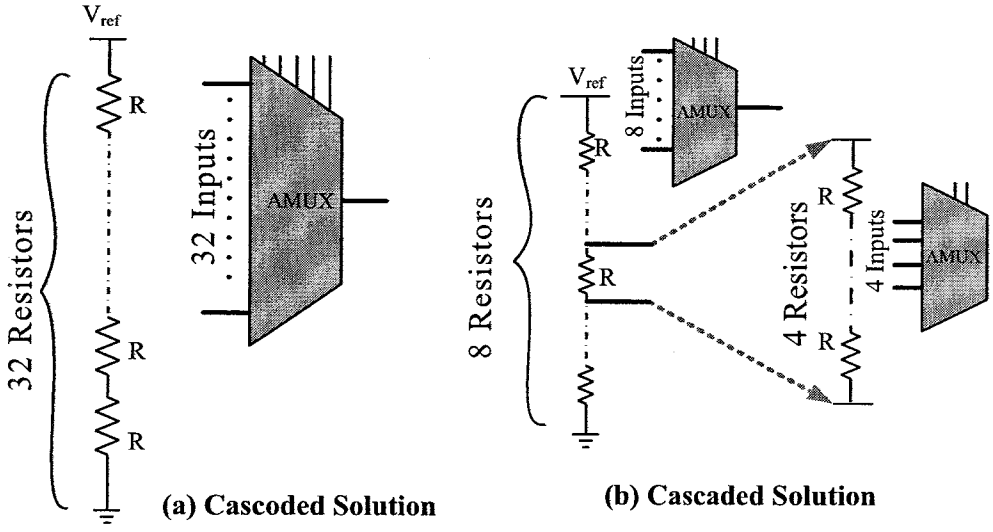
(c) Final color output: C0, C1, C2, C3

Figure 4.12: Experimental validation for one-stage interface circuit design

4.3.2 Two-Stage Design

In an effort to increase the resolution (number of colors detected) of the one-stage interface circuit, with minimum tradeoff to speed and power consumption, we have proposed a new design that is based on two cascaded stage.

The number of detected level can be increased to higher level for example 32-level by either increasing the number of resistors in one stage (i.e. cascoding resistors) or by having a pipelined or cascading 2 one stage design with 8 levels resolution on the first (coarse stage) and 4 levels on the second (fine stage) as shown in Fig. 4.13. However, cascoded solution requires more resistors (32) as opposed to 12 for cascaded solution. Obviously having more resistors occupies more area (especially in IC implementation). Furthermore, cascoded solution requires 32 clock cycles (at most) for a complete detection of one color, while cascaded solution takes at most 12 clock cycles. As a result, area for an on-chip integration, power consumption and speed are optimized by the cascading implementation (Fig. 4.13(b)) than in cascoded implementation (Fig. 4.13(a)).



• Resolution = 32	• Resolution = 32
• Number of resistors = 32	• Number of resistors = 12
• Speed = at most 32 clock cycles for a single detection	• Speed = at most 12 clock cycles for a single detection

Figure 4.13: Techniques of increasing resolution by (a) increasing number of resistors in one stage (cascoding) or (b) 2-one stage (cascading).

4.3.2.1 Operating Principle

Fig. 4.14 shows the block diagram of the proposed two-stage interface circuit. In this design the reading of the photovoltage and producing a corresponding digital output representing the color detected is done in two-stages: during the first stage a comparison is made to find the most significant bits (MSB) of the digital output and this interval is further subdivided in the second stage to produce the list significant bits (LSB) of the digital output. The final digital word is a combination of the MSB and LSB from both stages. The first and second stages are also referred as Coarse and Fine stage respectively accounting to their configuration. Basically the same circuit blocks are used as the one-stage design except for an additional voltage buffer that connects the first stage to the second which are resistor ladder that stores reference voltage levels; two analog multiplexers (AMUX) to switch through the reference levels based on their control signals; two comparators to decide the right windowed

interval in each stage; a counter to generate control signal for the AMUXs and few registers as storage elements.

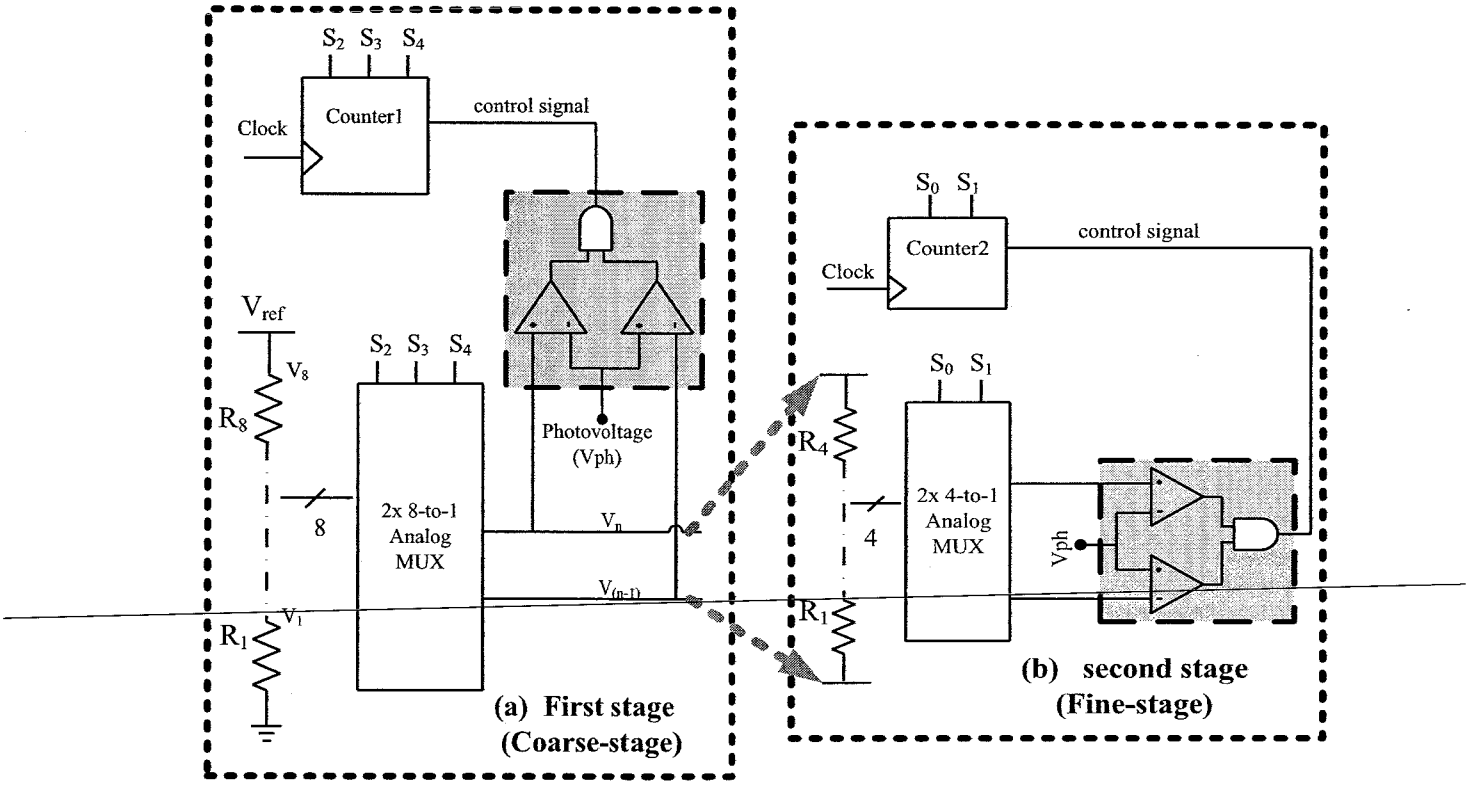


Figure 4.14: Two-stage interface circuit design (a) first (coarse) stage; (b) second (fine) stage.

The proposed two-staged interface circuit architecture is implemented for 5 bit (32 levels) of resolution) and the detailed operation is as follows. The photovoltage input is compared against the reference ladder in the first stage until the right coarse windowed interval is found. When the right interval is found in the coarse stage, its operation is halted and the state of the counter (3 bit digital value) is saved on registers (D flip-flops) for later use. Then the corresponding interval is used to generate a reference voltage for the resistor ladder in the second stage and hence further subdivided into 4 sub-levels. The same photovoltage is again compared in the second stage to find a finer (higher resolution) output. Again when the right interval is found in the second stage, its counter state (2 bit digital value) is saved on a register and combined with the 3 bit value from the coarse stage to form the final 5 bit digital word. When reading process is completed, the digital output that represents the detected color information is displayed in a display unit e.g. LED to a user.

4.3.2.2 Simulation Result

The two-stage design is validated by simulation using PSPICE/Orcad software. The design is implemented for a 32 level resolution over a differential input of 4 V. Table 4.3 is the look-up table for the reference voltages and the corresponding color representation. The result from PSPICE is shown in Fig. 4.15. The staircase like signal is the signal from the analog multiplexers as they switch through the reference levels and the corresponding 5 bit output digital values.

Table 4.3: Reference windowed voltage intervals used during simulation and experiment. Each level in the coarse-stage is further subdivided in to 4 equivalent levels in the fine-stage as shown

Stage 1 (coarse-stage)

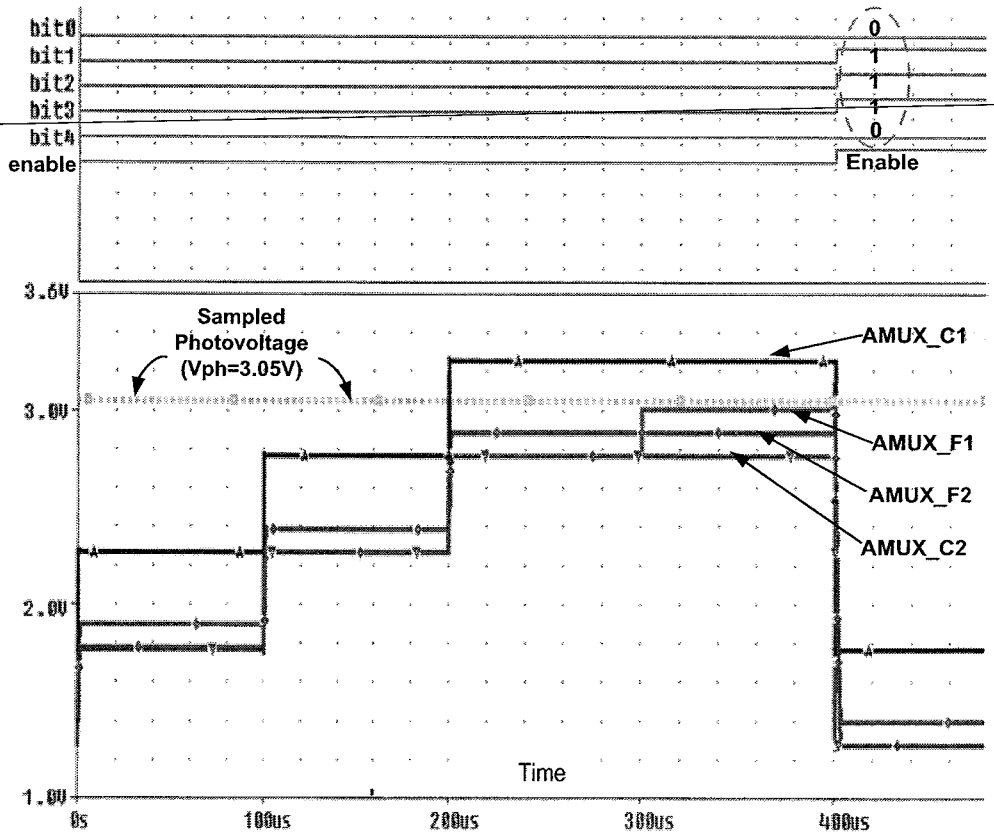
Color	MSB	Voltage(V)
C0	000	1.25-1.75
C1	001	1.75-2.25
C2	010	2.25-2.75
C3	011	2.75-3.25
C4	100	3.25-3.75
C5	101	3.75-4.25
C6	110	4.25-4.75
C7	111	4.75-5.25

Stage 2 (fine-stage)

Wavelength	LSB	Voltage(V)
C30	00	2.750-2.875
C31	01	2.875-3.000
C32	10	3.000-3.125
C33	11	3.125-3.250

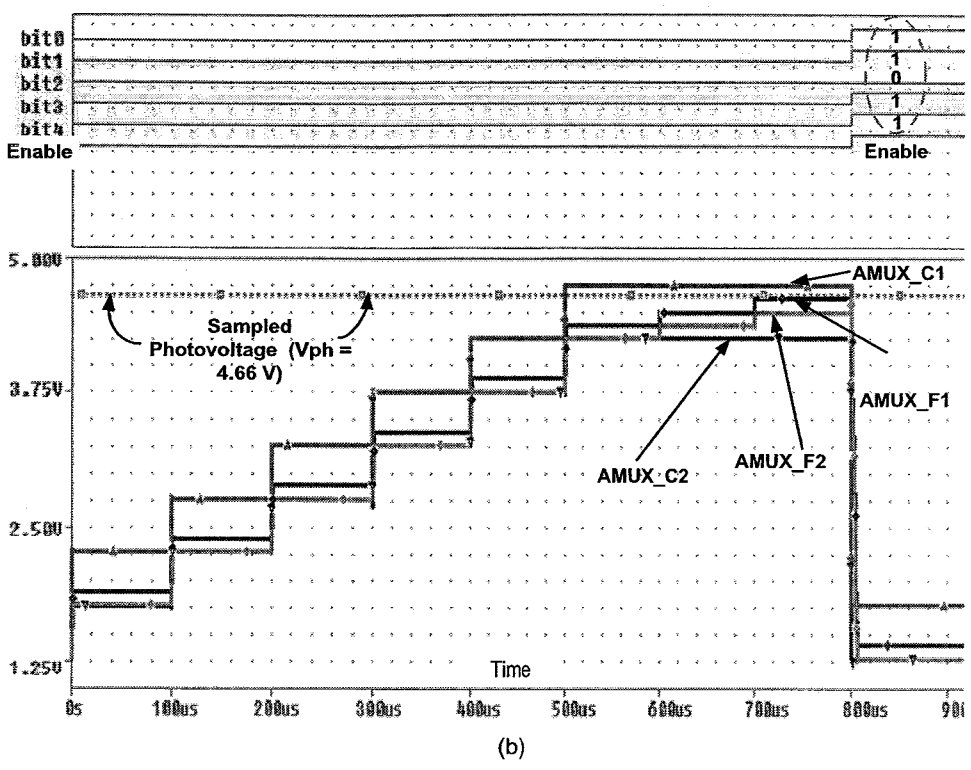
As discussed in the previous section each stage has two multiplexers: AMUX_C1 & AMUX_C2 in the coarse (first) stage and AMUX-F1 &AMUX-F2 in the fine (second) stage. During the first stage, the two multiplexers switch through reference voltages until the photovoltage voltage falls in a particular windowed interval, which is confirmed by the simultaneous high output from both comparators in the same stage. When the interval is found, the upper and lower voltage references are

transferred to the fine stage via a voltage buffer for further subdivision in the second stage. The same process is repeated in the second stage until the right fine interval is found. Finally, the MSB bits which are 'bit4', 'bit3' & 'bit2' and the LSB bits which are 'bit1' & 'bit0' are generated as the final digital output as shown in Fig. 4.15 (a) and (b). As can be seen in the figures, the first sampled photovoltage has a value of 3.05V and this is found in the fourth interval of the first stage giving an MSB of 011 and when first stage operation is completed the second stage is activates giving the LSB bits of 10. Combining the MSB and LSB bits gives 01110 as can be seen circled in Fig. 4.15 (a). Another example for a sampled photovoltage input of Vph = 4.66 V is shown in Fig. 4.15 (b).



(a)

(a)AMUX_C1 & AMUX_C2 (analog multiplexer 1 & 2 from coarse stage, and AMUX_F1&AMUX_F2 (analog multiplexer 1 & 2 from fine stage) for an input photovoltage Vph = 3.05 V.



(b) AMUX_C1 & AMUX_C2 (analog multiplexer 1 & 2 from coarse stage, and AMUX_F1&AMUX_F2 (analog multiplexer 1 & 2 from fine stage) for an input photovoltage Vph = 4.66 V.

Figure 4.15: PSPICE Simulation result for the proposed two-stage interface circuit.

4.3.2.3 Experimental Result

The proposed two-stage interface is further validated by experimental work in the laboratory using discrete off-the-shelf components. The main components used are basically the same as the one stage design: analog multiplexers (ADG408 & ADG409), LT1016 precision comparators, 74161 counters to generate the select signals for the multiplexers, and 74121 monostable one shot timer, LM324 operational amplifier as analog buffer. The experimental setup is as shown in Fig. 4.16.

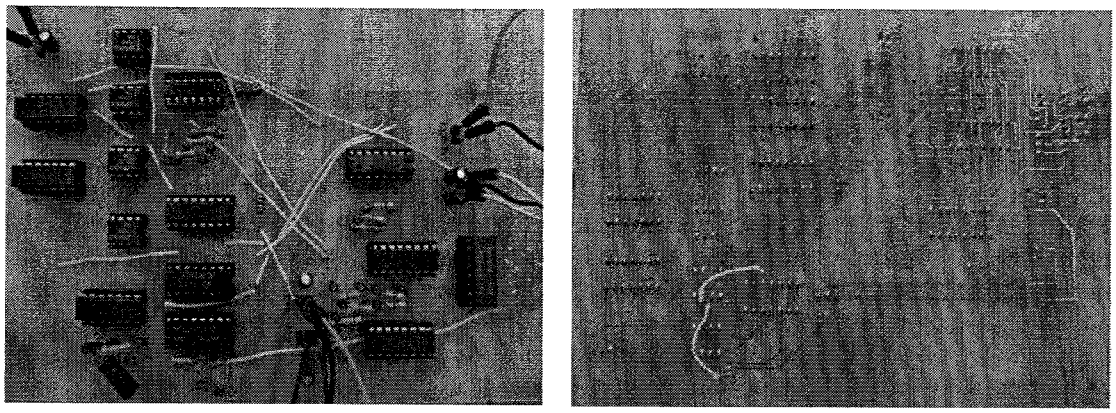
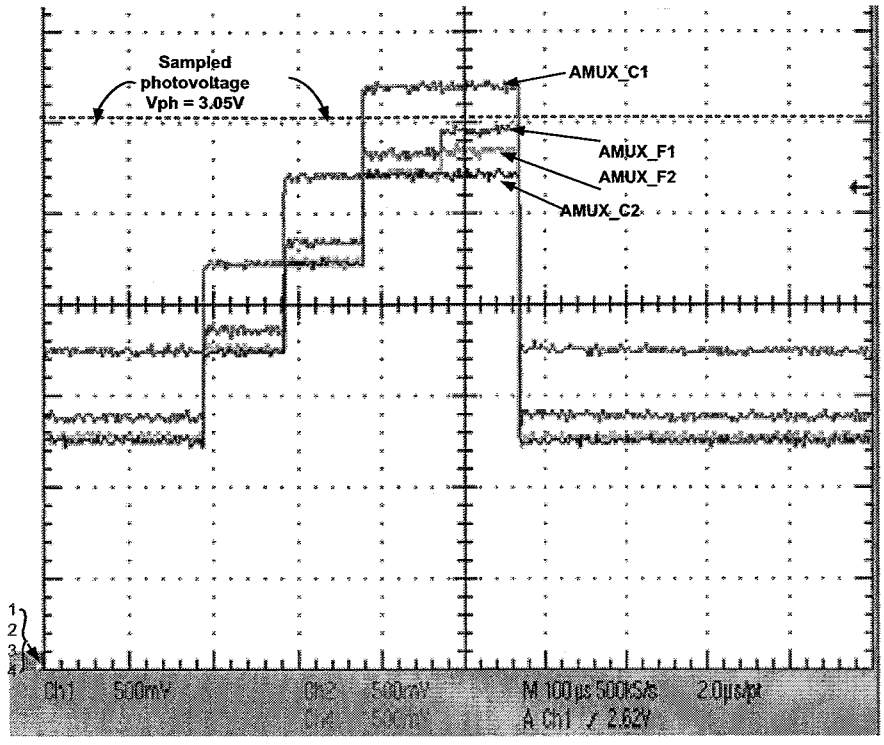


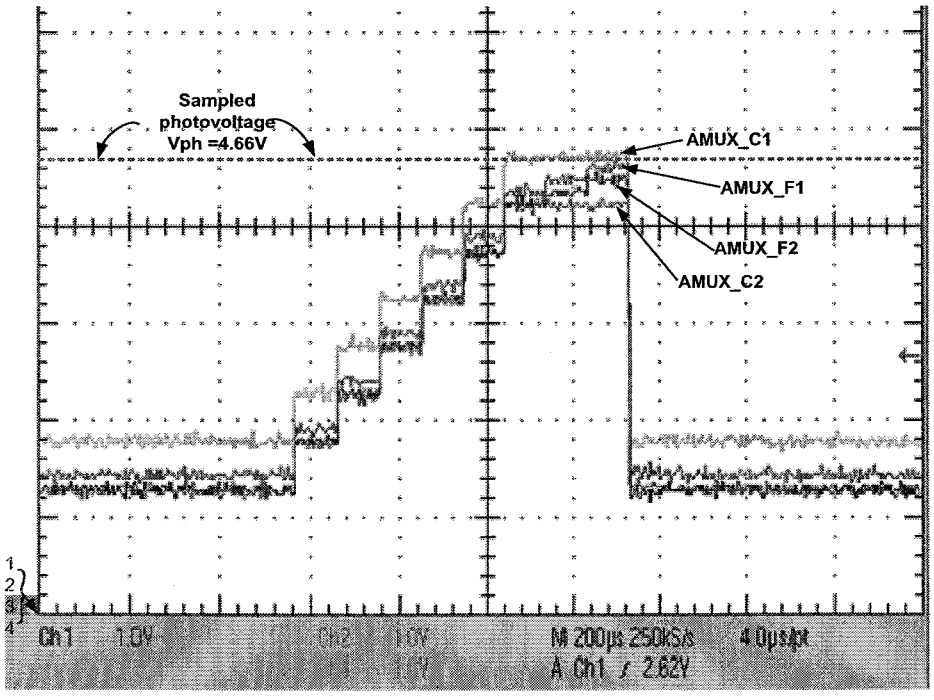
Figure 4.16: PCB Experimental setup of the interface circuit in the lab tested using off-the-shelf discrete components.

The look up table for the reference voltage levels and their color counterparts is as specified in Table 4.3. The screen capture from the TDS oscilloscope is as shown in Fig. 4.17 (a) through (d). The figures illustrate the analogue multiplexers and the resulting final digital output. For a sampled photovoltage of 3.05, as it is shown in Fig 4.17 (a), the coarse stage multiplexers (AMUX_C1 and AMUX_C2) switch until the sampled voltage falls in a particular interval which is fourth interval window (C3=011). When the first stage is completed the second stage is activated as shown (AMUX_F1 and AMUX_F2). The sampled value falls in the third interval (C32=10). The combination of the two digital outputs gives the final value of 01110 as shown circled in Fig. 4.17(c). The output is kept for some time by the one-shot timer for a user to properly discern the values. Fig. 4.16 (b) shows additional graphs of the multiplexer signals for a sampled photovoltage value of V=4.66. This voltage falls in the seventh interval at the coarse stage (C6=110) and in the fourth interval at the fine stage (C63=11) which gives a combined digital output of 11011 as shown circled in Fig. 4.17 (d).

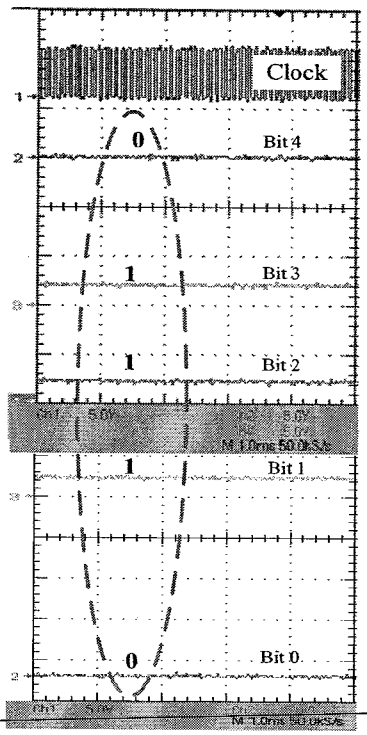
This concludes a single processing cycle by the interface circuit block. New sampling of voltage from the interface block is done at the start of each processing cycle. As shown from the result graphs, the experimental simulation agrees with the theoretical expectation as well as the simulation result from PSCPICE.



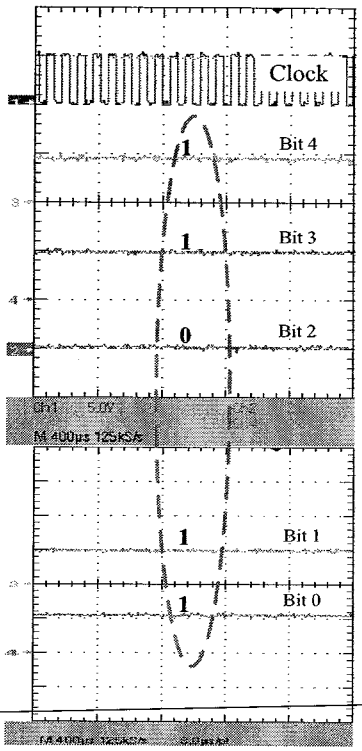
(a) AMUX_C1, AMUX_C2, AMUX_F1, AMUX_F2 graphs for Vph = 3.05 V.



(b) AMUX_C1, AMUX_C2, AMUX_F1, AMUX_F2 graphs for Vph = 4.66.



(c) 5bit digital output for Vph=3.66 V



(d) 5bit digital output for Vph=4.66 V

Figure 4.17: Experimental validation result of the proposed two-stage interface circuit using discrete components.

4.4 Summary

In this chapter, the proposed interface circuit is introduced. We have shown how the interface circuit is distinctive from conventional interface circuits as well as from a typical flash ADC. Moreover the working principles of two related designs: one-stage and two-stage interface circuit are discussed. Finally, we have presented the PSpice simulating result and experimental test data from PCS implementation to validate the proposed design.

CHAPTER 5

TOWARDS ULTRA-LOW POWER INTEGRATED CIRCUIT DESIGN

The fabrication of millions of transistors into a single chip was a fundamental stimulus in electronics, leading to the VLSI (Very Large Scale Integration) circuit concept [67]. The main drive for integrating a system is due to lower power consumption, Advancement in deep submicron technology and the market drive has resulted in the ability and the need to put entire systems on a single chip. As more and more integration is done on a single chip, it is increasingly likely that the chip will contain both analog and digital sections. Developing these mixed-signal (MS) systems-on-chip presents enormous challenges both to the designers of the chips and to the developers of the computer-aided design (CAD) systems that are used during the design process [68].

The main goal of this thesis is to fabricate a proof of concept integrated interface circuit prototype and validation via experimental testing. The design is a promising step towards an integrated single chip, portable, low power sensor microsystem and system-on-chip design for environmental monitoring applications. As discussed in the previous chapter, the proposed interface circuit is simulated in PSpice and validated with discrete components as a proof of concept. Finally, a functionally equivalent integrated circuit (IC) is designed and simulated in Cadence design system software using standard CMOS 0.35 μm Austria Microsystems technology (n-well technology). In this chapter the integrated interface circuit simulation and experimental results from fabricated prototype is presented.

5.1 Integrated Interface Circuit Design in Cadence – One-Stage

The proposed interface circuit architecture shown in Fig. 5.1 is essentially the same one-stage architecture discussed in the previous section with functionally equivalent blocks designed in 0.35 μm CMOS technology. However, it has significantly lower power consumption attributed to design optimization, integration and CMOS technology scaling.

As discussed in the methodology chapter, the bottom-up design approach is used. Accordingly, each constituent blocks of the interface circuit are designed and verified individually and then later assembled to make up the final circuit. The constituent blocks are assembled partly from the standard library provided by Austria Microsystems technology and partly built from scratch (from transistor level).

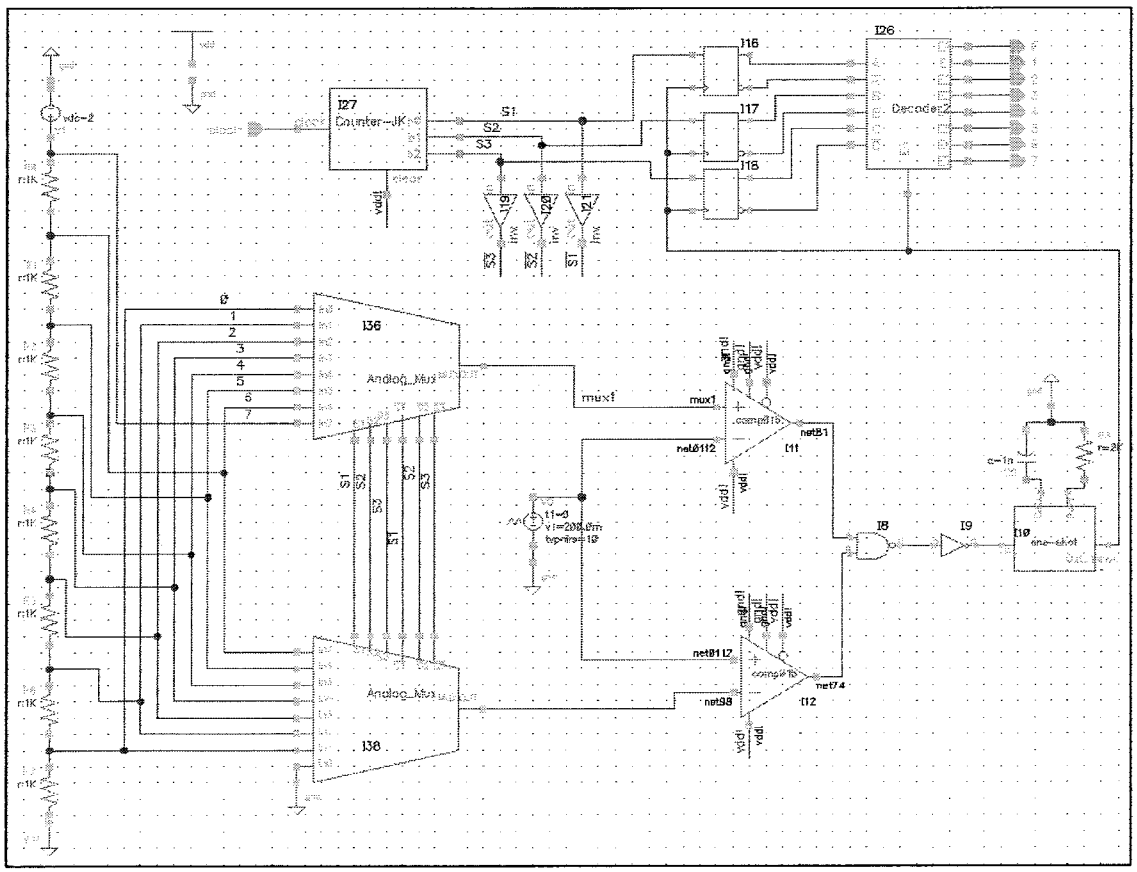


Figure 5.1: Proposed integrated interface circuit

The schematic and layout design of some of the blocks are discussed below. The building blocks of the design are resistor ladder, analog multiplexer, comparators, decoder, counter and an optional timer. It accepts analog photovoltage from the optical transducer and produces digital output that represent the incident light (i.e. λ) color with the help of pre-calibrated storage elements.

a) Analog Multiplexer

The CMOS analog Multiplexer is designed from scratch by using transmission gates. A transmission gate (TG) also known as analog switch is a bidirectional transmission element made by parallel combination of NMOS and PMOS transistors whose gates are controlled by complementary clock pulse. Transmission gates are widely used for analog multiplexing since they transfer analog voltage with minimal distortion or voltage drop and they have low complexity in terms of transistor count [69-71]. Fig. 5.2 shows the schematic design of the analog multiplexer from transmission gates and Fig 5.3 shows the corresponding layout design. From the post layout analysis, the power consumption of this block is 37pA and the maximum voltage drop found 27 nV which indicates good performance for the application at hand.

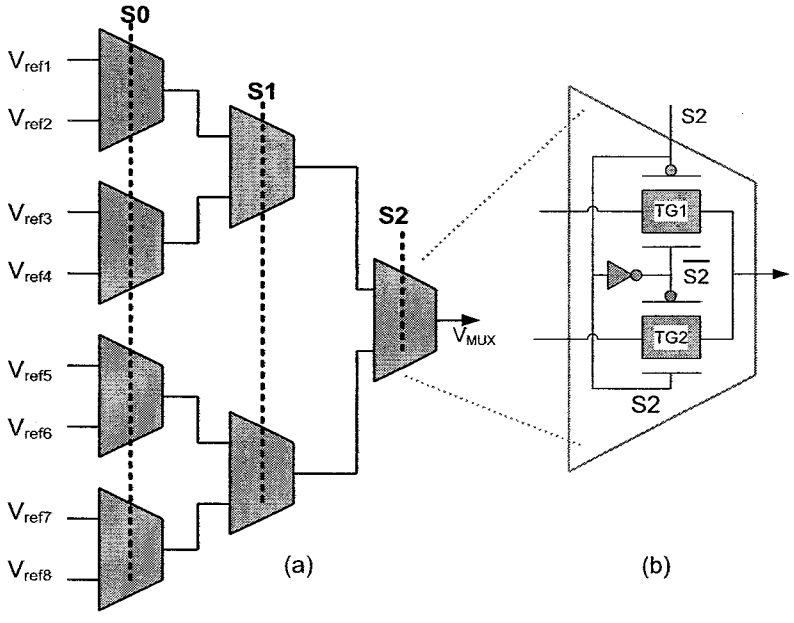


Figure 5.2: Analogue multiplexer (AMUX) (a) 8-to-1 AMUX; (b) Two transmission gates (TG1 & TG2) making up 2-to-1 AMUX.

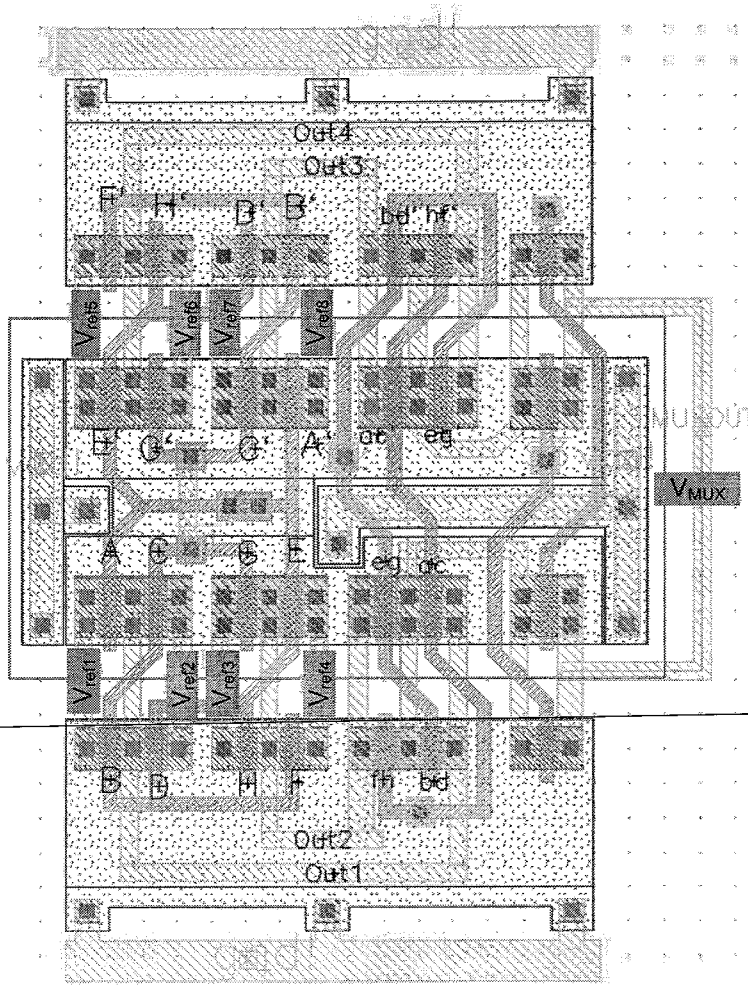
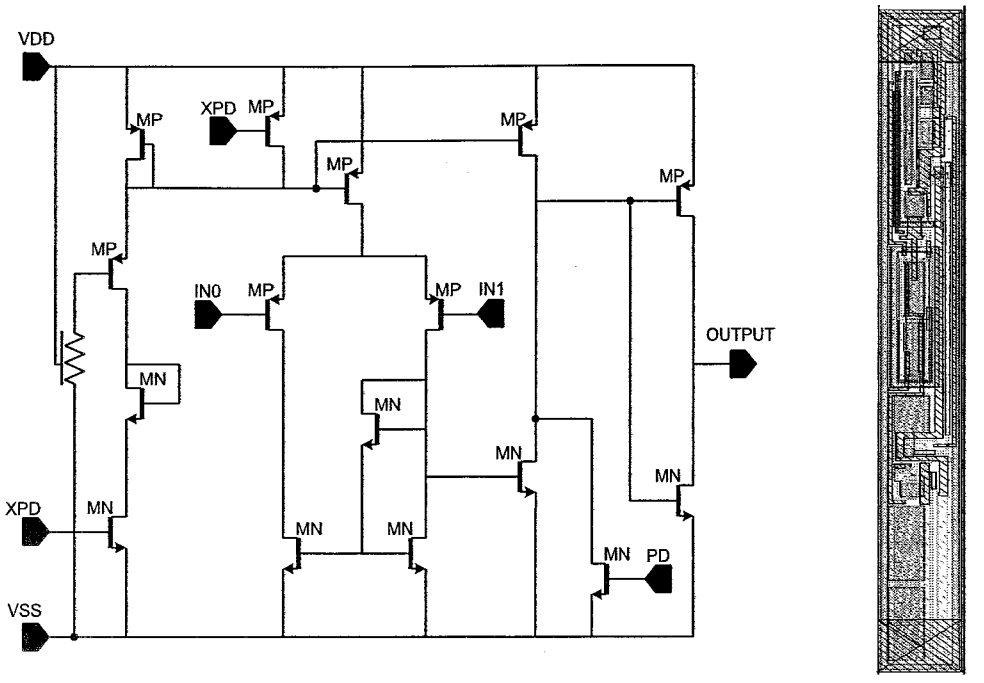


Figure 5.3: Analog Multiplexer Layout (14 NMOS and 14 PMOS transistors

b) Analog Comparator

The CMOS comparator, schematic and layout shown in Fig 5.4, is directly adopted from the AMS library. The CMOS comparator used draws a very low current and has no hysteresis.



(a) schematic (b) Layout

Figure 5.4: CMOS comparator

c) Counter

3-bit and 2-bit synchronous counters are designed to can be used in one-stage and 2-stage design. Fig. 5.5 shows a schematic diagram of 3-bit counter. The layout of this counter is assembled from JK flip-flops available in the standard AMS library.

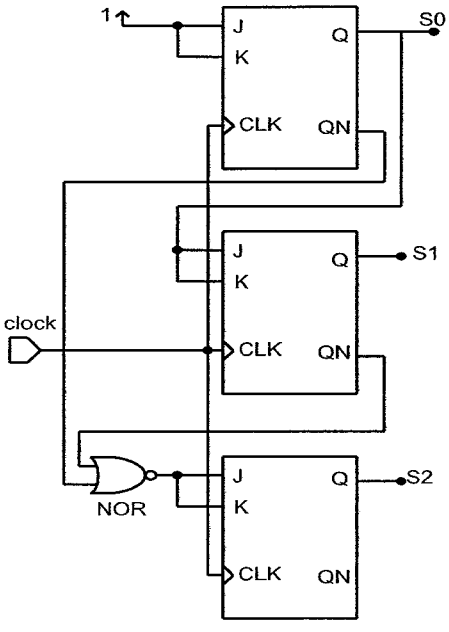


Figure 5.5: Counter Schematic

d) Decoder

The decoder block is designed using available NAND and NOR gates in the library. This block helps to have one active bit at a time to make it suitable for an LED based display. This block, shown in Fig. 5.6 is implemented or 3-to-8 decoding for one-stage implementation.

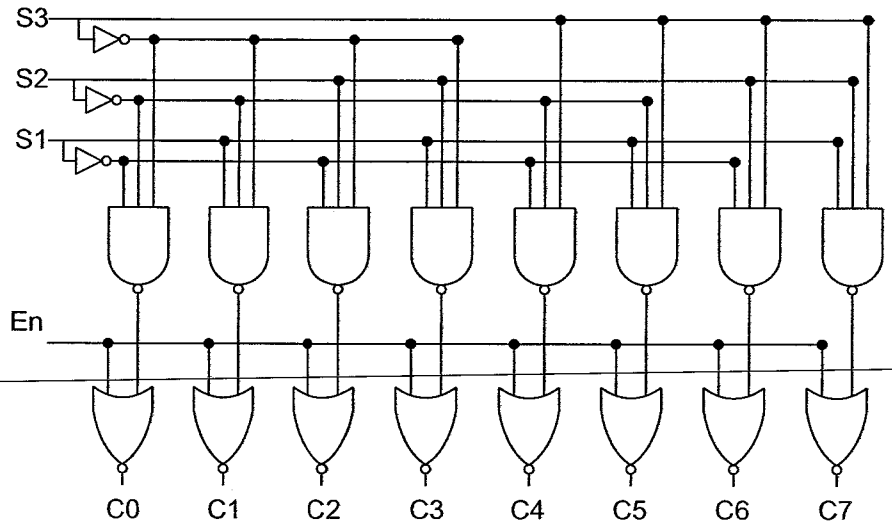


Figure 5.6: 3-to-8 decoder schematic

e) Timer block (optional block)

The timer block sets the duration of final active output by acting as 'Enable (En)' signal to the decoder. The interface circuit prototype uses simple display units (LED) and in order to avoid continuous current draw from the output ports (which implies higher power dissipation), a timer block that controls the active bit duty cycle, shown in Fig. 5.7, is proposed. This block is optional since it doesn't affect the basic functionality of the system rather the duration for the displayed output bits.

The operation of the proposed timer is as follows. Initially Q value or the output is assumed to be low implying PMOS transistor is turned ON resulting in the capacitor C_{ext} to be tied to vdd (supply voltage) and hence fully charged. When a rising edge at the clock input is encountered, Q goes high, NMOS transistor turns ON and PMOS transistor turns OFF. This will discharge the capacitor through the resistor R_{ext} until it reaches the lower switching level of the inverting Schmitt trigger [72] which then

clears the Q signal. Meanwhile the output signal (i.e. Q signal) is high for a period of time τ defined by the discharging process of the capacitor through the resistor and other incoming signals through the enable will be neglected.

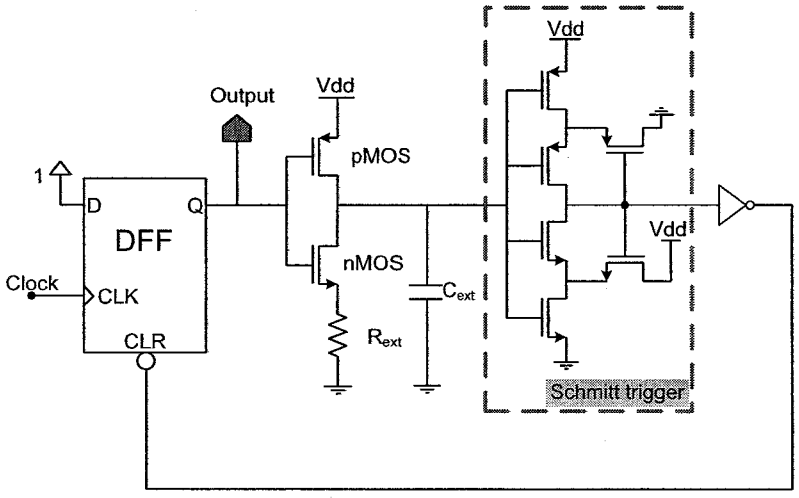


Figure 5.7: Proposed timer circuit schematic

τ is programmable solely via the externally attached R_{ext} and C_{ext}. Whenever a triggering signal through the clock appears, the one-shot holds the signal for time τ. The mathematical expression for the time constant is formulated and can be expressed by 2.1, where K is a constant varying from 0.7 to 1.2 depending on the initial charge of the capacitance. r_{ON} represents the NMOS transistor average 'ON' resistance.

$$\tau = k * C_{ext} * (R_{ext} + r_{ON}) \quad (2.1)$$

The proposed one shot timer is simulated with values for R_{ext} and C_{ext} set to 30 kΩ and 1 nF respectively. The time constant is expected to be between 26 μs and 37 μs by calculation. The above calculation is confirmed from the simulation result as can be seen in Fig. 5.8.

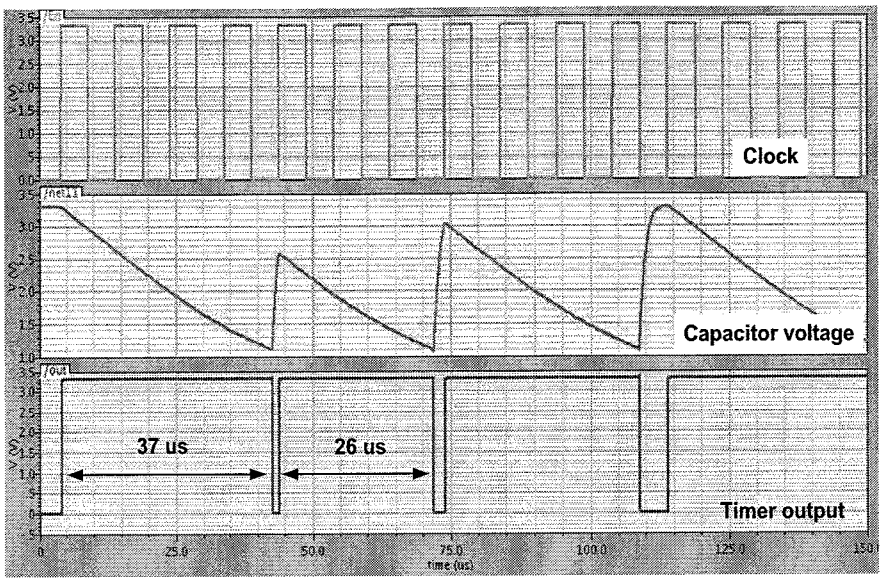


Figure 5.8: Simulation result of the proposed timer design.

5.1.1 Completed Chip Tape-Out

The proposed interface circuit is designed to be fabricated on a single chip using the 0.35 μm Austriamicrosystems CMOS technology. The chip also contains photodiode for a future characterization and an internal clock generator circuit (oscillator) for on-chip clock generation. The designed tape-out is shown in Fig. 5.9. It has a total area of 1900 μm by 1500 μm (2.85 mm^2) with the interface circuit core taking up 0.08 mm^2. The total power consumption of the proposed interface circuit is 37 μW at 1MHz. Having both analog and digital blocks the power consumption is mainly due to the static power in the analog blocks used which are comparators, analog multiplexers and the resistor ladder. Table 5.1 summarizes the specification of the designed chip.

Table 5.1: Summary of designed integrated interface circuit

Technology	0.35 μm CMOS
Voltage supply	3.3 V
Power consumption	37 μW
Full scale voltage	2 V
Interface circuit area	0.08 mm^2

Number of detected colors	8
Time required for color identification (max.)	8 μs

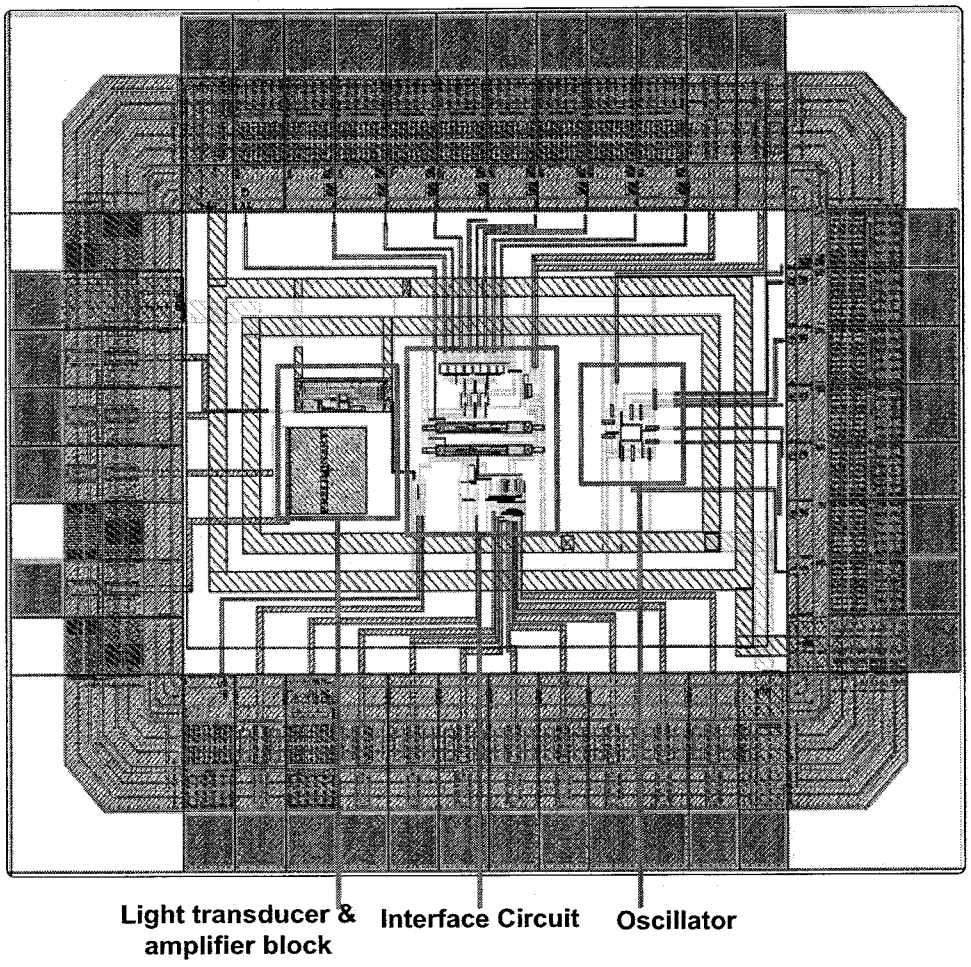


Figure 5.9: The completed tape-out of the chip

5.1.2 Simulation Result

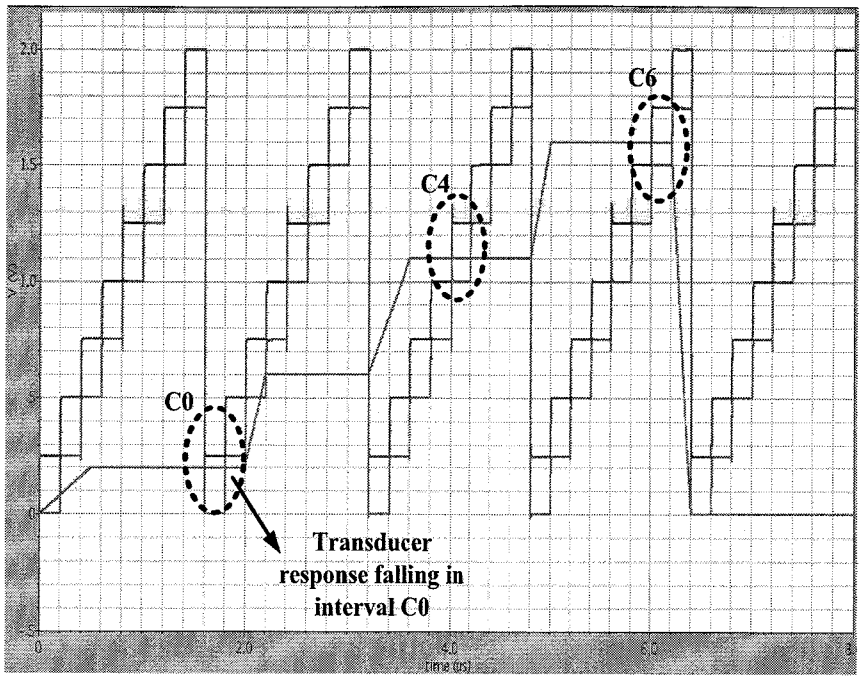
The proposed interface circuit from Fig. 5.1 is validated by simulation using Cadence Design System software and the result is shown in Fig. 5.10. The multi-bit digital output represents color of the detected light and which is obtained by comparing the light transducer voltage against pre-stored reference levels. The simulation is done over a differential voltage of 2.0 V and windowed voltage reference interval legend is given in Table 5.2.

Table 5.2: Reference level interval created for result interpretation

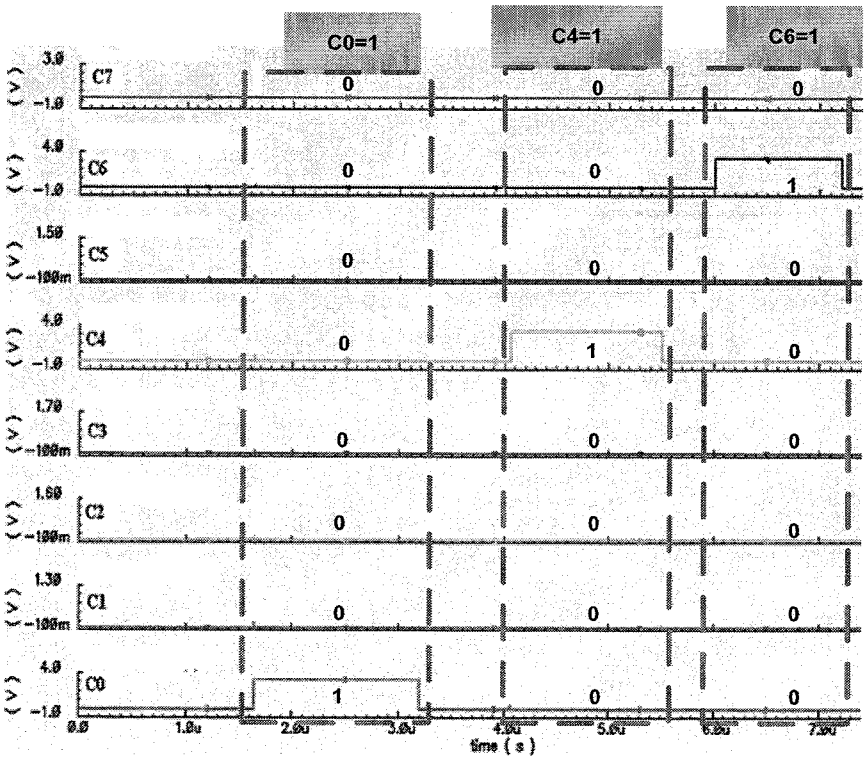
Color	C0	C1	C2	C3	C4	C5	C6	C7	Voltage intervals (V)
Violet	1	0	0	0	0	0	0	0	0.0-0.25
Blue	0	1	0	0	0	0	0	0	0.25-0.5
cyan	0	0	1	0	0	0	0	0	0.5-0.75
Green	0	0	0	1	0	0	0	0	0.75-1.0
Yellow-green	0	0	0	0	1	0	0	0	1.0-1.25
Yellow	0	0	0	0	0	1	0	0	1.25-1.5
orange	0	0	0	0	0	0	1	0	1.5-1.75
Red	0	0	0	0	0	0	0	1	1.75-2.0

Fig. 5.10 (a) illustrates the staircase like signals produced by the AMUXs and the piecewise sampled photovoltage (i.e. green). The digital outputs are designated as C0, C1, C2, up to C7 representing 8 different colors. For instance, the circled regions in Fig. 5.10 (a) represent the photovoltage falling inside the interval created by the two AMUXs. And Fig. 5.10 (b) shows the corresponding color representing bit having a high ("1") digital output while the rest have a low ("0") output. As such, when the input voltage from the transducer falls in the first interval, C0 (Violet) indicator goes high while the rest of the bits (C1 to C7) are low as shown. Similarly, it is shown when Yellow-green and Orange colors (C4, and C6 respectively) being detected at different times.

The transducer value is changed continuously to simulate real life color changes e.g. continuous color changes in a pH solution or fluorescence emission phenomenon. The simulation result shows the optical detector circuit is autonomous i.e. it can track the color change without any need of interference from a user.



(a) Signal at AMUX1, AMUX2 and photovoltage from Cadence simulation.



(b) Final digital output representing 8 colors (3-bit). Circled regions represent detection of C0, C4 and C6 colors.

Figure 5.10: Simulation result of one-stage integrated interface circuit design

5.1.3 Experimental Result

The proposed interface circuit is fabricated in a CMOS standard process using the 0.35 μm Austria Microsystems technology. Micrograph of the fabricated chip is shown in Fig. 5.11.

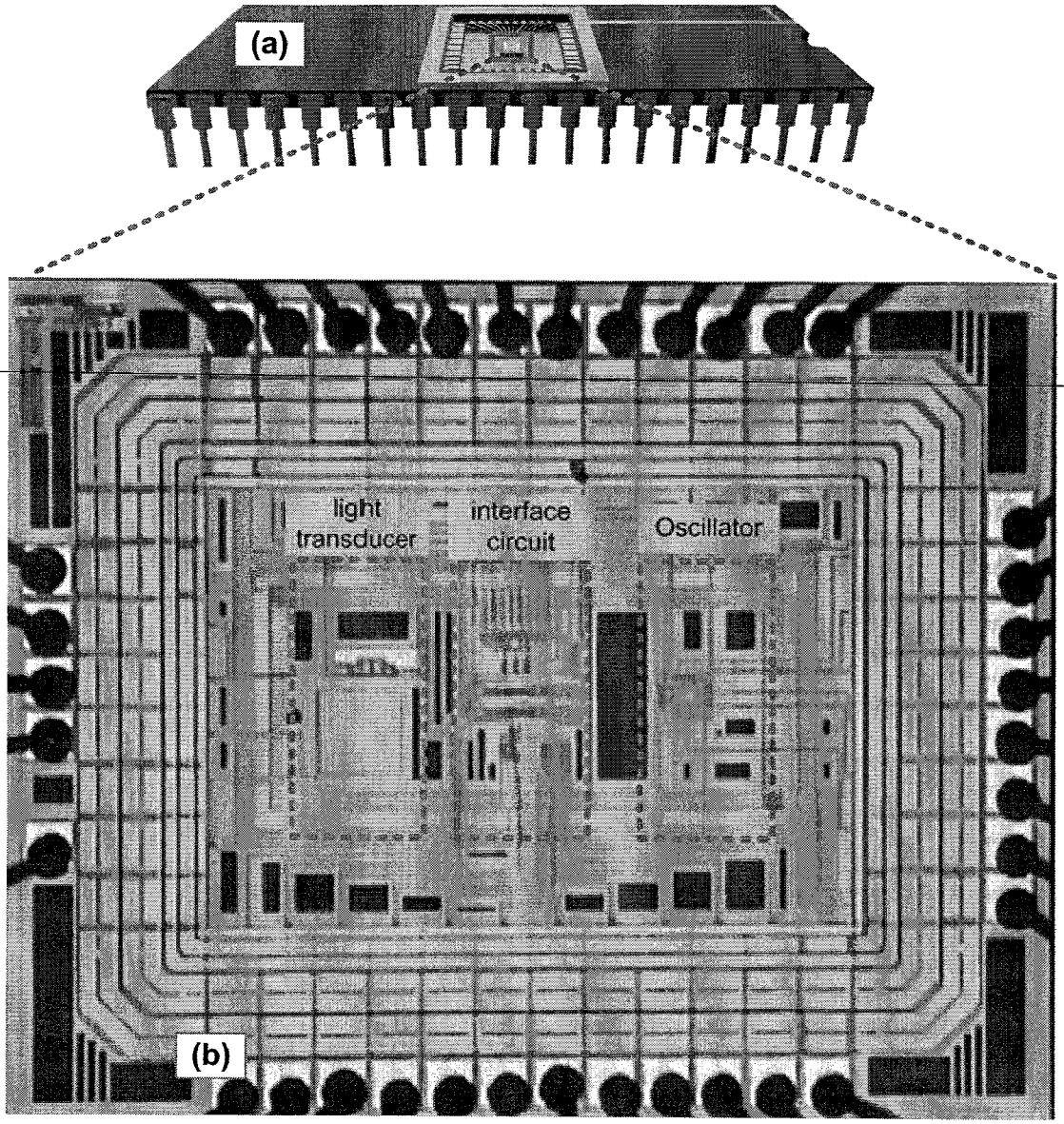
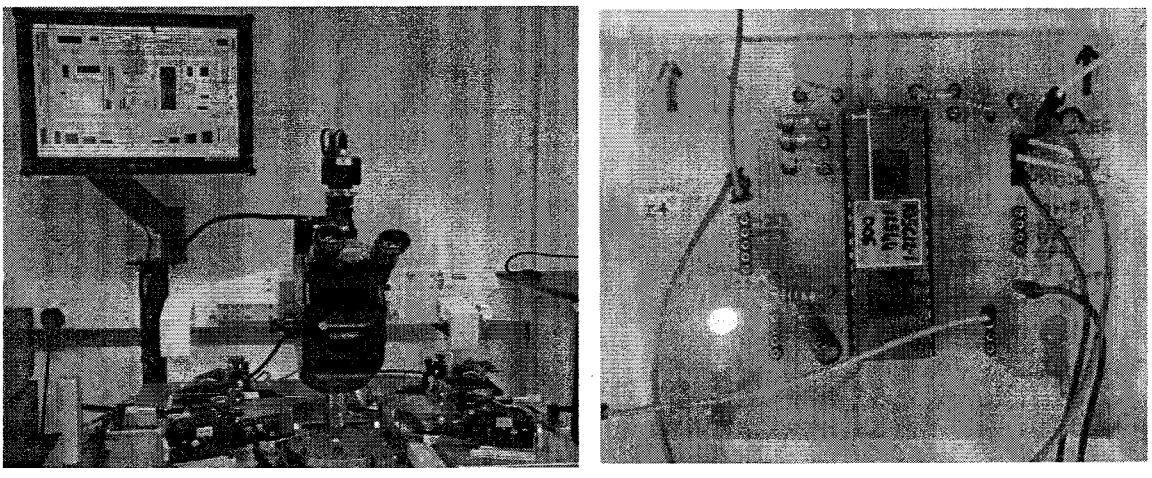


Figure 5.11: (a) Fabricated integrated interface circuit prototype: 40 pin DIP, ceramic package, open-able lid (b) Micrograph of the fabricated chip (core).

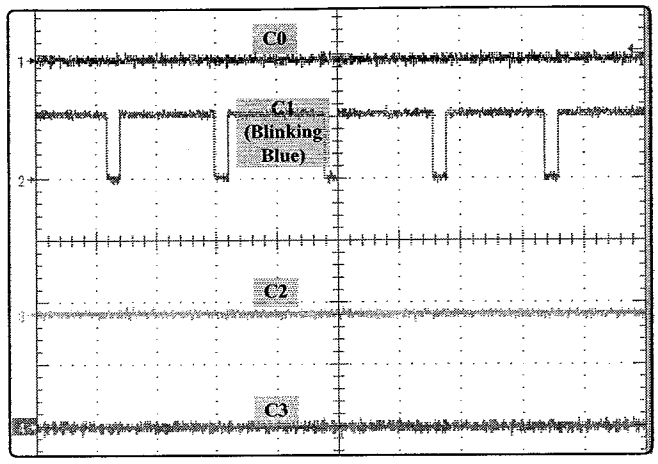
Fig. 5.12 shows the experimental setup to test the fabricated prototype chip. Experimental testing is conducted using Instek GW voltage source, Tektronics TDS 5104 Digital phosphor oscilloscope (4 channel display) and Agilent waveform generator. The reference voltage levels corresponding to the color wavelength are the same as what is used for simulation and are mentioned in Table 5.2 above.

Fig. 5.13 (a) to (c) shows the detected color output (digital output) from the chip for different optical transducer response as captured from the TDS oscilloscope screen. Since the oscilloscope has only 4 channels, 4 digital output bits of the 8 bits (indicator LEDs) are shown at a time. Fig. 13(a) shows a high C1 output ("1"), indicating the detected color falls in the interval 250 mV to 500 mV (which, referring to Table I, is a Blue color). Similarly Fig. 5.13(b) and (c) show the digital output for an optical transducer voltage of 1.21 V and 1.9 V respectively. The output bits refresh (the indicator LEDs blink) every detecting cycle preparing for a new sampled input from the transducer.

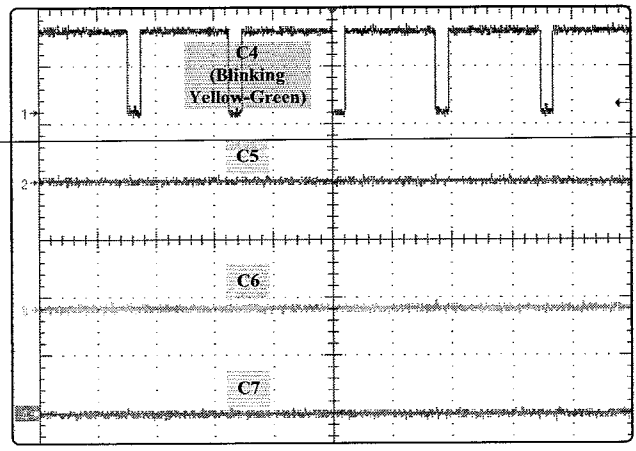


(a) (b)

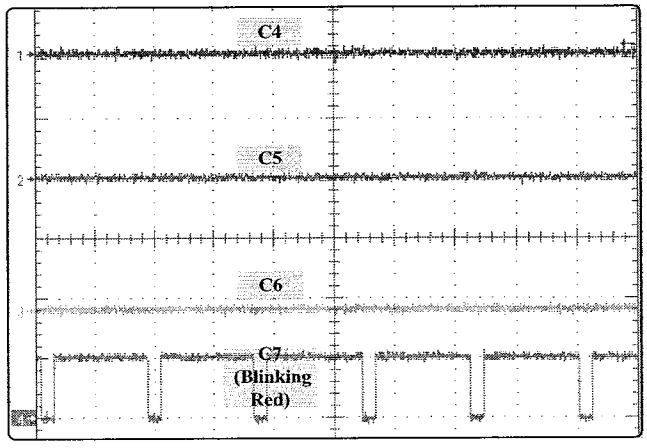
Figure 5.12: (a) Probe station setup of fabricated chip.(b) Fabricated chip with external resistor ladder for experimental testing.



(a) Digital output for an optical transducer value V=480 mV. Bit C1 blinks indicating Blue color is detected.



(b) Digital output for an optical transducer value V=1.21V. Bit C4 blinks indicating Yellow-Green color is detected.



(c) Digital output for an optical transducer value V=1.9 V. Bit C7 blinks indicating Red color is detected.

Figure 5.13: Experimental result from fabricated prototype. (Only 4 output bits are shown at a time out of 8 bits from a 4 channel oscilloscope). Active bit duty cycle is set to be ≈ 80%.

5.2 Two-Stage Design in CMOS

The two stage interface circuit is designed in an effort to increase the resolution (number of colors detected) of the one-stage interface circuit. This design is implemented for 32-level resolution and validated via design in Cadence system design software. Fig. 5.14 shows the block diagram of the two-stage interface circuit. IT basically uses the same building blocks as one-stage design.

In both coarse and fine level stages the main building blocks are resistor ladder that stores reference voltage levels; 8-to-1 and 4-to-1 analog multiplexer (AMUX); four comparators; a 3 bit and 2 bit synchronized counters and 5 bit registers and unity gain buffers.

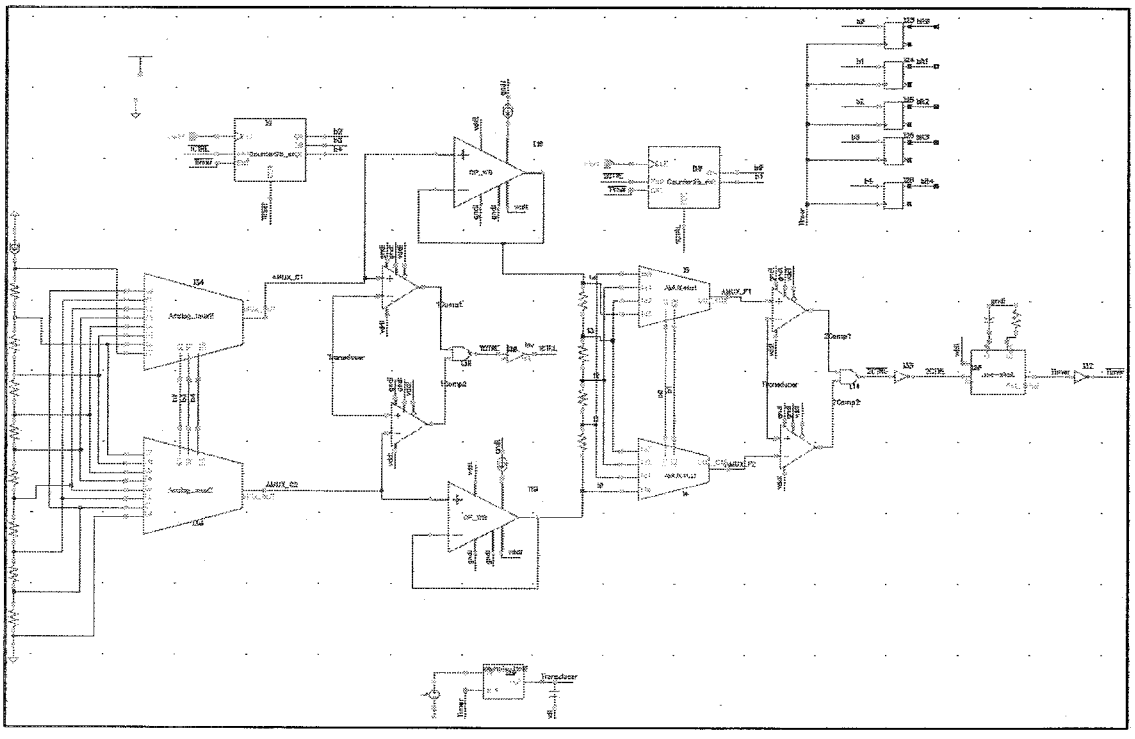


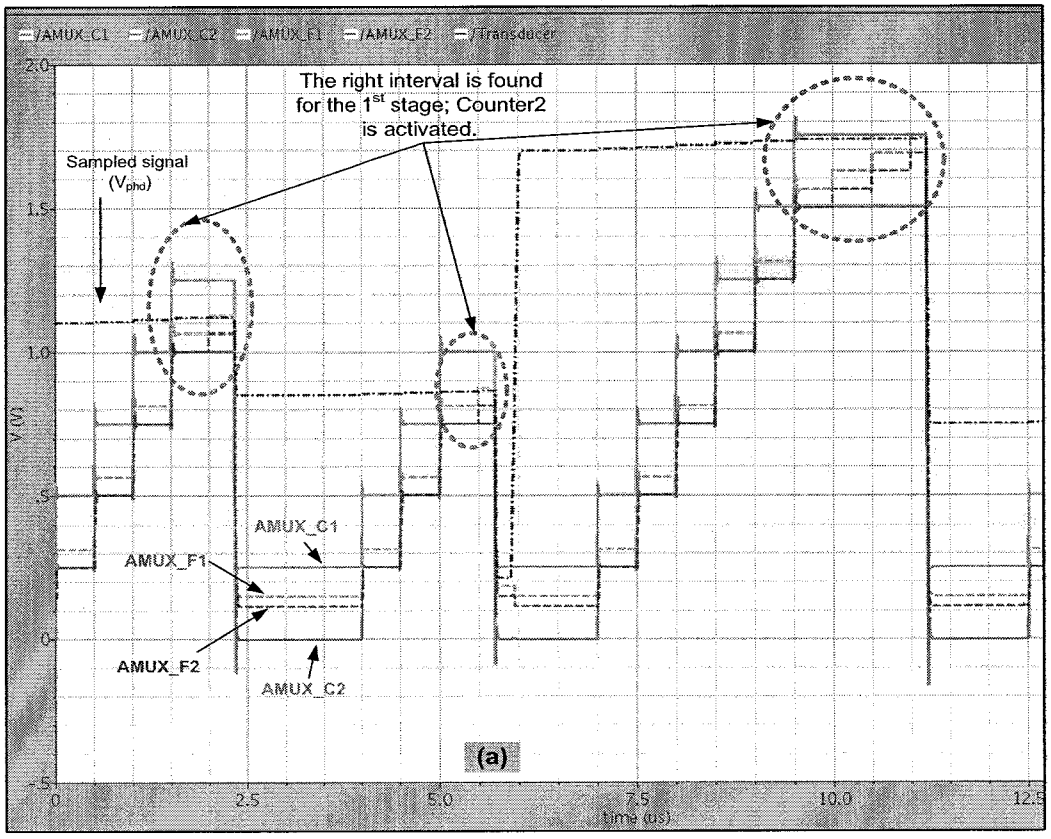
Figure 5.14: Two-stage schematic design in cadence

5.2.1 Simulation Result

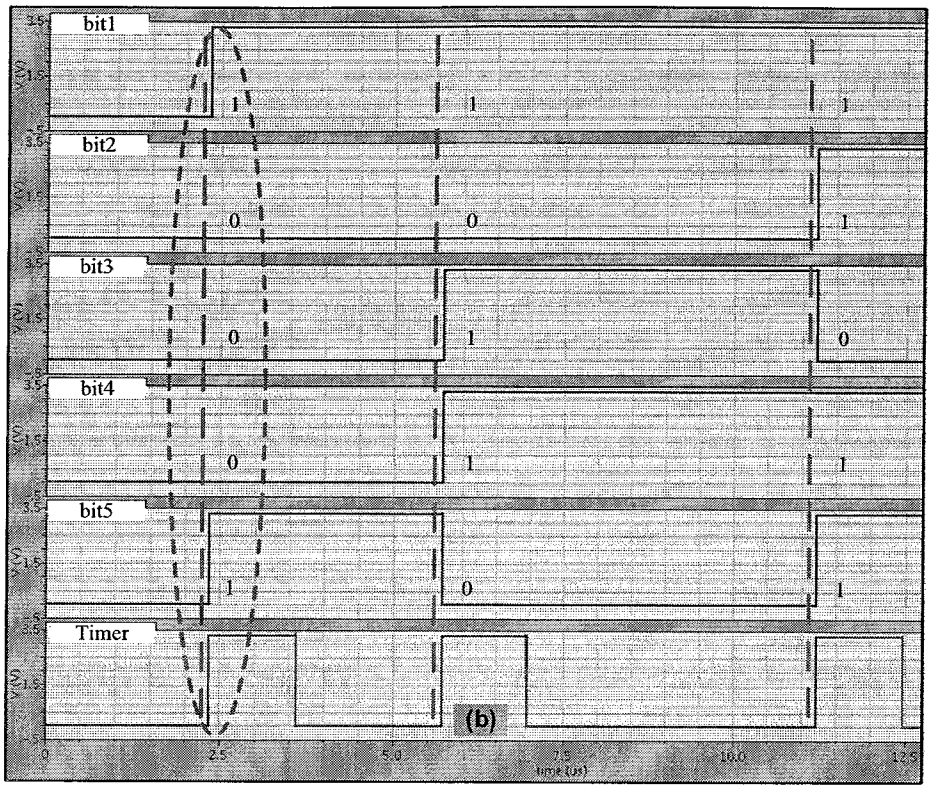
The proposed interface circuit is validated by simulation using Cadence Design Systems on 0.35um Austria Microsystems process technology and the result is shown

in Fig. 5.15. For simulation purpose the sensor electronics response is replaced by a voltage source.

As shown in the Fig. 5.15 the staircase like signal is the signal from the analogue multiplexers as they switch through the reference resistors. Each stage has two multiplexers: Coarse stage AMUX_C1 & AMUX_C2 and fine stage AMUX-F1 & AMUX-F2. During the first stage, the coarse stage counter keeps counting and the AMUX_C1 and AMUX_C2 switch through reference voltages until the sampled voltage from the transducer block falls in a particular interval, which is confirmed by the simultaneous high output from the two comparators. When the interval is found, the upper and lower voltage levels are transferred to the fine stage for further subdivision as shown circled in Fig. 5.15. Finally, the counter states, 3 bits from the counter of stage one form the MSB bits (bit3, bit4 and bit5) and the 2 bits from the counter of stage two form the LSB bits (bit1 and bit2) of the 5 bit final digital output is shown in Fig. 5.15.



(a) The circled parts indicate when the sampled signal from the light transducer block falls inside an interval;



(b) The final digital word output is shown as circled.

Figure 5.15: Cadence Simulation result of 2-stage interface circuit design.

As can be seen in the figures, the first sampled voltage from light transducer block has a value of 1.1 V and this is found in the fourth interval of the first stage (counting starts from interval '000') giving an MSB of '100' and in the fine stage it is found at second stage giving the LSB bits of 01. Combining the MSB and LSB bits gives '10001' as can be seen circled in Fig. 5.15.

5.3 Summary

In this chapter, the main highlight of the thesis which is fabrication and testing of the integrated interface circuit is presented. The results agreed with what is expected in simulation and with the proof of concept validation results in the previous chapter.

CHAPTER 6

DICUSSION AND COMPARISON

The last two chapters have discussed in detail the architecture of the proposed interface circuit for One-stage and Two-stage (pipeline) design along with the simulation and experimental results for discrete and integrated circuit implementation. Result graphs from experimental and simulation has shown the design can successfully read the photovoltage input from a sensor and output a corresponding digital value representing the color. The proposed interface circuit is presented in this thesis in conjunction to an OPT301 optical transducer element. However it can be used as an interface circuit to any sensor system with monotonous voltage output.

6.1 Comparison with other Interface Circuits

The proposed architecture offers a few functionality advantages over conventional optical sensor setup. It requires only fixed number of comparators and multiplexers and a few logic gates. The advantage of the proposed architecture is that the number of required components is fixed regardless of the number of detected colors. This feature is important especially in component count (i.e. low cost) and low power consumption. From the results, it can be shown that the architecture is simple, consumes ultra-low power and yet capable of distinguishing different colors efficiently.

Table 6.1 illustrates a comparison of the proposed interface circuit design as part of a sensor microsystem against other optical sensors of related applications on aspects of implementation, component count as well as power consumption when the information is available.

Table 6.1: Comparison Table

Ref.	Power consumption	CMOS technology	Final Output signal	Remark
[16]	2 W (1.998 W microcontroller & 0.8mW by optical sensor)	AMI 1.5 μm	analog voltage output	Microcontroller (ADC + DSP, memory units) is used for Data Processing.
[73]	-	DIMES 1.6 μm	Digital output	Microcontroller (DSP, memory units are needed) to identify color
[39]	400 μW	n-well 0.7 μm	Digital output	Microcontroller (DSP, memory units are needed) to identify color
[74]	1250 μW	DIMES 1.6 μm	Frequency output	PC or microcontroller (DSP, memory units are needed are needed) to identify color
This work (1-stage)	37 μW	AMS 0.35 μm	Detected Color (Digital word)	Color is identified readily - No further processing is needed
This work (2-stage)	280.5 μW	AMS 0.35 μm	Detected Color (Digital word)	Color is identified readily - No further processing is needed

CHAPTER 7

CONCLUSION AND FUTURE DIRECTION

7.1 Conclusion

Sensors are important devices in our day to day life. Optical sensors are preferred for various applications due to their non-intrusive nature and are commonly used to monitor the environment. For a portable and efficient sensor system, as easy-to use and simple, low cost interface electronics is necessary. In this thesis, we have presented an ultra-low power interface circuit design targeted for use with optical sensors for simple environmental monitoring applications. The interface circuit is able to provide a user ready digital output directly to a LED based display unit and tell the sensed data by the optical sensor system. The proposed design is implemented as discrete system for a proof of concept validation and later a it is fabricated using 0.35 μm standard CMOS technology showing that the proposed interface circuit is suitable for integration in a single chip along with the sensor microsystem. And in contrast to conventional systems, the proposed design avoids the need for an ADC, DSP and memory units which leads to reduced power, reduced complexity and cost. Moreover, it is ideal to be used for simple autonomous and portable real-time monitoring applications.

Two related interface circuit architectures are proposed and validated in this project - namely: One-stage and Two-stage (pipelined) interface circuit design. The proposed design has been implemented for 4, 8, and 32 levels of resolution (i.e. wavelength/intensity) with minor change in number of components.

This thesis contributes towards low power sensor development by proposing simple yet efficient; ultra-low power interface circuit that can be integrated. The thesis focuses on the design of simple readout measurement design suitable for integration in CMOS technologies. The main motivation is to realize simple, low cost and low power frontends for optical sensors and microsystems for integration in field sensing applications, for example, in application where level of concentration or pH is required to conduct regulatory measurements. In addition, there are many applications where a high accuracy in sensing is not essential; in such cases, a simple interface circuit can not only save the design time, but may also offer area and power advantages over the more complex circuits. Therefore, one of the purposes of this research has been to realize simple circuit topologies that may benefit such applications.

To that end, a single chip integrated circuit (IC) is designed and fabricated using commercially available 0.35 μm CMOS standard process. The design is validated via simulation and experimental results from discrete component implementation (i.e. PCB) as well as from fabricated prototype (i.e. IC).

7.2 Future Recommendation

This research work focuses mainly on proposing and validating a proof of concept interface circuit architecture. The proposed system can have a promising application for on-the-spot integrated analysis of biochemical and environmental analyte in the field due to its low power consumption and simplicity.

Few things that could be done to improve this research project in the future can be as follows:

a) The CMOS design made use of a number of available standard library cells provided by foundry. These cells are not necessarily optimized for the application intended. Hence for future implementation the design can be improved in terms of power consumption, area and speed by designing optimized cells for the application.

b) The proposed architecture uses external resistors as analog memory storages, to store photovoltage values for later retrieval. This was done from the desire to keep the freedom of adjusting the resistor values at will. For future implementation the storage resistors should be replaced with internal low power programmable storages for a more efficient and portable system.

c) The proposed interface circuit is discussed in conjunction with an external photodiode. Future recommendation on this aspect would be integrating the entire sensor microsystem: light transducer, the signal conditioning block and the interface circuit on the same chip.

d) In order to have a reliable and repeatable response under various environmental conditions, a compensation mechanism should be implemented for more robust design, e.g. temperature compensation.

REFERENCES

[1] J. Fraden, *Hand Book of Modern Sensors: Physics, Designs, and Applications*, 3rd ed. New York: Springer, 2004.

[2] S. K. Islam and M. R. Haider, *Sensors and low power signal processing*: Springer, 2009.

[3] T. Singh, "Capacitive sensor interface circuits," PhD, Electronics and Telecommunications, Norwegian University of Science and Technology (NTNU), Trondheim, 2009.

[4] J. H. Huijsing, "Smart Sensor Systems: Why? Where? How?," in *Smart Sensors System.* vol. 1, G. C. M. Meijer, Ed., ed Delft, Netherlands: John Wiley & Sons, Ltd, 2008.

[5] V. Chodavarapu, "Integrated CMOS Sensor Microsystems for Biochemical Monitoring " PhD, Electrical Engineering, University of New York, Buffalo, 2006.

[6] L. Yao, "Integrated CMOS - Based Biochemical Sensor Microsystems," Doctor of Philosophy, Electrical and Computer Engineering, McGill University, Montreal, 2010.

[7] P. A. Lieberzeit and F. L. Dickert, "Sensor technology and its application in environmental analysis," *Analytical and bioanalytical chemistry,* vol. 387, pp. 237-247, 2007.

[8] M. Tabacco and T. DiGiuseppe, "Optical chemical sensors for environmental control and system management," *Advances in Space Research,* vol. 18, pp. 125-134, 1996.

[9] R. Narayanaswamy, "Tutorial review—Optical chemical sensors: transduction and signal processing," *Analyst,* vol. 118, pp. 317-322, 1993.

[10] W. Jin, *et al.*, "Continuous Intra-Arterial Blood pH Monitoring by a Fiber-Optic Fluorosensor," *Biomedical Engineering, IEEE Transactions on,* vol. 58, pp. 1232-1238, 2011.

[11] G. Lu, *et al.*, "Design and testing of a CMOS BDJ detector for integrated micro-analysis systems," *Microelectronics journal,* vol. 32, pp. 227-234, 2001.

[12] R. Yotter, *et al.*, "Optimized CMOS photodetector structures for the detection of green luminescent probes in biological applications," *Sensors and Actuators B: Chemical,* vol. 103, pp. 43-49, 2004.

[13] A. Sohanghpurwala, *et al.*, "Optical Replacement of pH Electrode," *Sensors Journal, IEEE,* vol. 9, pp. 219-220, 2009.

[14] Hai-xu Chen, *et al.*, "Colorimetric optical pH sensor production using a dual-color system," *Sensors and Actuators B: Chemical,* vol. 146, pp. 278 - 282, 2010.

[15] A. Pacquit, *et al.*, "Development of a volatile amine sensor for the monitoring of fish spoilage," *Talanta,* vol. 69, pp. 515-520, 2006.

[16] Z. Fu, "Integrated CMOS sensor microsystem for optical sensing and processing," PhD, Electrical Engineering, University of New York, Buffalo, 2009.

[17] M. O'Toole and D. Diamond, "Absorbance Based Light Emitting Diode Optical Sensors and Sensing Devices," *Sensors,* vol. 8, pp. 2453-2479., 2008.

[18] A. Safavi and H. Abdollahi, "Optical sensor for high pH values," *Analytica Chimica Acta,* vol. 367, pp. 167-173, 1998.

[19] P. E. Henning, "Application of advanced time-resolved fluorescence detection techniques for remote pH sensing with optical fibers," PhD, Chemistry, University of Wisconsin, Milwaukee, 2009.

[20] A. Lobnik, *et al.*, "Optical Chemical Sensors: Design and Applications," in *Advances in Chemical Sensors*, W. Wang, Ed., ed Slovenia: InTech, 2012.

[21] A. S. Jeevarajan, *et al.*, "Continuous pH monitoring in a perfused bioreactor system using an optical pH sensor," *Biotechnology and Bioengineering,* vol. 78, pp. 467-472, 2002.

[22] A. De Marcellis and G. Ferri, *Analog circuits and systems for voltage-mode and current-mode sensor interfacing applications*: Springer, 2011.

[23] L. Spangler, "Factors influencing the design of microsystems," in *Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004*, 2004, pp. 687-691.

[24] C. Falconi, *et al.*, "Electronic interfaces," *Sensors and Actuators B: Chemical,* vol. 121, pp. 295-329, 2007.

[25] A. Arnau, "A review of interface electronic systems for AT-cut quartz crystal microbalance applications in liquids," *Sensors,* vol. 8, pp. 370-411, 2008.

[26] G. Meijer, "Interface electronics and measurement techniques for smart sensor systems," *Smart Sensor Systems,* pp. 23-54, 2008.

[27] A. Rossini, "Design of mixed analog/digital interface circuits for sensors and micro-systems," PhD, ELECTRONIC ENGINEERING, COMPUTER SCIENCE AND ELECTRICAL, UNIVERSITY 'OF PAVIA, 2006.

[28] B. Razavi, *Design of analog CMOS integrated circuits*. Singapore: McGraw-Hill, 2001.

[29] H.-x. Chen, *et al.*, "Colorimetric optical pH sensor production using a dual-color system," *Sensors and Actuators B: Chemical,* vol. 146, pp. 278-282, 2010.

[30] A. S. Raja and K. Sankaranarayanan, "Use of RGB Color Sensor in Colorimeter for better Clinical measurement of Blood Glucose," *BIME Journal,* vol. 6, pp. 23-28, 2006.

[31] E. J. Netto, *et al.*, "A fiber-optic broad-range pH sensor system for gastric measurements," *Sensors and Actuators B: Chemical,* vol. 29, pp. 157-163, 1995.

[32] Y. Mendelson, "Optical Sensors," in *The Biomedical Engineering Handbook*, J. D. Bronzino, Ed., second ed Boca Raton: CRC Press LLC, 2000.

[33] Colette McDonagh, *et al.*, "Optical Chemical Sensors," *Chemical Reviews,* vol. 108, pp. 400-422, 2008.

[34] A. Dybko, "Fundamentals of Optical Chemical Sensing," in *Optical Chemical Sensors*. vol. 224, F. Baldini, *et al.*, Eds., ed Dordrecht, The Netherlands: Springer, 2004, pp. 47 - 59.

[35] R. Narayanaswamy, "Tutorial review-Optical chemical sensors: transduction and signal processing," *Analyst,* vol. 118, pp. 317-322, 1993.

[36] G. Gauglitz, "Direct optical sensors: principles and selected applications," *Analytical Bioanal Chemistry,* vol. 381, pp. 141-155, 2005 Jan.

[37] J. Lin and D. Liu, "An optical pH sensor with a linear response over a broad range," *Analytica Chimica Acta,* vol. 408, pp. 49-55, 2000.

[38] O. S. Wolfbeis, "Chemical Sensing Using Indicator Dyes," in *Optical Fiber Sensors*. vol. IV, J. Dakin and B. Culshaw, Eds., ed Boston-London: Artech House, 1997, pp. 53-107.

[39] A. Fernandes, *et al.*, "Smart-optical detector CMOS array for biochemical parameters analysis in physiological fluids," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 3192-3200, 2008.

[40] D. A. Skoog, *et al.*, *Fundamentals of Analytical Chemistry*, 8th ed. CA: Pacific Grove, 2007.

[41] J. Norman F. Sheppard and A. Guiseppi-Elie, "pH Measurement," in *Measurement, Instrumentation and Sensors Handbook*, J. Webster, Ed., ed Florida: CRC Press and IEEE Press, , 1999.

[42] S. Vuppu, "A Microcontroller-based Wireless Optical PH Sensor," MSc, Computer Science and Electrical Engineering, University of Maryland Baltimore County, 2008.

[43] R. G. Jackson, *Novel Sensors and Sensing*: Taylor & Francis, 2004.

[44] R. A. Yotter and D. M. Wilson, "A review of photodetectors for sensing light-emitting reporters in biological systems," *Sensors Journal, IEEE,* vol. 3, pp. 288-303, 2003.

[45] M. J. D. a. P. K. Basu, "Silicon Photodetectors," in *Silicon Phtonics - Fundamentals and Devices*, ed: John Wiley & Sons, 2012, pp. 197-247.

[46] B. V. Zeghbroeck. (2011). *Principles of Semiconductor Devices*. Available: http://ece-www.colorado.edu/~bart/book/

[47] G. LAngerfelder, *et al.*, "A novel color sensitive CMOS detector," *Nuclear Instruments and Methods in Physics Research Section A,* vol. 610, pp. 50-53, 2009.

[48] Z. Fu, *et al.*, "CMOS-based colour-change pH measurement system," *Electronics letters,* vol. 45, pp. 1138-1140, 2009.

[49] G. N. Lu, *et al.*, "Design and testing of a CMOS BDJ detector for integrated micro-analysis systems," *Microelectronics Journal,* vol. 32, pp. 227-234, 2001.

[50] R. F. Wolffenbuttel, "Optical Sensors Based on Photon Detection," *Smart Sensor Systems,* pp. 79-120, 2008.

[51] H.-S. L.-t.-V. Converter, "Product Identification Number TSL 257, manufactured by Texas Advanced Optoelectronic Solutions Inc," ed: TX.

[52] Burr-Brown, "Integrated Photodiode and Amplifier—OPT301," ed. Tucson, AZ, 1994.

[53] G. Minas, *et al.*, "On-Chip Integrated CMOS Optical Detection Microsystem for Spectrophotometric Analyses in Biological Microfluidic Systems," in *Industrial Electronics, IEEE*, 2005, pp. 1133 - 1138.

[54] M. A. Shinde, "Measurement of pH using fiber opticsensor Based on colorimetry."

[55] D. P. Poenar, *et al.*, "Colour sensor for (bio) chemical/biological discrimination and detection," *Materials Science in Semiconductor Processing,* vol. 5, pp. 17-22, 2002.

[56] A. Ruckelshausen, *et al.*, "Microcontroller-based multi-sensor system for online crop/weed detection," in *BRIGHTON CROP PROTECTION CONFERENCE WEEDS*, 1999, pp. 601-606.

[57] D. A. Visan, *et al.*, "System with microcontroller for photometric measurements in technological installations and optical communications systems," in *Electronics Technology (ISSE), 2011 34th International Spring Seminar on*, 2011, pp. 505-508.

[58] "PSpice User's Guide," Cadence Design Systems, United States of America.June 2004.

[59] M. Cooney, "Cadence Design Flows," University of HawaiiFed 18 2010.

[60] B.-H. G. a. K.-S. Chong, "Low Power Asynchronous Circuit Design: An FFT/IFFT Processor," in *CMOS Processors and Memories*, K. Iniewski, Ed., ed Singapore: Springer, 2010.

[61] I. Hatirnaz, "Cadence Design Tools Tutorial," ed, 1998.

[62] A. J. L. Martin, "Tutorial Cadence Design Environment " October 2002.

[63] R. J. Baker, *CMOS: Circuit design, layout, and simulation* vol. 18: Wiley-IEEE Press, 2011.

[64] J. D. Corbeil Jr and M. J. Saunders, "Method for performing design rule check of integrated circuit," ed: Google Patents, 2008.

[65] G. Betta, *et al.*, "Temperature measurement by multifiber optical sensor," *Instrumentation and Measurement, IEEE Transactions on,* vol. 49, pp. 1004-1008, 2000.

[66] H. Escid, *et al.*, "0.35 μm CMOS Optical Sensor for an Integrated Transimpedance Circuit," *International Journal on Smart Sensing and Intelligent Systems,* vol. 4, 2011.

[67] V. MICHAL, "Design of CMOS Analog Integrated Circuits as Readout Electronics for High-TC Superconductor and Semiconductor Terahertz Bolometric Sensors," PhD, Theoretical and Experimental Electrical Engineering, UNIVERSITY PIERRE ET MARIE CURIE, Paris, 2009.

[68] K. Kundert, *et al.*, "Design of mixed-signal systems-on-a-chip," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 19, pp. 1561-1571, 2000.

[69] A. Patel, *et al.*, "Analog multiplexing in time domain for biochemical measurement processing," in *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, 2002, pp. I-60-3 vol.1.

[70] F. Maloberti, *Analog design for CMOS VLSI systems* vol. 646: Springer, 2001.

[71] Robert C. Chang and B. J. Sheu, "Analog and VLSI Circuits," in *transmission gate*. vol. 3, W.-K. Chen, Ed., ed chicago: CRC, 2002.

[72] P. Chan, *et al.*, "A programmable clock oscillator for integrated sensor applications," in *Electron Devices Meeting, 1998. Proceedings. 1998 IEEE Hong Kong*, 1998, pp. 144-147.

[73] G. De Graaf and R. Wolffenbuttel, "Smart optical sensor systems in CMOS for measuring light intensity and colour," *Sensors and Actuators A: Physical,* vol. 67, pp. 115-119, 1998.

[74] J. H. Correia, *et al.*, "A single-chip CMOS optical microspectrometer with light-to-frequency converter and bus interface," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 1344-1347, 2002.