Low Power Bio-potential Amplifier (for EEG)

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Supervised by Dr Likun Xia

Dissertation submitted in partial fulfilment of
the requirements for the
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(Electrical and Electronics Engineering)

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CERTIFICATION OF APPROVAL

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Approved by,

_____

(Dr Likun Xia)

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK
September 2013

CERTIFICATE OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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LIM YONG HOOI

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Abstract

The size and dependency on power supply of current biopotential data acquisition systems prohibit continuous monitoring of biopotential signals through battery powered devices. As the interest in continuous monitoring of EEG increases for healthcare and research purposes such as seizure detection, there is an increasing need to bring down the power consumption on the biopotential amplifier (BPA). BPA is one of the most power consuming components in the biopotential data acquisition system. In this FYP, we will develop a method to improve the existing BPA using MIMOS 0.35um process technology through implementation of various low power flicker noise cancelation techniques. Techniques used include low impedance node chopping and non-overlapping demodulation chopping. The scope of this FYP is focusing on design and simulation on Cadence software in circuit level implementation. This work provides insights as well as a starting point in lowering the power consumption of bio-potential data acquisition system. This will help to enable battery power system for continuous monitoring of EEG signals in the future. This final report discusses on both the literature review, background of the projects and methodology as well as the outcome of the work. The report is concluded by suggesting future works that can be carried out in this final year project (FYP).

1. Background of Study

Biopotential signals such as electroencephalogram (EEG), electrocardiogram (ECG) and electromyogram (EMG) are essential in modern medical diagnosis. In modern clinical practice, biopotential signals are often recorded with power consuming equipment that operate on regulated power supply such as power supply from the wall socket. The size and dependency on power supply prohibit continuous monitoring of these biopotential signals. Hence, there is an increasing need for low-power portable biopotential data acquisition system [2-5].

Front-end circuit of the biopotential data acquisition system is typically very power consuming and is normally the bottleneck of the extracted signal quality [5]. This is especially true for the biopotential amplifier (BPA). However, low power requirement for portable biopotential data acquisition system imposes several constraints on the signal performance of the BPA [5]. In fact, low power always corresponds to poor noise immunity in analog circuitry [6]. This tradeoff is magnified by the fact that biopotential signals are usually in low frequency range from DC to several hundreds hertz, hence susceptible to large amount of flicker noise or 1/f noise [5-8].The spectrum of these biopotential signals are also overlapping with interferences such as 50/60Hz power line interference which increase the design difficulties. The figure 1 and table 1 below show the frequency and amplitude characteristics of typical biopotential signals together with nearby contaminating signals [9].

As the need of portable biopotential data acquisition system arises, researchers in this field are constantly exploring new circuit techniques in the quest of reducing power consumption of the BPA design while preserving its common mode rejection ratio (CMRR).

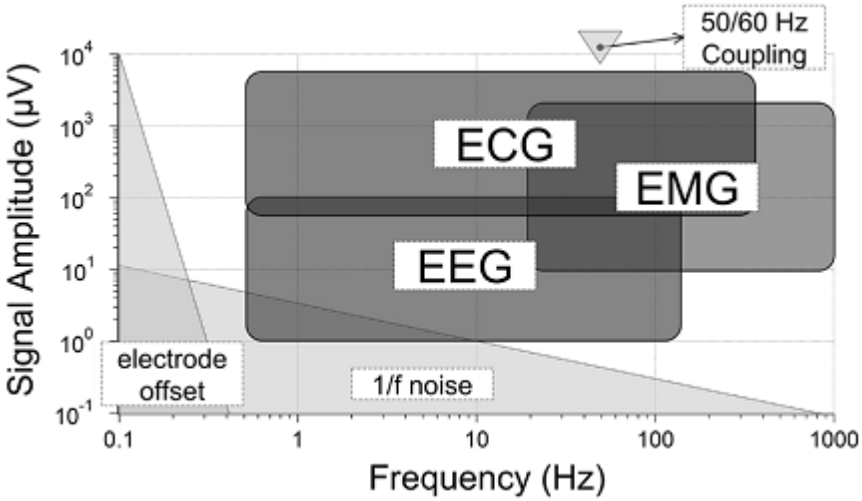


Figure 1: Characteristics of biopotential signal and nearby corrupting signals [9].

Physiological Signals	Measurement Range	Gain Needed(dB)	Frequency Range(Hz)
Electroencephalogram (EEG)	25-300 uV	50-72	DC-150
Electrocardiogram (ECG)	0.5-4 mV	28-46	0.01-250
Electromyogram (EMG)	0.1-5 mV	27-60	DC-500

Table 1: Properties of biopotential signals [6].

2. Problem Statement

2.1. Problem Identification

Current biopotential data acquisition systems have high power consumption and are dependent on stationary regulated power source such as power from wall socket. It has becomes a major obstacle for continuous biopotential data acquisition as the system has low portability. Continuous monitoring of biopotential signals is increasingly important for applications such as diagnosis of brain and cardiovascular disease as well as early detections. Due to the fact that low power design corresponds to deterioration of noise performance and limits applicable circuit techniques, more mature circuit technique and structure has to be developed to facilitate the growth of portable biopotential data acquisition system. As biopotential amplifier (BPA) consumes a lot of power among all the circuitry components inside the biopotential data acquisition system. It has become one of the most interesting problem. This final year project (FYP) aims to propose a novel design to meet requirement of low power BPA.

2.2. Significance of Project

This FYP aims to improve existing low power BPA design in order to facilitate the growth in biomedical research and applications. The proposed approach in BPA will help to improve battery-powered portable biopotential data acquisition system.

3. Objective and Scope of Study

3.1. Objective

In general, this FYP goal is to develop a new low power biopotential amplifier (BPA) that does not sacrifice common mode rejection ratio (CMRR) and noise performance.

In short, this FYP aims to:

1. To develop a method to improve existing BPA in term of power consumption while maintaining noise at acceptable level
2. To evaluate the proposed BPA performance on power consumption and noise level with reference to existing technique

3.2. Scope of Study

The overall FYP plan is to minimize power consumption of biopotential amplifier (BPA) using various techniques. In the duration of Final Year Project 1 and Final Year Project 2, we target on lowering the power consumption of the BPA itself.

The scopes for this FYP are:

1. Evaluate and implement suitable op-amp design for low power BPA
2. Research on possible alternatives to reduce power consumption

4. Relevancy of the Project

This research field of this project is especially relevant to current booming of biopotential signal processing researches such as EEG and ECG. As CISIR is one of the key research centers for biomedical applications in UTP, and even in Malaysia, it is important to have custom hardware design such as BPA to strengthen on biomedical hardware research. Further research on portable biopotential data acquisition system will require mature circuit techniques on low power BPA, which is the main focus of this FYP.

5. Feasibility of the Project within the Scope of Time Frame

It is very interesting to go for low power design of whole biopotential data acquisition system. However, as we take into account time feasibility, the FYP has been mainly focusing on improving power consumption of the BPA. The design and circuit performance evaluation will be proceeded based on Cadence simulation. This makes it achievable and feasible in the duration of FYP.

6. Literature Review

This literature review cover challenges of current biopotential data acquisition system design and the existing strategies to overcome the problems. Both low power BPA design techniques and circuit techniques to improve biopotential signal quality are reviewed.

6.1. Flicker noise cancelation technique

In biopotential amplifier, there are various type of noise such as thermal noise and flicker noise. Flicker noise or 1/f noise are dominant noise source in low frequency range. As EEG signals are low frequency signals (DC to 150Hz), flicker noise can corrupt the EEG signals if flicker noise cancelation techniques are not being implemented in BPA. This flicker noise are usually associated to operational amplifier (op-amp) circuitry in the BPA [10]. In fact, flicker noise is the result of imperfect silicon structure at interface of gate oxide and silicon substrace in MOS transistor channel [11]. Techniques such as auto-zeroing, correlated double sampling and chopper-stabilizing are some of the common technique used to minimize flicker noise in BPA [12]. Auto-zeroing technique samples noise and offset in the sampling phase and subtract them from the contaminated signal in the signal-processing phase. Low frequency random noise changes slowly and the noise experienced in the sampling phase and processing phase will be somewhat similar. Hence, the technique is effective against low frequency noise and DC offset. This technique imposes a highpass effect onto the flicker noise and DC offset. However, as it is a sampling technique, its effectiveness depends on autocorrelation between sampling phase and signal-processing phase noise. This results in a raised noise floor in higher frequency spectrum which the noise is largely consisting of white noise instead of flicker noise [12]. Correlated Double Sampling (CDS) was firstly introduced as to remove switching transient and can be applied to attenuate flicker noise [13]. It is a particular case of auto-zeroing where the noise and offset are sampled twice in a single clock cycle. It has similar effect on the noise performance of the circuit [12].

Unlike auto-zeroing and correlated double sampling, chopper stabilization technique does not depend on sampling. Recent works on BPA design, such as BPA's in reference [5-8, 14], favor chopper stabilization technique to overcome flicker noise. In chopper stabilization technique, the input signal is modulated to higher frequency region with a chopping frequency of f_{chop} before passing through the amplifier. The output of the amplifier is then demodulated again by f_{chop}. This effectively avoid biopotential signal being corrupted by flicker noise. Artifacts and flicker noise that has been frequency up-converted by f_{chop} can then be filtered using a lowpass filter. The amplified biopotential signal is cleaned up without raising the noise floor [6, 12]. The figure 2 below shows the principle of the chopper stabilization technique in sequence [12]. However, large bandwidth in amplifier is required as the biopotential signal has been modulated to high frequency region. This become a big challenge for designers as distortion arises when bandwidth of amplifier is limited with low power design [8].

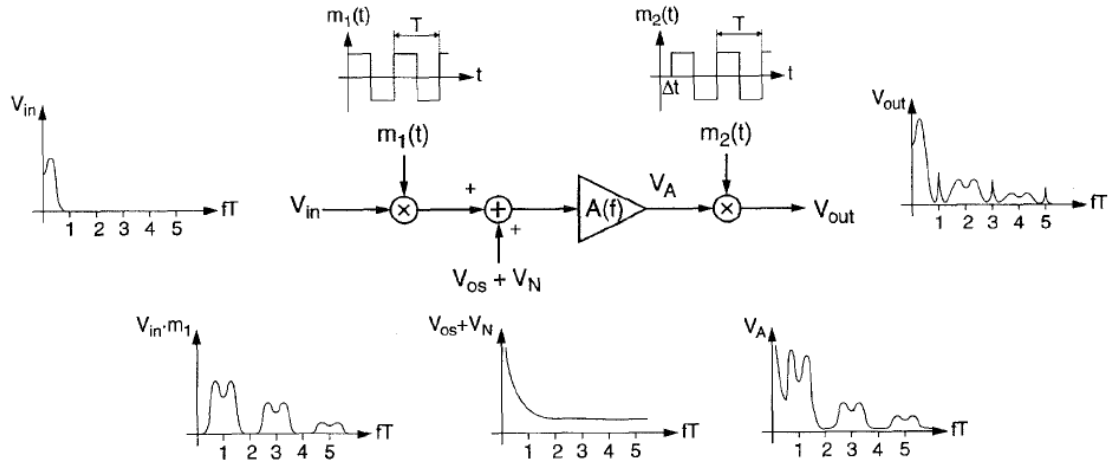


Figure 2: Principle of chopper stabilization technique (without LPF stage) [12]

6.2. Low power chopper stabilization technique

Chopper stabilization technique usually requires a low pass filter at the output to filter out artifacts and up-converted flicker noise. Normally, a separate active low pass filter is used, leading to extra power consumption. This can be improved by adding a feedback capacitor in the same feedback loop after demodulation instead of having an additional stage [6].

Unfortunately, this is still power consuming due to the need of large bandwidth to avoid distortion. A novel technique of chopping spike filter (CSF) is proposed in order to filter the out the spikes artifacts generated by the chopper [5]. This method employs track and hold technique by only tracking the part of signal that is clean without spike artifacts and hold it during the occurrence of artifacts. The schematic below shows the chopping spike filter with its principle operations. However, selection of the duty cycle for track and hold period is essential and difficult to control.

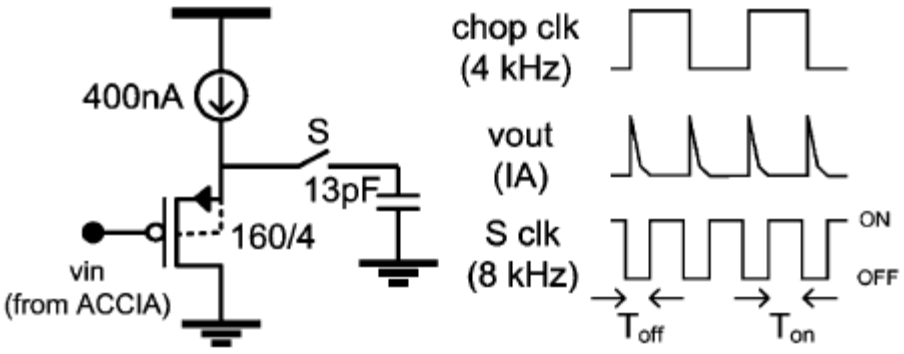


Figure 3: Chopping Spike Filter with its principle operations [5]

Instead of lowering power consumption from redesigning filters, the authors in [8] employ chopping technique in low-impedance node to relax settling time constant requirement, suppressing second harmonic distortion. This relaxation of settling time constant make reduction of current consumption possible as less current is needed to charge parasitic capacitances and ensure strict settling time requirement is met. The work incorporates a chopper circuit into a modified version folded-cascode amplifier, making sure the chopping is performed in low-impedance node. This allows partitioning of current for noise efficiency maximization [8]. The figure 4 below illustrates how a folded-cascode amplifier is modified to include chopper circuit in low-impedance note.

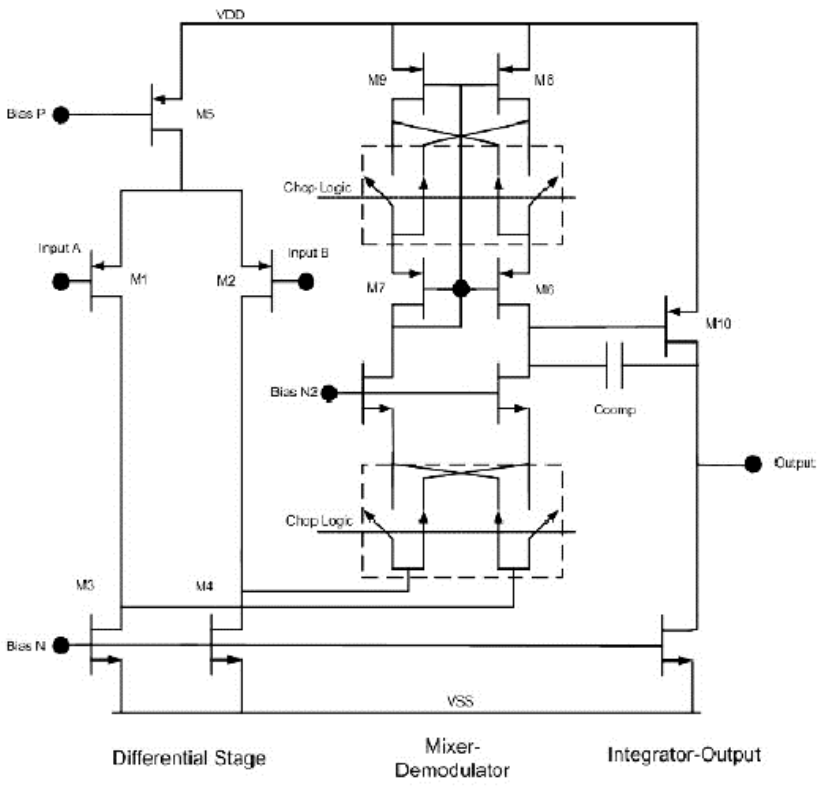


Figure 4: Addition of chopper circuit into classical folded-cascode amplifier [8]

6.3. Differential electrode offset

Often, skin-electrode interface does not have perfectly match impedance. Mismatch is also common in biopotential electrode in polarization voltages [14]. It gives rise to differential electrode offset (DEO) [9]. Hence, biopotential systems should have front-end circuit with low noise, high CMRR and sub-Hertz highpass filtering in order to maintain the signal clarity. A chopper stabilizing BPA with current feedback and AC coupling in current domain is implemented to combat DEO [5]. By utilizing a stage of transconductance with lowpass cutoff frequency, f_p, the output voltage is first low-passed and converted into current to feedback into the chopper amplifier for suppression of the DEO. This AC coupling method essentially high-pass filter out the DEO [5]. The authors in reference work [7] utilize a similar method by proposing a Gm-C filter for the current feedback loop of the instrumentation amplifier.

However, the active AC coupling methods [5, 7] has been commented as only for filtering limited amount of DC offset [5, 15, 16]. There is also concern about additional power consumption since it has an active feedback loop. Hence, passive AC coupling can be used as one of the alternative choice. In order to use passive AC-coupling, large value of DC blocking capacitance is needed to minimize the effect of capacitive divider between the DC-blocking capacitor and parasitic capacitances. The authors in reference work [14] avoid the use of external capacitance by achieving large capacitance value with PMOS parasitic capacitance between gate and bulk, and CMRR is governed by the equation below.

$$CMRR \approx \frac{C_{DC}}{\Delta C_{mismatch}}$$

where C_{DC} is the DC-blocking capacitance and $C_{mismatch}$ is the capacitance mismatch of the parasitic capacitance.

It is difficult to accurately control of PMOS gate-to-bulk capacitance (Cgb) because it is nonlinear capacitance. Hence, these capacitance are implemented in PMOS varactor structure as a tunable capacitor. A varactor structure is basically a parallel connected PMOS with different size where each of the PMOS's Cgb is controlled to be two distinct fixed value. This digital control scheme allows accurate control of the tunable capacitor. By using this technique, passive AC-coupling become a feasible solution as we can have large DC-blocking capacitance on-chip with accurate control.

6.4. Multiple op-amp BPA architecture

Three op-amps BPA architecture usually provides high input impedance and high CMRR without trimmings [17]. Although single op-amp BPA can provide active DC-blocking using feedback, the requirement of a subtractive node makes it difficult to be implemented [18]. The authors in [18] suggest two op-amps in the first stage, one for each input, making it possible to feedback the low frequency components V_c derived from the output of the third op-amp output. As compared to active DC blocking, this does not require a subtractive node as the V_c can be directly fed into the circuit as shown in the figure 5 below. However, as op-amps are normally high in power consumption,

the use of three op-amps in this structure makes it not suitable for low power BPA design.

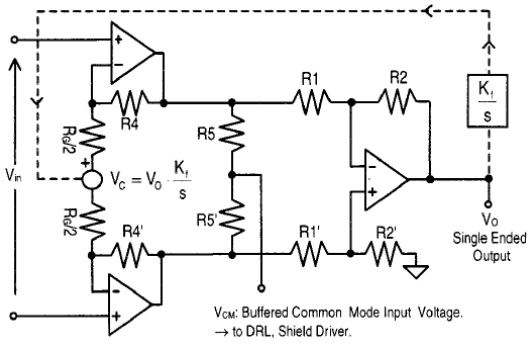


Figure 5: Three op-amps structure proposed by [18].

There are also some two op-amps BPA architecture that employs active DC-blocking to yield precise control in DC rejection. Reference work [19] employ two op-amps as an input stage and feedback DC output voltage using a fully differential network. The feedback mechanism has been simplified into the figure 6. Similarly, the use of multiple op-amps makes it unsuitable for low power applications.

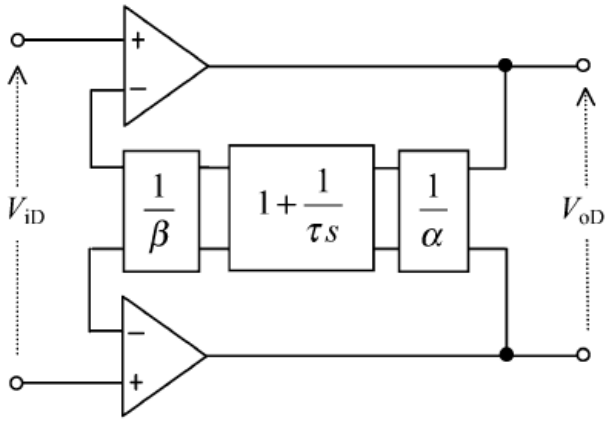


Figure 6: Simplified output DC feedback proposed by [19]

6.5. Power line interference cancelation technique

In order to handle power line interference to avoid the biopotential signals corruption, a direct interference canceling (DIC) technique has been proposed [20]. As the 60Hz frequency and sine wave waveform of power line interference is known, DIC technique minimizes the effect of power line interference based on the information. This technique firstly apply a bandpass filter at a narrow bandwidth with center

frequency of 60Hz to extract the power line interference. Then the extracted signal is fed into a custom PLL circuit to generate in-phase and quadrature-phase signal of the power line interference. These signals having identical frequency as the power line interference will then be provided to DIC loop to effectively cancel power line interference[20]. However, this method may not be applicable for low power application as it requires additional op-amps. Moreover, it is not reported if the DIC will reject part of biopotential signal since it contains signal very close to 60Hz as well.

Issue	Solution	Description	Weaknesses
Flicker Noise -Arise from MOS channel	Auto-zeroing [12]	Samples noise and offset in the sampling phase and subtract it from the contaminated signal in the signal-processing phase	- Effectiveness depends on autocorrelation of noise between the 2 phase - Raise noise floor in higher frequency spectrum
	Correlated double sampling [12]	Auto-zeroing operation with sample and hold stage in the back	- Similar effect on noise performance with auto-zeroing
	Chopper stabilization [5-8, 12, 14]	Modulate input signal to higher frequency region with a chopping frequency of fchop before amplification. Amplified output is demodulated by fchop to effectively avoid signal contamination by flicker noise without raising noise floor	- Need larger bandwidth in amplifier as the biopotential signal is up-converted to higher frequency by f_{chop}
Low power BPA design -Focus on Chopper Stabilization	Low pass filtering by feedback capacitance[6]	Add a feedback capacitor in the gain feedback loop instead of having another active low pass filter stage	- Still power consuming due to the need of large bandwidth
	Chopping spike filter[5]	Track and hold technique that track clean signal and hold when chopping artifacts are expected to occur. This reduce the bandwidth and power needed	- Careful selection of the duty cycle for track and hold period is essential
	Chopping at low-Z node[8]	Modified version folded-cascode amplifier allow chopping to be done in low-impedance node. This avoid strict settling time constant requirement and hence, reduce current consumption	- Special design of the amplifier is needed - Modification is needed for implementation on other amplifier topology

Differential electrode offset	Active AC coupling using current feedback[5, 7]	Utilize a stage of transconductance with low-pass cutoff frequency. Output voltage are low-passed and converted into current for feedback	- Has been commented as only able to filter limited amount of DC-offset[5, 15, 16]
	Passive AC coupling with novel PMOS tunable capacitance[14]	Large value of DC-blocking capacitance is needed to minimize the effect of capacitive divider. Avoid using external capacitance by achieving large capacitance value with PMOS parasitic capacitance between gate and bulk	- Varactor structure is needed and tuning is important for signal performances
Need for simpler active DC-blocking implementation	Multiple op-amp BPA architecture[18, 19]	Multiple op-amp structure enable simpler feedback structure without the need for a subtractive node	- High power consumption due to using multiple op-amps in the main path as well as feedback loop
Power line interference	Direct Interference Canceling (DIC)[20]	Bandpass filtered the signal at a narrow bandwidth with center frequency of 60Hz A custom PLL circuit generates in-phase and quadrature-phase signal of the power line interference based on the bandpassed signal. These signals are provided to DIC loop to effectively cancel power line interference	- May not be applicable for low power application as it requires additional op-amps - It is not reported if the DIC will reject biopotential signal that is very close to 60Hz

7. Methodology

7.1. Research Methodology

The research methodology serve as a guide and plan on how the research should be carried out for the whole duration of the final year project. This improves the time effectiveness of the research works carried out. The general flow of our research methodology is included in figure 7.

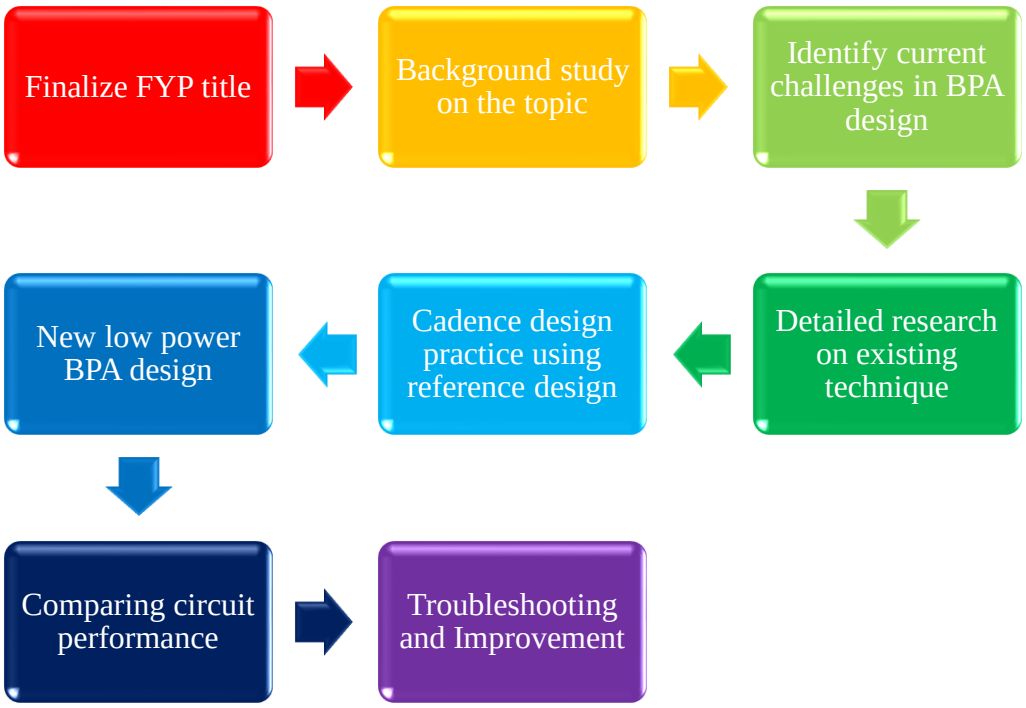


Figure 7: Flow of Research Methodology

Since this topic is relatively new to us, a comprehensive literature review at the early stage of the research works helps us to understand better on performance issues of low power BPA. As we are using 0.35um fabrication process for designing, we can utilize technique that require higher V_{cc}. However, this will come at a price of increase power consumption in some cases as finer process have lower V_{cc} but at the same time,

smaller voltage headroom. After the proposed BPA is completed, various performance evaluation focusing on power consumption and noise level are carried out with reference to existing BPA designs.

7.2. Project Activities

In order for better organization of research work, all the activities are categorized into 3 main stages which are Early Research Study, Design Implementation and Design Improvement. FYP1 basically concentrates much more on Early Research Study and the first few of basic design implementation. In FYP2, we concentrate much more on Design Implementation and Design Improvement phase activities such as implementation of low power BPA and performance evaluation with reference to existing BPA.

7.2.1. Early Research Study

In early research study, we mainly focus on literature review on various kinds current existing of BPA designs. The scope of the literature review move from reviewing general topology of BPA circuit into major challenges of current BPA design in the later stage. The scope of study is then narrowed down to overcoming part of the challenges identified. The literature review will then go on to find out existing strategies to overcome these challenges such as power line interference. From time to time, the author continue to discussion with supervisor for more insights and suggestions for the project. The whole Early Research Study phase is expected to be completed within FYP1 duration.

7.2.2. Design Implementation

This design implementation phase will cover FYP1 and FYP2. It includes implementation of a reference design from literature review as well as implementation of proposed BPA design in the second half of its duration.

- Reference Design Implementation

In the first half of the duration, suitable reference design will be identified through detailed literature review before we try to implement through Cadence. Some of the particularly interesting topologies for BPA such as chopper-stabilizing and auto-zeroing BPA may be good candidates of reference design implementation. Also, it is preferred to use reference design with around 0.35um fabrication process which is similar to the fabrication process that we are planning to use. Different fabrication process allow different V_{cc}. This affects the suitability of the design to be implemented in our targeted fabrication process.

- Proposed Low Power BPA Implementation

  This phase includes re-designing the BPA in order to bring down power consumption wherever it is possible. In short, we will propose a method to improve on the circuit performance of BPA with low power.

7.2.3. Design Improvement

In design improvement phase, we will fine-tune and modify the proposed BPA structure in order to improve the overall performance as seen in figure 8.

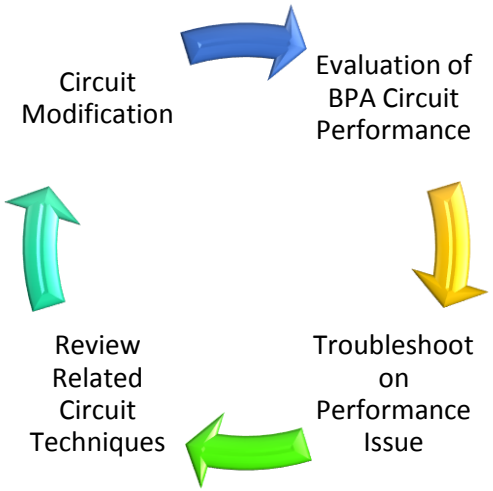
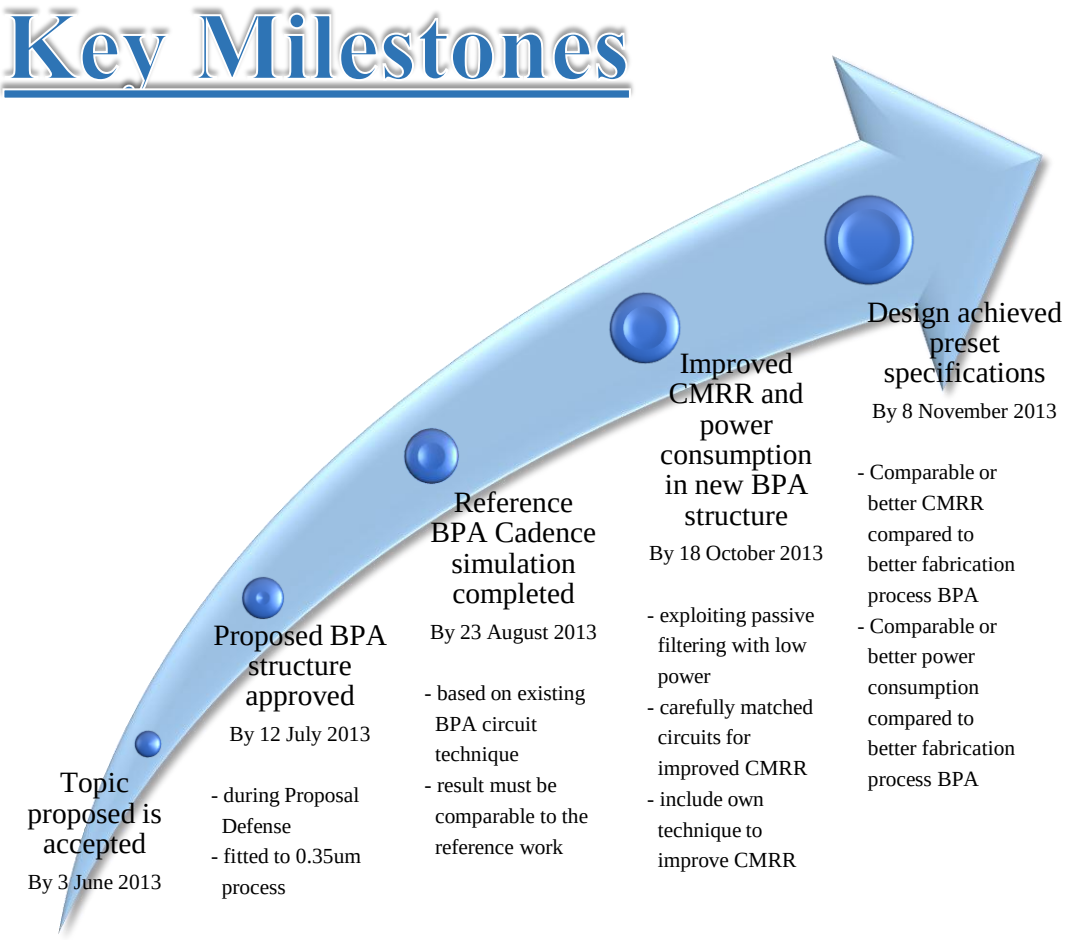


Figure 8: Cyclic Process for Design Improvement

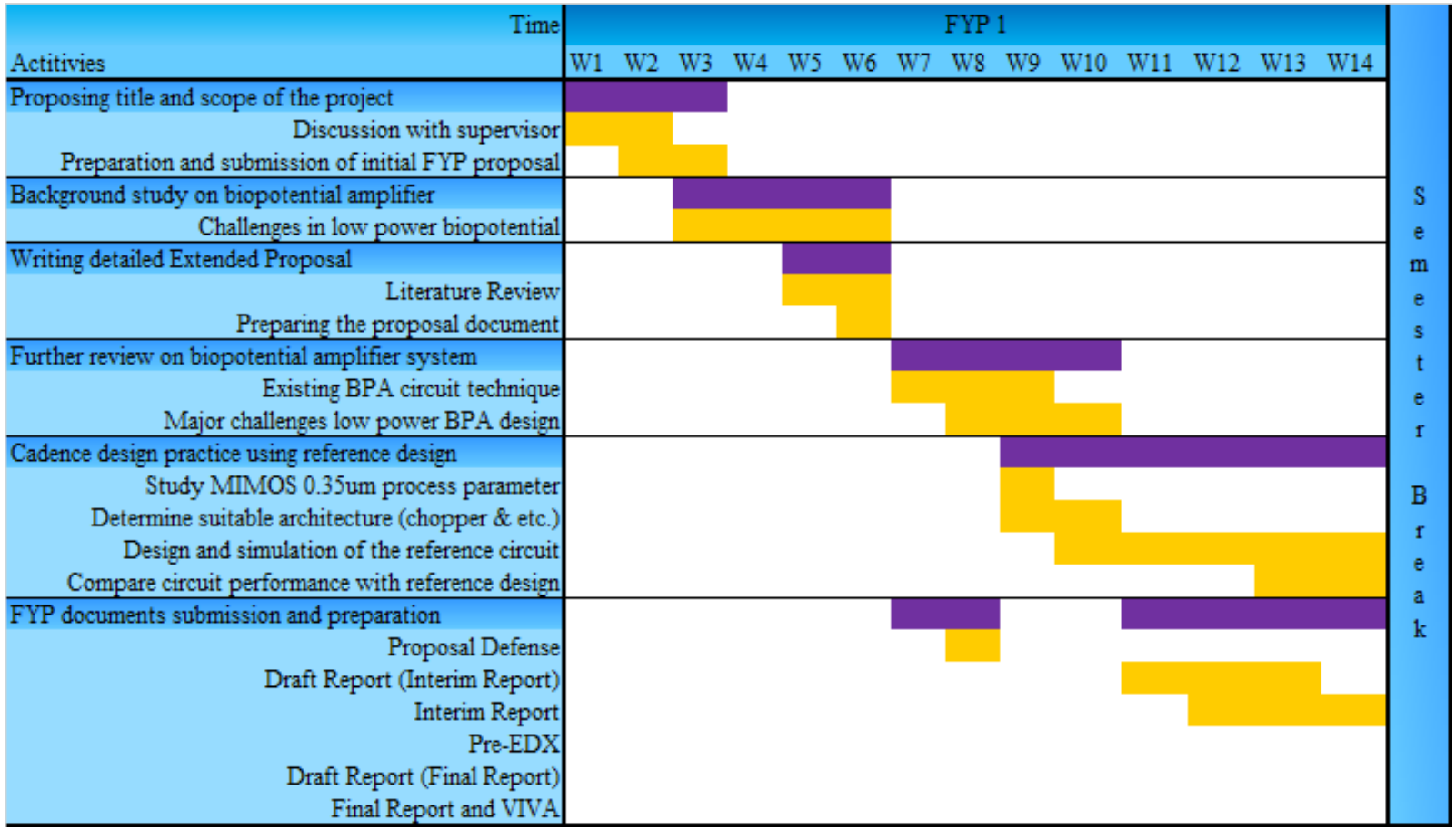
Proper documentation of results and techniques will be done in parallel with the process of design improvement. At the same time, the results obtained will constantly

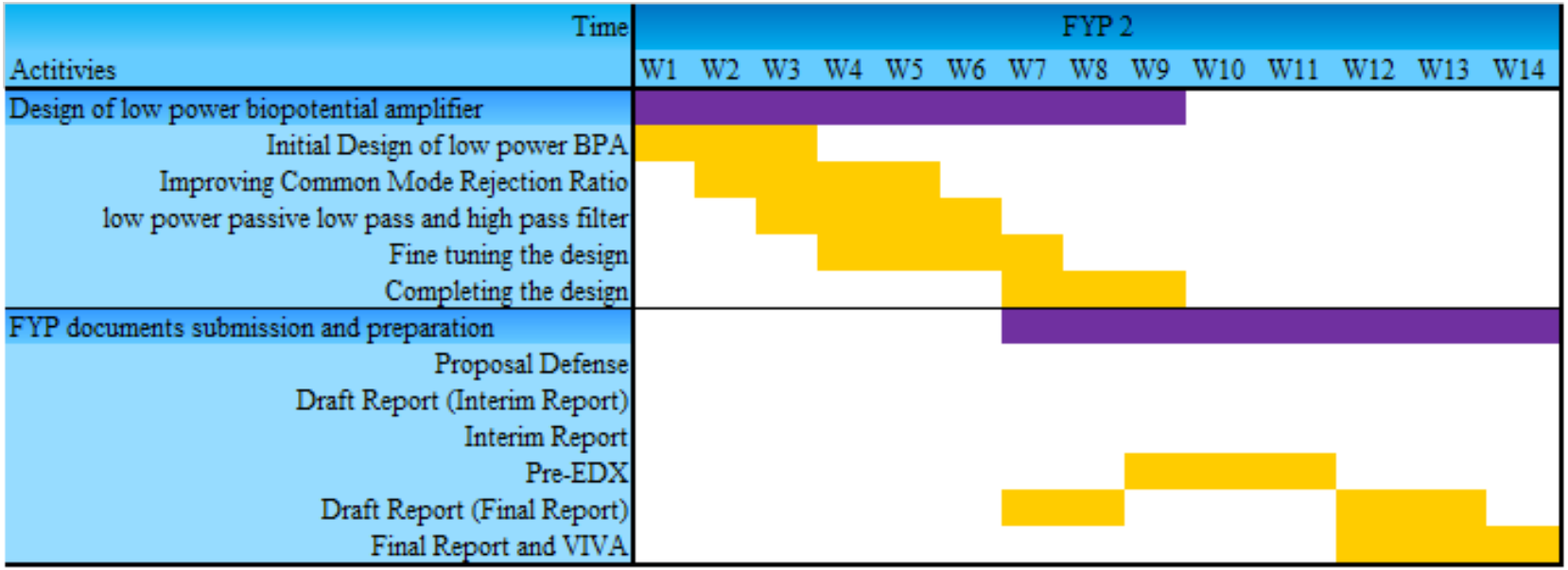
be reviewed with supervisor for further improvement and necessary modification will be carried out.

8. Key Milestone



9. Gantt Chart




Time
Actitivies
FYP 2
W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14
Design of low power biopotential amplifier
Initial Design of low power BPA
Improving Common Mode Rejection Ratio
low power passive low pass and high pass filter
Fine tuning the design
Completing the design
FYP documents submission and preparation
Proposal Defense
Draft Report (Interim Report)
Interim Report
Pre-EDX
Draft Report (Final Report)
Final Report and VIVA

10. Initial Design Iteration: Pseudo-Differential Biopotential Amplifier

10.1. BPA Architecture Design Considerations

After reviewing through different technique for flicker noise cancelation for BPA, chopper stabilization is more favorable as flicker noise can be reduced while preserving the white noise floor. The Figure 9 below shows the proposed BPA architecture that will be used in this FYP. State-of-the-art BPA techniques allows cancelation of motion artifacts via multiple op-amp configuration. However, as power consumption is an issue in our design, we resolve to a more passive motion artifacts reduction method. As smaller half-cell potential electrode has smaller motion artifacts, AgCl electrode which has half-cell potential of 0.223V become a viable solution. The Table 2 below shows the half-cell potential of various electrodes. Figure 10 shows the impedance model of electrode.

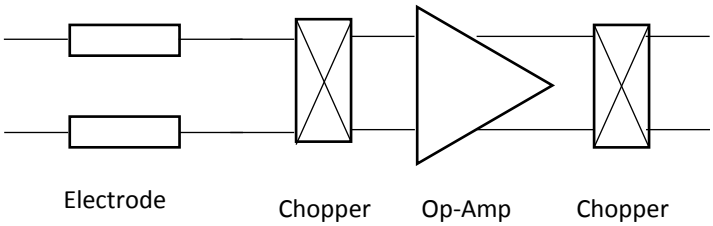


Figure 9: Proposed Architecture for BPA

Metal and Reaction	Half-cell potential, V
$Al \rightarrow Al^{3+} + 3e^-$	-1.706
$Ni \rightarrow Ni^{2+} + 2e^-$	-0.230
$H2 \rightarrow 2H^+ + 2e^-$	0.000 (by definition)
$Ag + Cl^- \rightarrow AgCl + e^-$	+0.223
$Ag \rightarrow Ag^+ + e^-$	+0.799
$Au \rightarrow Au^+ + e^-$	+1.680

Table 2: Half-cell Potential for Different Electrodes[1]

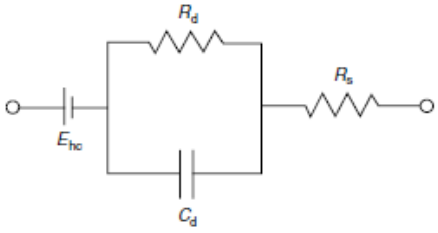


Figure 10: Equivalent Model for Electrode[1]

In term of choice of operational amplifier, telescopic cascode amplifier is chosen as it consume less power for the same amount of gain. In fact, both folded cascode architecture and telescopic architecture is interesting for the design. The Figure 11 below shows the structure of a folded cascode amplifier and telescopic cascode amplifier.

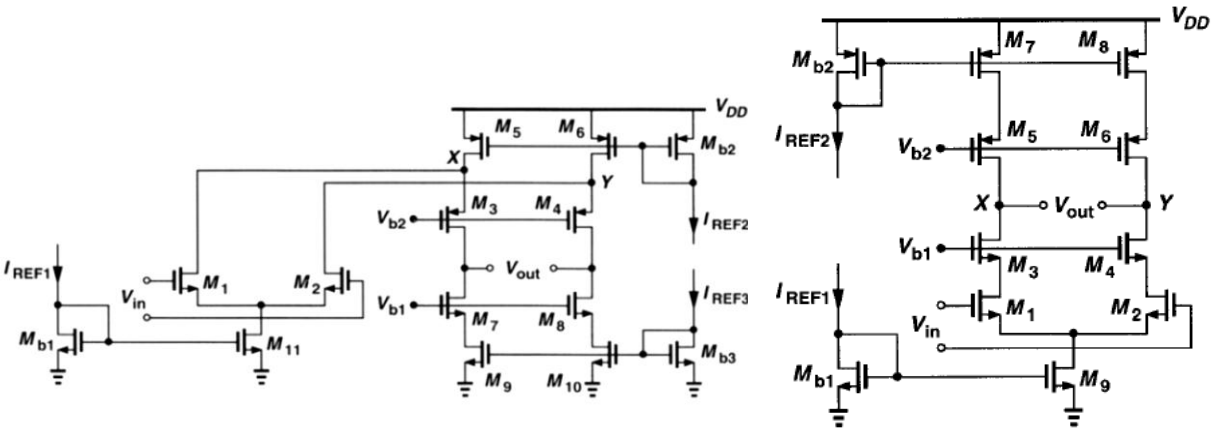


Figure 11: Folded Cascode Structure (left) and Telescopic Cascode Structure (right)

Folded cascode structure offers high output swing as well as low minimum V_{cm} requirement for the input signal. However, similar specification folded cascode amplifier will require two times the current, hence power consumption, if compared to telescopic cascode amplifier. Although a telescopic amplifier limits the available output swing as well as requires higher minimum V_{cm} of around 1.4V, it is more favorable considering 1.8-3.3V supply voltage of 0.35um process allows a lot of voltage headroom for our application.

10.2. BPA Specifications

Using the reference circuit in figure 12 below, we start to design our telescopic cascode amplifier which is the core of the proposed BPA. The telescopic cascode amplifier is designed to meet the system specification of the whole chopper stabilized BPA. The desired specification of the proposed BPA is shown in the table 3. The proposed design

utilizes supply voltage of 1.8V instead of 3.3V as it will still provide enough headroom to accommodate the output swing if the telescopic cascode amplifier is design properly.

Specification	Value	Units/Comments
Supply Voltage	1.8	V
Supply Current	<500	nA
Gain	>40	dB
Noise	<1	uV/sqrt(Hz) at noise floor (0.5Hz to 150Hz)
Output Capacitance	300	fF

Table 3, Key Specification for the Proposed BPA

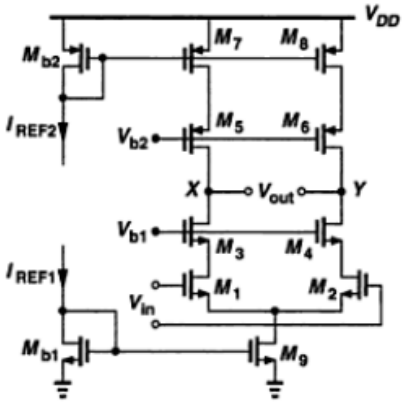


Figure 12: Reference Telescopic Cascode Op-Amp Structure[11]

10.3. MIMOS 0.35um Process Characteristics and Parameter Calculations

As we have just received the 0.35um process technology files, there are a few parameters that need to be calculated in order to facilitate the design of the proposed BPA. The parameters are given in term of BSIM3v3 model, and hence, typical design parameter such as kp and kn needs to be extracted. In order to calculate *kp* and *kn*,

$k_n = 0.5\mu_n C_{ox}$ $\quad\quad$ $C_{ox} = \frac{E_o E_r}{T_{ox}}$

Since *Eo*=8.85E-18 F/um and *Er*=3.97, while *Tox* in MIMOS 0.35um is 7E-9m and u_{no}=313.5 cm^2/V/sec

$$C_{ox} = \frac{(8.85 \times 10^{-12})(3.97)}{7 \times 10^{-9}}$$

$$C_{ox} = 0.005019\ F/m^2$$

$C_{ox} = 5.019 \times 10^{-15}\ F/\mu m^2$

For NMOS,

$k_n = 0.5 \times 0.03135 \times 0.005019$

$k_n = 7.868 \times 10^{-5}\ A/V^2$

$k_n = 78.68\ \mu A/V^2$

For PMOS, u_{po}=180.8 cm^2/V/sec

$k_n = 0.5 \times 0.01808 \times 0.005019$

$k_n = 4.537 \times 10^{-5}\ A/V^2$

$k_n = 45.37\ \mu A/V^2$

In term of channel length modulation effect, it will require simulation with Cadence to find out the *lamda* as it channel length modulation effect is modeled as early voltage. For MOSFET in this particular process, the minimum channel length is 0.35um while maximum is 20um. NMOS also has minimum width of 0.4um and maximum width of 20um. Hence, the available *W/L* ratio for single transistor can varies from 1/50 to 400/7. *W/L* ratio out of this range can be implemented by connecting multiple MOSFET in parallel.

10.4. Proposed Circuit

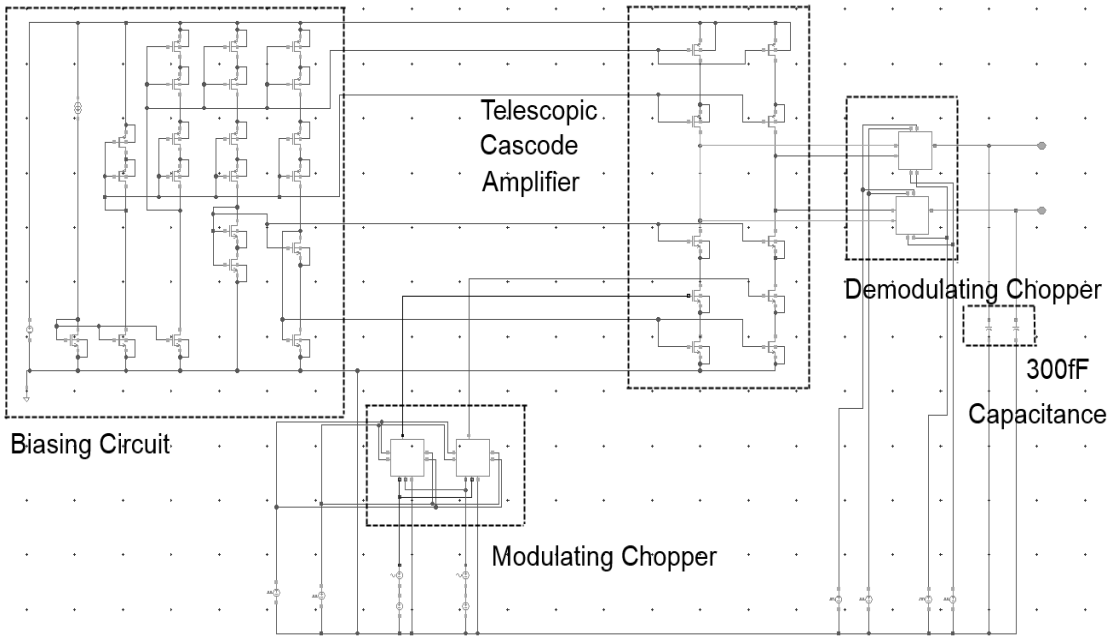


Figure 13, Proposed BPA Circuit

The figure 13 above shows the complete design for the proposed BPA circuit. It consists of modulating chopper, demodulating chopper and a telescopic cascode amplifier.

10.4.1. Telescopic Cascode Amplifier

Both PMOS and NMOS is utilized to design the telescopic cascode amplifier. These mosfets are sized to have V_{DSsat} of around 100mV at 200nA I_{DS} current. This allows around 1.3V of output swing in the telescopic amplifier. As PMOS nor NMOS follow CMOS square law in the equation below in low I_{DS} situation, DC sweep is utilized to properly select the size of PMOS and NMOS.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(VGS - Vth)^2$$

The required bias voltages can be calculated with the knowledge of V_{thn} and V_{thp}. The bias voltages in this work are described in the equations below.

$$V_{b1} = V_{DD} - |V_{thp}| - V_{ov}$$

$$V_{b2} = V_{DD} - |V_{thp}| - 2V_{ov}$$

$$V_{b3} = V_{thn} + 3V_{ov}$$

$$V_{b4} = V_{thn} + V_{ov}$$

$$V_{cm} \approx V_{thn} + 2V_{ov}$$

In this design, V_{b1}≈1.1V, V_{b2}≈1.0V, V_{b3}≈0.7V and V_{b4}≈0.5V while the common mode input voltage V_{cm} is around 0.569V due to transistor sizing. Similar W/L ratio and V_{DS} at I_{DS} of 200nA while tuning the gain to desired specification. Figure 14 illustrates the design and transistor sizing for the telescopic cascode amplifier.

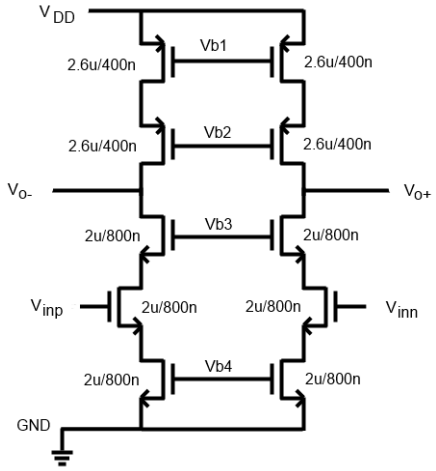


Figure 14, Telescopic Cascode Amplifier Transistor Sizing

In order to reduce power consumption, each transistor in the biasing circuit has I_{DS} of 10nA and has its sizing fitted to V_{DS} of 100mV. The whole biasing circuit thus consume about 50nA current. In order to consume two times more overdrive voltage, channel length of transistors M3 and M4 are four times longer as compared to transistors M6 and M7 based on the equation below.

$$\frac{W}{L} \propto \frac{1}{(V_{ov})^2}$$

Transistors M11 and M12 is sized to provide Vb3 of around 0.7V. Transistor M17 is scaled to consume 2 V_{ov} to tune V_{b4} to be around 0.5V. Figure 15 illustrates the detailed design of the biasing circuit.

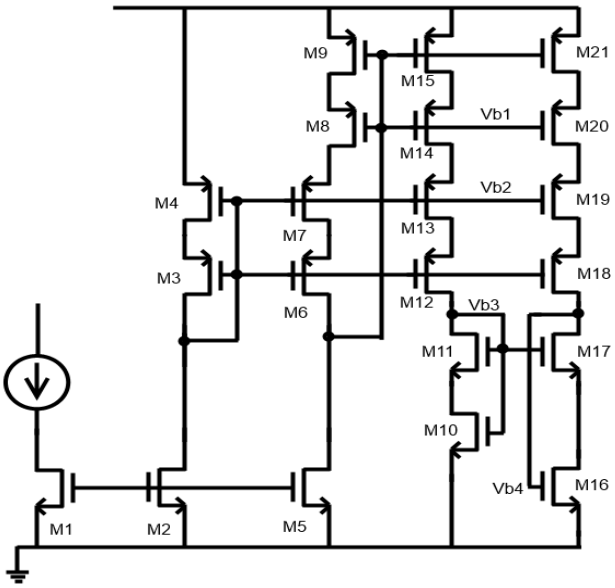


Figure 15, Biasing Circuit

Transistors	Width	Length
M1, M2, M5	800nm	4um
M3, M4	400nm	16um
M6, M7, M8, M9, M12, M13, M14, M15, M18, M19, M20, M21	400nm	4um
M10, M11	400nm	12um
M16	800nm	4um
M17	800nm	16um

Table 4, Transistor Size for Biasing Circuit

10.4.2. Chopping Switch Design

Modulating chopper switches pair in the design consist of a pair of NMOS switches with dummies for charge injection compensation. These switches are driven by 3V complementary clock signals. On the other hand, complementary CMOS switches structure is implemented as demodulating chopper switches in the design. Non-overlapping clock signals at 4V are used to drive the demodulating chopper switches. Sufficiently large W/L ratio is used for both transistor switches to reduce the ON-resistance. The figure 16 and figure 17 below show both the dummy switches and the complementary switch.

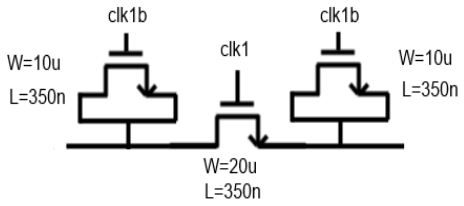


Figure 16, NMOS Switch with Dummies for Charge Injection Compensation

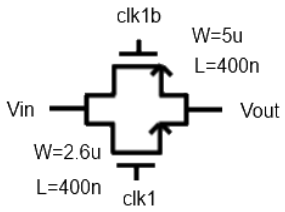


Figure 17, Complementary CMOS Switch for Charge Injection Compensation

11. Initial Design Iteration: Result & Discussion

11.1. Telescopic Cascode Amplifier

The proposed BPA is designed based on MIMOS 0.35um CMOS process and simulated using Cadence Virtuoso. Low power consumption of 0.81uW with gain of around 44dB is achieved in this design. The proposed BPA has noise floor of 314nV/sqrt(Hz) with an input signal of 300uV at 150Hz with distortion at around input signal as shown in figure 18, resulting noise level of 576nV/sqrt(Hz) around the input signal. The table 5 below summarizes the planned specification of the proposed circuit and the actual performance achieved.

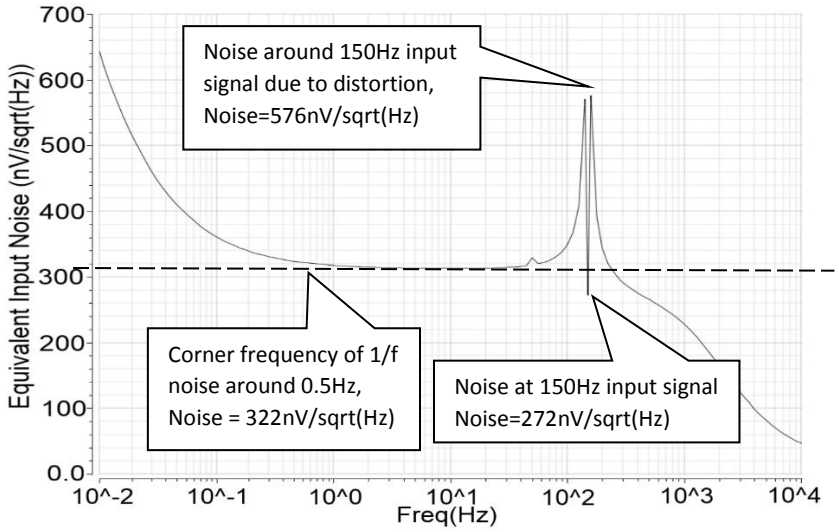


Figure 18, Noise Profile of the Proposed BPA with chopping frequency at 5kHz (input signal of 300uV at 150Hz)

Specification	**Design Specification**	**Performance Achieved**	**Units/ Comments**
Supply Voltage	1.8	1.8	V
Supply Current	<500	450	nA
Gain	>40	44	dB
Noise	<1	0.314	uV/sqrt(Hz)
Output Capacitance	300	300	fF
-3dB point	>150	1300	Hz

Table 5, Expected Specification & Actual Performance of Proposed BPA

11.2. Non-overlapping Clock for Demodulation Chopping

Overlapping clock in demodulation chopper switches results in temporary short circuit between two positive and negative output node of telescopic cascode amplifier. This creates greater chopping spike and requires larger current to drive the same 300fF of capacitance. By having non-overlapping chopping clock, temporary short circuit is avoided. This results in much smaller chopping artifacts. Figure 19 to figure 20 below show the difference between the two chopping clock schemes for demodulation chopping.

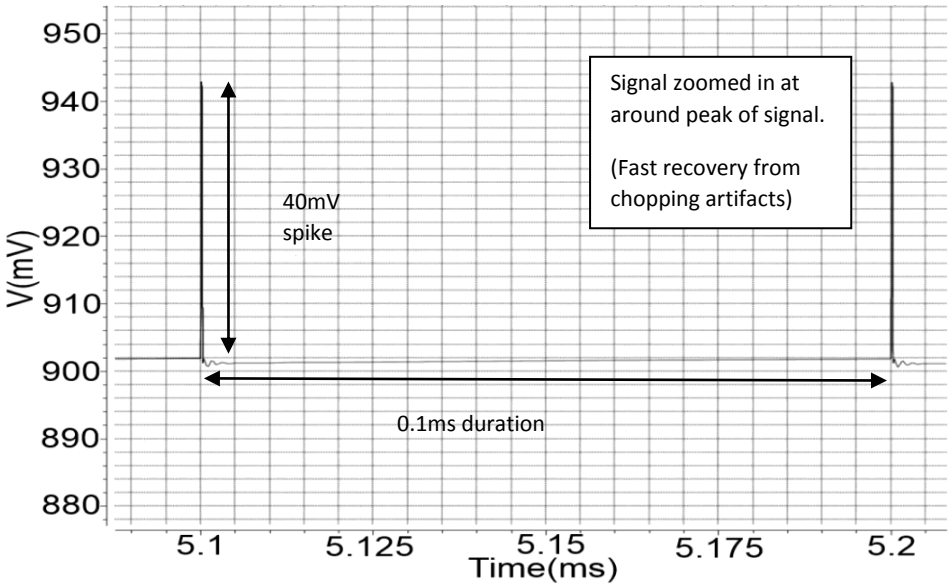


Figure 19, Zoom In on Chopping Artifacts with Non-overlapping Clock

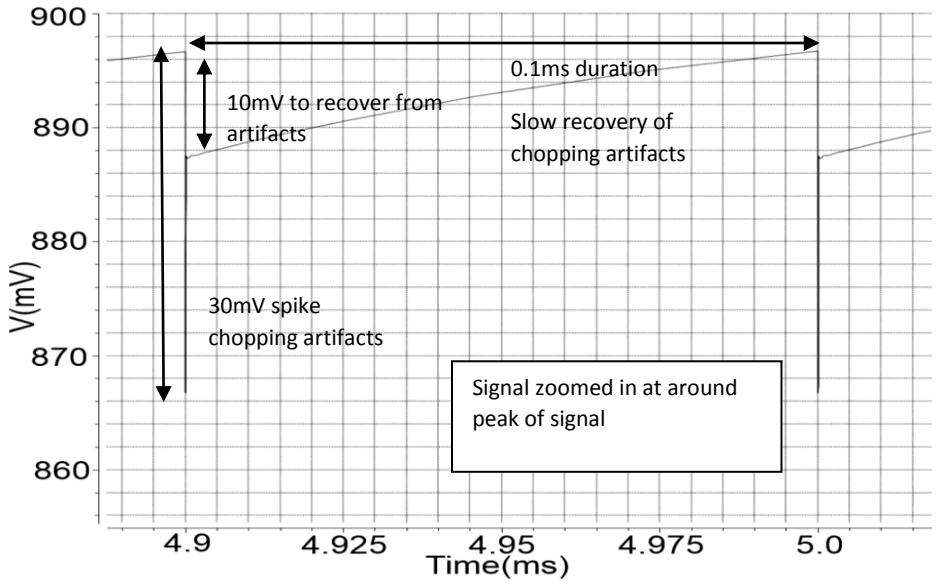


Figure 20, Zoom In on Chopping Artifacts without Non-overlapping Clock

V_{outp} and V_{outn} is shorted during the brief overlapping period if the demodulation chopping clock is overlapping. This charges load capacitance to the output common mode voltage, V_{cmo}. Hence, more current is need to recover from V_{cmo} in every chopping cycle, limiting the performance and power consumption requirement of BPA. It is clearly shown that non-overlapping demodulation chopping is superior in suppressing chopping artifacts in figure 19 and 20. The sharp spikes occur when the load capacitance

is floating for a brief period of both switches turning off in non-overlapping chopping. The capacitor is not charged nor discharged during this time. Hence, the output can be easily smoothened out using a lowpass filter to filter out the chopping spike.

12. Final Design Iteration: Fully Differential Biopotential Amplifier

In order to further improve the performance of the proposed BPA, we came out with a final design iteration. The final design iteration aims to solve several issues listed below.

- Reduces distortion around signals frequencies by improving drivability.
- Implement fully differential input to accommodate wide common mode input voltage swing.
- Further minimize chopping artifacts for better signal quality.
- Further driving down the noise floor of the BPA.

12.1. Design Architecture Consideration

In this final iteration, folded cascode amplifier is implemented as the amplifier core instead of telescopic amplifier due to its ability to accommodate common mode input voltage, $V_{cm,in}$, at 0V. This is particularly beneficial in order to increase the robustness of the design to use with different electrodes that have different half-cell potential. In term of chopper placement, settling time constant requirement can be relaxed by employing chopping at low-impedance node. Less current is needed to charge parasitic capacitance and hence reducing the power consumption needed. The implementation of low-impedance node chopping together with non-overlapping demodulation chopping further reduces chopping artifacts for better signal quality.

In order to improve drivability of the proposed BPA, transistors M3 and M7 is sized to have large transconductance, g_m. This is achieved by lowering down the $V_{DS,sat}$ of M3 and M7 to 50mV. As the drivability of the proposed BPA is increased, the

distortion around signal frequencies is reduced. The equation below shows the open loop gain of the folded casocde amplifier.

$$|A_v| \approx g_{m1}\{[(g_{m3} + g_{mb3})r_{o3}(r_{o1}||r_{o5})]||[(g_{m7} + g_{mb7})r_{o7}r_{o9}]\}$$

where g_m is the transconductance while r_o is the intrinsic resistance of the transistor

Transistors sizing are also carefully matched in order to optimize noise performance. As reported before, flicker noise is the dominant noise source in the EEG signal range. The equation below shows that the flicker noise is affected by the sizing of the transistor.

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot g_m \cdot \frac{1}{f}$$

However, thermal noise does affect the noise level in the amplifier. The thermal current noise is governed by $\overline{I_n^2} = 4kT\gamma g_m$, where the current noise exists as the current passing through drain and source. In term of input referred thermal noise, $\overline{V_n^2} \propto \frac{1}{g_m}$. By taking these noise source into consideration, the transistor is optimally sized to improve noise performance.

12.2. Proposed Circuit Design

Figure 21 below shows the proposed biasing circuit for the customized amplifier core. The biasing circuit has four linear series transistor to set vb2 and vb3 at desired bias voltage. This topology is beneficial as it requires less current pole to achieve similar biasing. Each current pole consumes about 50nA of current, leading to a total of 0.36uW of power allocation for the biasing circuit with 1.8V supply voltage.

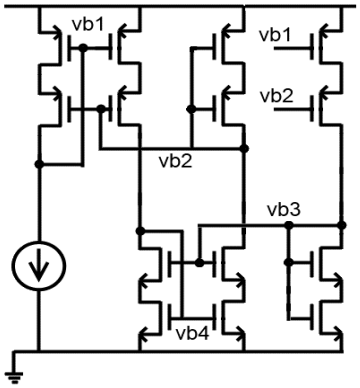


Figure 21, Biasing Circuit for the Proposed BPA

As reported before, folded cascode amplifier topology is utilized to design a customized amplifier core for low-impedance chopping and increased drivability. The proposed customized amplifier core have large Gm for smaller chopping artifacts. Low Z node chopping reduces current requirement for similar amount of artifacts tolerance. Non-overlapping demodulation chopping is also implemented to reduce chopping artifacts. Figure 22 below shows the customized amplifier core with the low-impedance demodulation chopping switches. Each current pole has 200nA in this customized amplifier core, making up a total of 800nA current consumption or 1.44uW power consumption with 1.8V supply voltage.

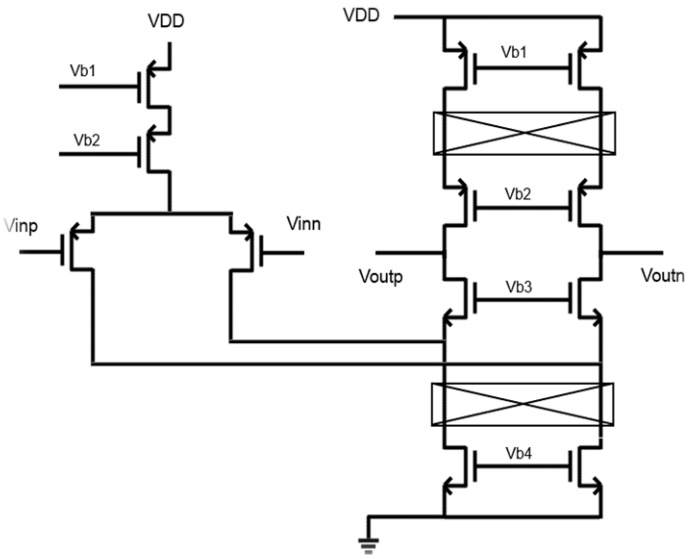


Figure 22, Customized amplifier core with low-impedance node chopping

13. Final Design Iteration: Result and Discussion

The proposed circuit is designed based on MIMOS 0.35um CMOS process and simulated using Cadence Virtuoso. The proposed circuit achieves low power consumption of 1.8uW with gain of around 60dB. Cadence PSS and PNoise analysis of the proposed BPA show noise floor of around 70nV/sqrt(Hz) with an input signal of 300uV at 150Hz. The noise around input signal due to distortion is minimized compared to the previous design. The corner frequency of the proposed design is around 10Hz. The figure 23 below shows the noise performance of the proposed circuit.

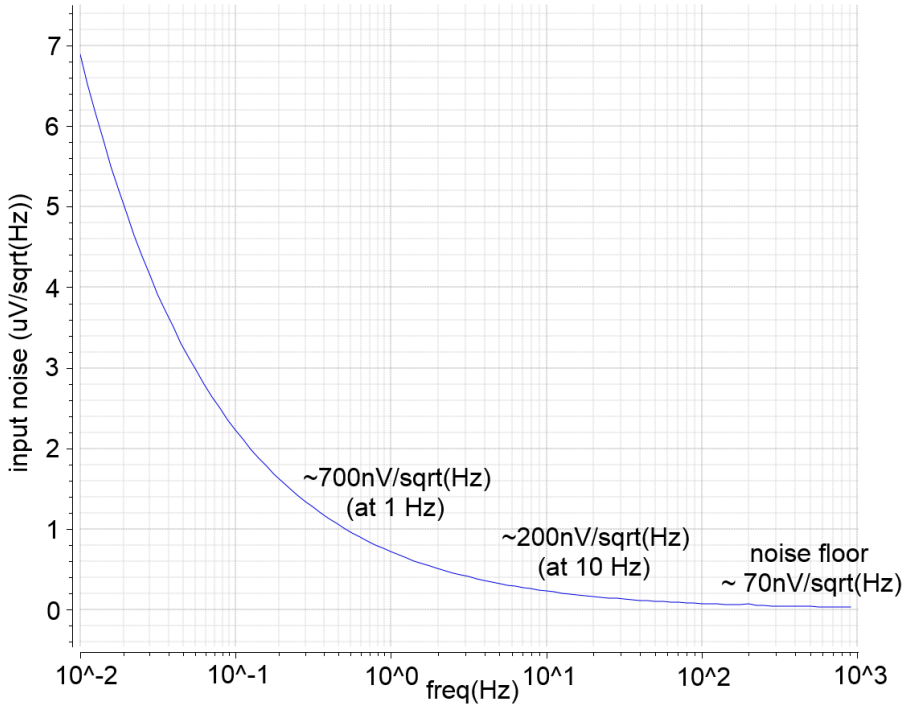


Figure 23, Noise performance of the proposed BPA

14. Conclusion

This FYP proposed a chopper-stabilized low power front-end BPA for portable EEG application. Chopper-stabilization helps in minimizing flicker noise in the BPA. Chopping artifacts is reduced by utilizing non-overlapping clock in demodulation chopping. The proposed design is simulated using Cadence Virtuoso with MIMOS

0.35um fabrication technology. In the initial iteration, much lower power consumption of 0.81uW is achieved in this design with noise performance of 314nV/sqrt(Hz). The final iteration of the BPA design tradeoff some power consumption to improve noise performance as well as increase the design robustness towards V_{cm} swing. The final iteration achieves low power consumption of 1.8uW with noise floor of around 70nV/sqrt(Hz) and corner frequency of 10Hz. Both the noise performance and power consumption is improved through the study of this FYP.

15. Future work

In this FYP, an ultra-low power front-end BPA for portable EEG application has been designed. This work is implemented with Cadence Virtuoso simulation in MIMOS 0.35um AMS process and has achieved around 60dB gain, noise level of 70nV/sqrt(Hz) with power consumption of around 1.8uW. This work has been focusing on open-loop system with the initial intention of reducing power consumption. However, the lack of gain feedback limits the design freedom to further lower down flicker noise of the proposed BPA. It is known that by increasing the length of the MOSFET, the flicker noise can be reduced. However, large MOSFET length will increase the r_o of the MOSFET and the gain of amplifier, leading to output saturation if gain feedback is not being implemented. Flicker noise of MOSFET transistor M3 and M7 is identified as the main source of flicker noise in the system due to low-impedance node chopping. Hence, future FYPs should focus on implementing capacitive feedback to accurately control the gain as well as enable more vigorous low noise design.

16. Reference

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