DEVELOPING A MOTOROLA 68000 TRAINING BOARD

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
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Universiti Teknologi Petronas
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CERTIFICATION OF APPROVAL

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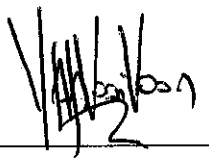
Approved:



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TRONOH, PERAK

June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Ahmad Zhafri bin Ahmad Zahir

ABSTRACT

The aim of this project is to build a Motorola 68000 microprocessor training board using modular approach to aid the teaching and learning process for the microprocessor subject in Universiti Teknologi Petronas (UTP). The board is designed in modular approach to nurture more understanding among the students on the system itself. The final system consists of 3 different separated cards; the central processing unit (CPU) card, the memory card, and a serial/parallel interface card and a backplane. Wire wrapping method is used to build the training board. This project involves circuit design study, parts substitution study, and the board construction itself. Basically, the board features a Motorola 68000 microprocessor, 10-MHz crystal clock, buffer circuits, memory decoder circuits, EPROM modules, SRAM modules, serial interface, and parallel interface. This board can be connected to a personal computer (PC) through serial interface for program downloading purposes, and the output is connected through the parallel interface available on-board. It is envisaged that the final system would be utilized as a learning tool for the microprocessor course (EAB2023).

ACKNOWLEDGEMENTS

Final Report for Final Year Project was produced when the project has come to the end. Throughout this project, numbers of people have contributed in achieving the objectives.

Firstly, the author's heartfelt gratitude is forwarded to the supervisor, Dr. Yap Vooi Voon, for his advice, which guided the author throughout this project.

Author wish to thank all the colleagues Mohd Shah Reza, Rohaizad, Atiqah Farhana, and Adli Shahrul who taught, guided, advised, shared-knowledge, comments and helps throughout the project.

Finally, thank you to all the others whose names has failed to mention on this page, but has in one way or another contributed to the accomplishment of this project.

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LIST OF ABBREVIATIONS

UTP	Universiti Teknologi Petronas
PLD	Programmable Logic Device
IC	Integrated Circuits
EPROM	Erasable Programmable Read Only Memory
ROM	Read Only Memory
PIC	Programmable Integral Controller
BGACK	Bus Grant Acknowledge
BR	Bus Request
SRAM	Static Random Access Memory
RAM	Random Access Memory

CHAPTER 1
INTRODUCTION

1.1 Background Study

The Motorola 68000 is a popular microprocessor and had been in the market since 1980. It had been used in various applications including the earlier personal computers. Although Motorola had stopped the production in 2000, there are various semiconductor companies who reproduce the microprocessor today. Fundamentally, it is a 16-bit microprocessor with 32-bit features. In short, it provides up to 32-bit programming environment to the users.

The 68000 is a suitable microprocessor to be used as a teaching tool. It has a simple and well defined architecture. In addition, it is well supported by text books and software tools.

1.2 Problem Statement

Using a 68000 based microprocessor for learning tool is feasible, given its' popularity and well-defined architecture. Thus, a training board is needed. The whole computer system is placed on the board. They include the clocking part, all buffers, buses, memory modules and interfacing ports.

Currently UTP utilizes the 68000 microprocessor as a teaching aid for the microprocessor course. As mentioned earlier, the aim of this project is to build a training board for the 68000 using the modular approach. This approach is aimed to nurture more understanding among students on the system itself as it is visually separated.

1.3 Objective & Scope of Study

The objective of this project had been covered in earlier sections. This section will continue to examine the scope of study for this project. It is envisage that the scope of the study includes detail study on both hardware and software aspect of the 68000 microprocessor system.

Initial case study was done through reviewing a standard book. The book Microprocessor Systems Design by Alan Clements is the main reference for this activity. Details on designing the system are available in the book. This book provides a clear idea of what the system should have, how it interacts, and how to practically connect and test them. Alan Clements also provides clear explanations on how to build the board using modular approach; to have few cards and connect them with buses.

The board is built by using modular approach rather than having everything on one single board, based on the existing Flight68K-MKII training board. Modular approach is an approach that dividing the Flight68K-MKII into sub-boards or cards. Those cards will then be directly connected using buses placed on a backplane card. The main reason of having this design is to allow the students to access the major components and to test major components independently. It is envisaged that this approach would encourage better understanding among the students of microprocessor system in logical and systematic manner.

In addition it is more feasible to have this setup to ensure fewer defects. Note that the existing Flight68K-MKII circuit design will be used as the main design. This will allow the same firmware to be used in this project. Furthermore, segregated cards help us to trace error faster and precise. For instance, the board is built module by module. Once the CPU card had been completely built, basic functions such as clocking signal, HALT/RESET signal, and the buffer functions could be checked already. Thus, we could be sure that further defects might not likely come from the card.

In terms of time needed to have all the 3 cards built, it may need more or less the same period of time if the system was built on a single board. However time to counter defects predicted to be significantly reduced, as each and every function allows them to be diagnosed independently.

CHAPTER 2
LITERATURE REVIEW

Fundamentally, a computer system is being built in this project. Computer system literally means a system which have several sections and functions, combined together to function as a computer. A basic computer system consists of a central processing unit (CPU) or also known as microprocessor to act as the brain for the whole system. A computer system also features read only memory (ROM) modules to store firmware or basic operating system (OS) in order to get the whole thing run as a system systemically. Then, it also has random access memory (RAM) modules to enable programs and command being stored and executed. Nevertheless, interfacing devices is obviously needed, there comes the input and output (I/O) elements such as serial port, keypad, and LCD displays. All components must be connected accordingly by address bus, data bus, and control bus.

The whole 68000 microprocessor system is built by this basic model;

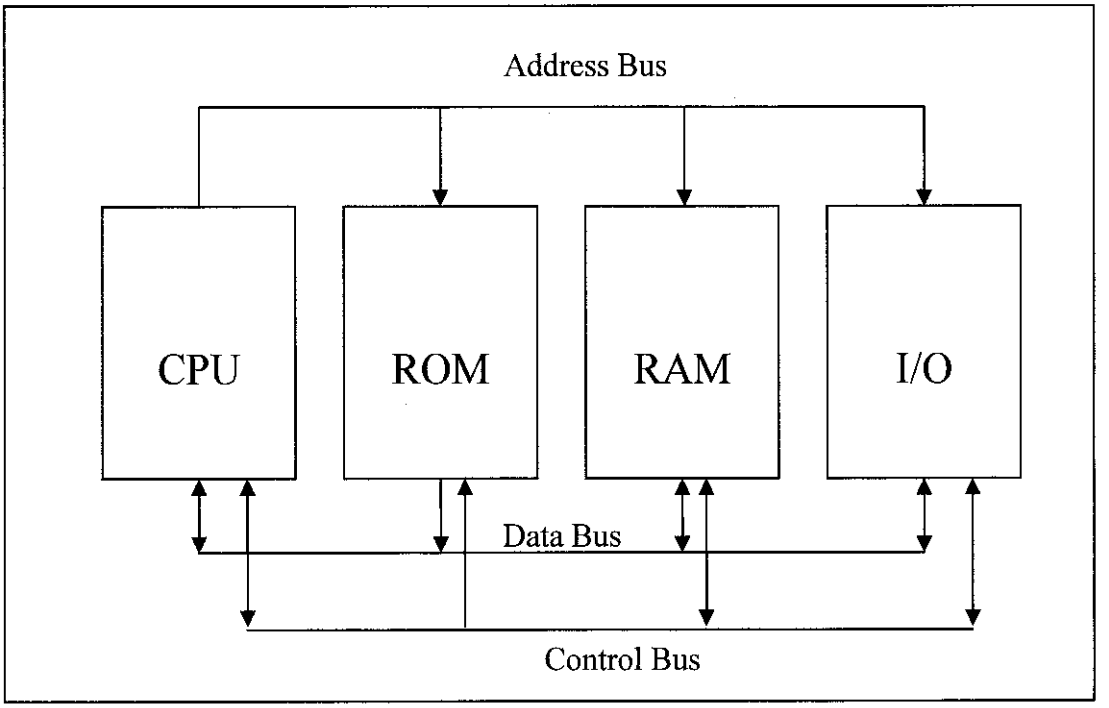

Figure 1 Block Diagram of Basic Microprocessor System.

The CPU is the brain of the system. This is where all arithmetic and logical operation take place. Generally CPU consists of an arithmetic logic unit (ALU) and a control unit. ALU performs arithmetic and logic operations. The control unit extracts instructions from memory, decodes and executes them properly. It may also need to recall ALU whenever appropriate. [1]

ROM component acts as the computer memory. Unlike RAM, ROM is un-erasable and non-volatile, which means it will not lose its contents even if there is no power supply available. ROM is usually used to store. This firmware may also be called as a tiny operating system.

RAM is a type of memory that can be accessed randomly. This means that any byte of memory can be accessed without touching the previous bytes. There are two types of RAM, dynamic and static. They differ in the technology they use to hold data. Dynamic RAM needs to be refreshed thousands of times per second. Static RAM does not need to be refreshed, which makes it faster; but it is also more expensive than dynamic RAM. Both types of RAM are volatile, meaning that they lose their contents when the power is turned off. [2] In this project, SRAM is used.

I/O is used to describe any program, operation or device that transfers data to or from a computer and to or from a peripheral device. Peripheral device includes keypads, LEDs, and etc. In this project, these devices are placed on a PIT board, where all inputs and outputs are coming from and to them.

Address bus contains address lines, data bus contains data lines, and control bus contains control lines. Note that both data and control lines are bi-directional while address line is uni-directional. Bi-directional means that data can be transmitted or received in two way communication.

CHAPTER 3
METHODOLOGY

3.1 Research and Circuit Design

For this project, the Flight68K-MKII training board is used as a main guide. Complete circuit diagram of the board is readily available in the owner's manual.

However, some modifications have to be done. For instance, the Flight68K-MKII boards do not have buffers, while in this project, the board need buffers to enhance the capability of the signals to go throughout the bus system. The idea of having buffers is to enhance the capability of driving more signals on the appropriate pin. In this project, buffer ICs of 74LS244 and 74LS245 is used. Address and control lines are connected directly to the 74LS244 buffers while data lines being connected to the 74LS245 buffers. The buffered output then made available at the bus, to be used by the whole system. [3]

In addition, further modifications were also done on some other part of the board. The memory decoder circuits used in the Flight68K-MKII board utilizes programmable logic device (PLD). [4] The barrier here will be the source code. As the source code is not readily available, it is good to replace the PLDs with logic gates combination setup. This setup will then cultivate better understanding of the circuit, and assists in troubleshooting and analysis tasks.

The next stage is to come out with the circuit diagram itself. As the board consists of 3 separate cards; the CPU card, memory card, and serial/parallel interface card, there are three separate circuit diagram to be designed. EAGLE Layout Editor 4.13 is used to draw all three circuit diagram for the cards. The circuit diagram then being studied and finalized before further process takes place. This is very crucial to ensure minimum problems arise regarding the circuit design itself in future.

3.1.1 CPU Card

In this project, four dual 4-bit tri-state non inverting buffers, 74LS244 and two 8-bit 3-state non inverting bus transceiver buffers, 74LS245 are used. These ICs are connected directly from the 68000 microprocessor and the output will be the buffered version of the input pins. Let say for example, a data line D0 is being connected to pin 18 of one of the 74LS245 IC, the output corresponds to pin 18 will be pin 2, which is the buffered D0.

Address lines and control lines are connected to the 74LS244 buffers while data lines are handled by the 74LS245 buffer. The 74LS244 buffers are enabled by the inverted Bus Grant Acknowledge (BGACK*) signal. BGACK* is pulled up to Vcc by a resistor and the address bus buffers are normally enabled. Whenever any part of the system wants to utilize the system bus, it will asserts Bus Request (BR*), then asserting Bus Grant (BG*) and BGACK*. This will then disabled the buffers and cause them to float, leaving the bus free for new bus master. [3]

Data bus buffers are controlled using the 74LS245. They are enabled by the buffered Read/Write (R/W*) pin. These buffers are enabled only when the 68000 executes a valid bus cycle to non-local memory. [3]

The output of these buffers will then be tapped to the bus, to be connected to the entire system. The circuit diagram for buffer circuitries is shown in Figure 2.

The clock signal is derived from a 10MHz crystal-controlled clock. The clock signal is buffered to enable the signal to be used externally without degrading the signal. The output of this clock is then connected directly to the clock (CLK) pin at the 68000 microprocessor through an inverter. Clocking circuitries is included in the CPU card circuit diagram in Figure 2.

A simple logic circuit to execute reset operation is used. The same circuit could also obtained information on the halt status of the CPU. Also refer Figure 2 for the circuit diagram of the clock and reset circuitries. A full processor reset is applied to the 68000 when both HALT* and RESET* pins are taken to low, either during power-up or when the RESET switch is depressed. In an event of halted microprocessor operation, the active low output from the halt pin of the microprocessor will be inverted and connected to an LED that will light up to indicate that the CPU is halted. [4]

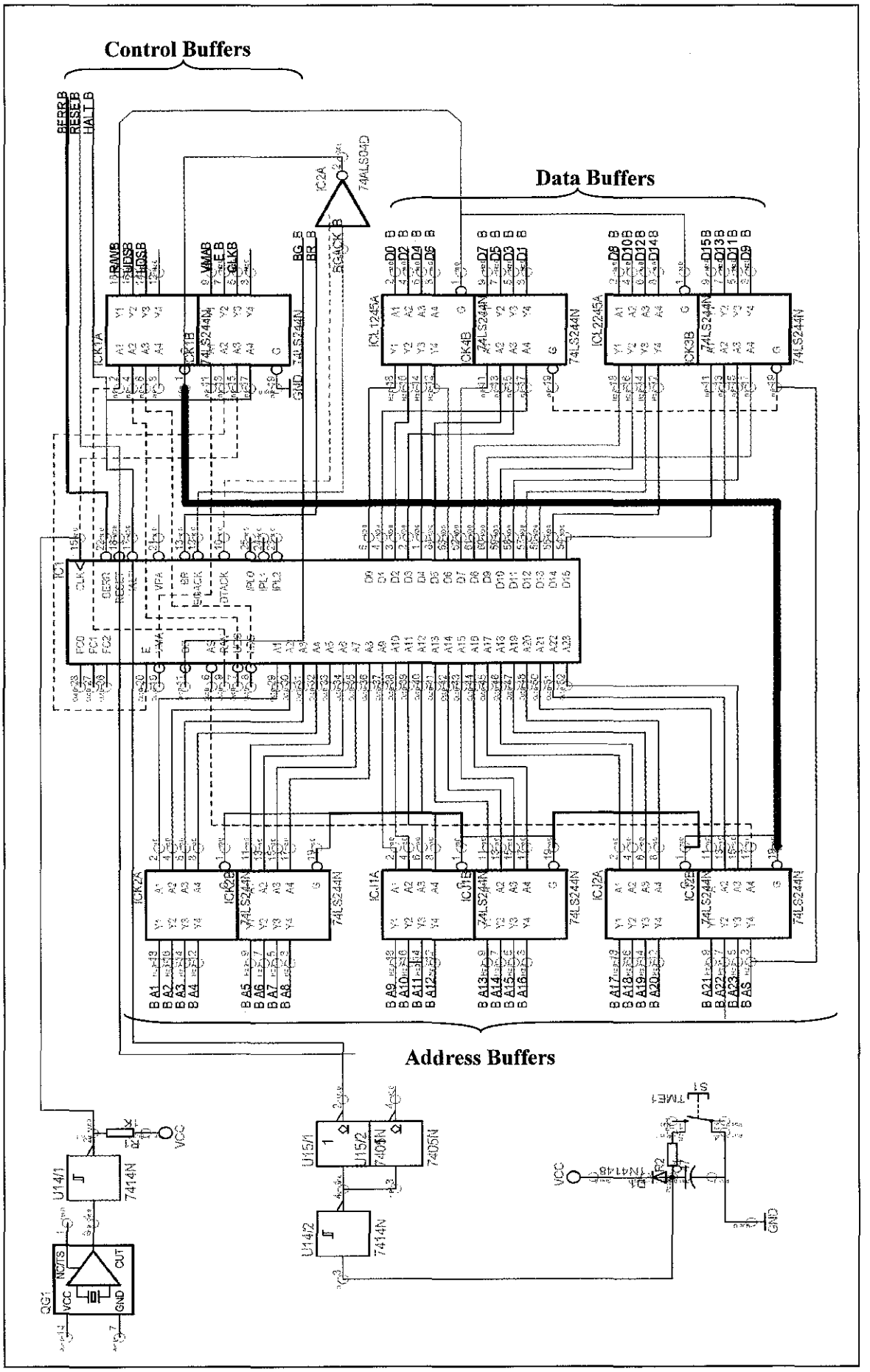

Figure 2 Circuit Diagram of CPU Card.

3.1.2 Memory Card

The EPROMs and RAMs are installed in pairs to provide a 16-bit data bus. The lower byte (D0-D7) is connected to memory device and the higher byte (D8-D15) is connected to another memory device. The address pins of all memories connect directly to the processor buffered address output lines. However, the 68000 has no A0 line, therefore 68000 A1 line goes to the memories A0, followed by A2 to A1, and so on.

Two AM27C512 EPROM with 512KB each is used. Thus a total of 1MB is available for the firmware, which is more than sufficient. The role of EPROM is to store firmware or the tiny operating system for the whole system to work and integrate well. Two memory modules are needed as they handle 8-bits only for each memory module. As we deal with 16-bits system, the first 8-bits is handled by one module while another subsequence 8-bits is handled by another module. These modules are also labeled as HI bytes and LO bytes to indicate which bits they handle.

Two UT6264 SRAM (8K X 8-bits) are used. Random Access Memory (RAM) is needed to store programs and commands and execute them. Again, RAM modules are also being connected in pair, to handle the first 8-bits and the subsequence 8-bits. A simple example, a 16-bits data is being moved from address line A1 to the memory sections. Therefore, the first 8-bit of the A1 data is being fed into the pin 12 of the upper RAM, while the balance 8-bits goes to the pin 12 of the lower RAM.

The Flight68K-MKII board uses PLDs in implementing the decoder part. As in this project, the decoders have to be redesigned to utilize only logic gates. The memory decoder decodes data between the memory modules and the microprocessor. Analysis of memory decoder circuitries could be done by using a logic probe indicates which is accessing which part of the memories. Complete memory decoder circuit diagram is available in Figure 3.

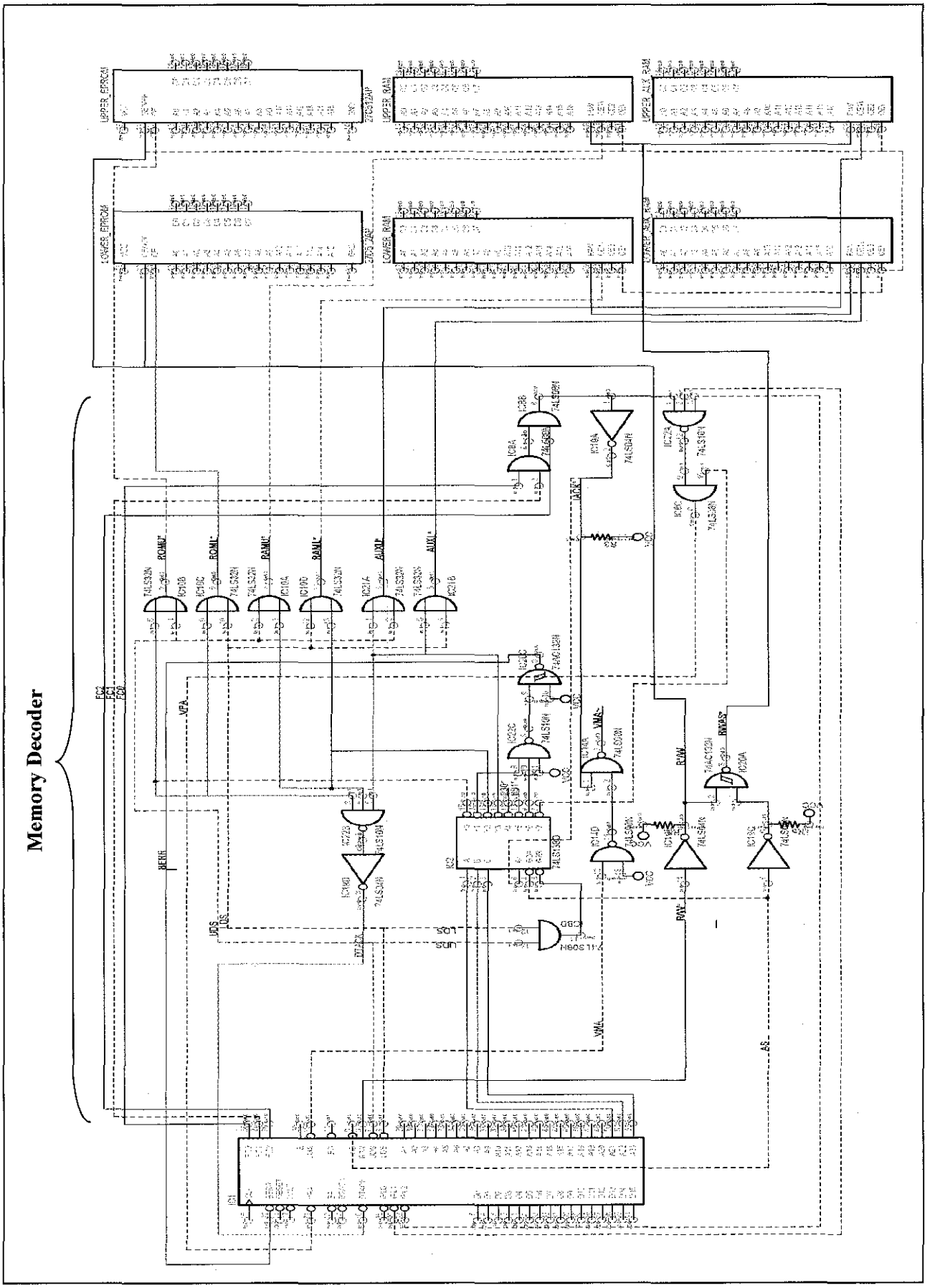

Figure 3 Circuit Diagram of Memory Card.

3.1.3 Serial/Parallel Card

The serial connection functions as a communication channel between the board and a personal computer. This connection is used for program downloading purpose. Referring to Figure 4, the serial connection was made by using a Dual Asynchronous Receiver/Transmitter (DUART), MC68681 chip. MC68681 provides two independent serial ports, a baud rate generator and a number of general purpose I/O pins.

Interfacing the processor with 68681 was made simple since the 68681 is a 68000 family peripheral. It is an 8-bit peripheral, thus only D0-D7 are used, along with the four lowest address lines connected to register select pins RS1-RS4, thus the device occupies 32 bytes of memory space. R/W*, DTACK*, and RESET* lines are connected straight to the appropriate pins on the bus. The same applied to CS* and IACK* pins where the appropriate pins are available on the bus. [4]

The 68681 DUART has an internal baud rate generator which requires a 3.6864MHz crystal clock to be connected between X1 and X2 (pin 32 and 33).

On the peripheral side, there are two each of serial outputs and inputs. The two outputs and inputs for each serial port are buffered by a RS232 quad line driver, DS1488 and a quad line receiver, DS1489. These then connect to external devices via two RS232 serial port connectors, P2 and P3.

The MC68230 Peripheral Interface/Timer (PI/T) is the other 68000 family peripheral. It provides digital I/O interfacing and a programmable timer.

On the peripheral side, there are 28 I/O pins. These are arranged in three ports of eight lines, PA0-PA7, PB0-PB7, PC0-PC7, and four handshake lines, H1-H4. All of these lines, along with 0V and +5V are brought out to 40-way IDC connector plug, SV3 and are all available to the user. Other pins such as R/W*, DTACK*, RESET*, CLK are connected with the respective same pins available on the bus while CS* is connected to 230* available on the bus. See Figure 4. [4]

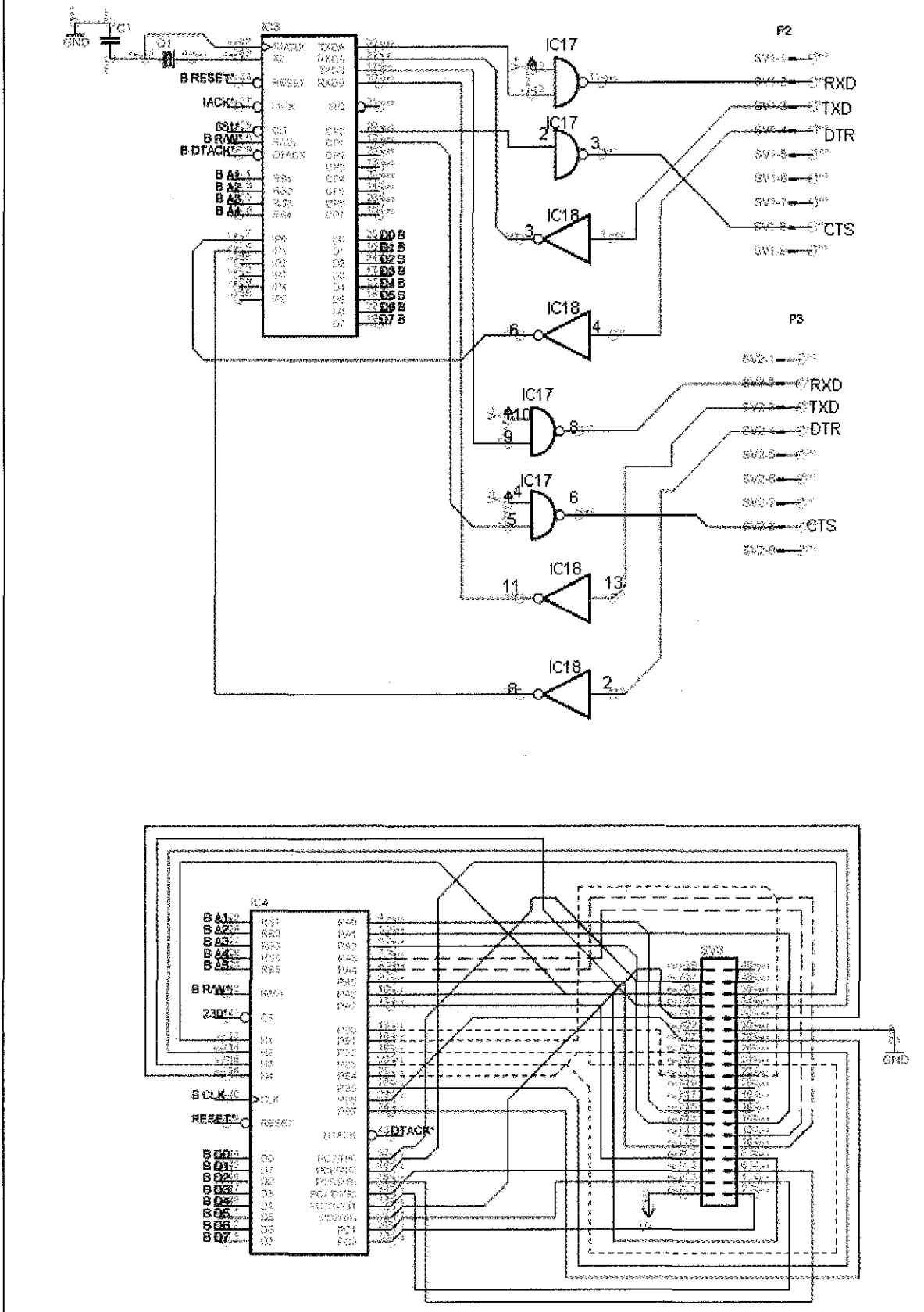

Figure 4 Circuit Diagram of Serial/Parallel Card.

3.2 Sourcing Parts & Components

This is a very initial step of constructing the board. Parts and components being used are listed down carefully. It is important to have all parts and components ready and available to ensure smooth circuit construction process.

3.3 Circuit Construction using Wire Wrapping Method

Circuit construction begins with IC socket being installed and labeled with wire wrap I.D. or masking tape. This provides the convenience of indicating which IC is which and to prevent wiring mistakes. Then, a coupling capacitor of 0.1uF is placed beside the socket. The idea is to get the coupling capacitor to be as closed as possible to the ICs.

Wiring process then begins by tapping wires for Vcc and Ground pins from each and every ICs. Note that all Vcc and Ground pins from each ICs will be individually tapped to the Vcc and Ground points rather than interconnect them with other ICs Vcc and Ground pins. This is crucial to avoid voltage loss in the system.

The rest of the wiring then follows; the CPU card, memory card, serial/parallel interface card, followed by the backplane. Color codes are used in this process. For instance, all Vcc wires are red colored, Ground wires are black colored, all address lines are white colored, data lines are yellow colored, while other control lines are green colored. Color codes provide the convenience in tracing the wire and in the later troubleshooting process.

A precaution practice is utilized after each and every wire wrap session to ensure there were no wiring mistakes happened. Wires may run up until hundreds of connections, which is almost impossible to retrace and fault find one by one later. Thus, continuity check is done after each wire wrapping session, to ensure consistent and accurate wirings are done.

3.4 Testing & Troubleshooting

3.4.1 Supply Voltage

Testing and troubleshooting follows after all connections being done. Vcc and Ground pins are the first points to be checked, even before getting ICs to be onboard. By supplying +5V from a power supply unit to the Vcc and Ground point on the backplane, voltage in each and every socket is measured with a multimeter to ensure every individual ICs obtained the +5V.

A problem of insufficient voltage supply aroused. Voltage available then was around 3.40V only which is not sufficient. It was found to happen due to the usage of alligator clips which connect power supply unit and the Vcc and Ground points. Multi-core wires then being soldered on the points and connected directly to the power supply unit. The voltage available at each and every ICs are found to be 4.95V which is sufficient enough.

Voltage supply is very crucial in this project because digital circuits are being utilized. Sufficient voltage is crucial in determining the appropriate logic levels. For instance, voltage between 4.75V and above will indicates High or Logic 1 while voltage of 2.75V and below indicates Low or Logic 0. Other voltage values between them indicate ambiguity. If then the voltage supply is insufficient and falls under ambiguity region, it is predicted that the system will not work appropriately as all logics had jumbled up.

3.4.2 Clocking Frequency

For this project, a 10-MHz crystal clock is used. An oscilloscope is used to ensure that the system is getting the same and right 10MHz clocking frequency once being powered up. The test points includes the output pin of the crystal clock itself, pin 15 of the 68000 microprocessor which is the clock input pin, pin 15 of buffer IC K1 which is the input clock for the buffer as well as pin 5 on the same IC K1 to see the buffered clocking signal. [5]

Theoretically, all test points must produce exactly the same clocking frequency to ensure every elements of the system synchronize well to each other. Figure below shows the 10MHz signal obtained on the test points.

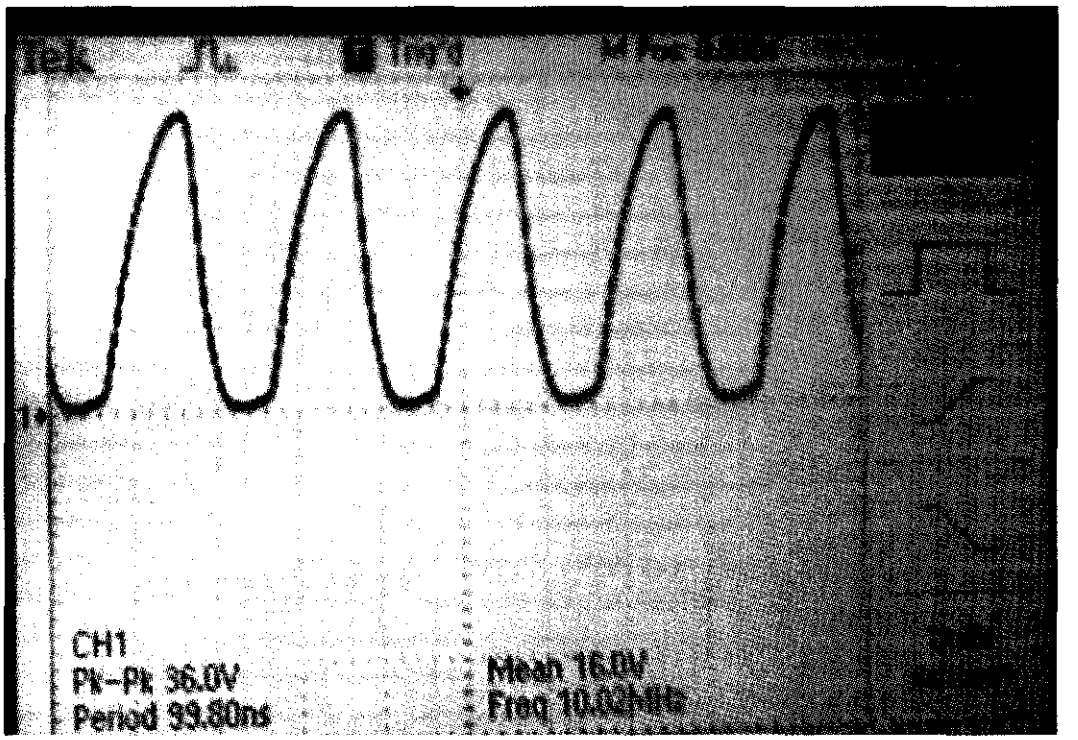

Figure 5 10MHz Clock Signal.

3.4.3 Continuity Tests

As per mentioned before, continuity test is done by using a multimeter. It will be set to measure resistance between two points. We know that an open circuit can also be said to have a very large amount of resistance while a short circuit condition can be said to have zero amount of resistance. Thus, when the resistance between two points is checked and they show almost zero ohms, this indicates that there were connections.

Even though consistent continuity checks was done for each and every time wire wrapping sessions ends, a comprehensive and extensive continuity test then done once again for the whole system once the construction works finished.

3.4.4 Logic Levels

Logic levels can be checked using a logic probe. This is very useful especially when checking the decoder part which comprises of logic gates. Appropriate input logic and its' correspond output logic could be checked using the logic probe.

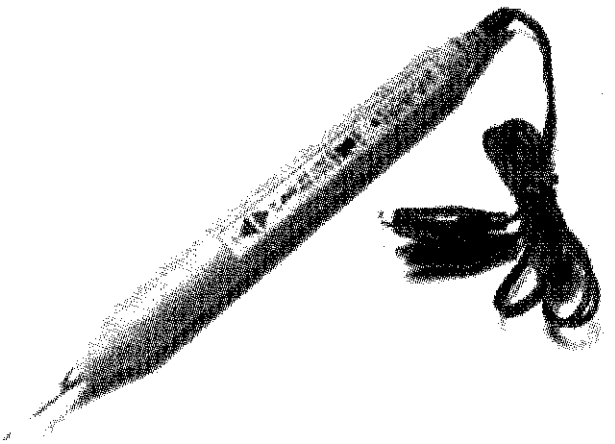

Figure 6 Logic Probe.

3.4.5 Identifying Faulty ICs

A universal programmer kit which comes with hardware to place ICs and software to communicate with ICs is used. Basically this software is used to program an extensive type of devices such as EPROM, Flash ROM, and PIC. However, the software also provide logic ICs and memory ICs test being done.

Another conventional method is by trial and error method. For instance, to ensure that the EPROM programmed is usable, it was substituted in a working training board available in the microprocessor lab. A smooth operation with the newly programmed EPROM modules indicates that they are in good and usable condition. The same goes to the 68000 microprocessor as there were some of them which sourced out from the store were found to be faulty when being used on a working board.

3.4.6 Serial Connection with PC Testing

Serial connection in this project provides communication channel for software downloading and memory reading from the PC and to the training board. Thus, the simplest way of testing the serial connection is to use the Crossware Embedded software used in the microprocessor lab. This software will indicates the output available from the board, as well as enable program compilation and downloading process to the 68000 microprocessor. Alternative software might be the Hyper Terminal software available in Windows.

In this particular project, the first output of the system will be a welcome note. It then allows access to the microprocessor system, whether to download a program, read the memory blocks, etc.

3.4.7 Parallel Connection Testing

Note that the Flight 68K-MKII board comes with a PIT board, where a number of output and input elements such as LEDs, motor, LCD display, and keypad is placed. Parallel connection is used to provide output or input on this board. Therefore, to test the port is to connect the PIT board to the 68000 system board. Write a simple program to light up LEDs, or run the motor, and see if we are able to get appropriate results.

CHAPTER 4

RESULTS & DISCUSSION (SYSTEM DESCRIPTION)

For the scope of this project, three sub-boards are built. They are the CPU card, memory card, and also the interface card. Following explanations will be done on part by part basis.

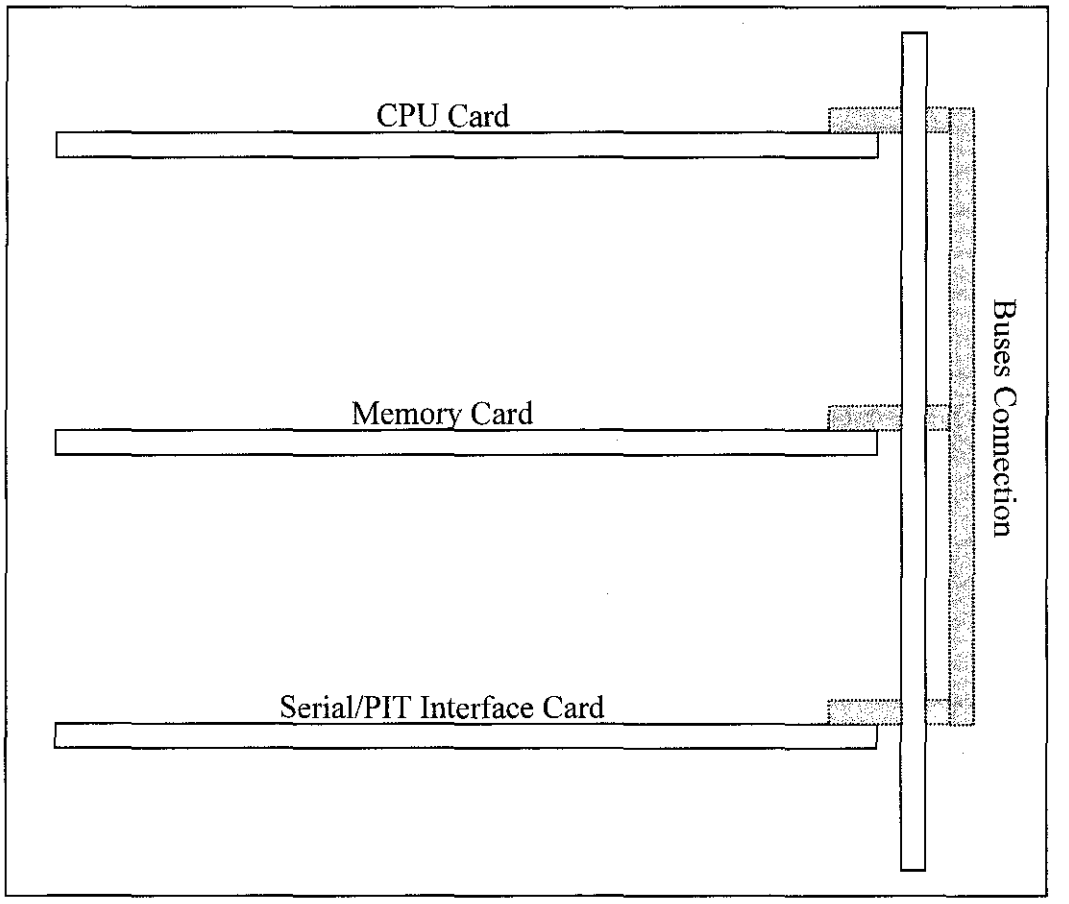

Figure 7 Sketch of Modular Approach Board.

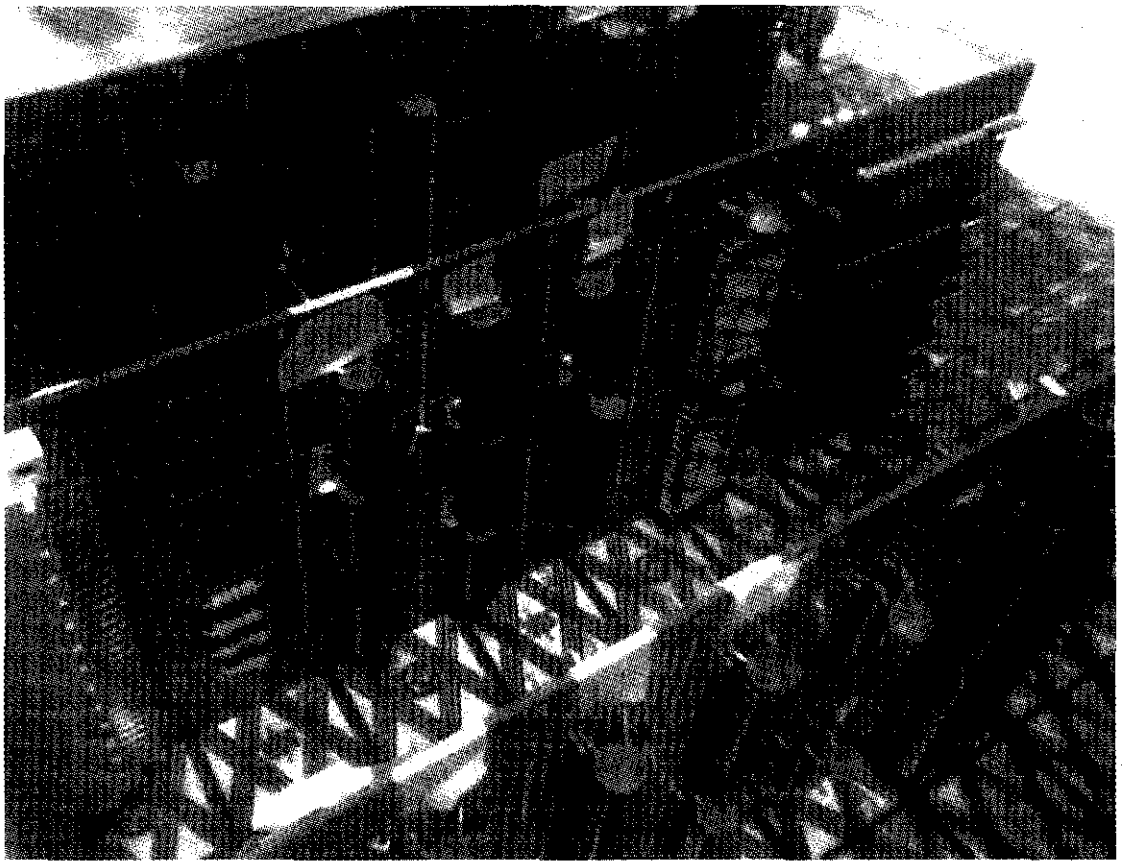

Figure 8 Image of Modular Approach Board.

4.1 CPU Card

CPU card consists of the 68000 microprocessor itself, the clock and halt/reset circuits, and the buffers. Buffers or line drivers is needed to drive the signals from the microprocessor to the entire system. Generally buffer is used to prevent interference among circuitries with the desired operation. Since Flight68K-MKII system is built on one board, it did not utilize buffer system. The add-on buffer circuit was done as per shown before. Clocking frequency for this particular board is 10MHz.

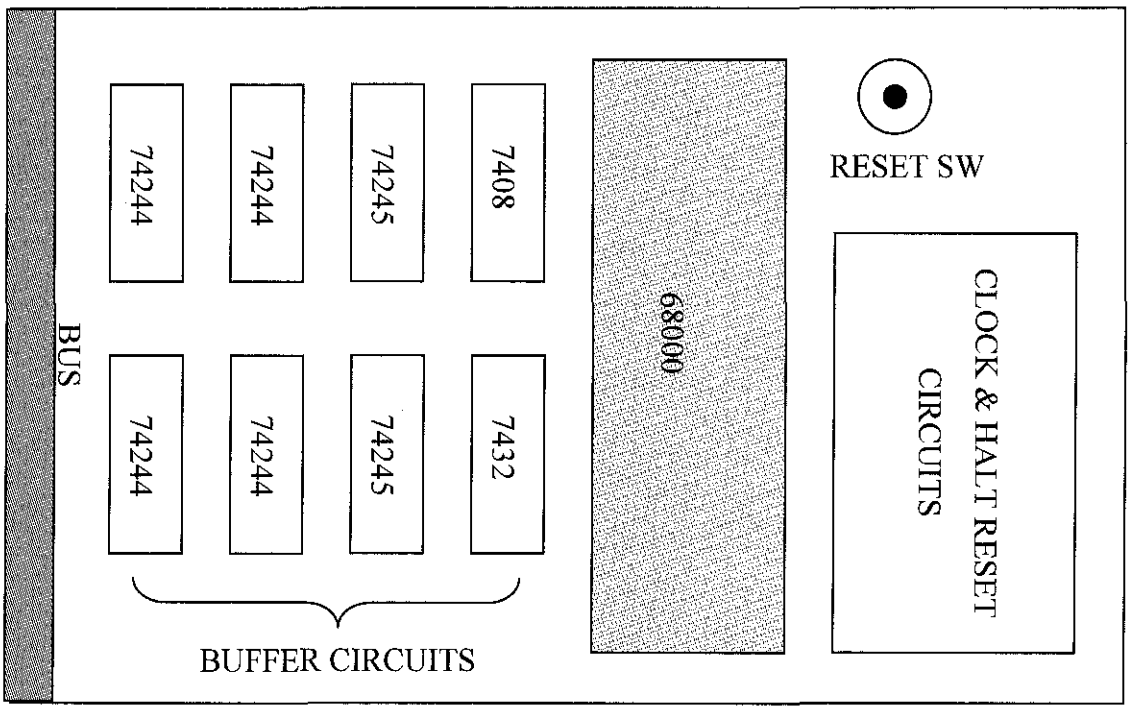

Figure 9 CPU Card Layout.

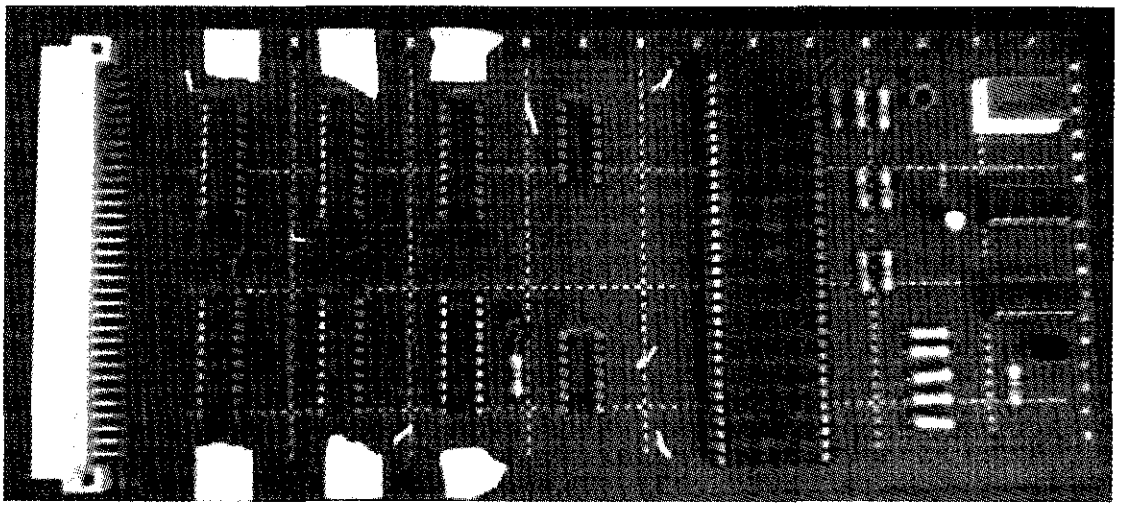

Figure 10 Image of CPU Card.

4.2 Memory Card

This card consists of memory decoder circuit networks, two EPROMs, and four SRAMs. Memory decoder consists of basic logic gates network is used to decode data and provides interfacing of the memory modules to the whole system.

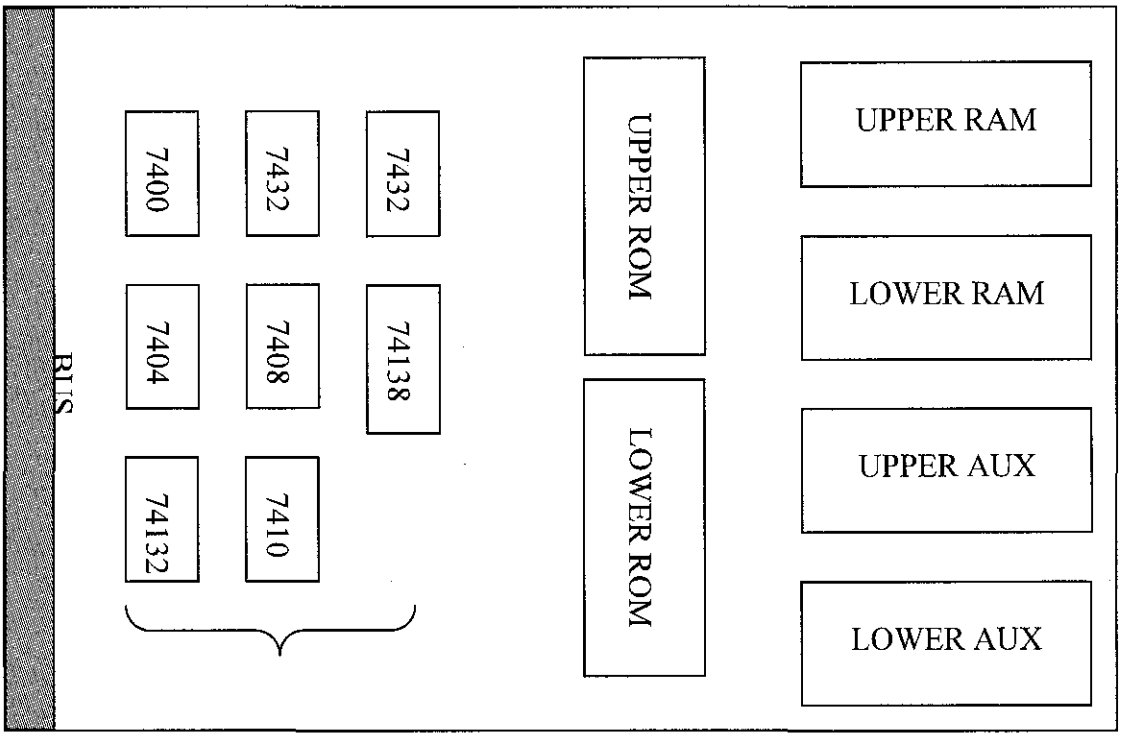

Figure 11 Memory Card Layout.

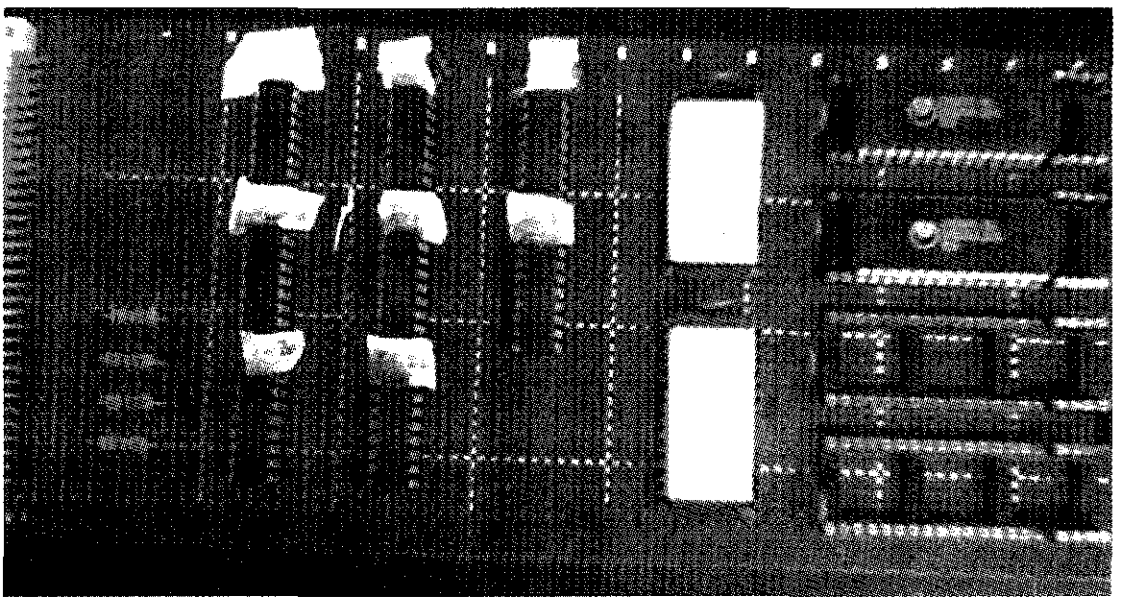

Figure 12 Image of Memory Card.

4.3 Serial/Parallel Interface Card

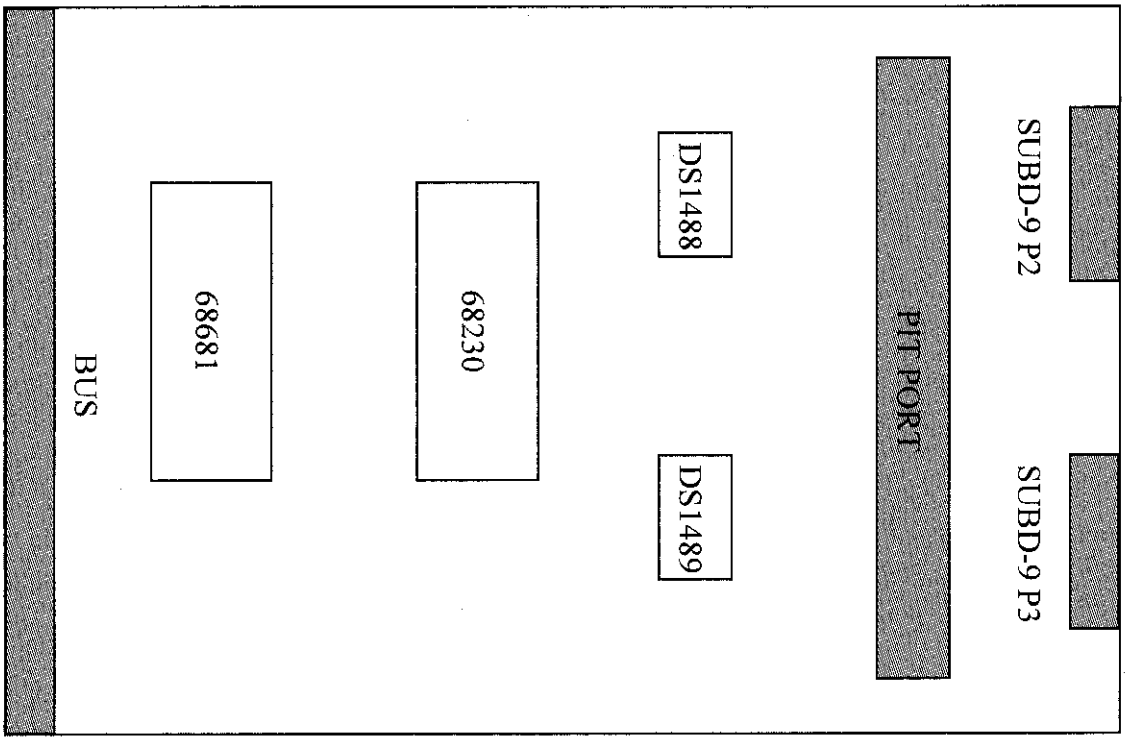

Figure 13 Serial/Parallel Interface Card Layout.

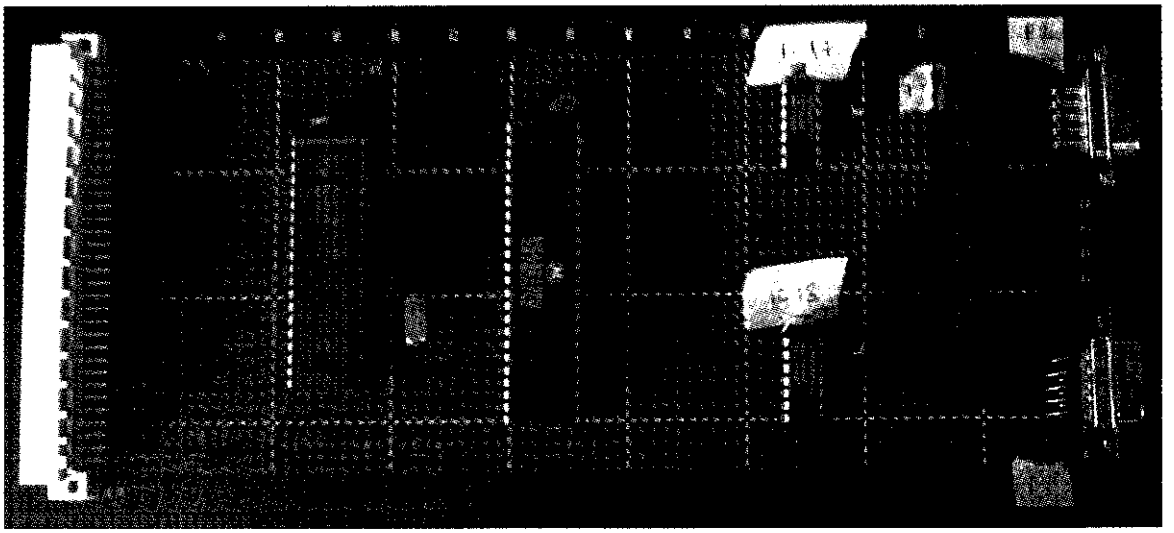

Figure 14 Image of Serial/Parallel Interface Card.

4.4 Bus Pin Allocations

A total of 96 points is available from the bus used. Pin allocations of the bus are showed in the figure below. Some points are left free to enable any expansion on the system later.

	a	b	c
1	GND	D0	A1
2		D1	A2
3		D2	A3
4		D3	A4
5		D4	A5
6		D5	A6
7		D6	A7
8		D7	A8
9		D8	A9
10		D9	A10
11		D10	A11
12		D11	A12
13		D12	A13
14		D13	A14
15		D14	A15
16		D15	A16
17			A17
18		IACK*	A18
19		230*	A19
20		681*	A20
21		FC0	A21
22		FC1	A22

23		FC2	A23
24		IPL0*	AS*
25		IPL1*	UDS*
26		IPL2*	LDS*
27		BERR*	R/W*
28		VPA*	DTACK*
29		E	BG*
30		VMA*	BGACK*
31		HALT*	BR*
32		RESET*	CLK

Figure 15 Pin Allocations on Bus.

4.5 Backplane

Backplane is a board which places three female 96 pins connectors in order to connect all the three card's buses. Direct connection is made from each pin of one socket to the same pins of other sockets. See Figure 16.

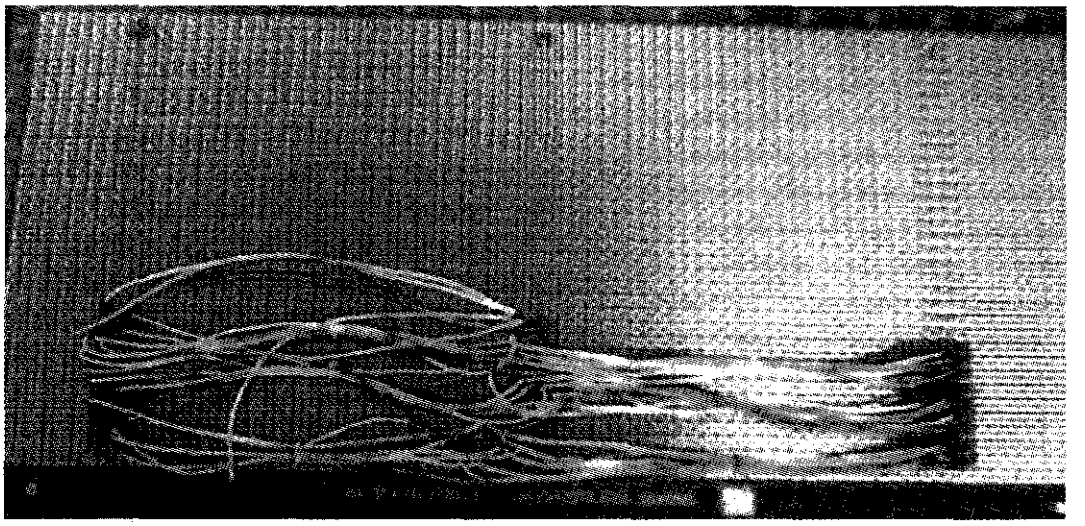

Figure 16 Image of Backplane.

CHAPTER 5
STATIC TESTING FOR MEMORY CARD

5.1 CPU Emulator

A testing procedure was done to test the memory card individually. In this project, the static testing is done. A CPU emulator was built. This emulator mimics some features of a microprocessor. This emulator have the address lines, data lines, as well as some control lines such as R/W*, AS*, UDS*, and LDS*. These lines will then be connected directly to the memory card. The concept of this emulator is to enable the addresses to be applied manually, and the resulting data could then be seen and displayed through the LEDs. [3]

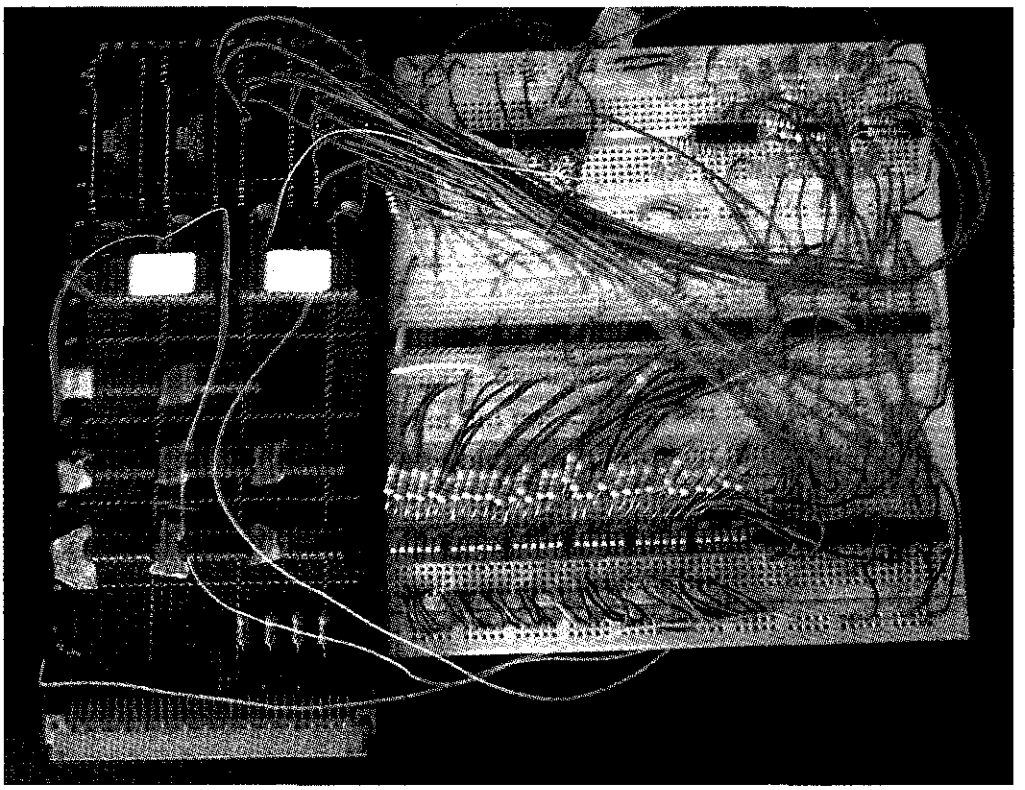

Figure 17 CPU Emulator & Memory Card Connected.

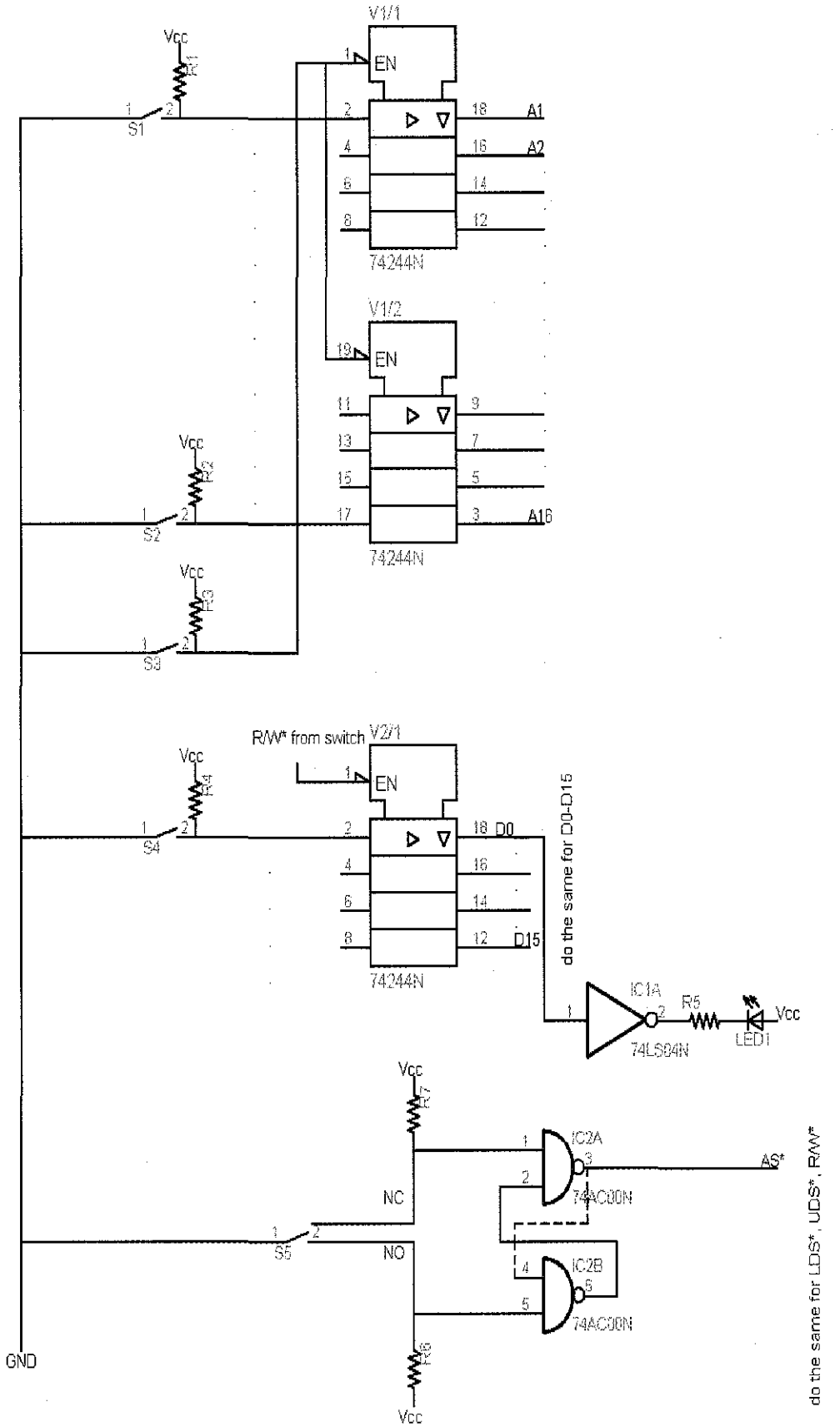

Figure 18 CPU Emulator Schematic Diagram.

5.2 Initial Observations

Initial observations shows that the data lines always give zeros regardless of any addresses applied on the memory card. Thus, from this initial observation, the memory could have some problems, for instance incorrect decoding activities. However further experiments and observations have to be carried out to investigate which part of the memory card is causing errors.

CHAPTER 6
CONCLUSIONS AND RECOMMENDATIONS

6.1 Introduction

The objective and scope of this project is discussed in detail in chapter one of this report. The discussions pointed out that the main objective is to develop a modular 68000 microprocessor system as a teaching aid. The reason for adopting the modular approach is that a modular system allows the students better access to the major components and to test these components independently. It is envisaged that this approach could aid the students to understand a microprocessor system.

6.2 A 68000 Modular Microprocessor System

A modular 68000 modular microprocessor system was designed and constructed using a wire-wrapping system. The modular system consists of three cards, that is;

6.2.1 A CPU Card

The CPU card features a Motorola 68000 microprocessor, 10-MHz crystal clock, and buffer circuits.

6.2.2 A Memory Card

The memory card consists of memory decoder circuits, EPROM modules, and SRAM modules.

6.2.3 An Interface Card

Lastly, interface card consists of serial interface chip, and a parallel interface chip.

6.3.2 Write a New Firmware

Chances of having incompatible firmware might lead to the problems, though it was very small. A new firmware may be written based on the available hardware design. This will ensure total compatibility between the designed hardware and the firmware.

In conclusion a modular 68000 microprocessor was build. However, due to lack of time several problems were not resolve in time and therefore it is recommended further tests are needed to resolve these problems so that the system will function correctly.

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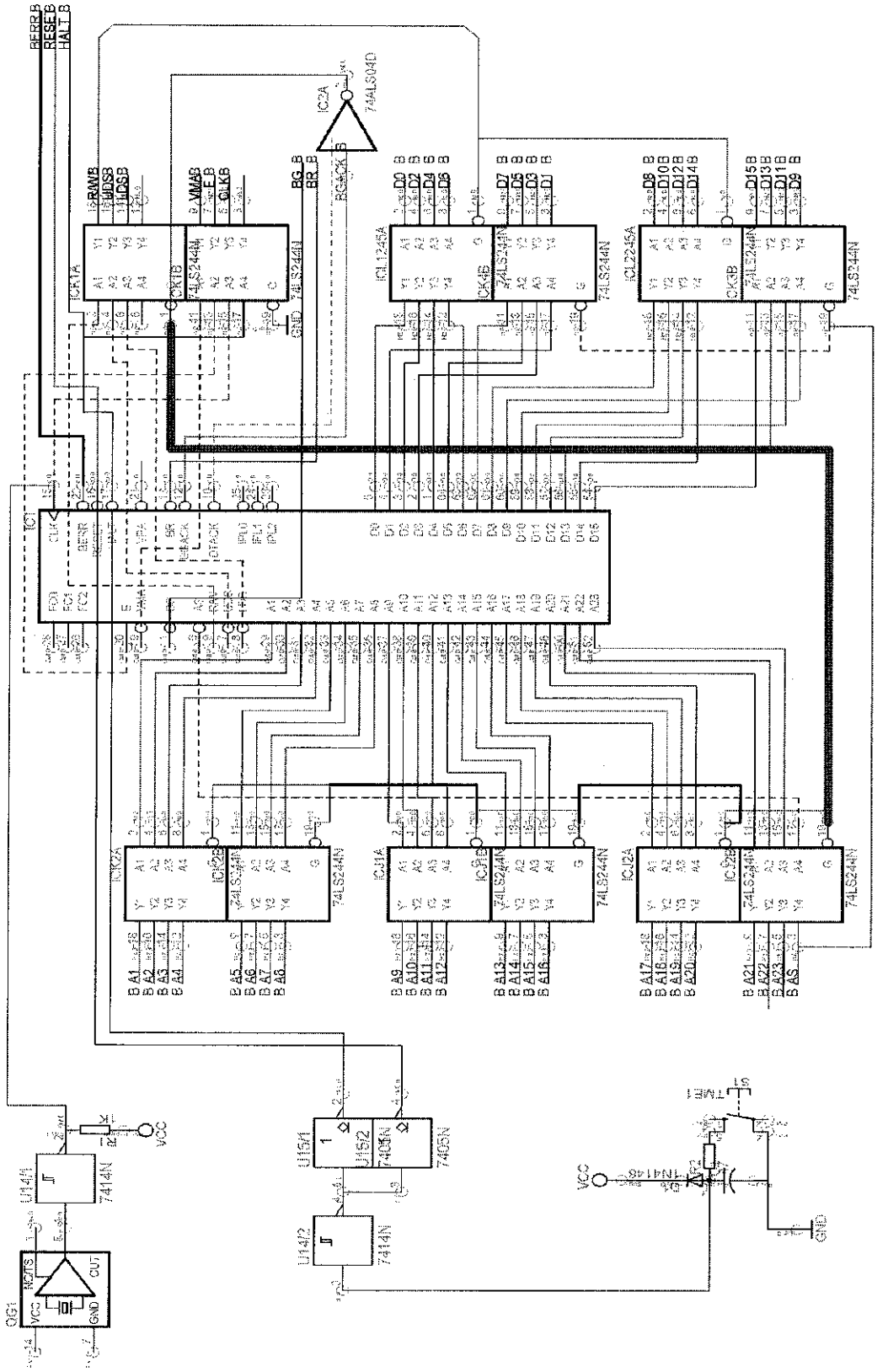
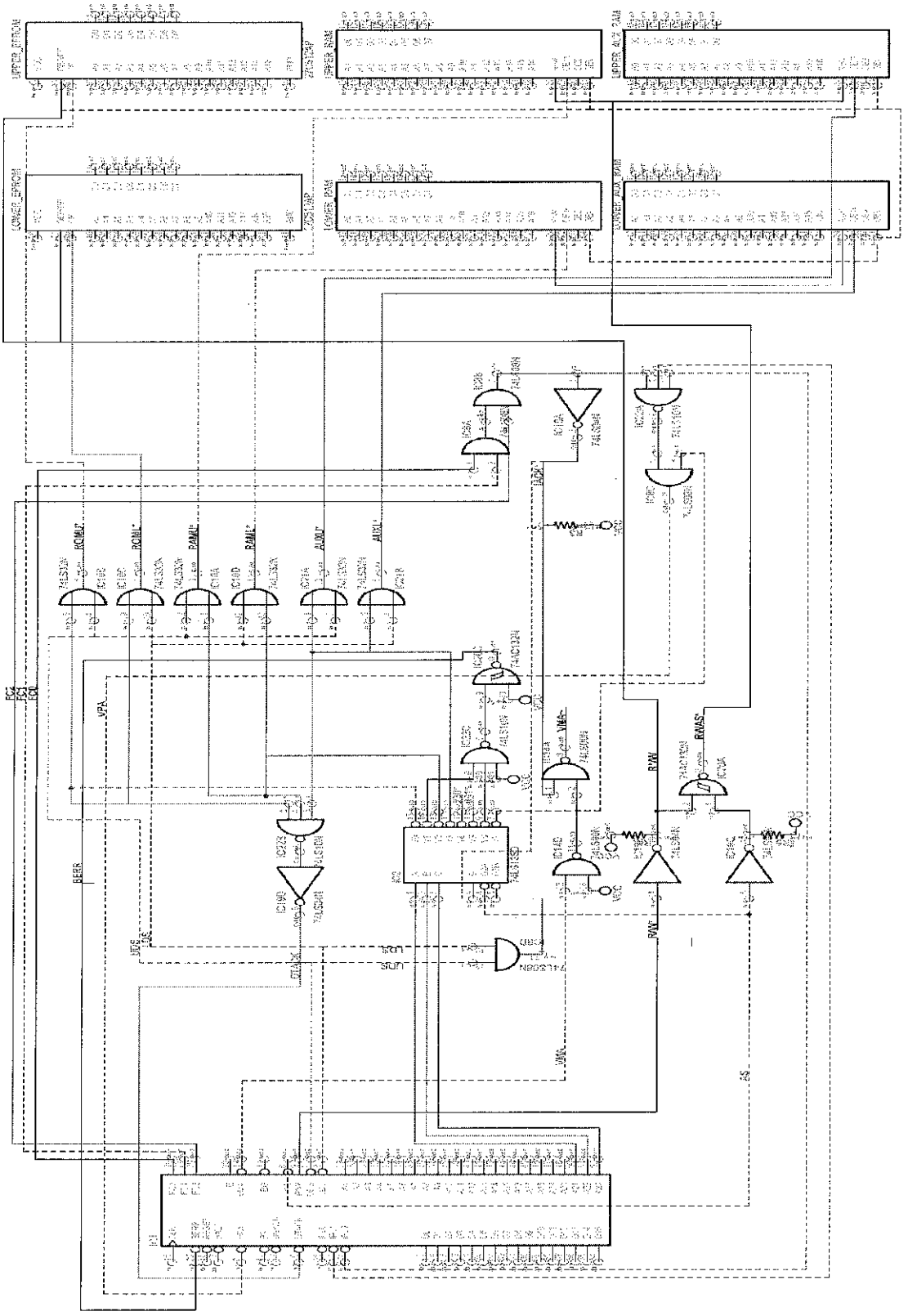
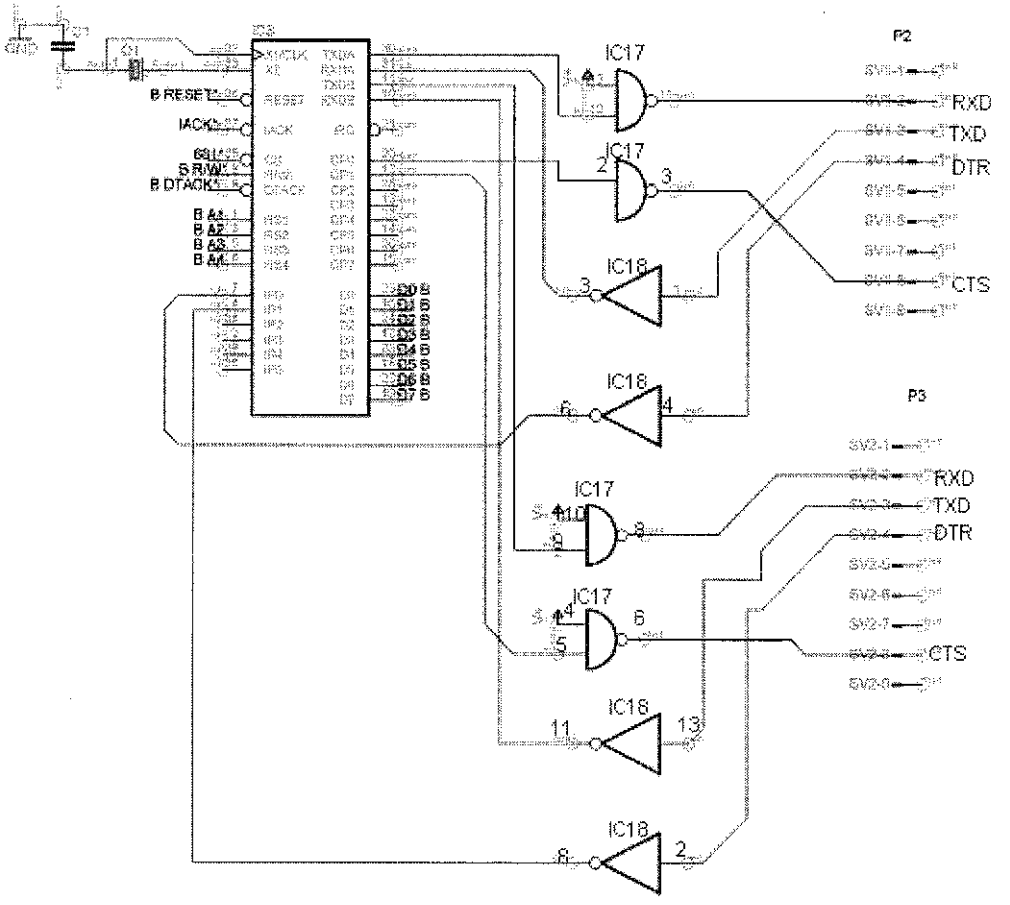
APPENDICES



Appendix I: Schematic Diagram of CPU Card



Appendix II: Schematic Diagram of Memory Card



Appendix III: Schematic Diagram of Interface Card