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Permanent address: House 188, Street 74, G-9/3 Islamabad, 44000, Pakistan.

Name of Supervisor: Dr. Mohammad Awan

Date: 10-7-2009

Date: 10-7-2009

UNIVERSITI TEKNOLOGI PETRONAS

Approval by Supervisor

The undersigned certify that they have read, and recommend to The Post-graduate Studies Programme for acceptance, a thesis entitled **"Design and Implementation of the Quadrature Voltage Controlled Oscillator for Wireless Receiver Applications Utilizing 0.13 μm and 0.18 μm Deep Sub-Micron RF CMOS Technology"** submitted by Saeed Zafar for the fulfillment of the requirements for the degree of **Doctor of Philosophy** in the **Department of Electrical and Electronics Engineering.**

10 - 7 - 2009

Date

Signature : _____

Dr. Mohammad Awan
Associate Professor
Electrical & Electronic Engineering
31750 Tronoh Perak
Tel: 05-368 7834 Fax: 365 7443

Main Supervisor : _____

DR. TUN ZAINAL AZNI ZULKIFLI
Senior Lecturer
School Of Electrical and Electronic Engineering
Universiti Sains Malaysia
Engineering Campus
14300 Nibong Tebal, Seberang Perai Selatan
Pulau Pinang

Co-Supervisor : _____

Date : 10 - 7 - 2009

UNIVERSITI TEKNOLOGI PETRONAS

Design and Implementation of the Quadrature Voltage Controlled Oscillator for Wireless Receiver Applications Utilizing 0.13 μm and 0.18 μm Deep Sub-Micron RF CMOS Technology

By

Saeed Zafar

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BANDAR SERI ISKANDAR,

PERAK

July 2009

DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

Signature : 

Name : SAEED ZAFAR

Date : 10-7-2009

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A Black Cloudy Afternoon

Saeed

ABSTRACT

The field of high-frequency circuit design is receiving significant industrial attention due to variety of radio frequency and microwave applications. This work proposes the low power, low phase noise and low phase error quadrature voltage controlled oscillator ($LP^3 - QVCO$) for wireless receiver applications. An enhanced investigation and design of the low power, low phase noise and low phase error quadrature voltage controlled oscillator ($LP^3 - QVCO$) is carried out in comparison to conventional $LC - QVCO$. The design, implementation and characterization of the complementary $LP^3 - QVCO$ is carried out with the integration of 40 Ω source damping resistor (R_{dmp}), tail biasing resistor (R_{tail}) and multifinger gate width configuration of the $pMOS$ varactors and 50 Ω impedance of common drain output buffers. The $LP^3 - QVCO$ implementation is carried out using 0.18 μm, 6 metal, 1 poly, 1.8 V and 0.13 μm, 8 metal, 1 poly, 1.2 V deep sub-micron $CMOS$ and $RF\ CMOS$ process technologies. The three different designs with the center frequencies of 2.8 GHz, 3.1 GHz and 3.8 GHz are implemented using 0.18 μm $CMOS$ and $RF\ CMOS$ process technology. The remaining four designs with the center frequencies of 4.35 GHz and 5 GHz are implemented using 0.13 μm $RF\ CMOS$ process technologies. The $LP^3 - QVCO$ design exhibit the measured phase noise of -110.13 dBc/Hz and -108.54 dBc/Hz at the offset frequency of 1 MHz, with multifinger gate width configuration of $pMOS$ varactor (3.125 μm $\times$ 64 = 200 μm) and (8 μm $\times$ 25 = 200 μm), respectively. The phase noise im-

provement of 1.63 dB is achieved in $LP^3 - QVCO$ design implemented with (3.125 μm $\times$ 64 = 200 μm) multifinger gate width configuration of $pMOS$ varactor in comparison to (8 μm $\times$ 25 = 200 μm). The measured center frequency of the $LP^3 - QVCO$ is 4.35 GHz with the frequency tuning range of 4.21 GHz to 4.44 GHz. Both $LP^3 - QVCO$ core power dissipation is 3.36 mW from 1.2 V dc power supply. The measured phase error is less than 0.2°. The calculated figure of merit (FOM) is -177.6 dBc/Hz. The symmetrical spiral inductor is also used with patterned ground shield (PGS). The quality (Q) factor of inductor is 18.6 and is implemented using 0.13 μm $RF\ CMOS$ process technology.

ABSTRAK

Bidang rekabentuk litar frekuensi-tinggi kini mendapat perhatian industri disebabkan kepelbagaian kegunaan frekuensi radio dan gelombang mikro. Kerja ini mencadangkan pengayun kuadratur terkawal voltan berkuasa rendah, bising fasa yang rendah and ralat fasa yang rendah ($LP^3 - QVCO$) untuk keguanan penerima tanpa wayar. Suatu peningkatan dan rekabentuk pengayun terkawal voltan ($LP^3 - QVCO$) berkuasa rendah, bising fasa yang rendah, ralat fasa yang rendah telah dilaksanakan berbanding kepada $LC - QVCO$ yang konvensional. Rekabentuk, pelaksanaan dan pencirian memperlengkapkan $LP^3 - QVCO$ telah dilaksanakan dengan penyepaduan bersama pelemah perintang sumber (R_{dmp}) 40 Ω, perintang pincang ekor (R_{tail}), konfigurasi varaktor $pMOS$ lebar pintu pelbagai jari dan suatu penimbal keluaran parit sepunya berimpedans 50 Ω. Perlaksanaan $LP^3 - QVCO$ menggunakan teknologi pemprosesan kedalaman sub-mikron $CMOS$ dan $RF\ CMOS$, 0.18 μm, 6 logam, 1 poly, 1.8 V dan 0.13 μm, 8 logam, 1 poly, 1.2 V. Tiga reabentuk berbeza menghasilkan frekuensi tengah 2.8 GHz, 3.1 GHz dan 3.8 GHz telah dilaksana menggunakan teknologi pemprosesan $CMOS$ 0.18 μm. Selanjutnya empat rekabentuk berfrekuensi tengah 4.35 GHz dan 5 GHz telah dilaksana menggunakan teknologi pemprosesan $RF\ CMOS$ 0.13 μm. Reabentuk $LP^3 - QVCO$ menunjukkan bising fasa -110.05 dBc/Hz dan -108.54 dBc/Hz pada frekuensi ofset 1 MHz, masing-masing dengan konfugurasi varaktor $pMOS$ pelbagai lebar pintu (3.125 μm $\times$ 64 = 200 μm) dan (8 μm $\times$ 25 =

200 μm). Penambaikan bising fasa 1.63 dB telah dicapai oleh $LP^3 - QVCO$ yang laksanakan dengan konfugurasi varaktor $pMOS$ lebar pintu (3.125 μm $\times$ 64 = 200 μm) dibandingkan kepada (8 μm $\times$ 25 = 200 μm). Frequensi te-ngah $LP^3 - QVCO$ yang ukur adalah 4.35 GHz dengan julat talaan frekuensi 4.21 GHz ke 4.44 GHz. Lesapan kuasa teras kedua-dua rekabentuk $LP^3 - QVCO$ adalah 3.45 mW daripada pembekal kuasa 1.2 V. Ralat fasa yang diukur adalah kurang daripada 0.2°. Rajah merit (FOM) yang dikira ialah 177.6 dBc/Hz. Gegelong induktor yang simmetri telah digunakan bersama "patterned ground shield" (PGS). Faktor kualiti (Q) induktor ialah 18.6 dan dilaksana menggunakan pemprosessan teknologi $RF\ CMOS$ 0.13 μm.

TABLE OF CONTENTS

TABLE OF CONTENTS xi

LIST OF TABLES xv

LIST OF FIGURES xvi

ABBREVIATIONS xx

1 BACKGROUND 1

1.1 Introduction 1

1.2 Objectives 4

1.3 Research Scope 5

1.4 Thesis Organization 6

2 LITERATURE REVIEW 9

2.1 Introduction 9

2.2 Modern RF Communication System 9

2.2.1 RF Transceivers 10

2.3 Frequency Synthesizer Architecture 13

2.4 CMOS Oscillator Basics and Main Types 13

2.4.1 Spiral Inductor 15

2.4.2 Varactors 19

2.5 LC Oscillator 20

2.5.1 Cross-Coupled Oscillators 24

2.5.2 Colpitts Oscillators 27

2.5.3 Negative ($-G_m$) Oscillators 29

2.6 CMOS VCO Topologies 30

2.7 Quadrature Voltage Controlled Oscillator 32
2.8 Oscillator Performance Parameters 36
2.8.1 Phase Noise 36
2.8.2 Leeson's Equation 37
2.8.3 Linear Time Varient (LTV) System 40
2.8.4 Figure of Merit (FOM) 44
2.8.5 Frequency Tuning Range 45
2.9 State of the Art Oscillators 46
2.10 Summary 47

3 LP^3-QVCO DESIGN 50
3.1 Introduction 50
3.2 Voltage Controlled Oscillator Design 50
3.2.1 Oscillator Design Techniques 52
3.2.2 Inductor Design 56
3.2.3 Integrated Capacitors 60
3.2.4 Varactor Design 62
3.2.5 Output Buffer Design 63
3.3 LP^3-QVCO Design 66
3.3.1 LP^3-QVCO Design No. 1 71
3.3.2 LP^3-QVCO Design No. 2 71
3.3.3 LP^3-QO Design No. 3 73
3.3.4 LP^3-QVCO Design No. 4 - 5 76
3.3.5 LP^3-QVCO Design No. 6 - 7 78
3.3.6 LP^3-QVCO Component Parameters 78
3.4 LP^3-QVCO Design Flow 79
3.5 Summary 81

4 LP^3-QVCO IMPLEMENTATION 83
4.1 Introduction 83

4.2 Implementation and Layout 83
4.2.1 Layout of Design No. 1 84
4.2.2 Layout of Design No. 2 and 3 84
4.2.3 Layout of Design No. 4 and 5 88
4.2.4 Layout of Design No. 6 and 7 93
4.3 LP^3-QVCO Chip Pin Configurations 93
4.4 LP^3-QVCO Measurement Test Setup 96
4.5 LP^3-QVCO Fabricated Chips 99
4.5.1 LP^3-QVCO Fabrication Using 0.18 μm Process 99
4.5.2 LP^3-QVCO Fabrication Using 0.13 μm Process 103
4.6 Summary 107

5 RESULTS AND DISCUSSION 109
5.1 Introduction 109
5.2 LP^3-QVCO Simulation and Measurement Results 109
5.3 LP^3-QVCO Results Discussion 118
5.4 LP^3-QVCO Results Comparison 121
5.5 Summary 123

6 CONCLUSIONS AND FUTURE WORK 126
6.1 Introduction 126
6.2 Conclusion 126
6.3 Future Work 128

References 130

A Inductor Design 144

B Physical Realization of pMOS Varactor 147

C LP^3-QVCO Measurement Results 152

Index 166

LIST OF TABLES

2.1 State of the art oscillators performance parameters summary. 48

3.1 π-model of spiral inductors extracted from ASITIC. 59
3.2 Common-drain buffer parameters. 65
3.3 Buffer bias circuit parameters. 66
3.4 QVCO design parameters summary. 79

4.1 LP^3-QVCO chips pin configurations. 95
4.2 Dimensions of fabricated LP^3-QVCO chips. 107

5.1 LP^3-QVCO simulation results summary. 113
5.2 LP^3-QVCO and conventional QVCO phase noise. 116
5.3 LP^3-QVCO measurement results. 119
5.4 LP^3-QVCO measurement results comparison to state of the art work. 124

A.1 Symmetrical spiral inductor design parameters using ASITIC. 146

LIST OF FIGURES

2.1 Block diagram of analog RF system 11
2.2 Block diagram of heterodyne and homodyne receivers 12
2.3 Example of MB-OFDM frequency synthesizer 14
2.4 Feedback oscillatory system 15
2.5 π-equivalent inductor model 18
2.6 pn-junction diode varactor 20
2.7 MOS varactor 21
2.8 Ideal and realistic LC-tanks and series parallel conversion 22
2.9 Magnitude and phase of the impedance of a LC-tank vs frequency . . 24
2.10 Cross-coupled oscillator 25
2.11 MOS and cross-coupled MOS equivalent model 25
2.12 Magnitude and phase of the cross coupled oscillator 26
2.13 Colpitts oscillator and equivalent circuit model 27
2.14 One port oscillators 29
2.15 SS and DS VCO 31
2.16 Signal injection in oscillator 33
2.17 Two oscillator coupled together 34
2.18 Oscillator frequency spectrum 38
2.19 Oscillator SSB phase noise 39
2.20 Impulse response of LC-tank 41
2.21 Conversion of noise source to phase fluctuations and phase noise side bands 43
2.22 VCO sensitivity 46

3.1 DS-VCO topology 53

3.2 LP^3-VCO with tail biasing resistor, damping resistor and multifinger gate structure. 57
3.3 1.24 nH inductor s-parameters 58
3.4 1.19 nH inductor s-parameters 59
3.5 Symmetrical spiral inductor with PGS 61
3.6 Tuning characteristics of pMOS varactor 63
3.7 Common drain buffer 64
3.8 Common drain buffer bias circuit 65
3.9 LP^3-QVCO with nMOS coupling 67
3.10 LP^3-QVCO block diagram 68
3.11 LP^3-QVCO with common drain buffers 70
3.12 LP^3-QVCO design no. 1 72
3.13 LP^3-QVCO design no. 2 74
3.14 LP^3-QO design no. 3 75
3.15 LP^3-QVCO design no. 4 - 5 77
3.16 LP^3-QVCO design flow 80

4.1 Layout of design no. 1 85
4.2 Layout of design no. 2 86
4.3 Layout of design no. 3 87
4.4 Layout of design no. 4 89
4.5 Layout of design no. 5 90
4.6 Layout of design no. 6 91
4.7 Layout of design no. 7 92
4.8 QVCO chip pins configuration 94
4.9 LP^3-QVCO measurement test setup 98
4.10 Design no. 1. A 2.8 GHz LP^3-QVCO magnified micrograph. 100
4.11 Design no. 2. A 3.1 GHz LP^3-QVCO magnified micrograph. 101
4.12 Design no. 3. A 3.8 GHz LP^3-QVCO magnified micrograph. 102

4.13 Design no. 4. A 4.35 GHz LP^3-QVCO magnified micrograph. 103
4.14 Design no. 5. A 4.35 GHz LP^3-QVCO magnified micrograph. 104
4.15 Design no. 6. A 5 GHz LP^3-QVCO micrograph. 105
4.16 Design no. 7. A 5 GHz LP^3-QVCO micrograph. 106

5.1 Source damping resistor variation against phase noise at the offset frequency of 100 KHz. 110
5.2 Phase error accuracy with coupling factor (K) variations. 111
5.3 Transient analysis of simulated LP^3-QVCO design. 112
5.4 Transient output of measured LP^3-QVCO chip. 114
5.5 Output frequency spectrum of measured LP^3-QVCO chip. 114
5.6 Measured phase noise of LP^3-QVCO chip. 116
5.7 Measured frequency tuning range and output power vs varactor dc tune voltage. 117
5.8 Measured FOM against frequency tuning range. 119
5.9 LP^3-QVCO phase noise comparison to state of the art work. 122
5.10 LP^3-QVCO phase error comparison to state of the art work. 123

A.1 Patterned ground shield used in LP^3-QVCO design no. 1, 2 and 3 . . 145

B.1 A pMOS varactor layout of LP^3-QVCO design no. 4 148
B.2 A pMOS varactor layout of LP^3-QVCO design no. 5 149
B.3 A pMOS varactor layout of LP^3-QVCO design no. 6 150
B.4 A pMOS varactor layout of LP^3-QVCO design no. 7 151

C.1 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 1 153
C.2 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 1 154
C.3 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 2 155

C.4 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 2 156
C.5 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QO design no. 3 157
C.6 Transient analysis of measured LP^3-QO design no. 3 158
C.7 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 4 159
C.8 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 5 160
C.9 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 5 161
C.10 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 6 162
C.11 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 6 163
C.12 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 7 164
C.13 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 7 165

ABBREVIATIONS

ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits
BPF	Band Pass Filter
BSF	Band Select Filter
CMOS	Complementary Metal-Oxide-Semiconductor
dBc	Decibel Below Carrier
dBc/Hz	Decibel Below Carrier Per Hertz
DEM	Demodulator
DRC	Design Rule Check
DS-VCO	Double-Switch Voltage-Controlled Oscillator
DUT	Device Under Test
EM	Electro-Magnetic
FM	Frequency Modulation
FM 6	Finger Capacitor Metal 6
FOM	Figure Of Merit
FS	Frequency Synthesizer
GaAs	Gallium Arsenide
GHz	Giga Hertz
GSG	Ground Signal Ground
GSM	Global System for Mobile Communications
IC	Integrated Circuit
IF	Intermediate Frequency
I/O	Input Output
IRF	Image Reject Filter
ISF	Impulse Sensitivity Function

KHz	Kilo Hertz
LC	Inductor Capacitor
LNA	Low Noise Amplifier
LO	Local Oscillator
LPE	Layout Parasitics Extraction
LPF	Low Pass Filter
LP^3-QVCO	Low Phase Noise, Low Power and Low Phase Error Quadrature Voltage-Controlled Oscillator
LTI	Linear Time-Invariant
LTV	Linear Time-Variant
LVS	Layout Versus Schematic
MB-OFDM	Multi Band Orthogonal Frequency Division Multiplexing
MCM	Multi Chip Module
MEMS	Micro-Electro-Mechanical System
MOS	Metal-Oxide-Semiconductor
MHz	Mega Hertz
MIM	Metal-Insulator-Metal
OFDM	Orthogonal Frequency Division Modulation
Osc	Oscillator
PA	Power Amplifier
PCB	Printed Circuit Board
PDA	Personal Data Assistant
PGS	Patterned Ground Shield
PLL	Phase Lock Loop
Q	Quality Factor
QVCO	Quadrature Voltage-Controlled Oscillator
RF	Radio Frequency

RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
rms	Root Mean Square
SA	Spectrum Analyzer
SIPC-QVCO	Source-Injection Parallel Coupled Quadrature Voltage-Controlled Oscillator
Si	Silicon
SiGe	Silicon Germanium
SSA	Signal Source Analyzer
SSB	Single Side Band Mixer
SS-VCO	Single-Switch Voltage-Controlled Oscillator
SNR	Signal-to-Noise Ratio
SOC	System-On-Chip
UTM	Ultra Thick Metal
UWB	Ultra Wide Band
VCO	Voltage-Controlled Oscillator
VLSI	Very Large Scale Integrated Circuit

CHAPTER 1

BACKGROUND

1.1 Introduction

In recent years, there has been a strong growth in the modern wireless data and voice communication standards in numerous frequency bands. Modern transceivers for the wireless communication consist of many building blocks, such as low-noise amplifiers ($LNAs$), mixers, frequency synthesizers (FS), filters and amplifiers [1]. With the advancement of radio frequency (RF) technology and requirement for more integration, new RF wireless architectures are needed. There is a tremendous demand of mobile communication and wireless communication systems in today's modern life. This has placed certain limitations and requirements on the communication channel bandwidths and spacing. The modern wireless communication systems rely strongly on frequency conversion and switching of one frequency band to other frequency bands [1], [2].

Frequency synthesizer is one of the most critical components in the wireless transceiver. It greatly affects the overall performance of the wireless transceiver system [3]. Frequency synthesizers are commonly used as a local oscillator (LO) in the wireless transceivers for frequency translation and channel selection. The key idea is to downconvert the RF signal to the baseband signal and it is also known as direct conversion or zero-IF receiver. To avoid the loss of information, the down conversion must provide quadrature outputs for the frequency and phase modulated signals. Therefore, frequency synthesizer requires the accurate quadrature signal generation from local oscillator (LO) [1]. RF transceivers require quadrature signal and quadrature voltage controlled oscillator ($QVCO$) provides the best solution for the generation of the quadrature signal [4].

The silicon technology has become popular after more than thirty years of development [1]. A new generation of wireless transceivers are being integrated into $CMOS$ technology. This includes the digital and mixed analog-digital baseband circuits, which influence the choice of radio transceiver architectures. The $CMOS$ technology calls the elimination of discrete components in the favor of high level on-chip integration [5]. In general, there are various technologies available for the radio frequency integrated circuits ($RFICs$) implementation. The important technologies include Si-bipolar, $SiGe$ $HBTs$, $BiCMOS$, $CMOS$ and $GaAs$. There is a strong market pressure towards low price, compact size, lightweight and high performance in highly integrated consumer $RFICs$. $SiGe$ $BiCMOS$ is also one of the promising and competitive technologies for system-on-chip (SOC) designs. It combines the transistor performances competitive to other technologies with the advantages of process maturity and high integration level of Si technology. The reason is excellent RF performance of bipolar npn transistors combined with low power logic of $CMOS$, which enables the fabrication of highly integrated transceivers. The bipolar and $GaAs$ devices exhibit a relatively high unity gain cut-off frequency, an important characteristics for high speed applications. Noise is one of the major advantages of $SiGe$ over $CMOS$ technology for RF applications. The $1/f$ noise due to carrier trapping at interface states thermal noise due to gate and channel resistance are higher in $CMOS$ than $SiGe$. To reduce the noise very large $CMOS$ devices and large operating currents are often required [6].

However, recent development and scaling of deep sub-micron $CMOS$ technologies have made it more attractive to implement single chip solution for various building blocks of transceiver and complete wireless transceivers. The strong potential for low cost and fully integration (e.g., high packaging density for digital circuits at the latest $CMOS$ technology node) for $CMOS$ relative to $BiCMOS$ make it the preferred technology for the consumer applications. Advancement in $CMOS$ process technology has reduced the minimum channel length of MOS device with high f_T (in the order of 100 GHz) of the transistor [7] [8]. There is a strong motivation to carry

out research in the area of $CMOS$ implementations. Therefore, the prime technology for the RF building blocks is $CMOS$ due to its low cost, low voltage, low power and low substrate loss. The $CMOS$ scaling is helpful for digital circuits and analog circuits are faced by the constantly diminishing power supply voltage. However, to solve this problem analog circuits should be designed in special analog processes as compared to digital processes [9]. The scaling down of the $CMOS$ technology has to increase the operation frequency (f_T) and reduce the chip area with a tradeoff in the reduction of power supply voltage [10], [11], [12].

The advancement in the technologies have led the wireless system integration in compact integrated circuits (ICs). The increasing demand for the portable communication equipment has driven the research in the transceivers at low cost and low power dissipation. There is a great interest of integrating complete transceiver in a single-chip solution [12], [13]. The various examples are compact size cell phones, radio frequency identification ($RFID$) systems, personal data assistants ($PDAs$) for clinical applications and various sensors [14], [15]. Therefore, the deep knowledge of the oscillators is necessary to improve the performance of wireless communication system. The traditional approach of integrating different chips and their interconnections is by using multi-chip module (MCM), flip-chip solution or packaging technologies. However, it results in the increased cost, power dissipation and larger chip area [1], [16], [17].

The oscillators are the major bottleneck for the system-on-chip (SOC) realization of the wireless transceivers. The oscillator plays an important role in the performance of wireless transceivers. Voltage controlled oscillator (VCO) spectral purity performance can limit the RF transceiver's performance. This is due to poor quality of on-chip passive components in silicon integrated circuit technologies, such as low quality factor (Q) of the on-chip inductors and poor linearity of on-chip varactors. High quality passive devices are required for the design of high performance LOs, voltage controlled oscillators ($VCOs$) and quadrature voltage controlled oscillators $QVCOs$. There are various requirements for the oscillators to be used in communi-

cation system, such as wide tuning range, low phase noise, low power dissipation, low phase error, frequency sensitivity, gain variation and low cost [12], [18], [19], [20].

All above mentioned facts consideration motivates to design single fully integrated chip solution of analog integrated circuits such as $QVCO$. The $QVCO$ can work in digital circuits as well as analog circuits by using low cost complementary metal-oxide semiconductor ($CMOS$) technologies.

This work focuses the design, analysis and implementation of various $QVCOs$. An innovative design approach has been adopted to improve the performance parameters of the $QVCOs$. The major performance parameters involve low phase noise, low power dissipation and low phase error of the $QVCO$ circuits, have been improved. This results in the formation of $LP^3 - QVCO$ structure.

The $CMOS$ technology is chosen due to its low cost. The integration of $LP^3 - QVCO$ on single chip in silicon technologies results in saving the multi-chip solution of passive components. However, the fully integrated circuits result in the increased power consumption. On the other hand, the design of time variant circuits such as VCO and $QVCO$ is one of the challenging task with the fulfillment of modern wireless communication requirements [12].

1.2 Objectives

- In this work, the design, analysis and implementation of the $QVCOs$ are presented. The several questions are investigated such as major problems for the on-chip $QVCOs$ and the key role of $QVCO$ in modern communication system [1]. The phase noise, phase error, frequency sensitivity, gain and power consumption are the factors that influence the performance parameters of the $QVCOs$ [21], [22], [23]. "How is it possible to design low phase noise, low power and low phase error $QVCO$ circuits?" Fully differential VCO is the main vehicle moving towards the design of the $LP^3 - QVCO$. The design oriented technique is proposed for improving the performance parameters of the $QVCO$.

- The comparison of LP^3-QVCO designs with the integration of multifinger gate width configuration of the $pMOS$ varactor, damping resistor and tail biasing resistor are also presented.

- The design, simulations and implementation are carried out for the $LP^3 - QVCO$ architecture. The LP^3-QVCO design implementations are carried out using 0.13 μm and 0.18 μm deep sub-micron $RF\ CMOS$ process technologies.

- The comparison results of $LP^3 - QVCO$ with state of the art work are also presented in this thesis. The fabricated LP^3-QVCO prototypes are measured to prove the concept and improvement in the results are discussed.

1.3 Research Scope

This thesis includes the design evolution, optimization and comparison of the $LP^3 - QVCO$ topology for the wireless applications.

- This design includes the fully differential LC-tank cross-coupled VCO and leading towards the implementation of the $LP^3 - QVCO$ topology. The $LP^3 - QVCO$ is integrated with the tail biasing resistor (R_{tail}) in the order of 100 Ω, source damping resistor (R_{dmp}) of 40 Ω and multifinger gate width configuration of the $pMOS$ varactor. The R_{tail} resistor is used in comparison to active device based current mirror biasing circuit in $LP^3 - QVCO$. The current mirrors up-convert the $1/f$ noise of the active device and degrading the phase noise performance of the circuit.

- The $LP^3 - QVCO$ designs are fabricated with multifinger gate width configuration of $pMOS$ varactors (3.125 μm $\times$ 64 = 200 μm) and (8 μm $\times$ 25 = 200 μm), respectively. The measured phase noise improvement of 1.63 dB at the offset frequency of 1 MHz is achieved while using with 3.125 μm $\times$ 64 = 200 μm gate width configuration of the $pMOS$ varactors of proposed design in comparison to 8 μm $\times$ 25 = 200 μm gate width configuration of the $pMOS$

varactors of the conventional $QVCO$ topology. Both $LP^3 - QVCO$ designs are implemented using 0.13 μm deep sub-micron $RF\ CMOS$ process technology.

- The phase error of the $LP^3 - QVCO$ is optimized and effect of scaling ratio of 0.31 between the coupling transistor and switching transistor to the phase error variations are investigated through simulation and implementation verification. The different scaling ratio (K) is implemented in $LP^3 - QVCO$ designs and phase error is measured. The implemented $LP^3 - QVCO$ topology also results in the phase error of less than 0.2°.

- The $LP^3 - QVCOs$ are designed in 0.13 μm and 0.18 μm deep sub-micron $CMOS$ and $RF\ CMOS$ process technologies, respectively. A comparison study concluded in describing the difference of using current mirrors based active device, tail biasing resistors, pn-junction varactors, $pMOS$ based varactors, circular spiral inductors and symmetrical spiral inductors. The highest FOM achieved in $LP^3 - QVCO$ is -187.1 dBc/Hz and -177 dBc/Hz while using 0.13 μm and 0.18 μm process technologies, respectively. The highest measured phase noise of $LP^3 - QVCO$ is -118.2 dBc/Hz and -115.1 dBc/Hz at 1 MHz offset frequency, while using 0.13 μm and 0.18 μm process technologies, respectively. The measured $LP^3 - QVCO$ tuning range of 310 MHz is achieved with pn-varactors using 0.18 μm process technology and 230 MHz is achieved with $pMOS$ varactors using 0.13 μm process technology, respectively.

1.4 Thesis Organization

This thesis explains the design, analysis and implementation of an innovative $QVCO$ design architecture. The $QVCO$ is one of the important $CMOS$ radio frequency integrated circuit ($RFIC$) building blocks of RF transceiver architecture. The proposed $QVCO$ is designed for the wireless receiver applications.

Chapter 2 gives an introduction of the modern wireless communication system, importance of oscillators and quadrature $VCOs$. It also includes the brief intro-

duction of the modern RF communication system, super heterodyne, homodyne receivers and frequency synthesizers. The basic LC-tank $CMOS$ oscillator types and $CMOS - VCO$ topologies are also explained. The phase noise theories include linear time invariant system (LTI) and linear time variant system (LTV), are also explained. The $CMOS$ $QVCO$ performance parameters of various state of the art oscillators are also summarized in this chapter.

In chapter 3, the $LP^3 - QVCO$ design is described, starting from VCO and $LP^3 - VCO$ design and moving towards the $LP^3 - QVCO$ design. The innovative design techniques are adopted in the $LP^3 - QVCO$ designs. The on-chip spiral inductor π-model parameters, Q-factor and inductance variations are also described. The patterned ground shield PGS is used with the spiral inductors. The pn-junction and $pMOS$ varactors are the main types used in $LP^3 - QVCO$ designs. The varactor capacitance variation with dc control voltage is also presented. Common drain buffers with bias circuits are used in the $LP^3 - QVCO$ circuits. Next, seven $LP^3 - QVCO$ designs with their component parameters are discussed. Finally, the $LP^3 - QVCO$ design flow is presented.

Chapter 4 describes the implementation and physical realization of the $LP^3 - QVCO$ architecture. The physical realization of the $LP^3 - QVCOs$ include the layout design. Next, implementation of $LP^3 - QVCO$ is described briefly. This also includes the pin configuration of the $LP^3 - QVCO$ chips. The measurement test setup of the $LP^3 - QVCO$ prototypes is also discussed. The measurement test setups include the phase noise, transient analysis, RF output frequency spectrum and dc analysis of the $LP^3 - QVCO$ designs. The fabricated $LP^3 - QVCO$ prototype micrographs and their dimensions are also included in this chapter.

Chapter 5 explains the simulation and measurement results of the $LP^3 - QVCO$ architectures. The simulation results of source damping resistor variation with phase noise are also presented. The simulation results of $pMOS$ varactor, coupling factor (K) and phase error are also described. The $LP^3 - QVCO$ simulation and measurement results include the phase noise, frequency spectrum, transient analysis and

phase error plots. The results are also compared to state of the art research work.

In chapter 6, conclusion and future work recommendations are presented.

Appendix A describes the patterned ground shield design and inductor design parameters used in $ASITIC$.

Appendix B describes the layout structure of $pMOS$ varactors with multifinger gate width configurations.

Appendix C describes the brief summary of the $LP^3 - QVCO$ performance parameter results. The phase noise and output frequency spectrum of the measured $LP^3 - QVCO$ designs are also shown.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter explains the importance of oscillators in the modern RF communication system. The super heterodyne receiver and homodyne receivers are briefly discussed which show the importance of the LO and quadrature VCO in the RF communication system. The basic types of the oscillators with discussion of $VCOs$ and $QVCO$ architecture are presented. The performance parameters of the oscillators such as tuning sensitivity, gain, phase noise and power dissipation are also explained briefly. The linear time variant (LTV) and linear time invariant (LTI) phase noise models are also described. The relevant state of the art oscillators performance parameters are also summarized in the last section.

2.2 Modern RF Communication System

The growth in radio frequency communication systems has led the communication system to new destination. This has helped to achieve high speed, high data transfer rate, compact size, low power consumption and cheap price of various electronic applications. With the advancement of electronic technology the RF and digital circuits can be implemented in a single-chip solution. The RF integrated circuits are available in many consumer electronics such as cellular phones, global positioning system (GPS) receivers, wireless transceivers, $PDAs$, computers and pagers. The $RFIC$ has reduced the implementation cost hence, realizing both analog and digital circuit blocks on the same chip. Next section describes the brief introduction of RF transceiver block diagram, homodyne and heterodyne receivers [2], [24], [25].

2.2.1 RF Transceivers

The general analog RF system architecture is shown in Fig. 2.1. RF system architecture consists of transmitter and receiver circuits. The transmitter block diagram is shown in Fig. 2.1 (a), which consists of voice circuit, modulator, power amplifier (PA) and antenna. The analog signal generated by the microphone is modulated by a carrier frequency signal. The resulted output signal is amplified and used to drive the antenna. The other side of RF system is based on receiver as shown in Fig. 2.1 (b). The receiver consists of antenna, low noise amplifier (LNA), downconverter, demodulator, audio amplifier and speaker. The signal is received by antenna and amplified by the LNA. After LNA the RF signal is fed to the mixer where intermediate frequency (IF) is used to downconvert the signal. The IF signal is generated by LO. The LO is tuned at certain frequency and desired frequency channel is selected by the frequency synthesizer. However, before sending the signal to the speaker demodulation is carried out by demodulator. The demodulated signal is amplified by the power amplifier and finally required signal is sent to the input of the speaker.

The block diagram of heterodyne[1] receiver is shown in the Fig. 2.2 (a). In a simplified heterodyne receiver the image reject filter (IRF) is used before mixer and channel select filter is also used after mixer block. Image reject filter is used to improve the signal-to-noise ratio (SNR) and rejects the image frequency of the signal. The channel select filter is used to select the frequency coming from the mixer block [1].

The block diagram of homodyne[2] receiver is shown in the Fig. 2.2 (b). In homodyne receivers, the LO frequency is same as the input carrier frequency. The key idea is to downconvert the RF signal to the baseband signal and hence, it is also known as direct conversion or zero-IF receiver. To avoid the loss of information the downconversion must provide quadrature outputs for the frequency and phase modulated signals. As it is zero-IF receiver, so the image problem is solved as it is

[1]Heterodyne is derived from the Latin roots hetero (different) and dyne (to mix).

[2]Homodyne is derived from the Latin roots homo (same) and dyne (to mix).

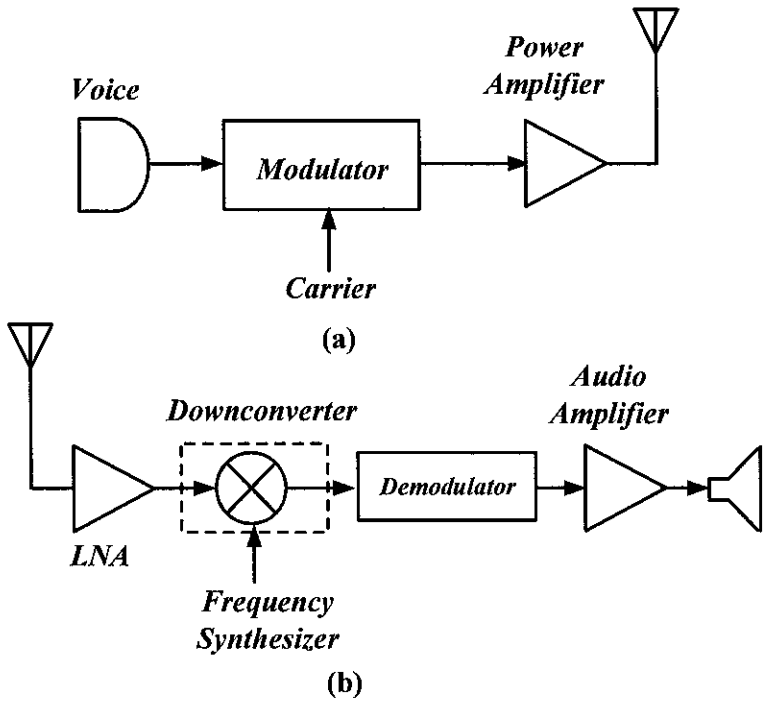


Figure 2.1 Block diagram of analog RF system (a) transmitter, (b) receiver

faced in heterodyne receivers. Hence, the image filter is not required in homodyne receivers. The channel select filter is also replaced by the low pass filter (LPF) and this structure requires the accurate quadrature LO. The LO signal is generated by frequency synthesizer (FS) circuit. The inphase (I) and quadrature (Q) signals are used for the multiplication of RF signals in the mixer block.

The transceiver performance is based on various factors, such as the distance between transmitter and receiver, the noise of LNA, oscillator phase noise, mixer noise figure, power consumption of the blocks and type of modulation. The well matched and precisely designed RF circuits such as LO, LNA, PA, mixer and filters can enhance the performance of whole transceiver significantly [1], [25], [26].

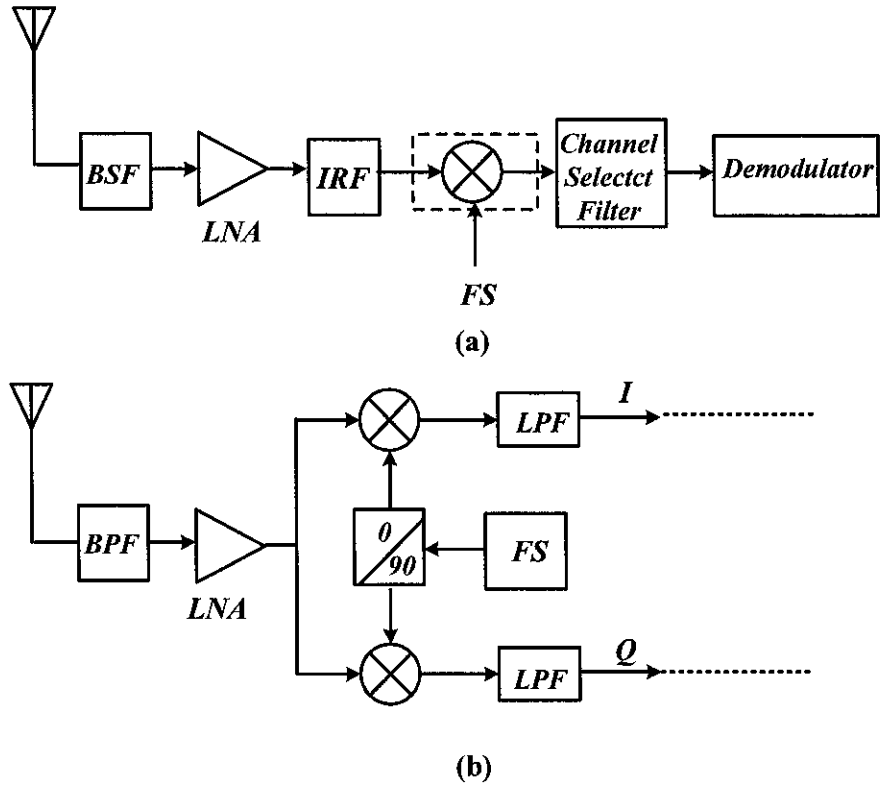


Figure 2.2 Block diagram of (a) heterodyne, (b) homodyne receivers

2.3 Frequency Synthesizer Architecture

Local oscillator is one of the important and critical part of the receiver architecture. LO generates a certain frequency and its frequency is divided depending on the architecture requirements. The divided frequency is used in mixer and other functional blocks. There are various types of frequency synthesizer architectures widely used to control the frequency, such as integer-N synthesizer [27], fractional-N synthesizer [28], [29], and dual-loop frequency synthesizer [30].

One of the proposed frequency synthesizer architecture for multi-band orthogonal frequency division multiplexing ($MB-OFDM$) for ultra-wideband (UWB) system is shown in Fig. 2.3 [31]. The architecture consists of two frequency dividers and three single-sideband mixers to generate the 3432 MHz, 3960 MHz and 4488 MHz frequencies. The basis of the frequency planing is as the following; each center frequency is generated by using a single-sideband (SSB) beat product of the oscillator frequency with another frequency derived from the oscillator. The other frequency is obtained by using a combination of frequency dividers and single-sideband (SSB) mixers.

For example, the center frequency of 4488 MHz is obtained by mixing the output of the VCO at 4224 MHz with 264 MHz (4224 MHz/16). To obtain a frequency of 3432 MHz, a 4224 MHz signal is mixed with 792 MHz. The 792 MHz signal is obtained by mixing 528 MHz (= 4224 MHz/8) with 264 MHz. By mixing 264 MHz signal with 4224 MHz, a 4488 MHz can be achieved [31].

2.4 CMOS Oscillator Basics and Main Types

Oscillator generates a time varying output when dc voltage is applied. The circuit should have self-sustaining mechanism which adds its own noise to grow and ultimately it becomes a periodic signal. A negative feedback system may oscillate or we can say oscillator is a badly designed feedback amplifier. Consider a simple feedback

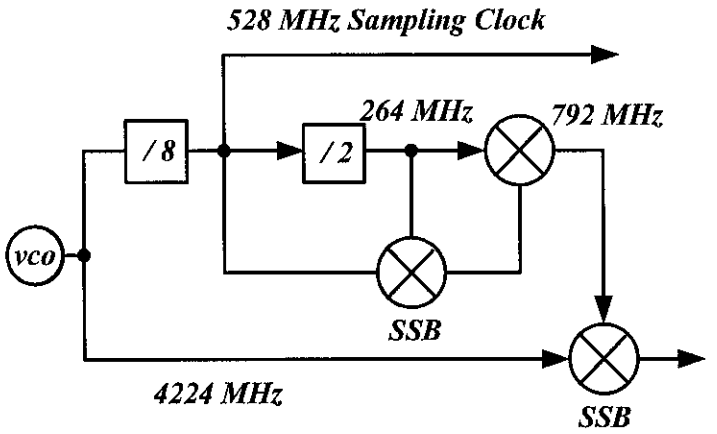


Figure 2.3 Example of MB-OFDM frequency synthesizer.

system shown in Fig. 2.4. The overall transfer function is given by Eq. (2.1).

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 - H(s)} \tag{2.1}$$

The oscillation may occur if the amplifier experiences enough phase shift at high frequencies ω_o at which overall feedback becomes positive. At ω_o, $H(j\omega_o)$ = -1, the closed loop gain reaches to infinity at ω_o. At this condition circuit amplifies its own noise components at ω_o indefinitely. However, we can conclude that circuit may oscillate if $|H(j\omega_o)| \geq 1$ and $\angle H(j\omega_o) = 180°$. This is also known as "Barkhausen criteria". In the practical consideration, the loop gain is normally chosen at least twice or three times the required value because of temperature and process variations [32].

Oscillators are widely used in different wireless applications. There are two main types of oscillators, one is ring oscillator and other is resonant oscillators. The ring oscillator and relaxation oscillator are major types of waveform oscillators. Low power, small die area and wide frequency tuning range are major advantages of the ring oscillator. On the other hand, when frequency increases the jitter and phase noise performance is degraded in ring oscillators. The relaxation oscillators have poor phase noise performance. In resonant oscillators, the crystal oscillators and *LC*-tank oscillators are widely used. In *RF* circuits, *LC*-tank or negative resistance and

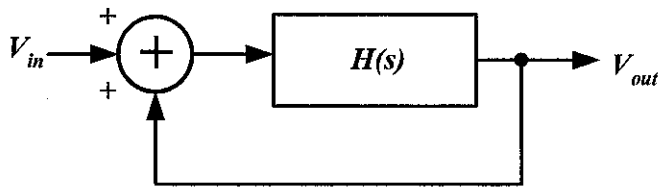


Figure 2.4 Feedback oscillatory system.

colpitts oscillator are mostly used. LC-tank oscillators exhibit outstanding phase noise performance. The LC-tank oscillator consists of inductor, varactor (variable capacitor) and active devices. However, the inductors and capacitors or varactors cover large area of the chip [32], [33], [34].

2.4.1 Spiral Inductor

The inductor is a major part of LC-tank circuits for the oscillators. The high quality factor (Q) of fully integrated inductor is one of the key challenges in the $RFIC$ design. In $RFIC$ design, significant research has been carried out to design the on-chip inductors. Therefore, Q factor of the inductor is challenging parameter in the $RFIC$ design and influences the performance of the transceivers. Fully integrated on-chip inductor results in smaller size of transceivers. The values of fully integrated inductors vary from 0.5 to 10 nH with the variation of quality factor and frequency range [12]. The Q factor of the inductor directly influences the phase noise performance of the oscillator. There are different types of the inductors used in today's oscillator architecture. In state of the art work, the monolithic inductors [35], active inductors based on the active device, [36] and micro-electro-mechanical system ($MEMS$) inductors [37] are used commonly.

The spiral inductor consists of self inductance and mutual inductance. The total inductance of the coil L_{tot} is expressed by Eq. (2.2),

$$L_{tot} = L_{self} + M_{+} - M_{-} \tag{2.2}$$

where L_{self} is the self inductance of all conductors segments, M_{+} is the mutual induc-

tance due to positive coupling between conductors and M_- is the mutual inductance due to negative coupling between conductors.

The mutual inductance is usually formed by the magnetic coupling between conductors. The mutual inductance value can be negative or positive depending on the opposite (out-of-phase) or same (in-phase) currents in the two conductors. It also depends on the distance between the two conductors. The mutual inductance is increased by increasing the number of the turns and dc resistance is decreased. Hence, the Q is increased. and can be expressed by Eq. (2.3).

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy lost per cycle}} \tag{2.3}$$

The energy stored by a inductor can be expressed by Eq. (2.4),

$$E_L = \frac{L.i_L^2}{2} \tag{2.4}$$

where i_L is the current flowing through the inductor. The inductor loss can be modeled as a series resistor R_L, and Q_L of inductor is given by Eq. (2.5) and Eq. (2.6),

$$Q = 2\pi \frac{\text{peak magnetic energy stored}}{\text{energy lost per cycle}} \tag{2.5}$$

$$Q = 2\pi \frac{\left(\frac{L.|i_L|^2}{2}\right)}{\left(\frac{R_L.|i_L|^2}{2T}\right)} \tag{2.6}$$

where the $|i_L|$ is the peak current flowing through inductor, T is the period of the cycle and ω is the operating frequency. Finally, the value of the Q is given by Eq. (2.7).

$$Q = \frac{\omega L}{R_L} \tag{2.7}$$

Skin effect is also one of the problem which results in the non-uniform current density at high frequencies. In this, the electromagnetic field and current in the

conductor decay rapidly and flows at the surface of the conductor. The eddy current effects should also be included in the value of R_L which is expressed as in Eq. (2.8),

$$R_L = \frac{l}{\omega.\sigma.\delta(1 - e^{-}t\delta)} \tag{2.8}$$

where σ is the conductivity of the conductor and δ is the skin depth which is given in Eq. (2.9),

$$\delta = \sqrt{\frac{1}{\pi\sigma\mu f}} \tag{2.9}$$

where μ is the relative permeability of the free space, is equal to $4\,\pi \times 10^{-7}$ H/m. While considering the conductor loss, the parasitic capacitance C_L, C_{ox}, C_{si} and resistance values R_{si} should be also be taken into account. The C_L can be expressed by Eq. (2.10),

$$C_L = n.w^2.\frac{\varepsilon_{ox}}{t_{oxm}} \tag{2.10}$$

where n is the number of the turns, w is metal width, ε_{ox} is the permittivity of the oxide layer between the two conductors, t_{oxm} is the thickness of the oxide layers between the two conductors.

The C_{ox} can be expressed by Eq. (2.11),

$$C_{ox} = \frac{1}{2}w.l.\frac{\varepsilon_{ox}}{t_{ox}} \tag{2.11}$$

where t_{ox} is the thickness of the oxide layer between inductor and substrate. The R_{si} and C_{si} can be expressed by Eq. (2.12) and Eq. (2.13) respectively,

$$R_{si} = \frac{2}{w.l.G_{sub}} \tag{2.12}$$

$$C_{si} = \frac{w.l.C_{sub}}{2} \tag{2.13}$$

where G_{sub} is the conductance per unit area, while C_{sub} is the substrate capacitance per unit area [18].

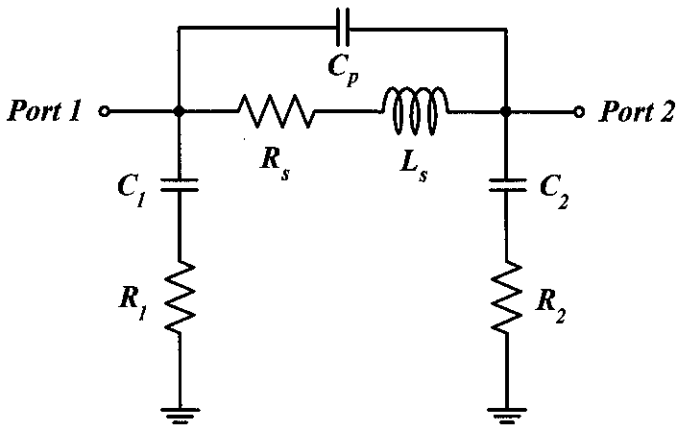


Figure 2.5 π-equivalent inductor model.

The most important parameter of the inductor design is quality factor (Q), the self resonance frequency and the size which depends on the layout and the process technology. The on-chip inductor size is in μm and usually covers the larger area on the chip [18]. The inductor equivalent circuit π-model is shown in Fig. 2.5. The inductor π-model can be extracted from y-parameters. The L_s describes the series inductance value and R_s describes the series resistance value, C_p models the capacitance between turns as well as the capacitance between underpass which connects the inner port of the inductor. R_1, R_2, C_1 and C_2 are the shield parasitics resistance and capacitance [35].

The on-chip inductors can be designed by Eq. (2.14),

$$L = \frac{\mu n^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho} + c_3\rho + c_4\rho^2\right)\right] \tag{2.14}$$

where μ is the permeability of the free space, ρ is the ratio of the $(d_{out}-d_{in})/(d_{out}+d_{in})$, d_{in} is the inner diameter of the inductor, d_{out} is the outer diameter, d_{avg} is the average diameter of the inductor equal to $(d_{out} + d_{in})/2$, c_1, c_2, c_3 and c_4 are model-fitting parameters depending on the geometrical layout [18].

Today, many tools are available for the design of the inductors such as "Analysis and Simulation of Spiral Inductors and Transformers" ($ASITIC$) [35], EM modulator, [38] "FastHenry" and "Momentum" (from ADS) [39]. These tools are very

helpful in the inductor design. All mentioned tools use process technology files in the design of the inductor. The process technology files are based on the various algorithms and parameters. This gives performance parameters such as Q, substrate capacitance and resistance values. The eddy current loss is the major problem faced with the inductors. Eddy current results in the loss of electromagnetic energy and low Q values [40].

2.4.2 Varactors

Varactor is one of the important component of LC-tank. Variable capacitor (varactor) is used to tune the oscillator frequency. The dc tune voltage of varactor is varied and frequency sweep is achieved. The Q factor of the capacitor is also one of the important factor in oscillator performance. The energy stored in the capacitor is given by Eq. (2.15),

$$E_c = \frac{C.v_c^2}{2} \tag{2.15}$$

where v_c is the voltage across capacitor and C is the capacitance value. The quality factor of a capacitor is given by Eq. (2.16),

$$Q = 2\pi \frac{\text{peak electric energy stored}}{\text{enegy lost per cycle}} \tag{2.16}$$

$$Q_c = 2\pi \frac{\left(\frac{C.|v_c|^2}{2}\right)}{\left(\frac{R_c|i_c|^2}{2T}\right)} \tag{2.17}$$

$$Q_c = 2\pi \frac{\left(\frac{|i_c|^2}{2\omega^2 C}\right)}{\left(\frac{R_c|i_c|^2}{2T}\right)} \tag{2.18}$$

$$Q_c = \frac{1}{\omega C R_c} \tag{2.19}$$

where v_c is peak voltage across capacitor and i_c is the peak current passing through the capacitor [18].

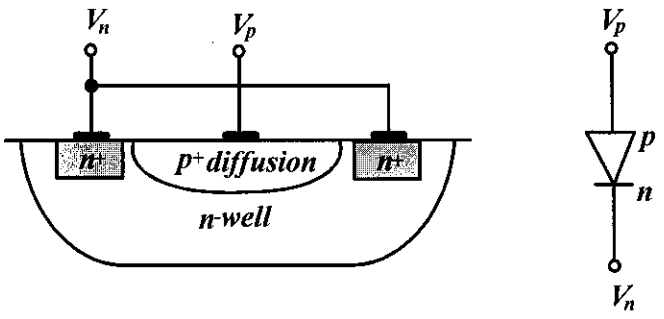


Figure 2.6 pn-junction diode varactor structure.

The *pn*-junctions and *MOS* varactors are two major types of varactors. Since, it is difficult to vary the monolithic inductors, so *LC*-tank capacitance is varied to tune the oscillator frequency. The reverse-biased *pn*-junction can serve as a varactor shown in Fig. 2.6.

The parasitic capacitance of the inductor and the transistors limit the tuning range because they cannot be varied with dc control voltage. The *pn*-junctions exhibits limited tuning range as capacitance varies slowly under reverse biasing and sharply under forward biasing condition. The other approach is *pMOS* varactors as shown in Fig. 2.7 (a). The drain, source and bulk are connected together. Depending on the gate to source voltage V_{gs} there could be different regions of operation. If $V_{gs} < V_{th}$ which corresponds the strong inversion mode operation of the *pMOS* varactor. In this mode, the channel consists of inversion layer and depletion region as shown in Fig. 2.7 (b). When V_{gs} is more positive and control voltage is negative then it corresponds to the accumulation mode, as shown in Fig. 2.7 (c). In this mode, the channel is populated by the majority of bulk charge carriers. In accumulation mode, the capacitance is given as $C_{ox} = \left(\frac{\epsilon_o}{t_{ox}}\right) WL = C_{max}$ [12], [23], [41].

2.5 LC Oscillator

LC oscillator consists of passive resonant circuits as shown in Fig. 2.8 (a). The inductor (L_1) and capacitor (C_1) resonate at frequency $\omega_{res} = 1/\sqrt{L_1 C_1}$. The

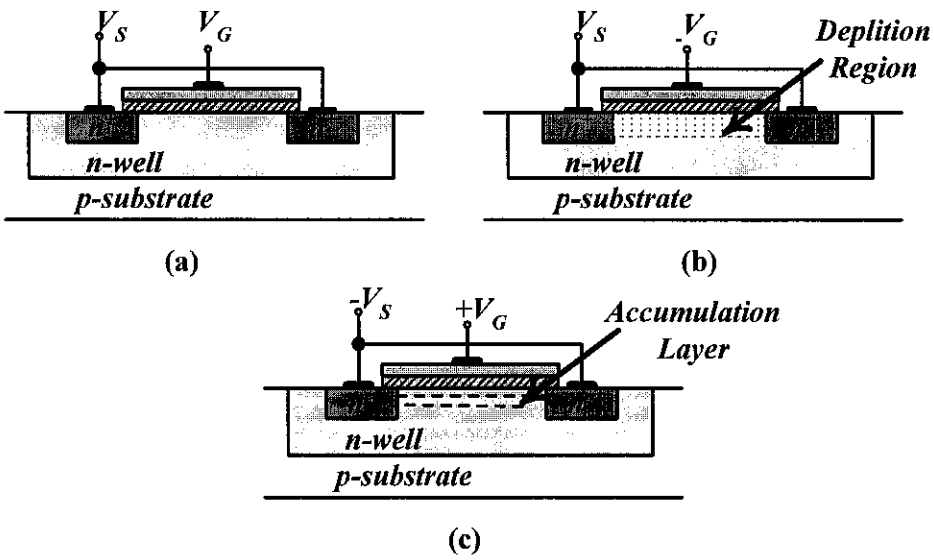


Figure 2.7 (a) MOS varactor structure, (b) MOS varactor in the depletion mode, (c) MOS varactor in the accumulation mode.

impedance of the inductor at this frequency is $j\omega_{res}L_1$ and capacitor $1/(j\omega_{res}C_1)$, are equal and opposite and thus resulting in infinite impedance and circuit may have infinite quality factor (Q). The inductors and capacitors actually suffer from resistive components. The series resistance of the metal wire used in inductor is shown in Fig. 2.8 (b). The Q factor of inductor is $L_1\omega/R_s$. The equivalent impedance is given by Eq. (2.20),

$$Z_{eq}(s) = \frac{R_s + L_1 s}{1 + L_1 C_1 s^2 + R_s C_1 s} \tag{2.20}$$

and the magnitude is given by Eq. (2.21).

$$|Z_{eq}(s = j\omega)|^2 = \frac{R_s^2 + L_1^2\omega^2}{(1 - L_1 C_1 \omega^2)^2 + R_s^2 C_1^2 \omega^2} \tag{2.21}$$

This shows that the impedance does not go to infinity and the circuit has some dependency on R_s. The series combination of the inductor is shown in the Fig. 2.8 (b) can be changed to parallel combination as shown in Fig. 2.8 (c). Fig. 2.8 (d) indicates the series combination of the inductor and series resistance and it can be changed to parallel combination which is shown in Fig. 2.8 (e). The L_p represents the

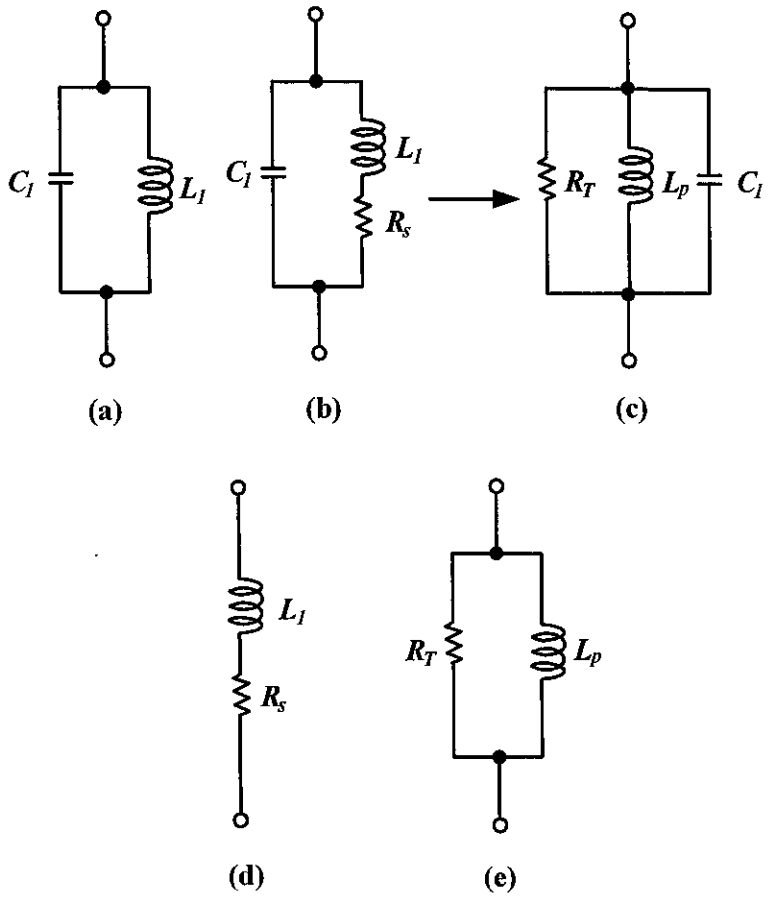


Figure 2.8 (a) Ideal (b) realistic LC-tanks (c) parallel and (d) series and (e) parallel conversion.

parallel equivalent tank inductance and R_T[3] represents the parallel equivalent tank resistance. For the two impedances to be equal:

$$L_1 s + R_s = \frac{R_T L_p s}{R_T + L_p s} \tag{2.22}$$

Let's consider only steady state response and substitute $s = j\omega$ in Eq. (2.22).

$$(L_1 R_T + L_p R_s) j\omega + R_s L_p - L_1 L_p \omega^2 = R_T L_p j\omega \tag{2.23}$$

The relationship holds for all values of ω,

$$L_1 R_T + L_p R_s = R_T L_p \tag{2.24}$$

$$R_s R_T - L_1 L_p \omega^2 = 0 \tag{2.25}$$

The value of R_T can be achieved as by Eq. (2.26).

$$L_p = L_1 \left(1 + \frac{R_s^2}{L_1^2 \omega^2}\right) \tag{2.26}$$

The $L_1\omega/R_s = Q$, value is greater than 3 for monotonic inductors. Hence, $L_p \approx L_1$

$$R_T \approx \frac{L_1^2 \omega^2}{R_s} \tag{2.27}$$

$$\approx Q^2 R_s \tag{2.28}$$

i.c. the parallel combination of the LC-tank reduces to a resistor, i.e. $1 = 1/\sqrt{L_p C_p}$. The phase difference between voltage and current drops to zero and magnitude of the tank versus frequency is shown in the Fig. 2.9. The behavior is inductive for $\omega < \omega_1$ and capacitive $\omega > \omega_1$. The phase of the impedance is positive for $\omega < \omega_1$ and negative for $\omega > \omega_1$ [12], [18], [42].

[3] R_p is a common abbreviation found in literature. However, R_T is also used instead, where T stands for "Tank".

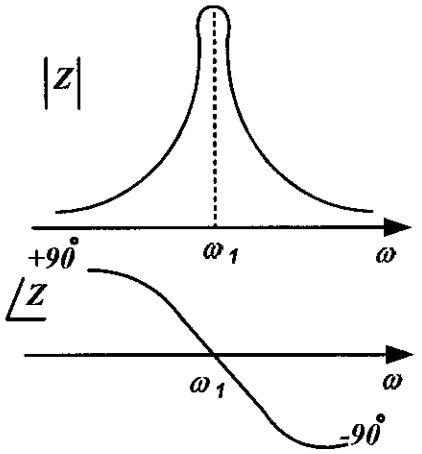


Figure 2.9 (a) Magnitude and (b) phase of the impedance of a LC-tank vs frequency.

2.5.1 Cross-Coupled Oscillators

The cross-coupled oscillator is shown in Fig. 2.10. It consists of two LC-tanks and cross-coupled active devices. The M_1 and M_2 should be identical and symmetrical. To find the input impedance R_{in}, of the cross-coupled pair, consider the Fig. 2.11 (a), in which small signal equivalent model of the transistor is shown. The small-signal equivalent model of the $nMOS$ cross-coupled pair is also shown in Fig. 2.11 (b), where V_{in} is the input voltage and I_{in} is the input current.

$$V_{in} = V_x - V_y \tag{2.29}$$

$$I_{in} = g_{m1}V_x = g_{m2}V_y \tag{2.30}$$

The R_{in} can be calculated as V_{in}/I_{in}

$$R_{in} = \frac{-\left(\frac{I_{in}}{g_{m1}} + \frac{I_{in}}{g_{m2}}\right)}{I_{in}} = \frac{-2}{g_m} \tag{2.31}$$

The differential output voltages V_x and V_y are 180° out of phase. The gain and phase of the of the cross-coupled oscillator are shown in Fig. 2.12. The two transistors

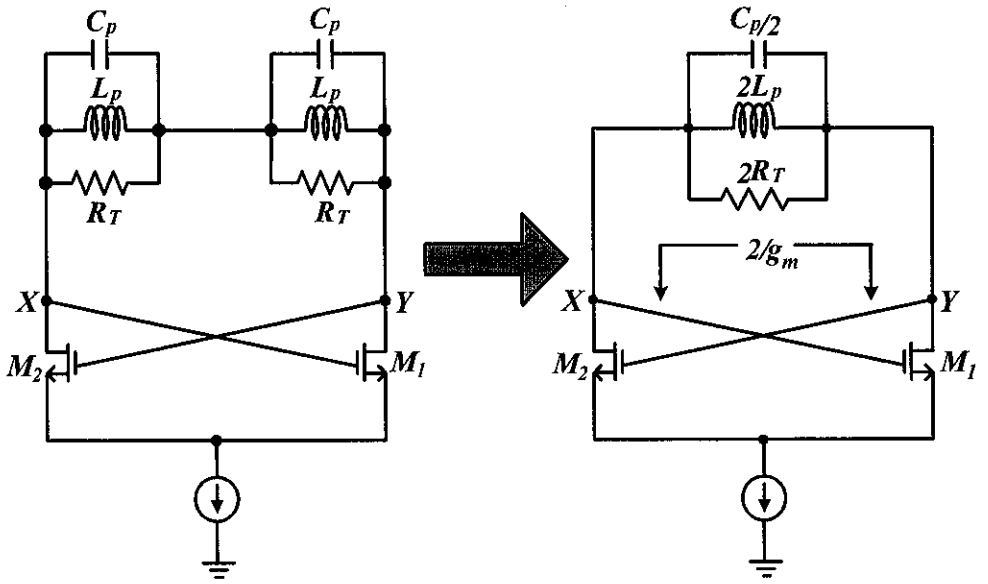


Figure 2.10 Cross-coupled oscillator.

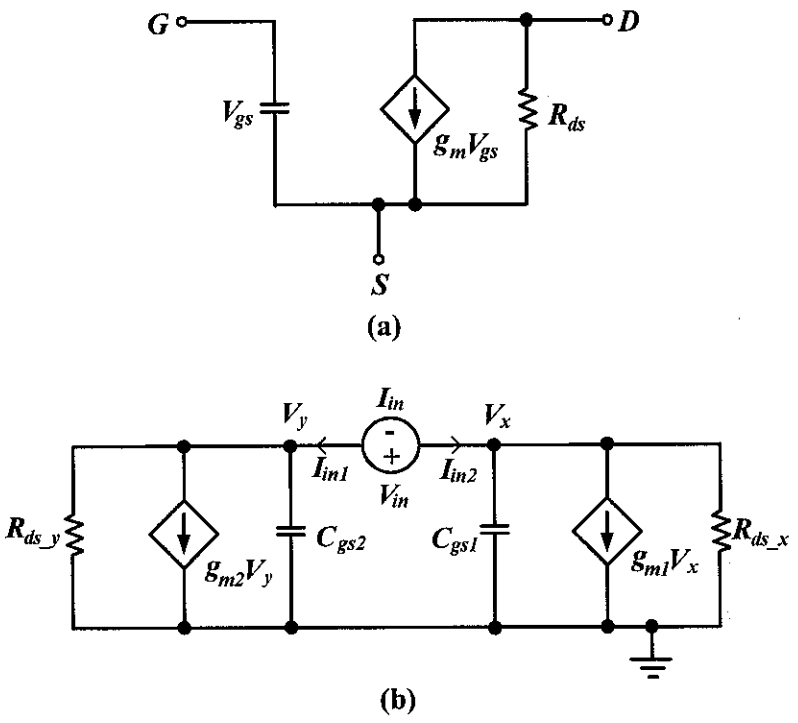


Figure 2.11 (a) MOS and (b) cross-coupled MOS equivalent model.

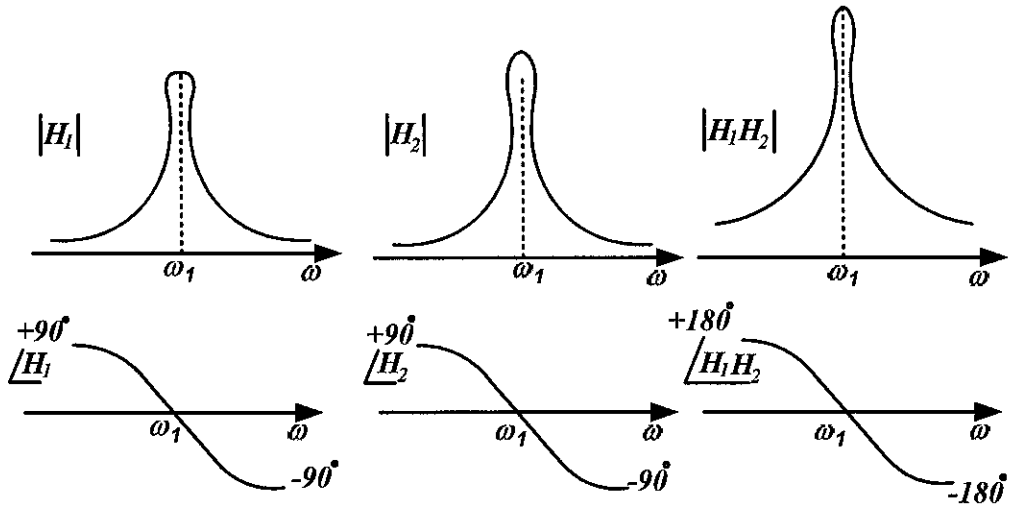


Figure 2.12 Magnitude and phase of the cross-coupled oscillator.

share the tail current equally. The circuit oscillates if $g_{m1}R_T g_{m2}R_T \geq 1$ where g_{m1} and g_{m2} are the transconductance of the transistors and R_T is the parallel tank resistance. The noise component at resonance frequency is continuously amplified by the active devices. The drain currents of M_1 and M_2 of the circuit varies according to the instantaneous values of V_x - V_y. The oscillation amplitude grows until the loop gain drops at the peaks, if the $g_{m1,2}R_T$ is sufficiently large and difference between V_x - V_y reaches a level that steers the entire tail current to one transistor, thus turning the other off. So, steady state currents I_{D1} and I_{D2} vary between zero and maximum current value [1], [12], [20].

There can be three possible situations by closely observing the closed-loop poles in the s-plane .

- If $g_m R_T < 1$ poles are located in left half s-plane, which shows oscillation will die.
- If $g_m R_T > 1$ poles are located in right half s-plane, which shows oscillation amplitude will grow.
- If $g_m R_T = 1$ poles are located on $j\omega$ axis, which shows that oscillation in steady

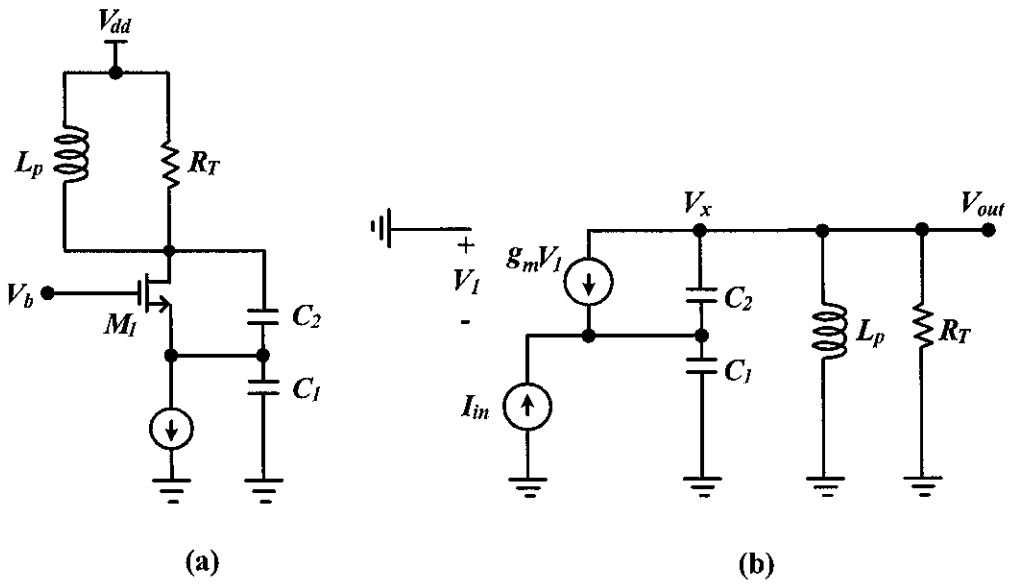


Figure 2.13 (a) Colpitts oscillator with input signal and (b) equivalent circuit model.

state and will be maintained [43].

2.5.2 Colpitts Oscillators

A colpitts oscillator consists of a single transistor and LC device. The capacitors and inductors determine the oscillation frequency of the circuit. The colpitts oscillator and it's equivalent circuit model is shown in Fig. 2.13 (a) and Fig. 2.13 (b), respectively. The current through the parallel combination of L_p and R_T is $V_{out}/(L_p s)$ + V_{out}/R_T and current through C_1 is equal to $I_{in} - V_{out}/(L_p s) - V_{out}/R_T$ which results in the expression given by Eq. (2.32).

$$V_1 = -\left(I_{in} - \frac{V_{out}}{L_p s} - \frac{V_{out}}{R_T}\right)\frac{1}{C_1 s} \tag{2.32}$$

The current through C_2 is $(V_{out} + V_1)C_2 s$ and the sum of the currents at output node results in Eq. (2.33).

$$\frac{V_{out}}{I_{in}} = \frac{R_T L_{ps}(g_m + C_2 s)}{R_T C_1 C_2 L_p s^3 + (C_1 + C_2)L_p s^2 + \left(g_m L_p + R_T(C_1 + C_2)\right)s + g_m R_T} \tag{2.33}$$

In Eq. (2.33), if $C_1 = 0$ the above equation reduces to $(L_p s \parallel R_T)$. The oscillator oscillates if the closed loop transfer function goes to infinity at an imaginary value of s, $s_R = jw_R$ and both of real and imaginary parts drops to zero at this frequency.

$$- R_T C_1 C_2 L_p \omega_R^3 + \Big[g_m L_p + R_T (C_1 + C_2) \Big] \omega_R = 0 \tag{2.34}$$

$$- (C_1 + C_2) L_p \omega_R + g_m R_T = 0 \tag{2.35}$$

Eq. (2.34), the $g_m L_p \ll R_T (C_1 + C_2)$ and results in the following expression given in Eq. (2.36).

$$\omega_R^2 = \frac{1}{L_p \left(\frac{C_1 C_2}{C_1 + C_2} \right)} + g_m R_T \tag{2.36}$$

From Eq. (2.35) the expression can be written as in Eq. (2.37),

$$g_m R_T = \frac{(C_1 + C_2)^2}{C_1 C_2} \tag{2.37}$$

where $g_m R_T$ is the voltage gain from the source of the M_1 to the output if $(g_{mb} = 0)$. This shows the minimum required gain to start the oscillation [12].

$$g_m R_T \geq 4 \tag{2.38}$$

However, in previous calculations capacitance C_p is neglected which appears in parallel with inductor. In Eq. (2.36), the capacitance C_p is included, the expression becomes Eq. (2.39),

$$\omega_R^2 = \frac{1}{L_p \left(C_p + \frac{C_1 C_2}{C_1 + C_2} \right)} \tag{2.39}$$

where C_p is included in parallel with series combination of the C_1 and C_2 [12].

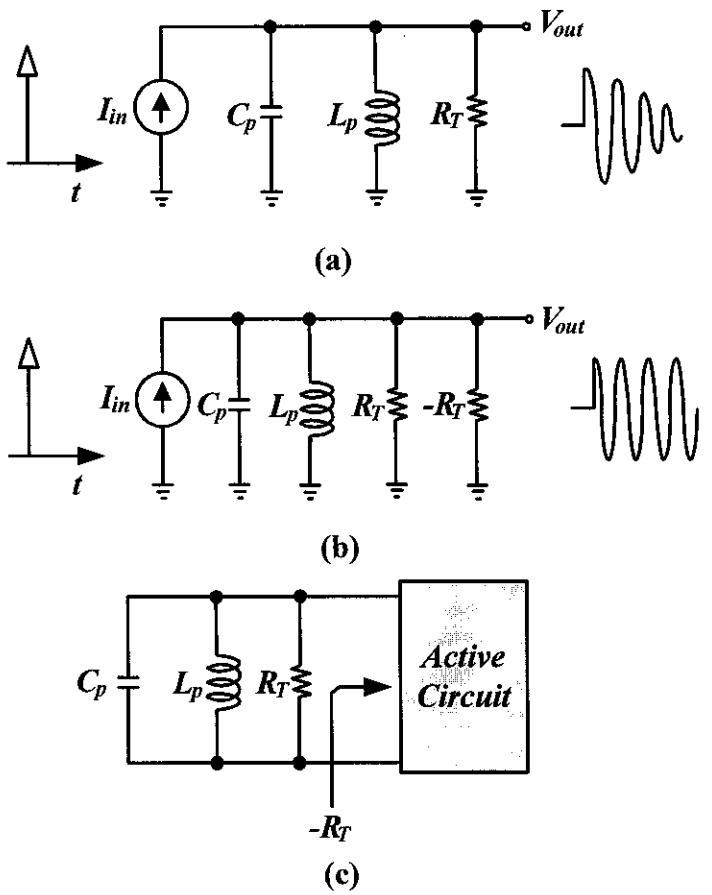


Figure 2.14 (a) Decaying impulse response of a tank, (b) addition of negative resistance to cancel in R_T and (c) use of active circuit to provide negative resistance.

2.5.3 Negative ($-G_m$) Oscillators

The LC oscillator consists of inductor, varactors (variable capacitors) and active device. Let's consider the LC-tank circuit as shown in Fig. 2.14 (a). When energy is injected in the circuit, the LC-tank tends to oscillate. The tank does not oscillate indefinitely because some of the stored energy is dissipated in R_T in every cycle. It results in decaying impulse response of the tank. The tank loss introduced by the inductors and capacitors are lumped into parallel resistor R_T with the equivalent inductance L_p and capacitance C_p. The LC resonator and its equivalent circuit

with parasitic resistance is shown in Fig. 2.14 (b). In Fig. 2.14 (c), to compensate tank energy the active device generates an impedance equal to $-R_T$. Therefore, $R_T \| (-R_T) = \infty$ and such topology is known as one-port oscillator. At resonance, the oscillation frequency is given as $\omega_{res} = 1/\sqrt{LC}$. The negative transconductance $(-G_m)$ VCO consists of LC-tank and one or two blocks of cross-coupled MOS transistors. The gate of one transistor is connected to the drain of the other and vice versa. The conductance observed from the drains of the two cross-coupled transistor block is negative and its value is $-G_m = -g_m/2$ (that is the reason these circuits are called $-G_m$ oscillators). There is direct dependence between the biasing of these transistors and the value of the negative resistance of the energy restorer in these oscillators. The $nMOS$ only cross-coupled oscillator transistors connected to the tank by its drains. They are biased by a resistor connected between the MOS source and ground or between tank or V_{dd}, as shown previously in Fig. 2.10. The drawback of this topology is the direct dependence of circuit properties with the voltage source fluctuations and technology parameter variations (e.g. V_{gs} voltage modifies the bias current). The non-constant value of the bias current can lead to an increment in the phase noise. The general definition of the $MOSFET$ small-signal transconductance is given by Eq. (2.40),

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{th}) \tag{2.40}$$

where μ_n is the effective electron mobility in the channel and C_{ox} is the oxide capacitance. The appropriate transconductance value depends on the LC-tank components and on the resistive parasitic components from the cross-coupled active devices. If the gain is too low the oscillation will not be sustained and if its value is too high there will be more parasitic and higher current consumption [12], [32], [44].

2.6 CMOS VCO Topologies

There are numerous $CMOS$ VCO topologies which are available in today's communication systems. The single switch VCO $(SS-VCO)$ and double switch $(DS-$

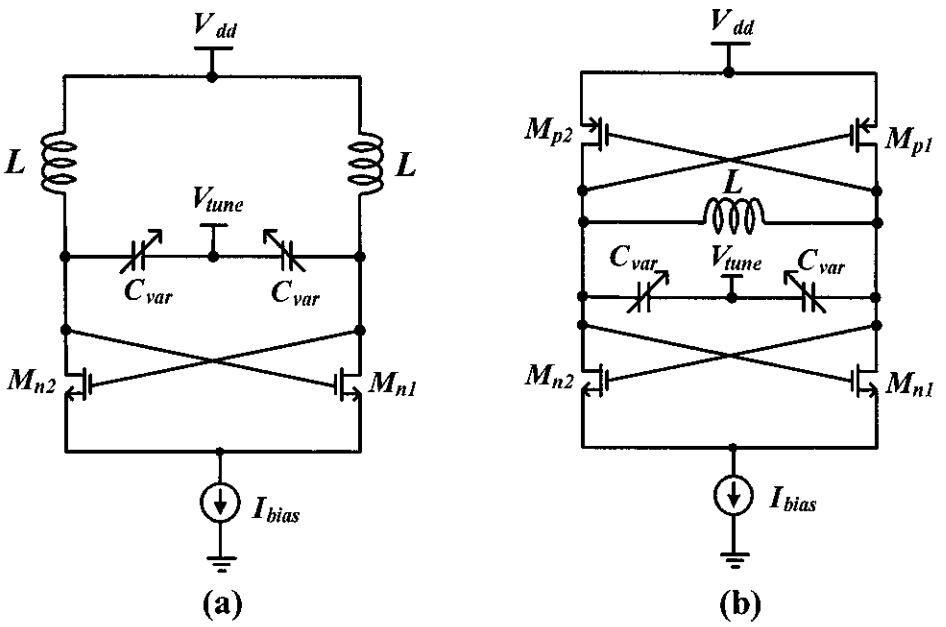


Figure 2.15 A circuit of VCO (a) $SS-VCO$, (b) $DS-VCO$.

VCO) are most commonly used in $RFIC$ transceiver architectures. Both uses negative resistance concept to cancel the losses in resonator. The transistor dimensions are set to achieve the required value of the negative resistance. The inductor Q factor also influences the performance of the VCO. High Q value of the inductors and enough transconductance of the active device leads to the higher amplitude of the VCO output swing. There are different biasing techniques used in $VCOs$ such as tail biasing, capacitive coupling and top biasing of the VCO circuit. By adding tail biasing i.e. current source effects the phase noise and oscillation amplitude of the VCO. The $1/f$ noise of the current mirror or current source is added in the VCO circuit and leads to the degradation in the phase noise of the VCO. Different techniques are used to reduce the $1/f$ noise by adding inductor degeneration or filters circuits. The basic $SS-VCO$ consists of two $nMOS$ cross-coupled transistors connected to the tank by its drains. The biasing is carried out by using a current source between MOS source and ground terminals (or between tank and V_{dd}), as shown in Fig. 2.15 (a). The drawback of this topology is the direct dependence of the properties of the

circuit with the voltage source's fluctuations and technology parameter variations. The non-constant value of the bias current can lead in poor phase noise. However, on the other hand $DS-VCO$ uses two blocks of cross-coupled pair transistor $pMOS$ and $nMOS$ and an MOS current source as shown in Fig. 2.15 (b). Cross-coupled oscillators have been preferred over other topologies due to their ease of implementation, relaxed start-up condition and differential operation.

The noise generated by the active devices of the complementary cross-coupled oscillator is maximum when the oscillator's phase is sensitive to perturbations. In this topology, the noise generated by both $pMOS$ and $nMOS$ transistors add to the overall active noise of the oscillator. The complementary cross-coupled $(DS-VCO)$ oscillator shows a better phase noise performance when compared to $SS-VCO$ for the same supply voltage and the bias current.

The complementary cross coupled oscillator presents a larger maximum output swing than $SS-VCO$ only cross-coupled oscillators. In complementary cross coupled oscillator, the additional $pMOS$ device enhances the overall phase noise performance. However, the major disadvantage of the $DS-VCO$ is that $pMOS$ device exhibits larger parasitic capacitances such as gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} usually five times more than the $nMOS$ device. However, the overall $1/f$ noise is not degraded as in $SS-VCO$ structure [12], [45], [46].

2.7 Quadrature Voltage Controlled Oscillator

The coupling is an external injection of the signal and results in the change or perturbation of the oscillation. Let's consider the VCO with $nMOS$ coupling M_{c1} and M_{c2} in Fig. 2.16 (a), and small-signal model in Fig. 2.16 (b). The V_{in} is injected at the gate of M_{c1} and M_{c2}, respectively. The output signal is injected into the LC-tank. If the frequency of V_{in} is same as the oscillation frequency of the oscillator, the coupling will shift only the phase of V_{out}. Therefore, the sum of $I_{Dc1}+I_{Ds3}$ and $I_{Dc2}+I_{Ds4}$ are changed by V_{in}, where I_{Dc} represents the drain current of the coupling transistor and I_{Ds} is the drain current of the switching transistor. Hence,

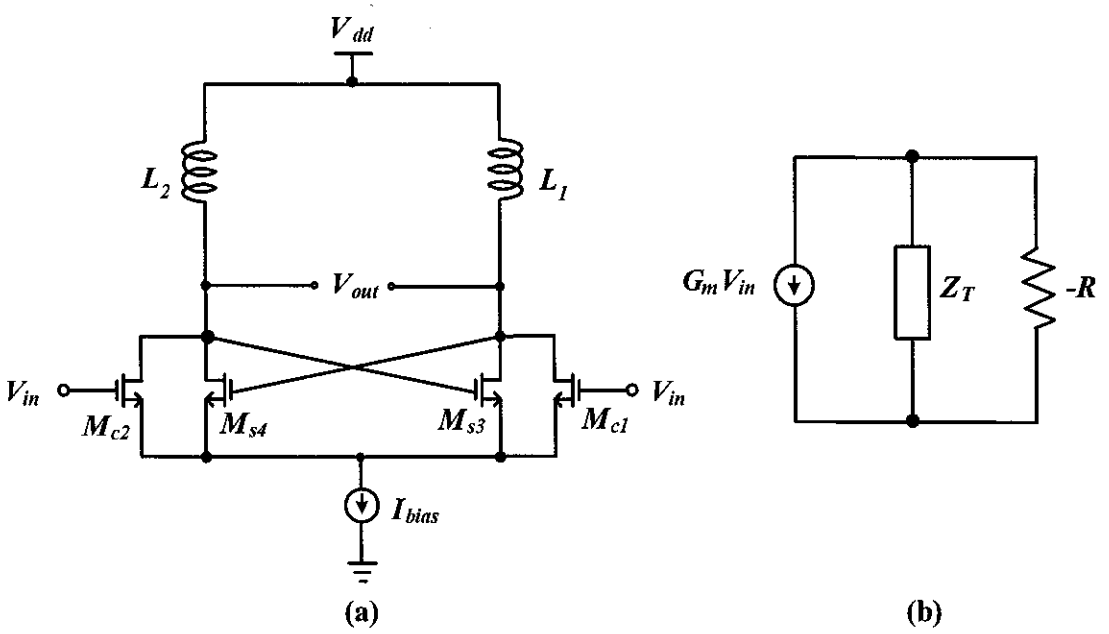


Figure 2.16 (a) Signal injection in oscillator (b) small-signal model.

the same property is adopted in quadrature VCO. This kind of coupling is called as unilateral coupling, as coupling from V_{in} to V_{out} is greater than that of V_{out} to V_{in}. The G_{mc} in a simple model represents the transconductance of the differential pair and Z_T shows the total tank impedance and $-R$ is negative resistance provided by the cross coupled pair. The $-R$ exactly cancels the loss in Z_T and ratio of the I_{Dc1}/I_{Ds3} or I_{Dc2}/I_{Ds4} are the coupling ratio. The two identical oscillators are coupled with parallel coupling transistors and operate with 90° phase difference. The quadrature voltage controlled oscillator provides quadrature output with the phase difference of 90° is shown in the Fig. 2.17 (a). The $QVCO$ consists of two fully differential LC-tank coupled $VCOs$. The $QVCOs$ are coupled in many ways, the most common method is using $nMOS$ transistors which forces the outputs of differential VCO to oscillate with phase difference of 90°. The small-signal equivalent model of $QVCO$ is shown in the oscillator Fig. 2.17 (b). The parallel combination of the $-R$ and Z_T is $-RZ_T/(Z_T - R)$, the value of V_2 and V_1 are computed as given by Eq. (2.41) and in Eq. (2.42), respectively.

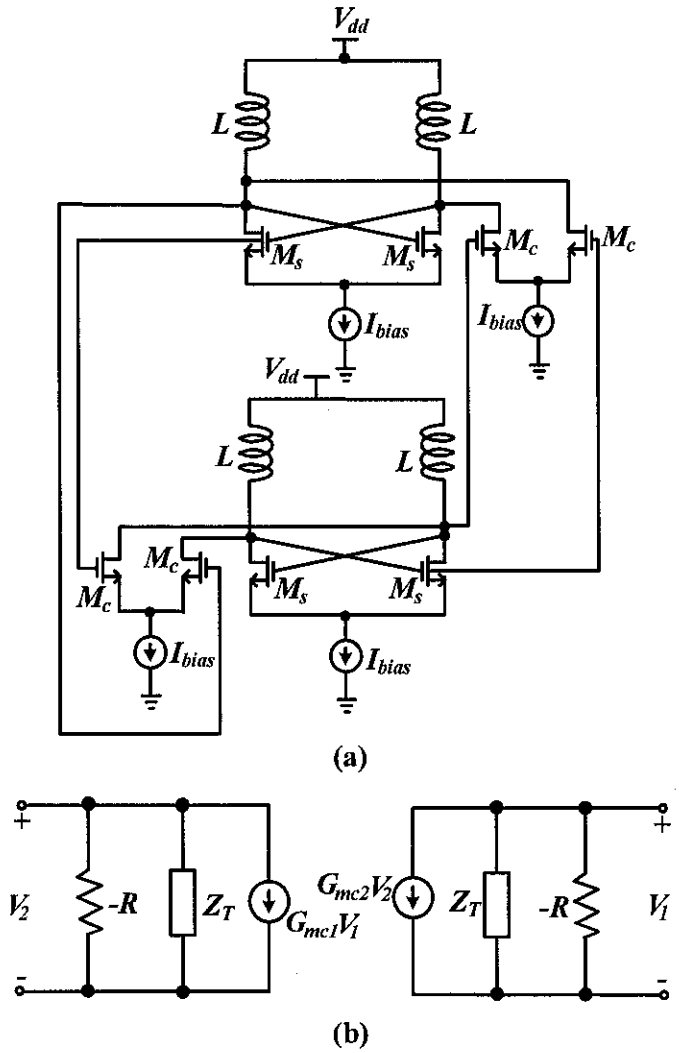


Figure 2.17 (a) Two oscillator coupled together (b) small-signal model of coupled oscillators.

$$V_2 = \frac{G_{mc}V_1(-RZ_T)}{Z_T - R} \tag{2.41}$$

$$V_1 = \frac{G_{mc}V_1(-RZ_T)}{Z_T - R} \tag{2.42}$$

Dividing Eq. (2.41) by Eq. (2.42) and considering V_1, $V_2 \neq 0$.

$$G_{mc1}V_1^2 - G_{mc2}V_2^2 = 0 \tag{2.43}$$

The Eq. (2.43) results in two following cases:

- If $G_{mc2} = G_{mc1}$, then $V_1 = \pm V_2$ which means that both oscillators operate with a phase difference of zero or 180°. It is called as in-phase coupling.
- If $G_{mc1} = -G_{mc2}$ then $V_1^2 + V_2^2 = 0$ and thus $V_1 = \pm jV_2$, this means that the phase difference is ± 90°. This kind of case is called as anti-phase coupling.

The proper sizing ratio of coupling transistor to switching transistor results in better phase noise results and less phase error. The width ratio of coupling transistor W_c to switching transistor W_s is called as coupling factor (K) given in Eq. (2.44) [12], [47].

$$K = \frac{W_c}{W_s} \tag{2.44}$$

There is one drawback associated with the coupling transconductance on the $QVCO$ oscillation frequency. The direct coupling of the transconductances attached to the LC-tank circuit can cause the center frequency deviation from its actual frequency by the factor Δf. The frequency shift can be calculated by Eq. (2.45),

$$\Delta f = \pm\frac{G_{mc}}{4\pi C} \tag{2.45}$$

where G_{mc} is the coupling transistor transconductance [48]. The asymmetrical frequency characteristic of LC-tank influences the frequency shift and results in the frequency change. The frequency change is added in actual oscillation frequency [49].

The frequency shift depends on the series loss of the individual LC-tank components. When inductor exhibits greater series loss (lower Q) than capacitor (varactor), the positive frequency shift occurs and when capacitor loss dominates, the negative shift occurs, respectively [50]. The actual frequency of the $QVCO$ can be calculated as by Eq. (2.46) [48],

$$f'_{osc} = f_{osc} + \Delta f \tag{2.46}$$

where f'_{osc} is the oscillation frequency of the $QVCO$ and is expressed by Eq. (2.47).

$$f'_{osc} = \frac{1}{2\pi\sqrt{LC}} \pm \frac{G_{m_c}}{4\pi C} \tag{2.47}$$

The different types of $QVCO$ architectures are available in the state of the art work. A quadrature colpitts VCO with a series-injection scheme for quadrature signal generation is also used low phase noise and better quadrature accuracy [51]. The LC series injection parallel coupled ($SIPC$) $QVCO$ topology is also adopted with the integration of open drain buffers. The use of open drain buffers results in the increased power consumption [52]. The low phase noise and low phase error $QVCO$ is also reported with the improvement of 6.3 dBc/Hz [53]. The 1.8 GHz LC $QVCO$ describes the improvement of phase noise and achieves quadrature accuracy [48]. The $QVCO$ is also designed with self-calibration technique. This uses a low speed amplitude error detector instead of a conventional high speed phase error detector. This compensates for phase noise and phase errors of LC $QVCO$ [54].

2.8 Oscillator Performance Parameters

Oscillator performance depends on various parameters. Some of the important parameters such as phase noise issues and figure of merit will be discussed in the following section.

2.8.1 Phase Noise

The phase noise in the oscillator has great importance because poor phase noise can lead to the degradation in the performance of the whole transceiver. Oscillator

consists of active and passive devices. Noise sources can be divided into two groups, namely device noise and interference. All devices exhibits some noise such as thermal noise, flicker noise and shot noise which lies in the category of device noise. Therefore, the substrate noise in the later group. Phase noise is the random variation of the frequency signal from its actual position or from its ideal position. The phase noise in actual oscillator cannot be removed totally and there is no phase noise in an ideal oscillator. The output spectrum of the ideal oscillator and actual oscillator is shown in the Fig. 2.18 (a) and (b) respectively [22], [55].

In *RF* circuits, the phase noise means that the output signal contains the energy components at other frequencies rather than from its carrier signal frequency. In actual oscillator the spectrum exhibits some skirts around the carrier signal while ideal oscillator's spectrum exhibits impulse shape. To express the phase noise we consider the unit bandwidth at an offset frequency of $\Delta\omega$ with respect to ω_o or we can say that ratio of power at particular offset frequency ($\Delta\omega$) from the carrier to the power at center frequency. The phase noise unit is "dBc/Hz". The phase noise can be expressed by Eq. (2.48),

$$L(\Delta\omega) = 10\log\left(\frac{P_{1Hz}(\omega_o + \Delta\omega)}{P_c}\right) \tag{2.48}$$

where P_c is the carrier power and ω_o represents the carrier frequency. The above expression shows that phase noise can be improved significantly as P_c is increased [56].

2.8.2 Leeson's Equation

D. B. Lesson [57] summarized the phase noise characteristics for oscillators. The phase perturbation at the oscillator input due to noise variation results in the frequency shift at the output. However, the single side band (SSB) noise exhibits the slope of $1/f^3$ which is 30 dB/decade at the offset frequencies below the flicker noise $1/f^2$ (20 dB/decade). The third part is $1/f$ noise which is called as thermal noise or noise floor at high offset frequencies. The asymptotic phase noise versus offset

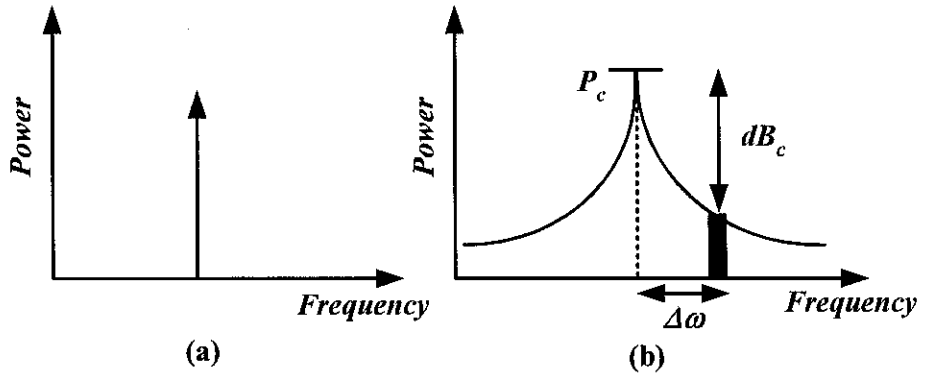


Figure 2.18 Frequency spectrum of an (a) ideal oscillator, (b) practical oscillator.

frequency of the oscillator is given in Fig. 2.19. The Leeson's equation is given by Eq. (2.49),

$$L(f_m, K_{vco}) = 10\log\left[\left(\frac{f_\circ}{2Qf_m}\right)^2\left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{f_m}\right)\right]+\frac{1}{2}\left(\frac{K_{vco}V_m}{2f_m}\right)^2\right] \tag{2.49}$$

where $L(f_m, K_{vco})$ represents the phase noise in dBc/Hz, $f_\circ$ is oscillation frequency (Hz), f_m is the offset frequency from the carrier in Hz. The F is a noise figure of the transistor amplifier, k is boltzman's constant in J/K, T is temperature in Kelvin, P_s shows the RF carrier output power in Watts, f_c is the flicker power corner in Hz, K_{vco} is VCO gain in Hz/V and V_m is the total amplitude of all low frequency noise sources [57].

The Eq. (2.49) shows that phase noise decreases as the square of the ratio of the sideband frequency f_m to oscillator carrier frequency $f_\circ$. It is also proportional to the $(FkT/2)$, which is the phase noise and half of the thermal noise appears at the input of the amplifier stage of oscillator. The dominant phase noise factor is P_sQ^2 and it should be large as possible to achieve better phase noise in $1/f^2$. The P_sQ^2 is the almost totally dominated by the tuning varactor, which is the only practical choice for the fast voltage controlled tuning over the required frequency range. The analysis of the passive devices is the key factor for the successful VCO design. The

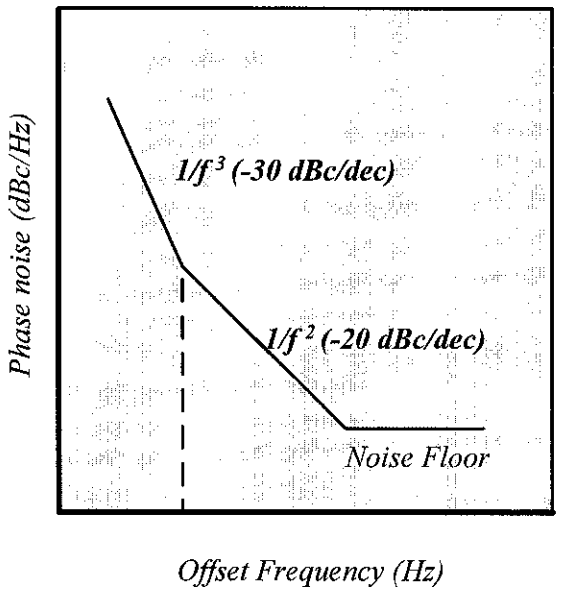


Figure 2.19 Oscillator SSB phase noise as a function of baseband frequency.

major drawback of the Leeson's equation is unspecified noise factor of proportionality F which depends on the oscillator topology.

There are many modifications carried out in Leeson's equation to express the phase noise analysis. However, the Abidi [58] has provided the unspecified noise factor of the Leeson's equation and the oscillator topology is also specified. Despite these analysis, the Leeson's equation do not give the accurate phase noise analysis. The Leeson's equation cannot make quantitative predictions about the phase noise, which shows that at least some of the assumption used in derivation is invalid or does not give the accurate picture.

However, there are many different techniques used to reduce the phase noise of oscillators, such as filtering technique to remove the high frequency noise [59]. The Lesson's equation is also modified and unspecified noise factor is expressed [58]. The influences of amplitude modulation to phase modulation due to varactors [60], modulation influences of tail capacitance [61] biasing circuit phase noise contribution such as tail biasing resistors [62] are also reported. The multifinger gate structure of the

MOS varactors is also implemented to reduce the $1/f$ noise contribution [63]. The source degeneration resistor is also implemented to reduce $1/f$ noise contribution in the oscillator circuits [64].

2.8.3 Linear Time Varient (LTV) System

The linear time-variant (LTV) phase noise model gives deep quantitative design but limited in their quantitative predictive power. Therefore, the LTV systems cannot perform frequency translation. The most importance of the LTV is the introduction of impulse sensitivity function (ISF). ISF quantitatively explains the effects of cyclostationary noise sources in oscillator .

To show the failure of time-invariance system and to explain the time-variance system in oscillators, let's examine an ideal noiseless LC-tank, in which impulse of current influences the system waveform. Consider an ideal LC-tank in Fig. 2.20, which is oscillating with some constant amplitude. Now, some energy is injected into the system and it tends to iterate between LC-tank and sinusoidal wave is observed, shown in Fig. 2.20. The dotted lines represent the presence of noise. The changes in the waveform is observed with the injection of $\delta(t-\tau)$ at different τ timings. It causes the displacement in the charge ΔQ across capacitor. The amplitude increases by the amount of $\Delta V = \frac{\Delta Q}{C}$. There are two cases, in first case, when impulse is injected at the peak of the oscillation the displacement of ΔV is observed but no change in the zero crossing of the waveform. Therefore, there is no impact in change of the phase. In second case, when impulse is injected near zero crossing of the wave, the significant change in the phase occurs while amplitude remains same. The impulsive input produces a step change in the phase, the impulse response can be written by Eq. (2.50),

$$h_\phi(t-\tau) = \frac{\Gamma(\omega_\circ \tau)}{q_{max}} u(t-\tau) \tag{2.50}$$

where $u(t)$ is a unit step function. The Γ is known as ISF and it is dimensionless, fre-

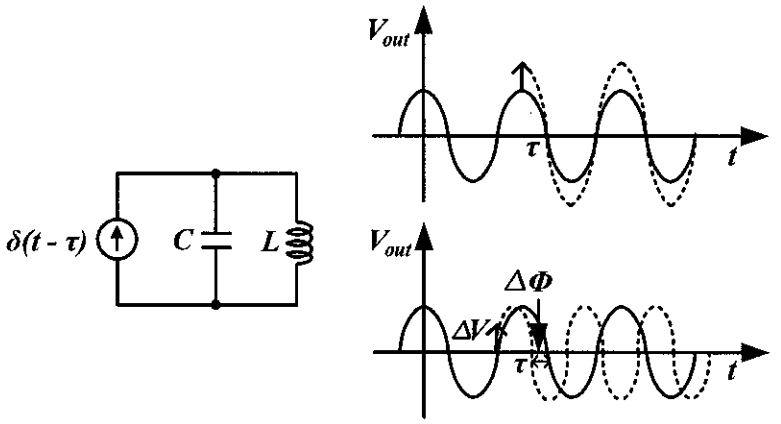


Figure 2.20 Impulse response of LC-tank.

quency and amplitude-independent function are periodic in 2π, q_{max} is the maximum charge around capacitor. The ISF has its maximum value near the zero crossings of the oscillation and zero value at maxima of the oscillation waveform.

After finding the value of ISF, we may compute the excess phase induced by the current $i(\tau)$ and is given by Eq. (2.51).

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_o \tau) i(\tau) d\tau \tag{2.51}$$

As ISF is a periodic in nature then we can expand it by using fourier series which is given by Eq. (2.52),

$$\Gamma(\omega_o \tau) = c_o + \sum_{n=1}^{\infty} c_n \cos(n\omega_o \tau + \theta_n) \tag{2.52}$$

where c_n is real and θ_n is the phase noise of n^{th} order harmonic of ISF and c_o is dc coefficient of the ISF. Consider a noise current $i(t)$, which is given by Eq. (2.53),

$$i(t) = I_n \cos\Big[(n\omega_o + \Delta\omega)t\Big] \tag{2.53}$$

where $\Delta\omega \ll n\omega_o$. By substituting Eq. (2.52) and Eq. (2.53) into Eq. (2.50) we will get the expression for $\phi(t)$ as given by Eq. (2.54).

$$\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \left(c_\circ + \sum_{n=1}^{\infty} c_n \cos(n\omega_\circ \tau) \right) I_n \cos(n\omega_\circ + \Delta\omega)\tau d\tau \tag{2.54}$$

The general solution of Eq. (2.54) is given below by Eq. (2.55).

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{max}\Delta\omega} \tag{2.55}$$

For $n = 0$, the $\phi(t)$ can be expressed by Eq. (2.56).

$$\phi(t) \approx \frac{I_\circ c_\circ \sin(\Delta\omega t)}{q_{max}\Delta\omega} \tag{2.56}$$

In Fig. 2.21, the results from Eq. (2.55) and Eq. (2.56) are summarized. This shows that the components of noise near integer multiples of carrier frequency which causes two equal sidebands at $\pm\ \Delta\omega$. Noise near dc gets upconverted, weighted by coefficient and $1/f$ device noise becomes $1/f^3$ noise near the oscillation frequency. The noise near the carrier is given by c_1 and white noise near higher integer multiples of the carrier undergoes down conversion, changing to $1/f^2$ region. By considering the fact, that injected noise result in two equal sidebands $\omega_\circ \pm \Delta\omega$ with the sideband reference around the carrier frequency signal. The noise power relative to carrier can be calculated by Eq. (2.57),

$$P_{dBc}(\Delta\omega) = 10\log\left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2 \tag{2.57}$$

where I_n is the amplitude of the noise component and it should be converted to root mean square (rms) value. It is clear that by minimizing the various coefficients c_n will minimize the ISF. Hence, the phase noise will be minimized. To underscore this point quantitatively, we may use Parseval's theorem and can be expressed by Eq. (2.58),

$$\sum_{n=1}^{\infty} c_n^2 = \frac{1}{\pi} \int_0^2 \pi |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \tag{2.58}$$

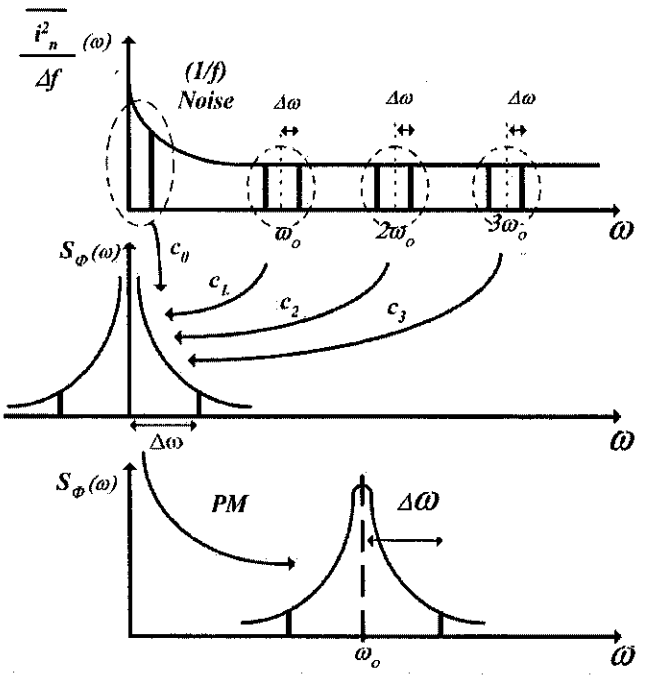


Figure 2.21 Conversion of noise source to phase fluctuations and phase noise side bands.

where Γ^2_{rms} is the rms value of the ISF. The phase noise in the $1/f^2$ region can expressed by Eq. (2.59).

$$L(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma^2_{rms}}{2q^2_{max}\Delta\omega^2}\right) \tag{2.59}$$

In Eq. (2.59), if all terms are fixed then phase noise can be improved by reducing Γ^2_{rms}. The $1/f^3$ region phase noise can be expressed by Eq. (2.60).

$$L(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}c_0^2}{8q^2_{max}\Delta\omega^2}\cdot\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.60}$$

Similarly, the $1/f^3$ corner in phase noise spectrum can be given by Eq. (2.61),

$$\omega_{1/f^3} = \omega_{1/f}\frac{c_o^2}{4\Gamma^2_{rms}} \approx \omega_{1/f}\left(\frac{c_o}{c_1}\right)^2 \tag{2.61}$$

where c_o is dc value of ISF and c_1 is the rms value of ISF. The ISF is a function of waveform, and under the control of the designer, normally by the adjustment

of rise and fall of wave i.e. by symmetrical waveform signal. These results are not anticipated by LTI approaches, and one of the deep insights by LTV model [19], [65]. The LTV model helps to describe most accurate phase noise for the oscillators. The LTV phase noise model is the most accurate model used for the prediction of phase noise in oscillator circuits. We can deduce following points from this model:

1. The ISF coefficients (c_n) should be minimized to achieve the low phase noise. The c_0 is important factor which results in up-conversion of $1/f$ noise.

2. The symmetry in the output waveform signal of oscillator can lead to minimization of phase noise.

3. The noise near integer multiples of the carrier frequency is up and down converted into close in phase noise.

4. The oscillation amplitude should be maximized to achieve better phase noise results. The quality factor of the LC-tank should be maximized.

2.8.4 Figure of Merit (FOM)

The figure of merit (FOM) is one of the key factors which is most widely used to examine the performance of the oscillator. The phase noise, power dissipation, offset frequency and carrier frequency are used in the formulation. The designers use this formulation to compare their oscillator performance with the state of the art work. Low phase noise at higher frequencies is one of the key challenges which is observed with FOM. The FOM can be given by Eq. (2.62),

$$FOM = L(\Delta\omega) + 20\log\left(\frac{\omega_o}{\Delta\omega}\right) - 10\log\left(\frac{P_{diss}}{1mW}\right), \tag{2.62}$$

where P_{diss} is the dc power dissipated in the oscillator and $L(\Delta\omega)$ is the phase noise [65], [66]. The Eq. (2.62) is used throughout in this thesis to calculate FOM.

2.8.5 Frequency Tuning Range

The output frequency of the oscillator is varied by varying the dc tune voltage, it is known as voltage controlled oscillator (VCO). The required tuning range is dictated by the variation of the VCO center frequency with process and temperature. The oscillation frequency of the VCO can be varied by the process variation and temperature. The sufficient tuning range is required to guarantee that VCO output frequency can be driven to the required value. The standard $VLSI$ process includes pn-junction capacitance of the reverse biased diode and MOS varactor. The Q factor of the varactor is also one of the important factors which influences the tuning range of the oscillator. The MOS varactors exhibit the better Q factor. The LC oscillators exhibit 10 % to 12 % limited frequency tuning range [12]. It is widely used in many applications which require the tunable frequency output. An ideal VCO exhibits the linear relation between control voltage and its output frequency signal. The VCO is the variation of the phase and frequency as the result of the noise on the control line. The noise is proportional to the (K_{vco}) and is given by Eq. (2.63),

$$\omega_{out} = \omega_o + K_{vco} V_{cont} \tag{2.63}$$

where ω_o shows the intercept corresponding with V_{cont}= 0 and K_{vco} is the gain of the circuit. To minimize the effect of the noise in V_{cont}, the VCO gain must be minimized. The $\omega_2 - \omega_1$ is the tuning range of the VCO and is shown in Fig. 2.22. The variable voltage ranges from V_1 to V_2 and the tuning range must span from ω_1 to ω_2. Thus, K_{vco} must satisfy the following requirement given by Eq. (2.64) [12].

$$K_{VCO} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1} \tag{2.64}$$

A significant research has been carried out to increase the tuning range of the oscillators. The wideband/dualband $CMOS$ VCO is presented with the wide tuning range. The tuning range is 98 % in two independent frequency bands with accurate quadrature signals outputs [67]. An inversion mode band switching varactors are

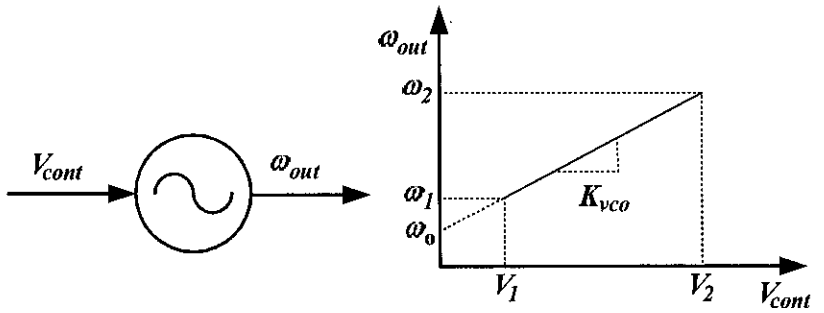


Figure 2.22 VCO sensitivity

used to achieve 29.12 % wide tuning range in the design of 5.9 GHz *CMOS VCO* design [68]. A frequency range of 600 MHz to 3.3 GHz is achieved in monolithic *CMOS PLL* based *VCO* [69]. Another work, presents the 3 to 5 GHz *UWB CMOS VCO*. The active inductors are used instead of passive inductors [70]. In state of the art works, such as Yoshihara [71] is using variable inductor to achieve the frequency tuning range of 2.13 GHz to 3.28 GHz in *VCO* design [71]. A frequency tuning range of 4.12 GHz to 4.89 GHz is achieved in oscillator [72]. Another work, reports the frequency tuning range of *QVCO* is 4.13 GHz to 4.89 GHz [73]. The 10 % frequency tuning range is achieved in $LP-SIPC\ QVCO$. The $LP-SIPC\ QVCO$ is implemented with *pMOS* varactors [52].

2.9 State of the Art Oscillators

This section explains the different state of the art oscillator's work. There are wide range of wireless communication systems which are integrated in *CMOS* process technologies and are getting more industrial attention. There are large number of radio frequencies integrated circuit articles and publications focusing on *CMOS* oscillators at various frequency ranges. Some of the published books also cover completely and partially design and integration of *CMOS* oscillators [1], [12], [20], [32], [45]. In summary of the different oscillators, *VCOs* and quadrature oscillator circuit architectures with their performance parameters are available. The performance parameters

include frequency tuning sensitivity, gain, supply voltage, power consumption, phase noise characteristics, output power, frequency spectrum and phase errors. However, the designs are also fully integrated in system-on-chip (SOC) while different state of the art works are integrating passive device such as inductors and varactors to off-chips. The multi-chip module and other techniques are used for their circuit implementation [16], [17]. Spiral inductors are most commonly used for the on-chip oscillator design. The inductor quality factor enhancement and reducing substrate losses of the on-chip designs are also carried out in state of the art work. The design of varactors with wide tuning sensitivity are also discussed in recent research work. There are various types of varactors used in LC-tanks. The MOS varactors and pn-junction varactors are most common in LC-tank based oscillator designs. However, the on-chip solution is the best choice and in literature $CMOS$ $VCOs$ are focusing at fully integrated oscillators [12] [45], [74].

It is very difficult to compare oscillator characteristics because of different operating frequencies, frequency tuning range, varactors, inductors, circuit topologies, buffer designs and process technologies.

The quadrature $VCOs$ and $VCOs$ in 0.18 μm and 0.13 μm $CMOS$ process technologies which are operating from 2.8 GHz to 5.5 GHz frequencies are best candidates chosen for the comparison of results. In 0.18 μm $CMOS$ process technology, there are six metal layers and one polysilicon. There are eight metal layers and 1 polysilicon in 0.13 μm $CMOS$ process technology. The various state of the art oscillators performance parameters are summarized in Table 2.1. The comparison includes the oscillator topologies, process technology, power dissipation, operating frequencies, tuning sensitivity or range, oscillator type, phase noise and figure of merit (FOM).

2.10 Summary

In this chapter, a brief introduction of modern wireless system is described. The homodyne and heterodyne receivers with the importance of oscillators and quadrature $VCOs$ are summarized. Local oscillators are used with $MB-OFDM$ frequency syn-

Table 2.1 State of the art oscillators performance parameters summary.

Ref No	Osc Type	Technology (μm)	Power (mW)	Frequency (GHz)	Tuning Range (GHz)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)
[4]	VCO	0.18	18.54	2.22	2.2-2.22	-103.5 @ 100KHz	-
[21]	QVCO	0.18	12	4.5	1	-123 @ 1MHz	-
[52]	QVCO	0.18	11	3.4	10 %	-114.3 @ 1MHz	-
[63]	VCO	0.13	7.5	5.2	5.17-5.34	-97 @ 100KHz	-182.6
[75]	VCO	0.35	16	2.9		-142 @ 3MHz	-189
[76]	VCO	0.18	10.8	5.16	4.16-5.53	-123.1 @ 1MHz	-187
[77]	VCO	0.18	3	5.0	4.61-5	-120.9	-189.6
[78]	QVCO	0.13	-	-	20 %	-122 @ 1MHz	-
[79]	QVCO	0.13	50	2.5	2.41-2.64	-139 @ 1MHz	-190
[80]	QVCO	0.13	4.8	4.5	-	-112 @ 1MHz	-181
[81]	QVCO	0.18	10.8	5.2	4.9-5.5	-117 @ 600KHz	-185
[82]	QVCO	0.18	21.6	5.6	0.33	-113 @ 1MHz	-174.6
[83]	QVCO	0.13	9	3.9	-	-117 @ 1MHz	-180
[84]	VCO	0.25	12.3	5	4.82-6.28	-119 @ 1MHz	-
[85]	QVCO	0.18	4.32	3.1	-	-102 @ 1MHz	-166
[85]	QVCO	0.13	9.6	10	-	-95 @ 1MHz	-163
[86]	QVCO	0.18	10	2.55	2.34-2.55	-120 @ 1MHz	-175.5
[87]	QVCO	0.18	13.5	3	-	-116 @ 1MHz	-177
[88]	QVCO	0.18	10.8	2.4	2.27-2.65	-105 @ 100KHz	-
[89]	VCO	0.18	12.6	4.8	-	-120 @ 1MHz	-182.5
[90]	QVCO	0.18	7.2	2.45		-115 @ 1MHz	-178
[91]	QVCO	0.18	5.4	1.1	-	-120 @ 1MHz	-173
[92]	QVCO	0.18	12.24	6	-	-106 @ 1MHz	-173
[93]	QVCO	0.18	2.7	5.25	-	-107 @ 1MHz	-177

thesizer to generate the various frequencies. The oscillator main types are described which are the potential candidate for the $RFIC$ designs. The LC-tank based oscillators and quadrature $VCOs$ are described. The main components of oscillator such as spiral inductor with equivalent π-model, quality Q factor and varactors are described. The main types of varactor are pn-junction varactors and $pMOS$ varactors. The performance parameters of varactors are also presented. Next, introduction of LC oscillators such as colpitts oscillator and -G_m oscillators are presented. The oscillator basic design is moving towards VCO and $QVCO$ designs. The oscillator performance parameters such as phase noise, figure of merit and frequency sensitivity are briefly discussed. The brief overview of Leeson's phase noise model based on LTI system, is presented. The LTV phase noise model for different VCO topologies is also explained. The phase noise formulation is also described for $DS-VCOs$. The various state of art $VCOs$ and $QVCOs$ performance parameters are also summarized in this chapter. The design of $VCOs$ and $QVCOs$ are chosen according to the frequency range, phase noise, tuning sensitivity and $CMOS$ process technologies.

CHAPTER 3

LP^3-QVCO DESIGN

3.1 Introduction

In the previous chapters, a brief overview of RF communication system, frequency synthesizer architecture and introduction of the different types of oscillator are described. The basic concepts and performance parameters of oscillators are also presented. In this chapter, the oscillator design methodology with innovative techniques is presented. The oscillator design is leading by $LP^3 - QVCO$ architecture design. The design flow of the $LP^3 - QVCO$ is also presented. The spiral inductor designs are also presented. The different innovative techniques are used to enhance the quality factor of inductor. Next, integrated capacitors and varactors are described, briefly. The characteristics of $pMOS$ varactors are also described. Finally, the designs of $LP^3 - QVCO$ with common drain buffers are explained. The design parameters of important components are also summarized in this chapter.

3.2 Voltage Controlled Oscillator Design

Voltage controlled oscillator (VCO) consists of cross-coupled active device pair and LC-tank. The cross-coupled pair compensate the tank energy loss for the successful oscillation. The design constraints are imposed on power dissipation, tank amplitude, frequency range, startup condition and spiral inductors.

The first factor requirement is, the maximum power constraint is imposed as maximum bias current I_{max}. The bias current is drawn from the dc power supply voltage source as given by Eq. (3.1).

$$I_{bias} \leq I_{max} \tag{3.1}$$

The next requirement is, the tank amplitude should be as large as possible from the

minimum tank voltage ($V_{tank,min}$). The tank voltage, (V_{tank}) can be expressed by Eq. (3.2),

$$V_{tank} = \frac{I_{bias}}{g_{tank,max}} \tag{3.2}$$

where $g_{tank,max}$ is the maximum tank transconductance of active device. The $g_{tank,max}$ is the worst case situation. The output voltage must be lower than the certain saturation voltage, so that VCO should operate in current limited[1] region instead of voltage limited[2] region. The lower (better) phase noise can be achieved with large output voltage swing [42].

The third requirement is, the tuning range of the oscillator. It should be wide as possible and cover certain minimum and maximum percentage of center frequency (ω). The lower frequency limit is given by Eq. (3.3).

$$L_{tank}C_{tank,min} \leq \frac{1}{\omega_{max}^2} \tag{3.3}$$

The expression for the upper frequency limit is given by Eq. (3.4).

$$L_{tank}C_{tank,max} \leq \frac{1}{\omega_{min}^2} \tag{3.4}$$

For the startup condition of oscillation, the $g_{active} > \alpha\ g_{tank,max}$. The minimum value of the $\alpha_{min} = 3$. The startup condition with a small-signal loop gain of at least α_{min} can be expressed by Eq. (3.5) [42],

$$g_{active} \geq \alpha_{min} g_{tank,max} \tag{3.5}$$

For $DS - VCO$ design, the transconductance of cross-coupled transistors is sum of the $nMOS$ and $pMOS$ transconductances, is given by $g_{active} = (g_{mn} + g_{mp})/2$. Also, the $g_{mn} = g_{mp}$. The g_{mn} can be calculated by Eq. (3.6),

$$g_{mn} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D} \tag{3.6}$$

[1]In current limited region, the tank amplitude grows linearly with the bias current according to $V_{tank} = R_{tank} \cdot I_{bias}$ until the VCO enters the voltage limited region.

[2]In voltage limited region, the tank amplitude will not grow further and the voltage limit of the voltage limited region is specified by the value of supply voltage.

where C_{ox} is the oxide capacitance equal to 9.47 fF/μm^2, μ_n is the electron mobility for $nMOS$ transistor, μ_n value for $nMOS$ is 390.3 cm^2/vs and $pMOS$ is 105 cm^2/vs in 0.18 μm $CMOS$ process technology. The drain current I_D is 1 mA. The (W/L) represents the transistor width and length ratio in μm. The $(W/L)_n$ for $nMOS$ in VCO design is (70/0.18) and $(W/L)_p$ for $pMOS$ is (200/0.18). The calculated transconductance for $g_{mn} = g_{mp}$ is 16 mS by using Eq. (3.6).

The oscillation frequency can be calculated from a well known expression given by Eq. (3.7),

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{3.7}$$

where f_{osc} is the oscillator center frequency and LC are the inductance and capacitance of the LC-tank [1].

3.2.1 Oscillator Design Techniques

A fully differential signal VCO $(DS-VCO)$ topology is chosen instead of $nMOS$-only VCO. The $DS-VCO$ consists of $pMOS$ pair on the top of a $nMOS$ cross-coupled oscillator. The fully differential oscillator topology is shown in Fig. 3.1. The LC-tank consists of spiral inductor (L) and variable capacitor (C_{var}). The variable capacitors are also called as varactors. The V_{tune} represents the dc tune (control) voltage of varactor. The variable capacitance is achieved with the variation of dc tune voltage and the frequency sweep is achieved at the output of VCO. There are various advantages and disadvantages of a $DS-VCO$ structure as compared to $nMOS$-only VCO structure.

The output amplitude of the $DS-VCO$ is twice than the $nMOS$-only VCO structure. Let's consider the left side M_{p2} is turned on while right M_{p1} transistor is off. The left side M_{n2} turns off while the right side M_{n1} turns on eventually. The left side M_{p2} carries the whole bias current while right M_{p1} transistor is off. The current flows from V_{dd} through M_{p2}, LC-tank and then from right M_{n1} transistor. However, the addition of $pMOS$ cross-coupled pair increases the noise contribution

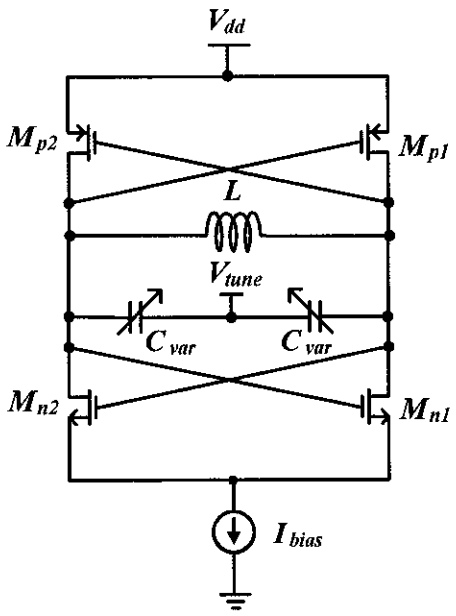


Figure 3.1 Fully differential VCO topology.

as compared to $nMOS$ only oscillator ($SS - VCO$). Thus, the peak differential output voltage swing is twice than $nMOS$-only VCO structure. The $DS - VCO$ appears to achieve better phase noise at a given power dissipation. A larger output voltage swing is achieved in $DS - VCO$ which improves the signal-to-noise ratio (SNR) [42]. A higher output voltage swing is achieved in the oscillator with the center-tapped inductor (CTI). Therefore, the tank circuit modification is required by adding capacitive dividers in the feedback path [1].

The complementary $DS-VCO$ exhibits higher transconductance than $SS-VCO$. The $DS-VCO$ exhibits the negative resistance $-\left(\frac{2}{g_{mn}}+\frac{2}{g_{mp}}\right)$, where g_{mn} and g_{mp} are the transconductances of the $nMOS$ and $pMOS$ transistors, respectively. However, on the other hand the transconductance of the $nMOS$-only VCO is $-2/g_{mn}$ with the same bias current. Hence, it is possible to compensate the losses with the lower bias current as compared to the $nMOS$-only VCO structure. The additional -g_m provided by $pMOS$ cross-coupled pair can cancel higher values of equivalent parallel resistance in LC-tanks [56].

By proper adjusting the (W/L) of the $pMOS$ and $nMOS$ cross-coupled pair, the transconductances of $nMOS$ ($M_{n1} \sim M_{n2}$) and $pMOS$ ($M_{p1} \sim M_{p2}$) should be same ($g_{mn} = g_{mp}$) as possible to get the symmetrical oscillation output swing. The better rise and fall time symmetry reduces the up-conversion of transistor $1/\Delta f^3$ noise. The $DS-VCO$ structure obtains the smaller $1/\Delta f^3$ noise corner in the phase noise.

The tail bias current source is one of the main noise sources in VCO. The flicker noise of current source is up-converted to LC-tank and degrades the phase noise of the oscillator. The flicker noise contribution from $nMOS$ ($M_{n1} \sim M_{n2}$) and $pMOS$ ($M_{p1} \sim M_{p2}$) cross-coupled pair is small due to the switching operation of the circuit [94]. The tail biasing active devices of the VCO core structure are replaced by the tail biasing resistor R_{tail}. The $1/f$ noise occurrence from the active device is removed and results in the improved spectral purity. The phase noise is related to the Leeson's equation expressed by Eq. (2.49). The modified form of this equation can be expressed by Eq. (3.8),

$$L(\omega) = F\frac{4kTR}{V^2}\left[\frac{\omega_o}{2Q\Delta\omega}\right]^2 \tag{3.8}$$

where V is the rms voltage across LC-tanks, $\Delta\omega$ is the frequency displacement from the fundamental frequency and Q is the quality factor of the LC-tank circuit. The F is referred to the oscillator noise factor and can be expressed by Eq. (3.9),

$$F = 1 + \frac{K_1\gamma I_{bias}R}{V} + K_2\gamma g_{mbias}R \tag{3.9}$$

where K_1 and K_2 are constants, γ is the transistor noise factor, R is the resonator equivalent resistance and g_{mbias} refers to the current source transistor conductance.

From Eq. (3.8), the phase noise is proportional to the reciprocal of the biasing current square.

$$L(\omega) \propto (I_{bias}^2)^{-1} \tag{3.10}$$

As the bias current increases in mA range, it results in the improved phase noise of the circuit. The tradeoff exists between the power consumption and phase noise. Current source can increase the overall phase noise performance of the circuit. In the

case of $nMOS$ based current mirror, a high current gain is usually chosen to lower the overall power consumption. The Eq. (3.9) demands the device with lower g_m results in low oscillator noise factor. However, the $1/f$ noise of the tail transistor remains unfiltered at the source node. Hence, to avoid the noise contribution from the active device, a resistor is used in the VCO bias circuit [62].

The multifinger gate structure of the $pMOS$ based varactor is used to reduce the $1/f$ noise. Multi-finger gate structure reduces the input gate resistance. Multi-finger gate structure shows better performance in terms of RF power and noise. By reducing the gate width and increasing the finger number in the design of gate configuration, it can enhance the $CMOS$ device RF power and noise performance. The improvement in RF power and phase noise is due to the reduction of gate resistance. However, this approach is not straight forward, as the substrate parasitic effects will be introduced due to lossy silicon (Si) substrates. The total width of the varactors remain same and it should result in similar flicker noise. Therefore, due to parasitics the flicker noise is changed, the higher resistance means higher flicker noise. The device with smaller width per finger results in reducing the flicker noise due to lower parasitic capacitance. The flicker noise can be expressed by Eq. (3.11).

$$L(\Delta\omega) \approx 10\log\left[\frac{i_f^2 c_o^2}{q_{max}^2 8(\Delta\omega)^2}\right] \tag{3.11}$$

Where i_f^2 is the flicker noise power spectral density, q_{max} is the offset frequency and c_o is the average value of impulse sensitivity function. The gate layout structures of the $pMOS$ varactors are split in different structures. This includes the different parasitic resistance and low resistance means low noise [63].

The source damping resistor R_{dmp} is used in the $DS-VCO$ structure. The source damping resistor is used to suppress the $1/f$ noise in the oscillator. The 40 Ω damping resistor provides better phase noise as compared to the other resistor values in simulation. In $CMOS$ oscillators, since the low frequency $1/f$ noise is up-converted to the oscillation frequency. The phase noise performance below several MHz offset frequency is dominated by the $1/f$ noise of MOS transistors. In MOS transistor, the

output noise current increase is proportional to the square of the transconductance. Large signal swing of the oscillator leads to larger variations in transistors. However, the large signal swing may generate excess $1/f$ output noise current during oscillation. The degeneration resistor can remove the excess $1/f$ output noise current [64].

The drawbacks of the $DS-VCO$ are due to the increase of parasitic capacitance. The cross-coupled $pMOS$ transistor pair exhibits more parasitics as compared to $nMOS$ cross-coupled device pairs. Thus, by increasing the parasitic capacitances the tuning range of the VCO is lowered. However, proper selection of $pMOS$ device parameters help to achieve the appropriate results.

The LP^3-VCO with source damping resistor, tail biasing resistor and multifinger gate width structure of the varactor is shown in the Fig. 3.2. The M_{p1} and M_{p2} are the $pMOS$ cross-coupled transistor pair, the M_{n1} and M_{n2} are the $nMOS$ cross-coupled transistor pair. Both $nMOS$ and $pMOS$ cross coupled pairs provide enough negative resistance to sustain and maintain the oscillation of the output. The C_{var} is $pMOS$ based active device varactor. The $pMOS$ varactor can also be replaced by pn-junction diode. The R_{dmp} is the source damping resistor of 40 Ω. The V_{tune} represents the dc tune (control) voltage of $VCO's$ varactor. The output frequency is varied with the change of the dc tune voltage. The R_{tail} is used for the LP^3-VCO biasing. The optimum value of the tail biasing resistor is selected according to the requirements of the LP^3-VCO design [95].

3.2.2 Inductor Design

The symmetrical spiral inductors are designed using "Analysis and Simulation of Spiral Inductors and Transformers" ($ASITIC$) for ICs [35]. The device is a symmetrical inductor as can be observed in R_1, R_2, C_1 and C_2. The inductor is designed with top-metal layer (metal 6) with inner-turn of metal 5 using 0.18 μm $CMOS$ process technology. The top metal thickness is in the order of 2.3 μm. The inductor is designed using single metal layer without metal stacking technique. The metal stacking technique is widely used in standard digital process in which ultra-

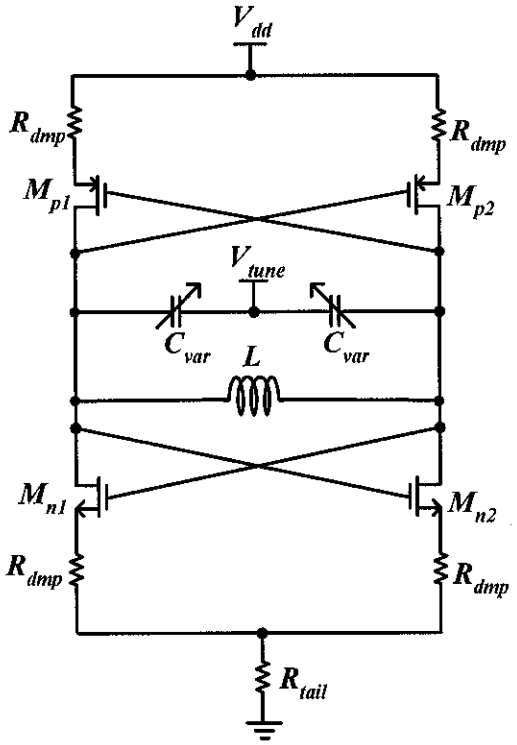


Figure 3.2 LP^3-VCO with tail biasing resistor, damping resistor and multifinger gate structure.

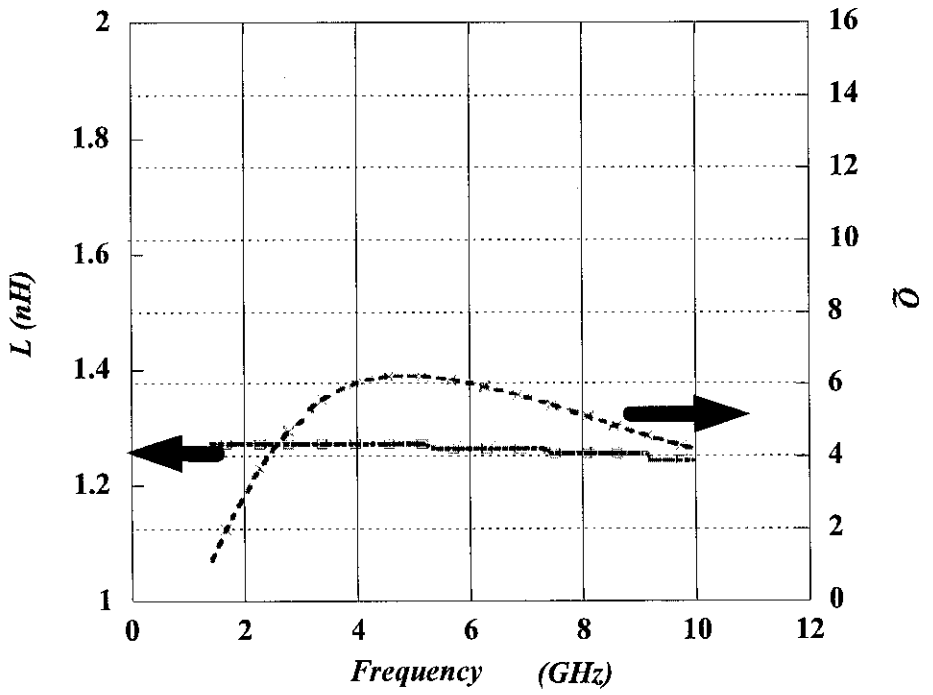


Figure 3.3 The s-parameter analysis using Cadence to verify the pi-model in 0.18 μm.

thick metal layer is not available. The inductor model is also verified using 1-port analysis. The s-parameters analysis are carried out to verify the inductance value. The effective L is at 1.24 nH at 4.224 GHz and quality factor is 6.1. The quality factor (Q) and inductance variation against frequency is plotted in Fig. 3.3 [95].

The s-parameters analysis of symmetrical spiral inductor in 0.13 μm $CMOS$ process technology are also shown in Fig. 3.4. The simulated quality factor of the inductor is in the order of 18. This inductor is designed using top metal layer Ultra Thick Metal layer (UTM) and metal top ($Met-Top$). The summary of the simulation results and inductor π-models for 0.18 μm and 0.13 μm $CMOS$ process technologies are shown in Table 3.1. This table includes the process technology, series inductance (L_s), series resistance (R_s), parasitic capacitances, parasitic resistances, inductor Q factors and self resonance frequencies of extracted spiral inductors.

The on-chip Q-factor can be enhanced by using following possible methods. For

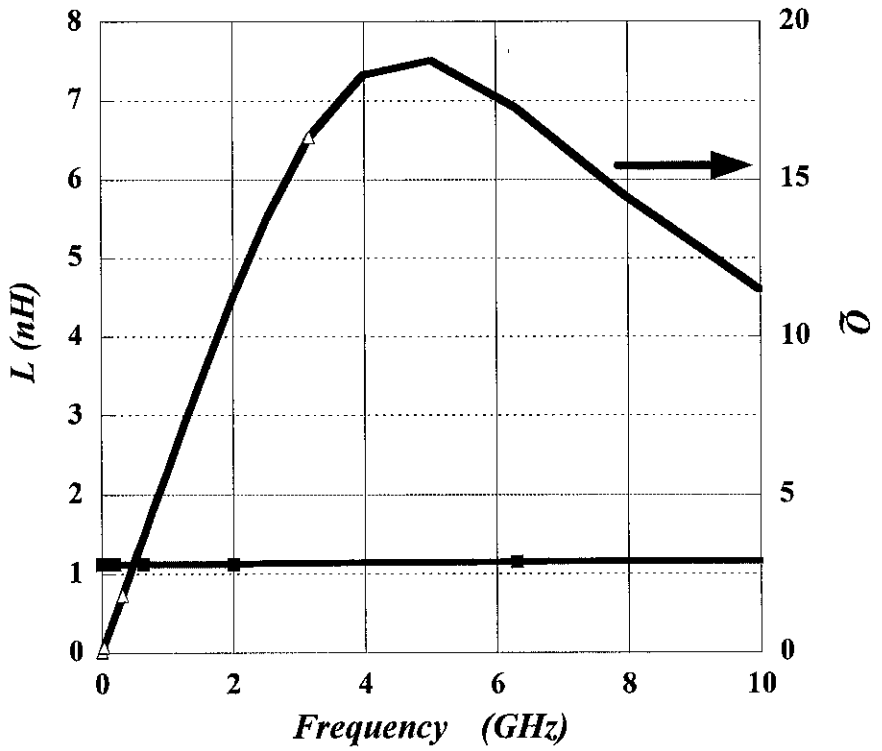


Figure 3.4 The s-parameter analysis using Cadence to verify the πi-model of 0.13 μm $CMOS$ symmetrical spiral inductor.

Table 3.1 π-model of spiral inductors extracted from ASITIC.

Tech(μm)	$L_s(nH)$	$R_s(\Omega)$	$R_1(\Omega)$	$C_1(fF)$	$R_2(\Omega)$	$C_2(fF)$	Q_{s1}	Q_{s2}	Q_d	$f_{sr}(GHz)$
0.18	1.26	2.96	451	80	453	78	7.77	7.81	9.30	15.9
0.13	1.19	1.21	747.2	32.6	770.1	32.3	18.6	18.6	21.1	26.3

the multiple winding inductors, the electromagnetic loss is more at the center of the spiral inductor. To avoid the electromagnetic loss, the innermost windings of inductor should be removed. For higher inductance value, the multiple inner windings are used. However, it results in loss, which can be reduced by optimum width of the inductor.

The on-chip spiral inductor performance is improved by using patterned ground shield (PGS) under the inductor. The PGS is used to minimize the effects of electric and magnetic coupling to the lossy substrate. The PGS can reduce the magnetic image current loss. It blocks the electromagnetic energy coupling to the substrate and reduces the eddy currents in the shield [96]. A patterned ground shield with inductor is shown in the Fig. 3.5. A PGS will allow the shield currents to flow perpendicular to conductive paths of spiral inductor. The PGS prevents the majority of eddy currents flow parallel to the inductor. The patterned ground shield consists of polysilicon and metal 1. The polysilicon slots are perpendicular to the current within the inductor. The degradation of the quality factor (Q) of the inductor can be compensated by using PGS. The separation between PGS and top metal layers are chosen carefully to enhance the performance of inductor. The metal 1 is used in the cross form over the poly strips to provide the ground connection.

Appendix A describes the patterned ground shield design implemented in $LP^3 - QVCO$ design no. 1 to 3. The inductor design parameters used in $LP^3 - QVCO$ design no. 4 to 7 $ASITIC$ are also summarized in this chapter.

3.2.3 Integrated Capacitors

Capacitors are widely used in IC design processes. The metal-insulator-metal (MIM) plate capacitors and polysilicon-based capacitors are mainly used. The MIM capacitors are used commonly instead of polysilicon-based capacitors due to their high Q factor and better performance. The MIM capacitor provides high Q and low parasitic bottom plate capacitance. In this work, MIM decoupling capacitors are used in the fabricated chips between power and ground pins. The decoupling capacitors are used to avoid the voltage fluctuations. It also requires at least one

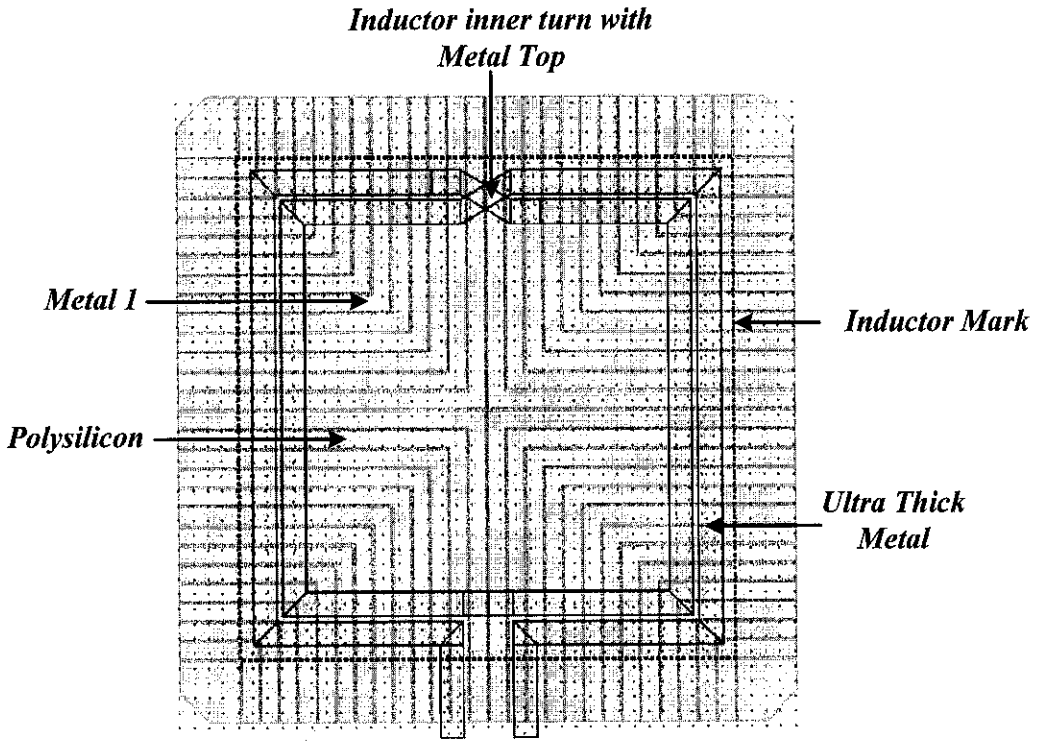


Figure 3.5 Symmetrical spiral inductor layout with PGS.

additional mask. A high Q metal finger capacitor can also be built by combing metal fingers deeply. As technology scales down and more number of metal layers are added to the metallization stack, its density tends to improve. However, there is no further masking required for the metal finger capacitors. Therefore, it is also becoming a popular candidate in IC designs [97]. MIM capacitors are used in 0.18 μm LP^3-QVCO and metal-metal finger capacitors are used in 0.13 μm LP^3-QVCO designs respectively.

3.2.4 Varactor Design

Varactors are one of the important building blocks of the LC-tank. There are different types of varactors used in the oscillator design. In this section, pn-varactors and $pMOS$ varactors are described briefly.

The reverse biased pn-junction varactors are commonly used in $CMOS$ process technology. pn-junction varactors are composed of $p+$, $n-$ diffusions and N or P wells. The pn-junction varactors provide the limited tuning range. In 0.18 μm process technology, the pn-junction varactors are used in LP^3-QVCO designs. The dc tune voltage is varied from 0 V to 1.8 V and frequency tuning range of oscillator is achieved. Both $P+$ and N-well taps are connected using metal 5. Top metal connection is recommended to minimize the interconnect losses.

The depletion mode $pMOS$ varactors are used in 0.13 μm $CMOS$ process technology. The drain, source and bulk ($D = S = B$) are combined together and dc tune voltage is applied at the gate of the transistor. The $pMOS$ varactors are simulated using "Cadence" tools [98]. The accumulation, depletion and inversion modes are clearly shown in Fig. 3.6. The capacitance is changed from smaller to larger value. The variation of $pMOS$ transistor capacitance is plotted against dc tune voltage. The simulation result is carried out in "Cadence Specter RF" [98]. The required capacitance is expressed by E.q. (3.12),

$$C_v = C_{ox} \times W.L.nf \tag{3.12}$$

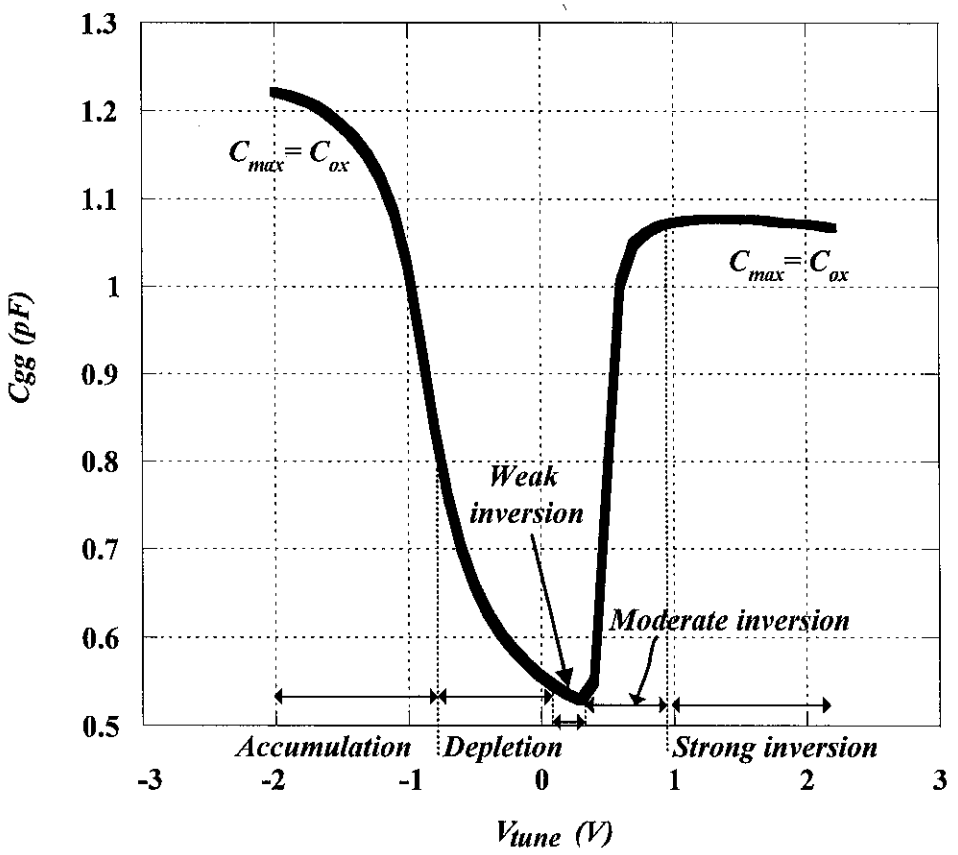


Figure 3.6 Tuning characteristics of pMOS varactor.

where C_{ox} is the oxidation capacitance, W and L are the width and length of the active device, and nf stands for the number of fingers.

3.2.5 Output Buffer Design

Buffers are necessary for VCO measurements to drive the instrumentation with 50 Ω load. Buffers should not load the oscillator excessively. In this work, on-chip $nMOS$ common drain (source follower) buffers are used. The common drain buffers are shown in the Fig. 3.7. In Fig. 3.7 (a), the biasing resistor is used to bias the buffer circuit. In Fig. 3.7 (b), two inductors are used. The 15.8 nH L_1 and L_2 are used at the buffer's gate and drain to avoid unwanted noise flow from the power supply. The

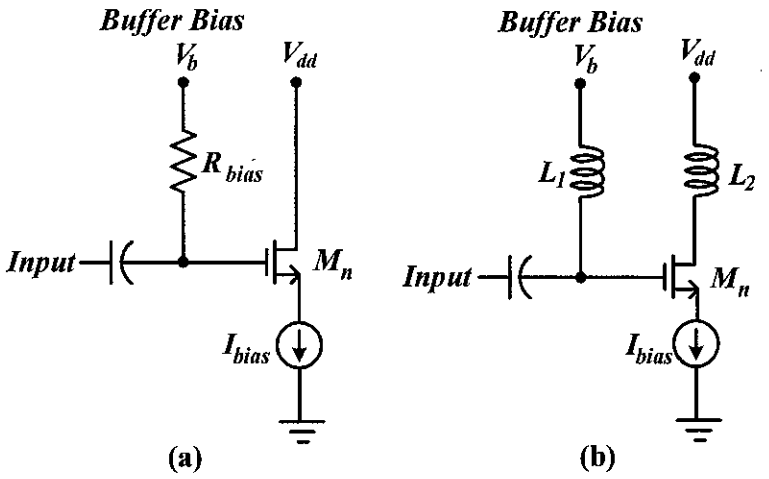


Figure 3.7 (a) Common drain buffer with biasing resistor and (b) with inductor.

$nMOS$ device parameters are chosen to get output impedance of 50 Ω. The output impedance of common-drain is $1/g_m$. The input capacitance of the common drain buffer is low and its bandwidth is high. The buffer operates at 1.2 V and 1.8 V for 0.13 μm and 0.18 μm $CMOS$ technologies, respectively. The bias voltage is controlled through bond pads. At the output of the oscillator, a dc blocking capacitor is used. As the oscillator *dc* output level varies with the power supply, the buffer is AC coupled to the oscillator output through 25 pF fingered metal 6 capacitor. In 0.18 μm $CMOS$ process technology, the MIM capacitor exhibits small backplate parasitics. Common drain buffer is added at each output of oscillator circuit and terminated with 50 Ω resistor. The current consumption of each buffer in 0.18 μm process is 2.4 mA from 1.8 V supply. The current consumption of buffer used in 0.13 μm process is 1.2 mA from 1.2 V supply. The common drain buffer parameters are summarized in Table 3.2. The $nMOS$ transistor width is 100 μm used in 0.13 μm and 0.18 μm $CMOS$ process technologies. Tail biasing resistors are also used in two $LP^3 - QVCO$ designs. The implementation is carried out using 0.18 μm $CMOS$ process technology. The current mirrors are also used in rest of the $LP^3 - QVCO$ designs and fabrication is carried out using 0.18 μm and 0.13 μm $RF\ CMOS$ process technologies. The current mirrors

Table 3.2 Common-drain buffer parameters.

Process (μm)	Width (μm)	Bias Voltage (V)
0.18	100	1.8
0.13	100	1.2

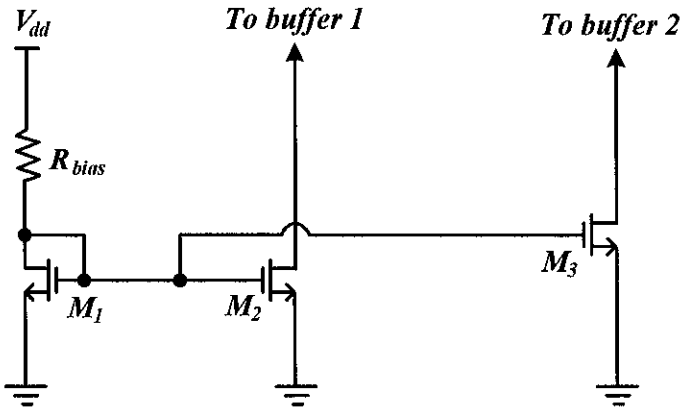


Figure 3.8 Common drain buffer bias circuit.

circuit is shown in Fig. 3.8 and transistor parameters are summarized in Table 3.3. A 7.9 KΩ biasing resistor (R_{bias}) is used in current mirror design. The $nMOS$ transistors M_1, M_2 and M_3 are also used in current mirror circuit. The drain-gate voltage of the M_1 is zero, therefore channel does not exist at the drain and transistor operates in the saturated region when threshold voltage is positive. M_1 is also called as diode connected. Let's consider M_2 also operates in the active region and both transistors have infinite output resistance. The drain current of the M_2 is controlled by the V_{GS2}, which is equal to the V_{GS1} [33]. The drain currents of the M_2 and M_3 are same and provided to the respective buffers of the $QVCO$.

The transistors width parameters are also summarized in Table 3.3.

Table 3.3 Buffer bias circuit parameters.

Device	Parameter Values
R_{bias}	7.9 KΩ
M_1	7.5 μm
M_2	75 μm
M_3	75 μm

3.3 LP³-QVCO Design

The $LP^3 - QVCO$ is designed using innovative techniques. First, $DS - VCO$ topology is the best choice for the integrated low phase noise $VCOs$. Second, a tail biasing resistor is used for $LP^3 - QVCO$ biasing. The R_{tail} is used instead of active device based current mirrors. Third, source damping resistors are used to achieve low $1/f$ noise. Next, the $pMOS$ varactors and pn-junction varactors are used in different designs of $LP^3 - QVCO$. The common drain buffers are used at each output of $LP^3 - QVCO$ circuit.

Two fully differential LC-tank $LP^3 - VCOs$ are parallel coupled to form $LP^3 - QVCO$ architecture. The coupling factor of the transistor is carefully chosen which is 0.31 to achievable. The $LP^3 - QVCO$ core is shown in Fig. 3.9. The $nMOS$ $M_{n1} \sim M_{n4}$ and $M_{p1} \sim M_{p4}$ transistors constitute the cross-coupled pairs. The cross-coupled pairs generate the negative resistance to cancel the LC-tank loss. The C_{var} represents the varactor capacitance. The V_{tune} represents the varactor dc tune voltage. The V_{tune} is varied from 0 V to 1.8 V for $LP^3 - QVCO$ designs using 0.18 μm process technology. Similarly, the V_{tune} is varied from 0 V to 1.2 V for the $LP^3 - QVCO$ designs using 0.13 μm process technology. The L represents the spiral inductor. The V_{dd} represents the dc power supply voltage. The $nMOS$ ($M_{c1} \sim M_{c4}$) are coupling transistors. The R_{dmp} shows the damping resistor. The $LP^3 - QVCO$ is biased with R_{tail} resistor. The unwanted $1/f$ noise contribution of active device is removed.

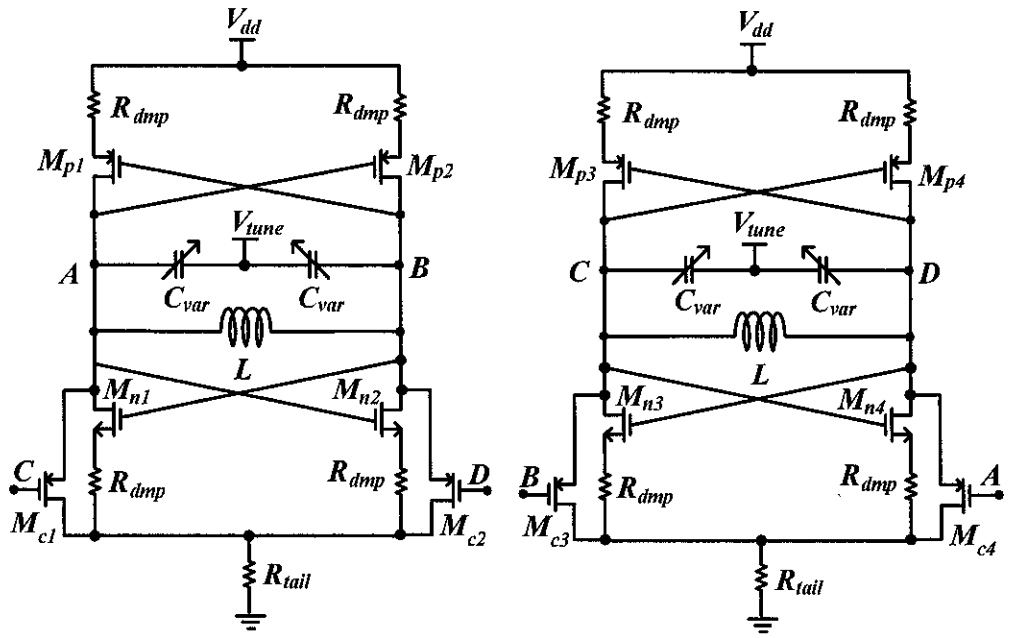


Figure 3.9 LP³-QVCO with nMOS coupling.

The A, B, C and D represent the $I+$, $I-$, $Q+$ and $Q-$ signals of $LP^3 - QVCO$.

The operation of the $QVCO$ can be explained as a linear feedback loop shown in Fig. 3.10 (a). The large signal transconductance of $nMOS$ ($M_{n1} \sim M_{n4}$) and $pMOS$ ($M_{p1} \sim M_{p4}$) cross-coupled pairs can be written as $-G_{m,np}$. The $nMOS$ $M_{c1} \sim M_{c4}$ are the coupling transistors and transconductance is $-G_{mc}$ which forces two LC-tank $VCOs$ to oscillate in quadrature. Fig. 3.10 (a) can be simplified as shown in Fig. 3.10 (b). The negative resistance cancels the LC-tank loss (i.e. neglecting R_T[3]). Now, consider the LC-tank oscillates at desired frequency and generates the voltage $I+$ and this voltage is transferred into point 4 through the transconductance of coupling transistor. The current enters into the tank 4 must be 90° out of phase with the voltage $Q-$ across the tank. Thus, $I+$ and $Q-$ are in quadrature. This process continues around the loop[4]. The signal moves from $I+$ to $Q-$, $Q-$ to $I-$, $I-$ to $Q+$

[3] R_T is the parallel equivalent resistance, representing the losses from the passive components in LC-tank circuit, discussed in Chapter 2.

[4] The total phase shift around the loop should be 360° and the gain is designed to be greater than

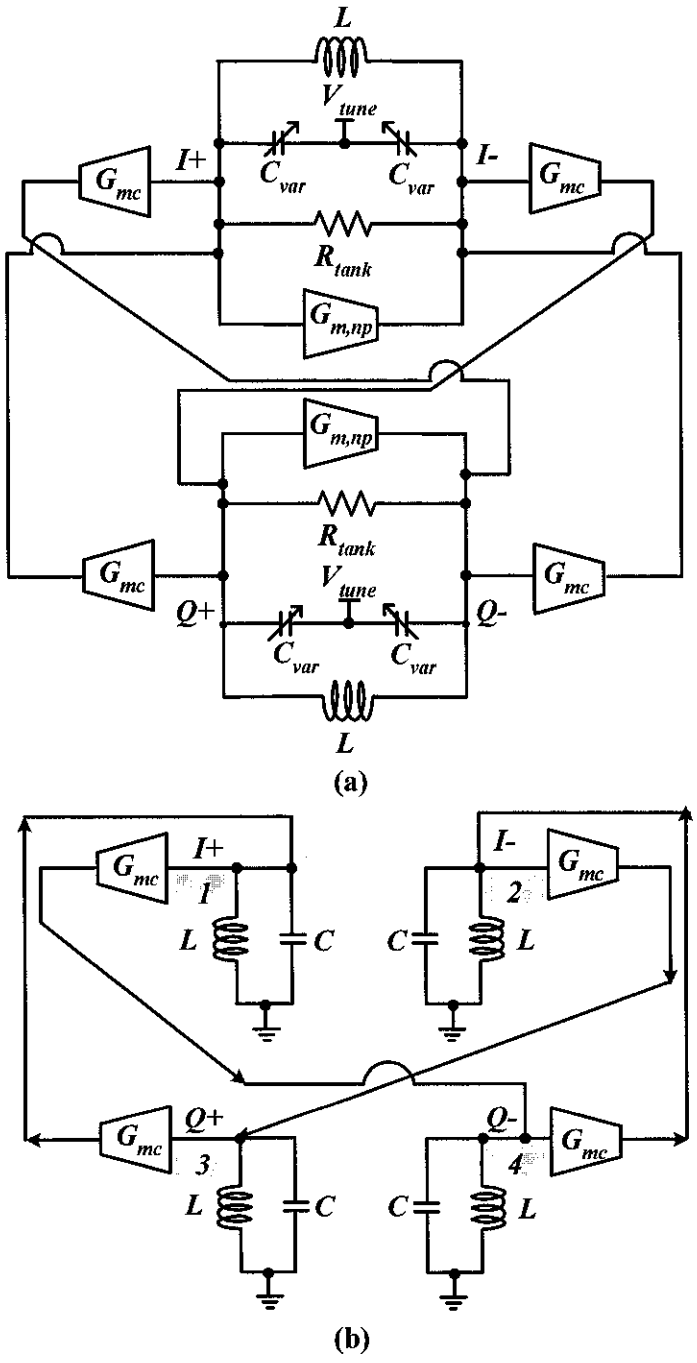


Figure 3.10 LP³-QVCO block diagram (a) with differential LC-tank VCO, -G_m circuit and coupling transistors (b) simplified block diagram and assuming R_{tank} compensated by -$G_{m,np}$.

and $Q+$ to $I+$. Hence, each output signal exhibits the phase difference of 90°. At $I+$, $I-$, $Q+$ and $Q-$ outputs, 360° or 0°, 270°, 90°, and 180° are obtained, respectively [99]. The $LP^3 - QVCO$ circuit with common drain buffer is shown in Fig. 3.11. The dc blocking capacitor (C_{dc_block}) is used at the output of the $LP^3 - QVCO$. The $LP^3 - QVCO$ core output is applied at the gate of buffer. Finally, the output signal is achieved at the respective bond pad. The output common drain buffer exhibits the impedance of 50 Ω. The I_{bias} represents the buffer bias. The buffer biasing is carried out by using R_{tail} and active device based current mirrors.

The tail biasing resistor, source damping resistors and multifinger gate structure of the MOS transistors are used together in the proposed $LP^3 - QVCO$ architecture. The p-channel $MOSFET$ device exhibits low $1/f$ noise as compared to n-channel device. The source damping resistors are used to reduce $1/f$ noise in the oscillator. However, oscillator exhibits the large output signal which results in the large transconductance (g_m) variations. Therefore, it may generate the excess $1/f$ noise current at the output. The excess $1/f$ noise results in the degradation of oscillator's phase noise. However, the proper selection of damping resistor results in a minimum phase noise of an oscillator [4]. The other technique includes the multifinger gate structure of MOS devices. The optimum value of source degeneration resistor results in the reduction of input gate resistance, leads in the improvement of RF power and better $1/f$ phase noise performance [63]. The multifinger gate structure configuration of $pMOS$ device is also used to achieve better phase noise performance. In third method, a tail biasing resistor is adopted instead of current mirrors [62].

These techniques are combined together in VCO circuit which exhibits 16 dB better phase noise results as compared to conventional VCO [95]. Therefore, the same method is applied for the proposed $LP^3 - QVCO$ circuit to achieve low power, low phase noise and low phase error.

In the following sections, seven $LP^3 - QVCO$ designs are described and discussed. The $LP^3 - QVCO$ implementation is carried out using 0.18 μm and 0.13 μm $CMOS$

1, hence meeting the "Barkhausen criteria" for the oscillation.

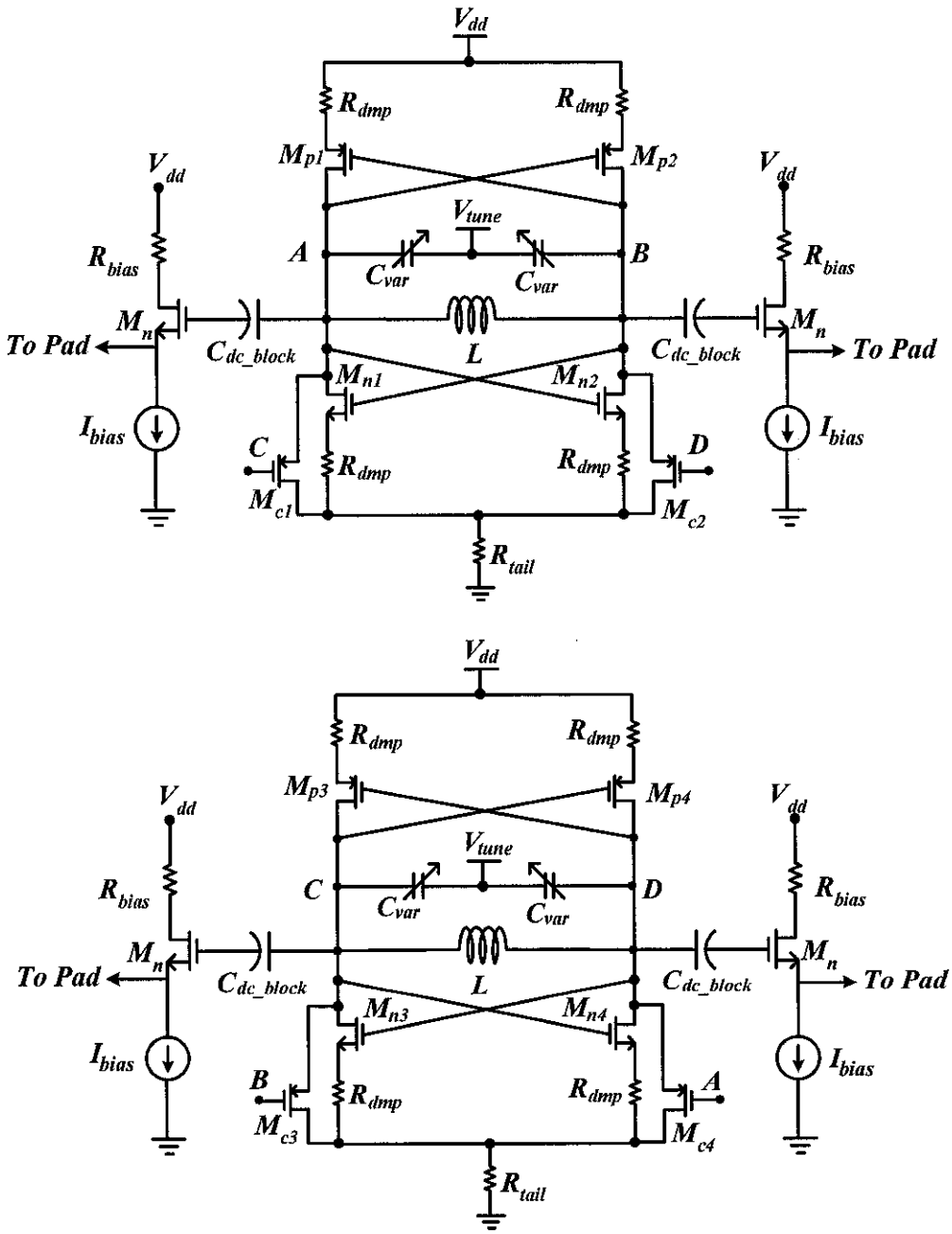


Figure 3.11 LP^3-QVCO with common-drain buffers.

and $RF\ CMOS$ process technologies, respectively.

3.3.1 LP^3-QVCO Design No. 1

In this section, a 2.8 GHz $LP^3 - QVCO$ design topology is discussed. The $LP^3 - QVCO$ design no. 1 is shown in Fig. 3.12. Two LP^3 $VCOs$ are parallel coupled by $pMOS$ ($M_{c1} \sim M_{c4}$) transistors to form a quadrature VCO. The cross-coupled pairs consists of ($M_{n1} \sim M_{n4}$) and ($M_{p1} \sim M_{p4}$) transistors. The equivalent circuit LC-tank loss is compensated by cross-coupled pairs. LC-tank consists of circular spiral inductors and pn-junction varactors to achieve the required frequency. The two circular spiral inductors with PGS are configured in parallel to achieve the inductance of 1.13 nH. The pn-junction based varactors are used in this design.

$LP^3 - QVCO$ is designed using 40 Ω source damping resistor (R_{dmp}), multifinger gate structure of MOS device and 130 Ω tail biasing resistor (R_{tail}). The $LP^3 - QVCO$ biasing transistors are replaced by tail resistor. These methods lead to the low power dissipation and $1/f$ noise improvement in $LP^3 - QVCO$. The common drain output buffers are used at each output of $LP^3 - QVCO$. The transconductance of common drain buffer is 20 mS. The dc blocking metal insulated metal (MIM) capacitors are used at each output of $LP^3 - QVCO$ core. The buffers are biased when dc bias voltage (V_b) is applied at the respective bond pads. The biasing voltage of 1.8 V is applied to achieve the output impedance of 50 Ω. The tail biasing resistors are used instead of current mirrors. The $LP^3 - QVCO$ design is carried out by using 0.18 μm, 1 poly and 6 metal $RF\ CMOS$ process technology [100].

3.3.2 LP^3-QVCO Design No. 2

Two fully differential LC-tank $LP^3 - VCOs$ are parallel coupled by $nMOS$ ($M_{c1} \sim M_{c4}$) transistors to form $LP^3 - QVCO$. The quadrature output signals are generated by coupling $LP^3 - VCOs$. The $LP^3 - QVCO$ design no. 2 is shown in Fig. 3.13. The circular spiral inductors with patterned ground shield are used in LC-tank of

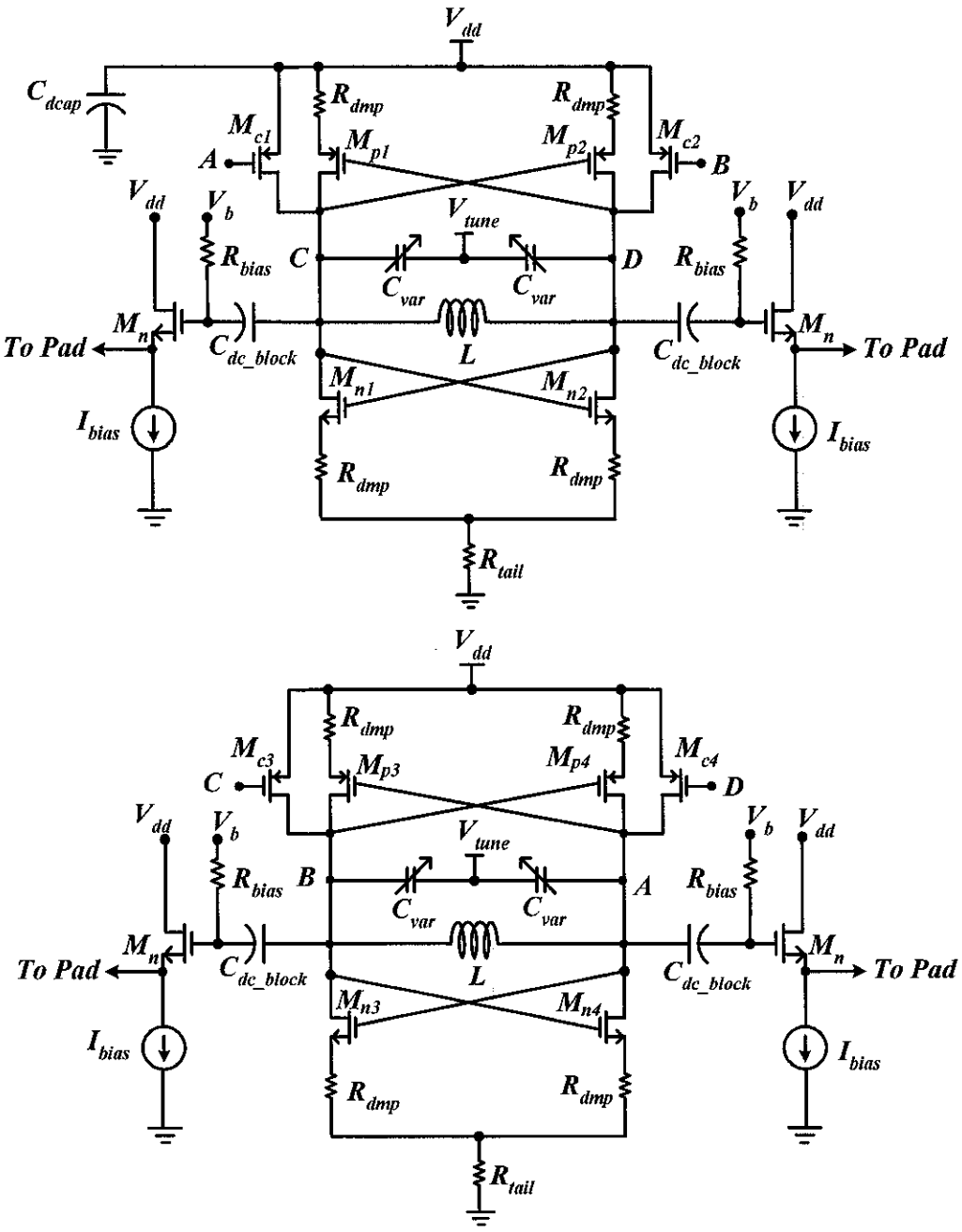


Figure 3.12 Schematic of LP^3-QVCO design no. 1 with output buffers.

$LP^3 - QVCO$. Two inductors are configured in parallel to achieve 1.13 nH inductance value. The patterned ground shield (PGS) is used under the inductors to improve by Q factor. The on-chip common drain buffer is used at each output of $LP^3 - QVCO$ with transconductance of 20 mS. The biasing resistors (R_{bias}) are used for the buffer's biasing between source and ground terminal of buffer transistor. The inductive degeneration technique is used to avoid power supply noise with common drain buffer. A 15.8 nH inductor (L_2) is used at the drain of the buffer transistor. The L_2 blocks the noise signal from power supply. The buffer is biased with 1.8 V dc voltage. The 15.8 nH inductor (L_1) is used between V_{bias} and buffer gate. The 32 pF dc blocking MIM capacitor (C_{dc_block}) is used to avoid the dc signal flow from the output of the oscillator. The 20 pF MIM capacitors (C_{dcap}) are used at each side of $LP^3 - QVCO$. The C_{dcap} are used between power supply and ground terminals to avoid power supply variations. The 40 Ω source degeneration damping resistor (R_{dmp}), 70 Ω tail biasing resistor (R_{tail}) and multifinger gate structure of MOS device are used in this design. The LC-tank consists of pn-junction varactors and circular spiral inductors. The $LP^3 - QVCO$ is designed using 0.18 μm, 1 poly and 6 metal $CMOS$ process technology [101].

3.3.3 LP^3-QO Design No. 3

LP^3 quadrature oscillator (QO) is also designed using the same technique as mentioned in $LP^3 - QVCO$ design no. 2. The LP^3 quadrature oscillator (QO) is shown in Fig. 3.14. The only difference between $LP^3 - QO$ design and design no. 2 is the absence of varactor circuit. In this design, the inductors and parasitic capacitances result in the oscillation of circuit. The rest of the schematic is same as compared to design no. 2. In this design, the frequency tuning range can not be achieved as there is no variable capacitor. The quadrature oscillator operates at fixed frequency of 3.8 GHz with quadrature outputs. The R_{dmp}, R_{tail} and multifinger gate structure of MOS devices are integrated in the $LP^3 - QO$. The MIM decoupling capacitors are also used at the output of $LP^3 - QO$. The quadrature oscillator is

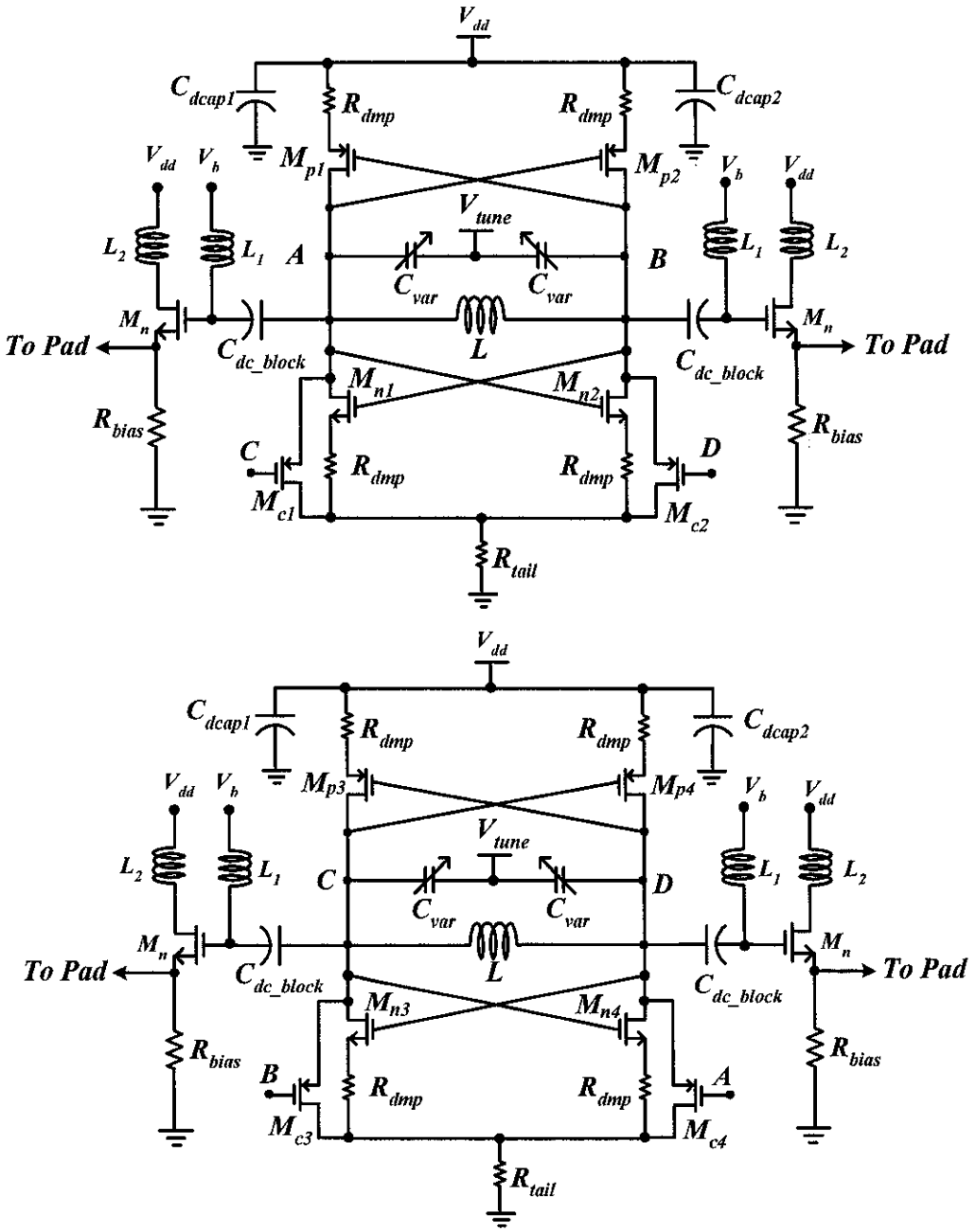


Figure 3.13 Schematic of LP^3-QVCO design no. 2 with output buffers.

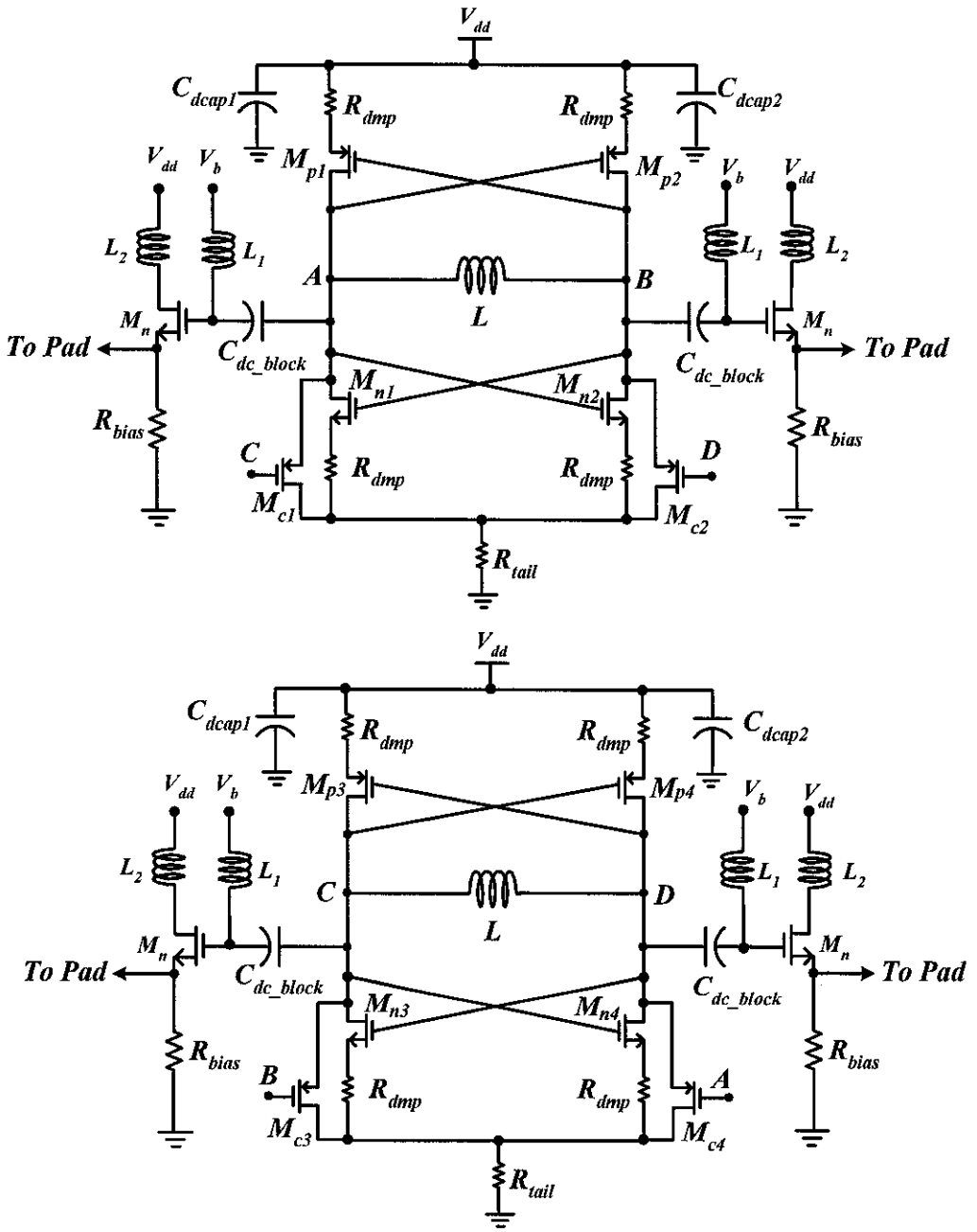


Figure 3.14 Schematic of LP³-QO design no. 3 with output buffers.

designed using 0.18 μm, 1 poly and 6 metal $CMOS$ process technology.

3.3.4 LP^3-QVCO Design No. 4 - 5

This section, presents the LC-tank based $LP^3 - QVCO$ design no. 4 and 5. The $LP^3 - QVCO$ designs use the combination of source damping resistor, tail biasing resistor and multifinger gate structure of MOS device. The $LP^3 - QVCO$ design is shown in Fig. 3.15. Two fully differential LC-tank $LP^3 - VCOs$ are parallel coupled by $pMOS$ ($M_{c1} \sim M_{c4}$) transistors to form $LP^3 - QVCO$. The coupling factor of 0.31[5] is chosen to achieve better phase accuracy. The $LP^3 - QVCO$ design no. 4 and 5 consist of $M_{n1} \sim M_{n4}$ and $M_{p1} \sim M_{p4}$ cross-coupled pairs. A symmetrical spiral inductor is designed and extracted in $ASITIC$ with the quality factor of 18.6. The polysilicon patterned ground shield (PGS) is used to enhance the quality factor of the inductor. $LP^3 - QVCO$ uses the combination of 40 Ω source damping resistor, multifinger gate structure of $pMOS$ based varactors and 102 Ω tail biasing resistor. The two designs are fabricated with different gate finger width configurations of the $pMOS$ varactors. A 4.3 GHz $LP^3 - QVCO$ design no. 4 uses (3.125 μm $\times$ 64 = 200 μm) and $LP^3 - QVCO$ design no. 5 uses (8 μm $\times$ 25 = 200 μm), respectively. Where 3.125 μm is the width per finger, 64 μm and 25 μm are the total number of fingers. The total gate width of $pMOS$ varactor is 200 μm. Both designs use common drain buffers (source-follower) circuit at each output. The buffer parameters are designed to achieve 50 Ω output impedance. A 10 pF dc blocking capacitor (C_{dc_block}) is used at each output of the $LP^3 - QVCO$. The decoupling capacitor (C_{dcap}) of 20 pF is also used between V_{dd} and ground terminals at each side of $LP^3 - QVCO$. The $LP^3 - QVCO$ design no. 4 and 5 implementation is carried out using 0.13 μm, 1 poly and 8 metal $RF\ CMOS$ process technology.

[5]The coupling factor vs phase error variation plot is shown in Chapter 5.

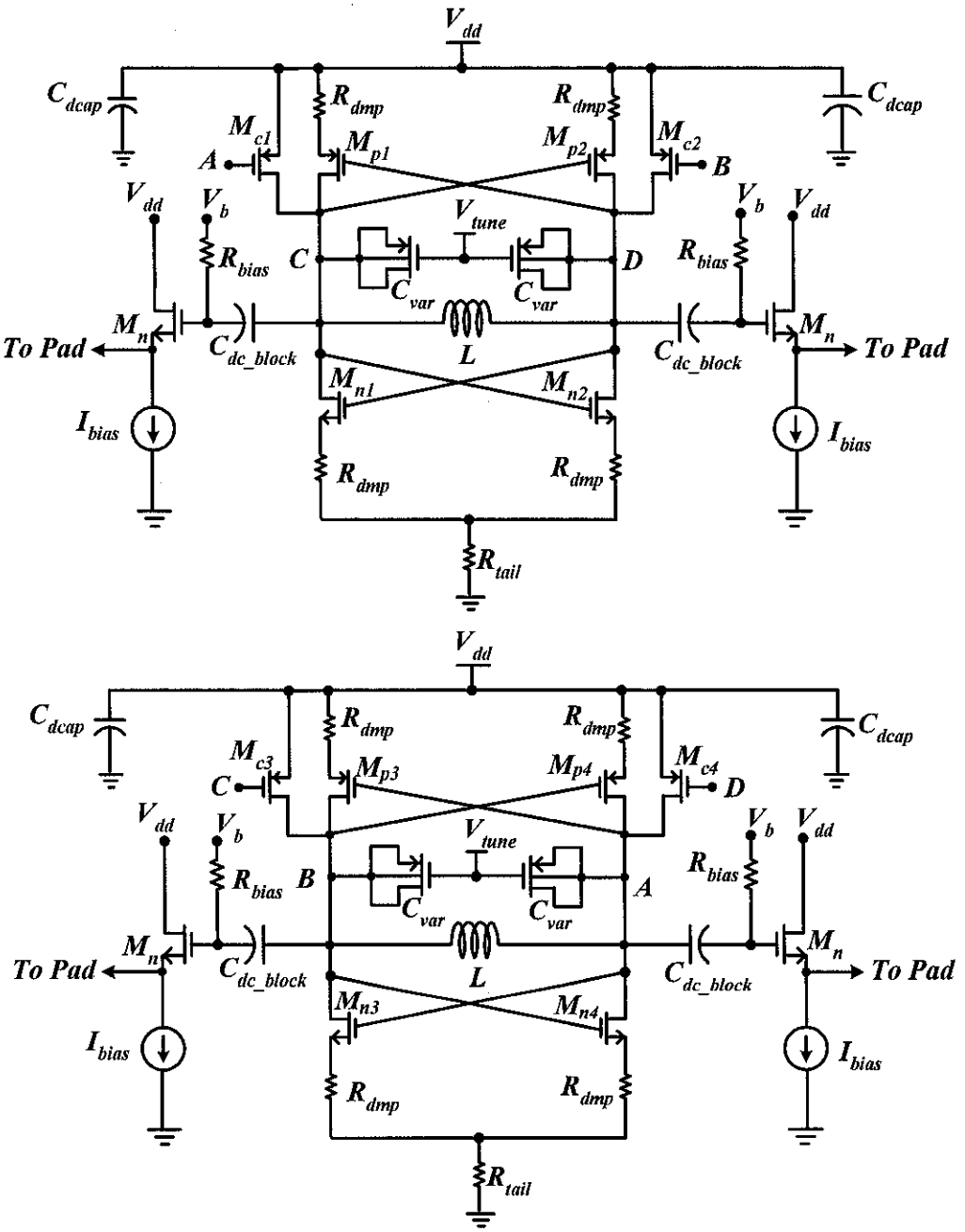


Figure 3.15 Schematic of LP^3-QVCO design no. 4 and 5 with output buffers.

3.3.5 LP^3-QVCO Design No. 6 - 7

Two complementary $LP^3 - VCOs$ are parallel coupled by $pMOS$ ($M_{c1} \sim M_{c4}$) transistors to generate quadrature output signals. The tail biasing MOS current mirror is replaced with tail biasing resistor, multifinger gate structure of MOS device and source damping resistor are the techniques used to achieve low phase noise in the $LP^3 - QVCO$ designs. The $pMOS$ varactors are used in both design. Both $LP^3 - QVCOs$ are designed with different gate finger width configurations of the $pMOS$ varactors to show phase noise improvement. The $LP^3 - QVCO$ design no. 6 uses (3.125 μm $\times$ 64 = 200 μm) while $LP^3 - QVCO$ design no. 7 uses (8 μm $\times$ 25 = 200 μm) gate finger width configuration of $pMOS$ varactor, respectively. Where 3.125 μm is the gate width of each finger, 64 and 25 are the total number of gate fingers. Both $LP^3 - QVCO$ designs use the 1.12 nH spiral inductor. The spiral inductor is extracted using $ASITIC$. The dc blocking capacitor (C_{dc_block}) of 1 pF is used at each output of $LP^3 - QVCO$ to block dc signal. The 20 pF decoupling capacitor (C_{dcap}) is also used between V_{dd} and ground metal wires at each side of the $LP^3 - QVCO$. The active device based current mirrors are used to bias the buffers. The current mirrors are shown previously in Fig. 3.8. A common drain buffers are also used in both designs, shown previously in Fig. 3.7 (a). The buffer is biased when 1.2 V dc voltage is applied at respective bond pad (V_b). The $LP^3 - QVCO$ design no. 6 and 7 are similar to the $LP^3 - QVCO$ design no. 5 and 6 shown in Fig. 3.15 except (C_{dc_block}) capacitance values. The proposed $LP^3 - QVCO$ is designed using 0.13 μm, 1 poly and 8 metal $RF\ CMOS$ process technology [102].

3.3.6 LP^3-QVCO Component Parameters

The parameters of above mentioned $LP^3 - QVCO$ designs (design no. 1 - 7) are summarized in Table 3.4. The $nMOS$ and $pMOS$ switching transistor's width and length ratios are represented by $(W_s/L)_n$ and $(W_s/L)_p$, respectively. The (W_c/W_s) represents the width ratio of the coupling transistor to switching transistor, respec-

Table 3.4 QVCO design parameters summary.

Design	Process (μm)	L (nH)	Var dimensions	$(W_s/L)_n$	$(W_s/L)_p$	W_c/W_s
1	0.18	1.13	*pn*-var (0.5 pF)	444	1111	0.32
2	0.18	1.13	*pn*-var (0.63 pF)	388	1111	0.28
3	0.18	1.13	-	388	1111	0.28
4	0.13	1.12	$3.125 \times 64 = 200$ μm	384	1538	0.31
5	0.13	1.12	$8 \times 25 = 200$ μm	384	1538	0.31
6	0.13	1.12	$3.125 \times 64 = 200$ μm	384	1538	0.25
7	0.13	1.12	$8 \times 25 = 200$ μm	384	1538	0.25

tively. Three $LP^3 - QVCO$ architectures (design no. 1 to 3) are designed by using 0.18 μm $CMOS$ and RF $CMOS$ process technology. The coupling factor of 0.32 and 0.28 are chosen for the design no. 1, design no. 2 and design no. 3, respectively. The design no. 4 to 7 $LP^3 - QVCO$ architectures are designed by using 0.13 μm RF $CMOS$ process technology. A $pMOS$ based varactors with multifinger gate width configuration are used in design no. 4 to 7. The coupling factor of 0.31 is used in design no. 4 and 5, respectively. This table also includes the inductance, varactor values and process technology. The design no. 4 to 7 use 1.12 nH symmetrical spiral inductors. Both inductors use PGS to avoid eddy current losses.

3.4 LP^3-QVCO Design Flow

The $LP^3 - QVCO$ architecture design flow is shown in Fig. 3.16. First, the design of $DS-VCO$ with source damping resistors, tail biasing resistors and multifinger gate width configuration of the $pMOS$ based varactors are implemented [95]. The design and optimization of power consumption, phase noise and phase error are carried out for $LP^3 - VCO$ architectures. The $LP^3 - VCO$ is redesigned, if required results are not achieved. Next, two $VCOs$ are parallel coupled by $nMOS$ or $pMOS$ transistors to form $LP^3 - QVCO$ architecture. The $LP^3 - QVCO$ architectures are designed with

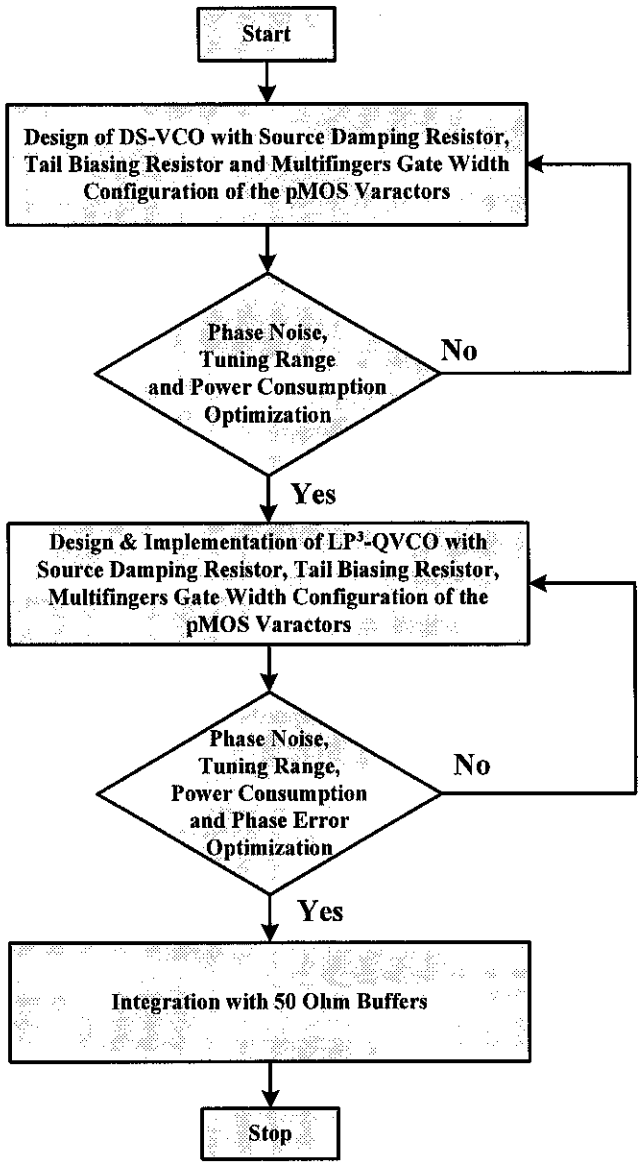


Figure 3.16 LP³-QVCO design flow.

the integration of above mentioned techniques. The phase noise, power consumption and tuning range optimizations are also carried out for $LP^3 - QVCO$ architectures. Finally, $LP^3 - QVCO$ integration is carried out with 50 Ω output buffers.

The implementation strategy is also explained in Chapter 4. Based on the conclusion and optimization, $LP^3 - QVCO$ architectures are implemented with common drain buffers. The LC-tank design includes the integration of spiral inductors with PGS. The circular spiral inductors and symmetrical spiral inductors are used in the designs of $LP^3 - QVCO$. The pn-junction varactors and $pMOS$ varactors are implemented in different $LP^3 - QVCO$ designs.

3.5 Summary

In this chapter, the innovative techniques are integrated in $DS - VCO$ design. The $DS - VCO$ design is leading towards the design of the $LP^3 - VCO$ architecture. The $LP^3 - VCO$ architecture is used in the design of $LP^3 - QVCO$. Different $LP^3 - QVCO$ designs are presented in this chapter. The innovative oscillator design techniques are also summarized in this chapter. Source damping resistor, tail biasing resistor, multifinger gate structure of the MOS varactor and fully differential VCO structure are adopted in the design of $LP^3 - VCO$ architecture. Next, spiral inductor designs are presented in 0.18 μm and 0.13 μm $CMOS$ process technologies. The s-parameters analysis are also carried out to verify the inductor π-model. The inductor π-model is extracted from $ASITIC$. The patterned ground shield (PGS) is used under the inductor to reduce the eddy currents. The integrated capacitors such as MIM and finger capacitors are also described, briefly. Next, different types of varactor designs are also discussed. This includes the pn-junction varactors and $pMOS$ based varactors. The simulation results show the $pMOS$ varactor capacitance behavior with the variation of the dc tune voltage. Common drain buffer with 50 Ω impedance matching is also presented. Next, seven $LP^3 - QVCO$ designs with the integration of buffer circuits and parameter values are discussed. The $LP^3 - QVCO$ design performance parameters are also summarized. Finally, the $LP^3 - QVCO$

CHAPTER 4

LP^3-QVCO IMPLEMENTATION

4.1 Introduction

The oscillator designs are fabricated on a wafer and testing is carried out in the laboratory. The laboratory equipment varies from small multimeters to signal source analyzer (SSA) or spectrum analyzer (SA). The testing of device is carried out in different ways, as mentioned in state of the art work [103], [104], [105], [106]. One method is on-wafer probing while other method involves the printed circuit board (PCB) formation and testing. In this work, the device under test (DUT) is done by on-wafer probing to avoid the packaging of the chips. However, on wafer testing method introduces challenges due to low substrate resistivity and low conductive metallization which encountered with low cost process. This requires a large pad size in the adaption of cascade ground-signal-ground (GSG) and ground-signal-ground-signal-ground ($GSGSG$) microprobe electrode probing provides significant rise in the pad substrate capacitance with a tradeoff of lower dc contact resistance. The ($GSGSG$) bond pad configuration is also implemented with $LP^3 - QVCO$ designs. The bond pads are used to measure the outputs, and to provide necessary dc voltage signals [105]. A testing and requirements of system-on-chip (SOC) has also been proposed [106]. The measurement test setup for $LP^3 - QVCO$ designs is also described. The physical realization of the $LP^3 - QVCO$ designs are also presented. $LP^3 - QVCO$ layouts and fabricated chips are also discussed with their pin configurations.

4.2 Implementation and Layout

After designing the circuits at transistor level, the next step is to prepare the designs for implementation. The symmetrical layout design of the $LP^3 - QVCO$

circuits is necessary for the achievement of better output performance results. In this section, seven layout designs of the proposed $LP^3 - QVCO$ are presented. The layouts are designed in "Virtuouse layout editor" using "Cadence" [98]. The layout verifications are carried out by "Caliber" (Mentor Graphics) tools [107].

4.2.1 Layout of Design No. 1

The $LP^3 - QVCO$ layout design no. 1 is shown in Fig. 4.1. It includes the LC-tank circuit and a cross-coupled transistor pairs. The inductors are configured in parallel combination to achieve the required inductance value. The $3D$ "Electrom-Magnetic" (EM) [38] simulations are required to be carried out to ensure the dc-Q of the inductors. The parallel combination of the inductors occupy larger area of the chip, and Q performance is also influenced by the parallel combination of the inductors. The circular spiral inductors are used with PGS to avoid the eddy currents. The pn-junction diode based varactors are also clearly indicated in the layout. The MIM decoupling capacitors are also shown in the Fig. 4.1. The power supply is decoupled with the utilization of MIM decoupling capacitors between positive power supply and ground terminals. The common drain buffers are also implemented at each output of the $LP^3 - QVCO$ circuit. The ground-signal-ground-signal-ground ($GSGSG$) bond pad configuration is implemented in the layout designs. The bond pads clearly indicate the signal names. Metal 1, metal 2 and metal 3 are used in the layout design no. 1. The higher metals are not used for components connections. In this design, the active devices are covered by double guard rings to increase the substrate isolation. The $LP^3 - QVCO$ layout is designed by utilizing 0.18 μm, 1 poly and 6 metal $RF\ CMOS$ process technology.

4.2.2 Layout of Design No. 2 and 3

The $LP^3 - QVCO$ layout design no. 2 and 3 are described in this section. The layout designs of $LP^3 - QVCO$ and $LP^3 - QO$ are shown in Fig. 4.2 and Fig. 4.3,

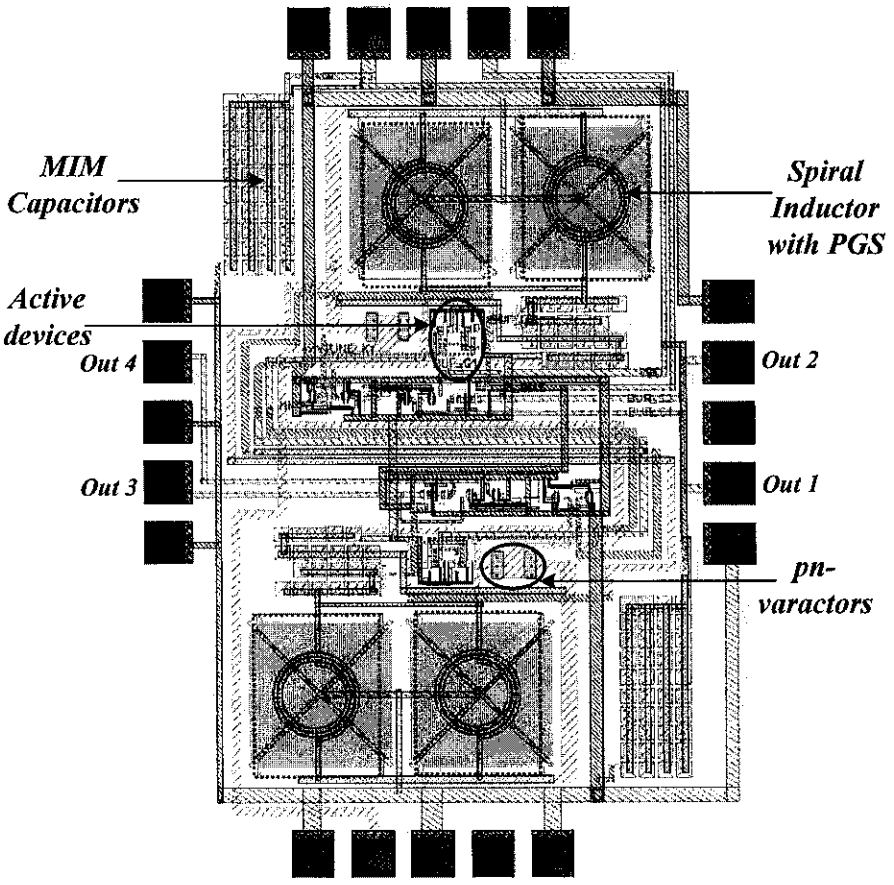


Figure 4.1 Layout of design no. 1

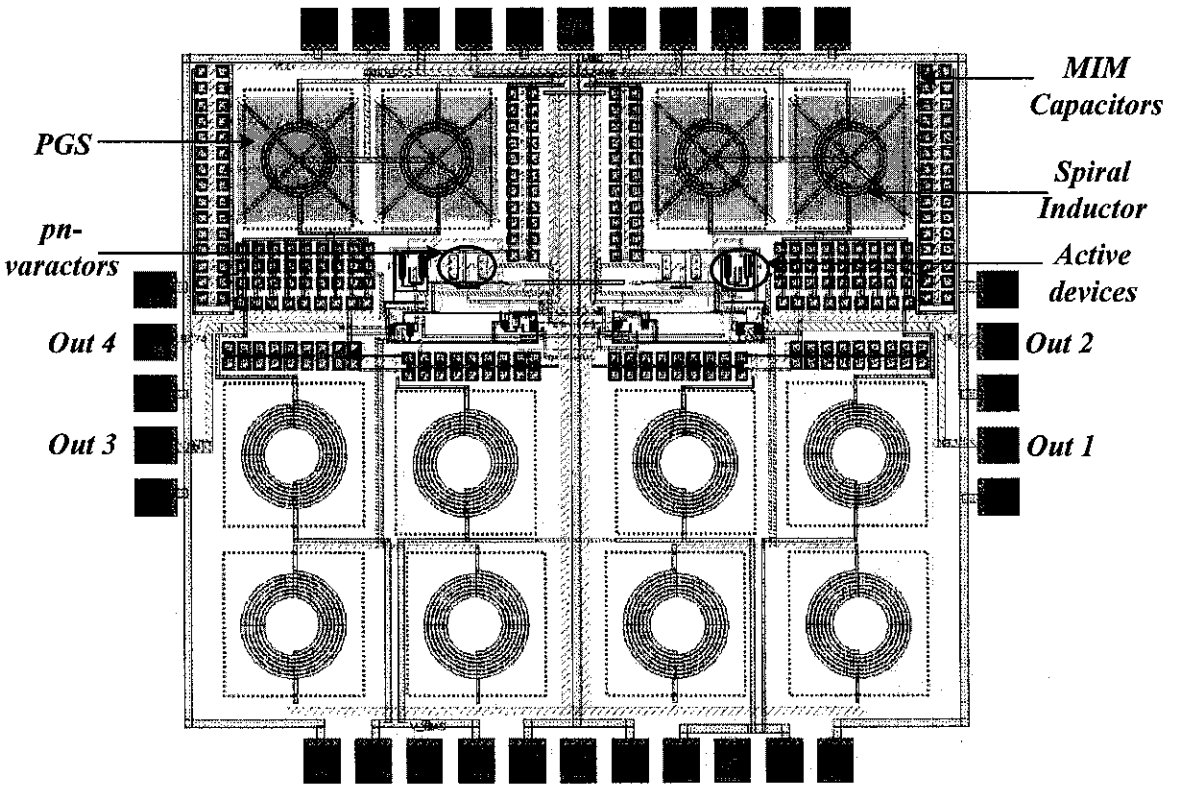


Figure 4.2 Layout of design no. 2

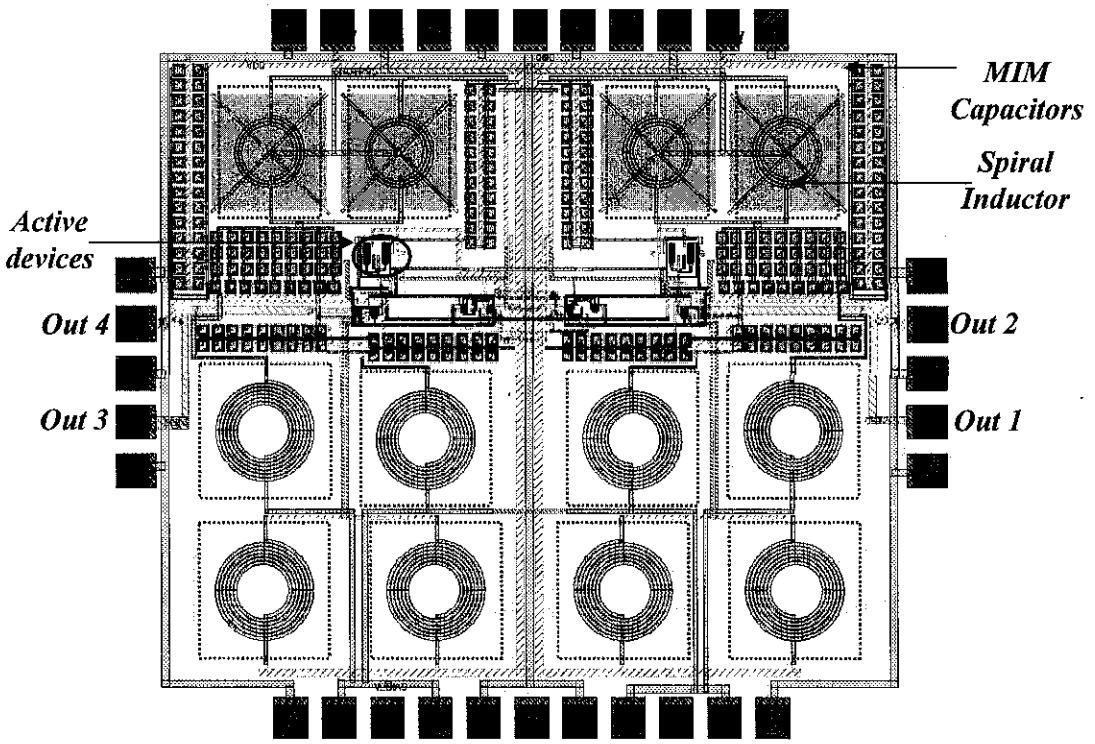


Figure 4.3 Layout of design no. 3

respectively. The major portion of the layout is occupied by the circular spiral inductors. The LC-tanks of both layouts compromise four circular spiral inductors with patterned ground shields (PGS). MIM decoupling capacitors are used between power supply and ground wires at each side of the layout to avoid the power supply variations. The pn-junction varactors are also used in LC-tanks of both layout designs. MIM capacitors are also used at each $LP^3 - QVCO$ output and buffer to block the dc signal. Common drain buffer configuration is shown in Fig. 3.7 (b). The total eight 15.8 nH inductors are utilized in both layout designs. The four common drain buffers contain the eight spiral inductors. Fig. 4.3 shows the layout design of the $LP^3 - QO$ circuit. It occupies the same area as in the layout design no. 2 shown in Fig. 4.2. The transistors, MIM capacitors and resistors are surrounded by double guard rings in both layout designs. The double guard rings are used with n-type tied to dc power supply V_{dd} and connecting p-type to ground terminals to provide the substrate isolation [108]. The ground-signal-ground-signal-ground ($GSGSG$) bond pad configuration is used in both layout designs. The dummy (D) bond pads are also implemented in both layout designs. The layout implementations of both circuits are carried out using 0.18 μm, 1 poly and 6 metal $CMOS$ process technology.

4.2.3 Layout of Design No. 4 and 5

In Fig. 4.4 and Fig. 4.5, the symmetrical layouts are designed for the $LP^3 - QVCO$ circuits. The center tapped symmetrical spiral inductor with PGS is implemented in both $LP^3 - QVCO$ layout designs, shown in Fig. 3.5. The "ultra-thick metal" UTM is used in most of the layout component connections. The sheet resistance of (UTM) is 5.2 Ω. The "metal-top" ($M - Top$) with sheet resistance of 22 Ω is also used in both layout designs for component interconnections. The $pMOS$ varactors with different finger width configurations are implemented in both designs. The strip and square shaped layouts of $pMOS$ varactors are implemented in $LP^3 - QVCO$ design no. 4 and 5, respectively. The physical realization of the $pMOS$ varactors used in $LP^3 - QVCO$ design no. 4 and 5 are shown in Appendix B. The multifingers gate

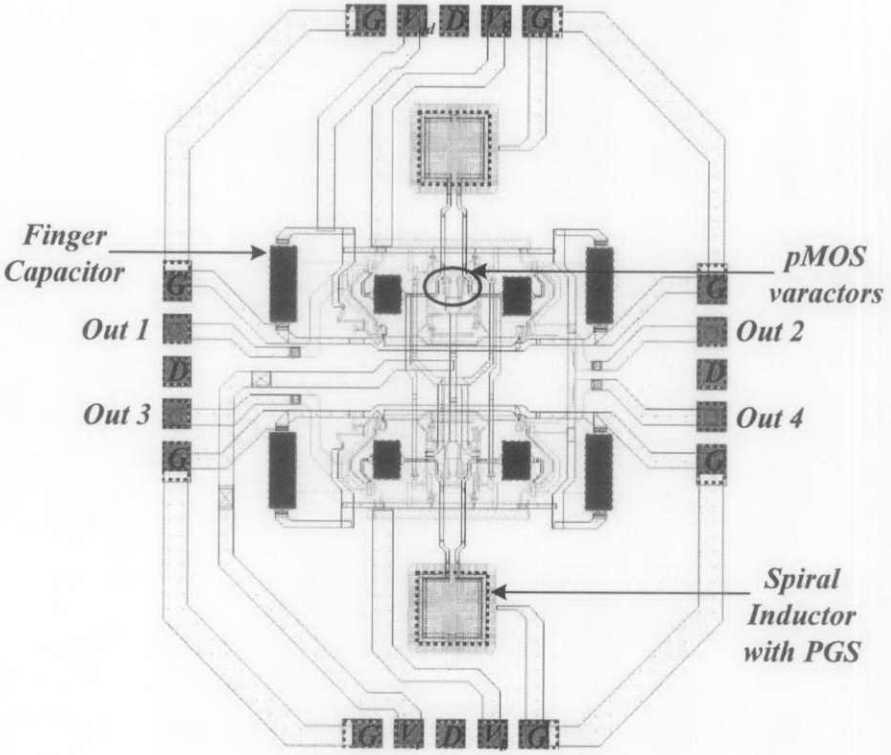


Figure 4.4 Layout of design no. 4

width configuration of design no. 4 and 5 result in different layout shapes. The dc power supply V_{dd} is decoupled by using finger capacitors ($FM-6$). The decoupling capacitors are implemented at positive power supply and ground terminals. The dc blocking capacitors ($FM-6$) are also used at the core output of LP^3-QVCO. The common drain buffer configuration is shown in Fig. 3.7 (a). The buffer bias voltage is applied at V_b bond pad. The tuning voltage is applied at V_t bond pad. The ground-signal-ground-signal-ground ($GSGSG$) bond pad configuration is used in the layout design. The layout implementations of both circuits are carried out using 0.13 μm, 1 poly and 8 metal $RF\ CMOS$ process technology.

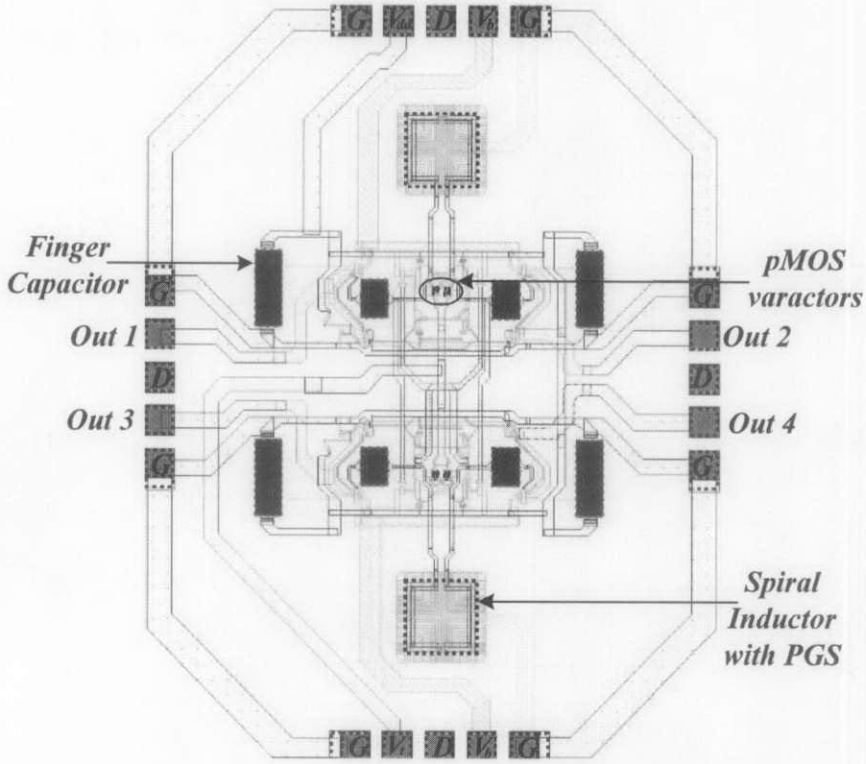


Figure 4.5 Layout of design no. 5

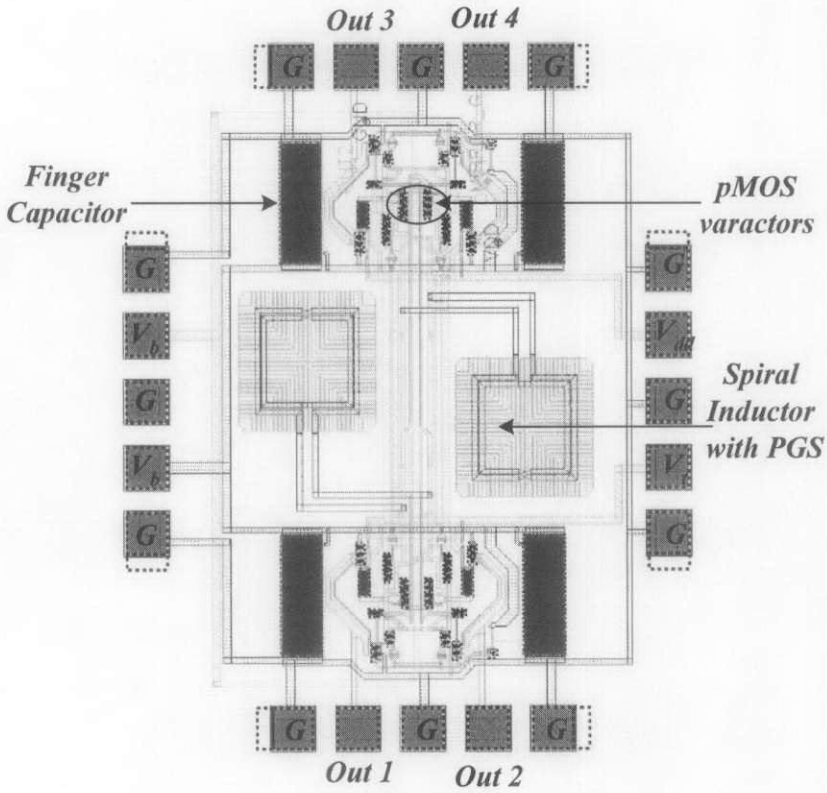


Figure 4.6 Layout of design no. 6

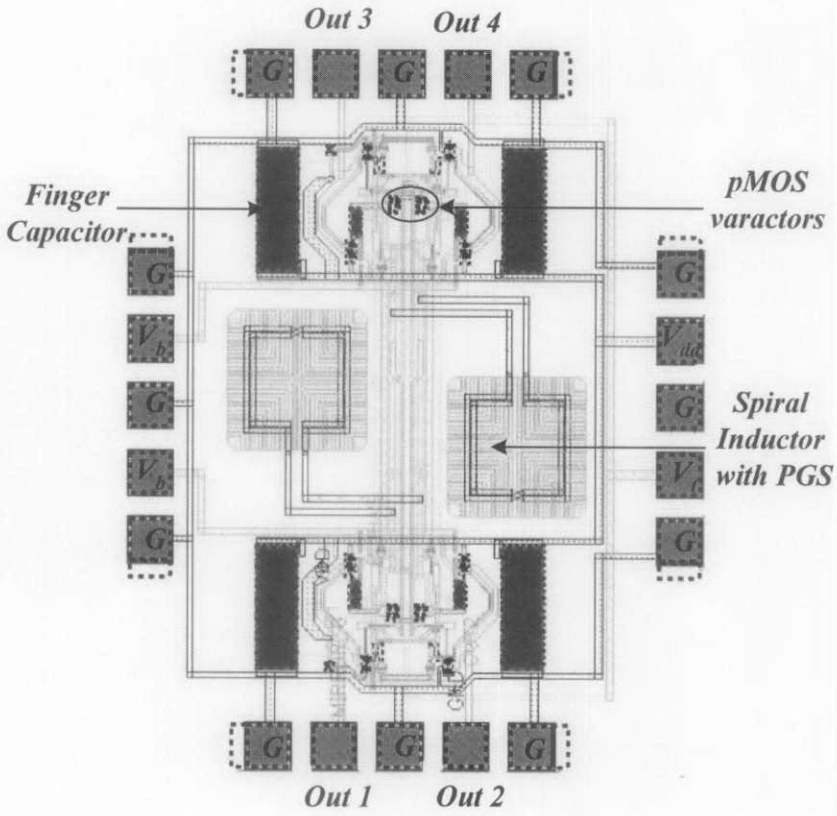


Figure 4.7 Layout of design no. 7

4.2.4 Layout of Design No. 6 and 7

The layout design no. 6 and 7 are shown in Fig. 4.6 and Fig. 4.7, respectively. The center tapped symmetrical spiral inductor with PGS is used in these layouts. The inductors are placed in the center of the chip as compared to the design no. 5 and 6. The multifingers gate width configuration of $pMOS$ varactors are used in both designs. The physical realization of the $pMOS$ varactors used in $LP^3 - QVCO$ design no. 6 and 7 are also shown in Appendix B. The fingers capacitors $(FM - 6)$ are also implemented at positive power supply voltage V_{dd} and ground terminals, at each side of the circuit. The $GSGSG$ bond pads configuration are also shown in both layout designs. The ground bond pads are distributed around the chip to reduce the effect of inductive down bond [56]. The common drain buffers are also implemented at each output of the $LP^3 - QVCO$ design. The common drain buffer is shown in the Fig. 3.7 (a), previously. The ground-signal-ground-signal-ground $GSGSG$ bond pad configuration is also implemented in both $LP^3 - QVCO$ layouts. The buffer bias, positive dc power supply and dc tuning voltages are applied at the respective bond pads. The layout of both circuits are designed by using 0.13 μm, 1 poly and 8 metal $RF\ CMOS$ process technology.

4.3 LP^3-QVCO Chip Pin Configurations

Fig. 4.8 shows the chip pin configurations of $LP^3 - QVCO$ designs. Fig. 4.8 (a) shows the pin configurations of $LP^3 - QVCO$ design no. 1, 4, 5, 6 and 7, respectively. There are 20 I/O pin connections of $LP^3 - QVCO$ design no. 1, 4, 5, 6 and 7. The pins configuration of $LP^3 - QVCO$ design no. 2 and 3 are shown in the Fig. 4.8 (b). Total 32 I/O pins are used in the implementation of $LP^3 - QVCO$ design no. 2 and 3. However, the pin signals are different for $LP^3 - QVCO$ designs. The configuration of each die pin is summarized in Table 4.1. This table describes the ground, positive dc power supply, buffer biasing voltage, dc tuning voltage of varactor, dummy and output pins of $LP^3 - QVCO$ designs. The V_{dd} pin indicates the positive voltage

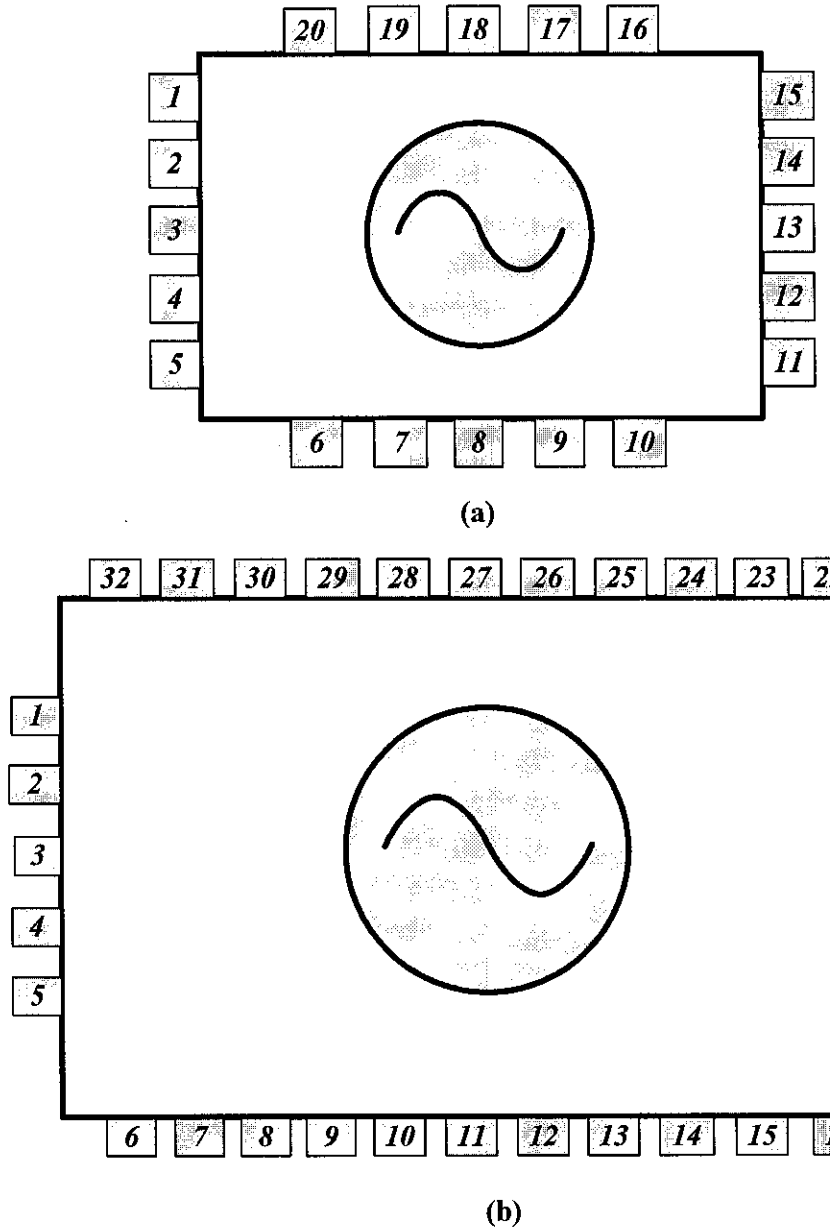


Figure 4.8 $LP^3 - QVCO$ chips configuration for (a) 20 pins and (b) 32 pins.

Table 4.1 LP³-QVCO chips pin configurations.

Design No.	Ground Pins	V_{dd} Pins	Buffer Bias Pins	V_t Pins	Dummy Pins	Outputs Pins
1	1, 3, 5, 6, 8 10, 11, 13, 15 16, 18, 20	19	17	7	9	2, 4, 12, 14
2	1, 3, 5, 6, 8, 10, 12, 14, 16, 17, 19, 21, 22, 24, 26, 28, 30, 32	23, 31	7, 9, 13, 15	25, 29	11, 27	2, 4, 18, 20
3	1, 3, 5, 6, 8, 10, 12, 14, 16, 17, 19, 21, 22, 24, 26, 28, 30, 32	23, 31	7, 9, 13, 15		11, 27	2, 4, 18, 20
4, 5	1, 5, 6, 10, 11, 15, 16, 20	19	9, 17	7	3, 8, 13, 18	2, 4, 12, 14
6, 7	1, 3, 5, 6, 8, 10, 11, 15,16 18, 20	14	2, 4	12	13	7, 9, 17, 19

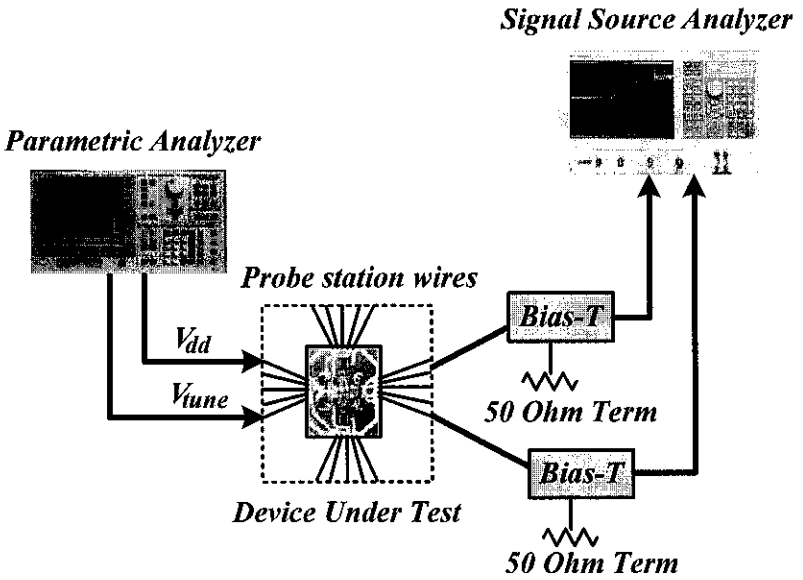
supply. The V_t pin indicates the dc tune voltage. The dc tune voltage is varied and $LP^3 - QVCO$ is set at different output frequencies. The (D) pin is a dummy or it has no-connection with circuit. The *Out 1*, *Out 2*, *Out 3* and *Out 4* indicate the $LP^3 - QVCO$ buffer outputs. The buffer bias V_b pin indicates the buffer biasing voltage. The buffer bias voltages are 1.2 V and 1.8 V for the $LP^3 - QVCO$ designs implemented using 0.13 μm and 0.18 μm process technologies, respectively.

4.4 LP^3-QVCO Measurement Test Setup

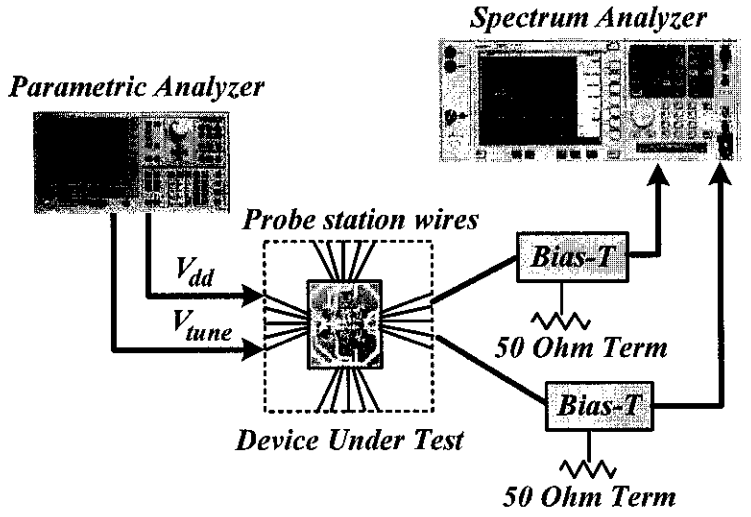
The $LP^3 - QVCO$ designs are measured on wafer probing method. The micro-probe station (model 9000), parameter analyzer (PA), digital oscilloscope, spectrum analyzer (SA), bias tee and signal source analyzers (SSA) are used to measure the $LP^3 - QVCO$ fabricated prototypes. Next, a brief overview of above mentioned equipment is given.

- A precision semiconductor parameter analyzer (PA) (Agilent 4156C) [39] is used to provide the dc sweep analysis, currents and power consumption of the designs.
- Probe station is used to measure the $LP^3 - QVCO$ on-wafer designs. The ground-signal-ground-signal-ground ($GSGSG$) configuration is used for the wafer probing.
- Spectrum analyzer (Agilent E 4440A) [39] is used to measure the output frequency spectrum and output RF power of $LP^3 - QVCO$ designs.
- Signal source analyzer (SSA) (Agilent E 5052A) [39] is used to measure the phase noise of the $LP^3 - QVCO$. Averaging (200 times) is also selected to achieve optimum value of phase noise.
- Tektronix digital phosphor oscilloscope (TDS 3012B) is used to measure the quadrature outputs, phase difference and transient sweep of the oscillator. Two $LP^3 - QVCO$ outputs are connected simultaneously to the oscilloscope.
- The bias tee is used to provide the $LP^3 - QVCO$ output connection to spectrum analyzer, signal source analyzer and digital oscilloscope.

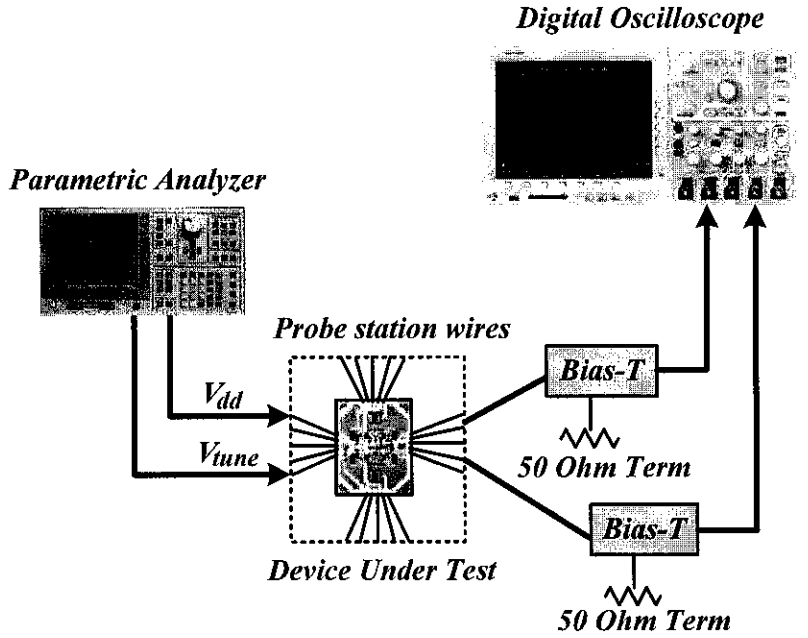
Each time two $LP^3 - QVCO$ outputs are measured using bias tee with termination resistance of 50 Ω. The $LP^3 - QVCO$ measurement test setups for phase noise, RF output power, frequency spectrum and transient analysis are shown in Fig. 4.9. Phase


Signal Source Analyzer
Parametric Analyzer
Probe station wires
Bias-T
V_{dd}
V_{tune}
50 Ohm Term
Bias-T
Device Under Test
50 Ohm Term

(a)


Spectrum Analyzer
Parametric Analyzer
Probe station wires
Bias-T
V_{dd}
V_{tune}
50 Ohm Term
Bias-T
Device Under Test
50 Ohm Term

(b)



(c)

Figure 4.9 (a) LP^3-QVCO measurement test setup for phase noise (b) LP^3-QVCO measurement test setup for RF output power and frequency spectrum and (c) LP^3-QVCO transient signal measurement setup.

noise measurement setup is shown in Fig. 4.9 (a). This setup contains the device under test (DUT), paramcter analyzer, bias tee and signal source analyzer. Signal source analyzer (SSA) is used to measure the phase noise of $LP^3 - QVCO$. The output frequency spectrum and RF power level measurement test setup is shown in Fig. 4.9 (b). The spectrum analyzer is used for the measurement of frequency spectrum and output power signal level. The transient analysis and quadrature phase error measurement test setup is shown in Fig. 4.9 (c). The digital oscilloscope is used to measure the transient analysis and phase accuracy of the quadrature outputs.

4.5 LP^3-QVCO Fabricated Chips

The $LP^3 - QVCO$ designs are fabricated using 0.18 μm and 0.13 μm standard $CMOS$ and $RF\ CMOS$ process technologies. This section, describes the seven fabricated $LP^3 - QVCO$ die designs. On-chip common drain buffers are also implemented at each output of the $LP^3 - QVCO$ designs. Three $LP^3 - QVCO$ designs (design no. 1, 2 and 3) are implemented using 0.18 μm process technology while remaining designs are fabricated using 0.13 μm process technology. The magnified micrographs of the fabricated dies are captured by microprobe station camera.

4.5.1 LP^3-QVCO Fabrication Using 0.18 μm Process

The fabricated $LP^3 - QVCO$ design no. 1 die micrograph is shown in Fig. 4.10. $LP^3 - QVCO$ die contains the pn-junction varactors and inductors. Two parallel circular spiral inductors are used to get the required inductance value. The PGS utilization is clearly shown. The MIM decoupling capacitors and pn-junction based varactors are also clearly indicated. The active devices are also encircled. Design no. 1 occupies an area of 3.3 mm^2. The $LP^3 - QVCO$ design no. 1 implementation is carried out using 0.18 μm, 6 metal and 1 poly $RF\ CMOS$ process technology.

The fabricated $LP^3 - QVCO$ design no. 2 die micrograph is shown in Fig. 4.11. This design is fabricated with on-chip common drain buffers. The buffer configuration

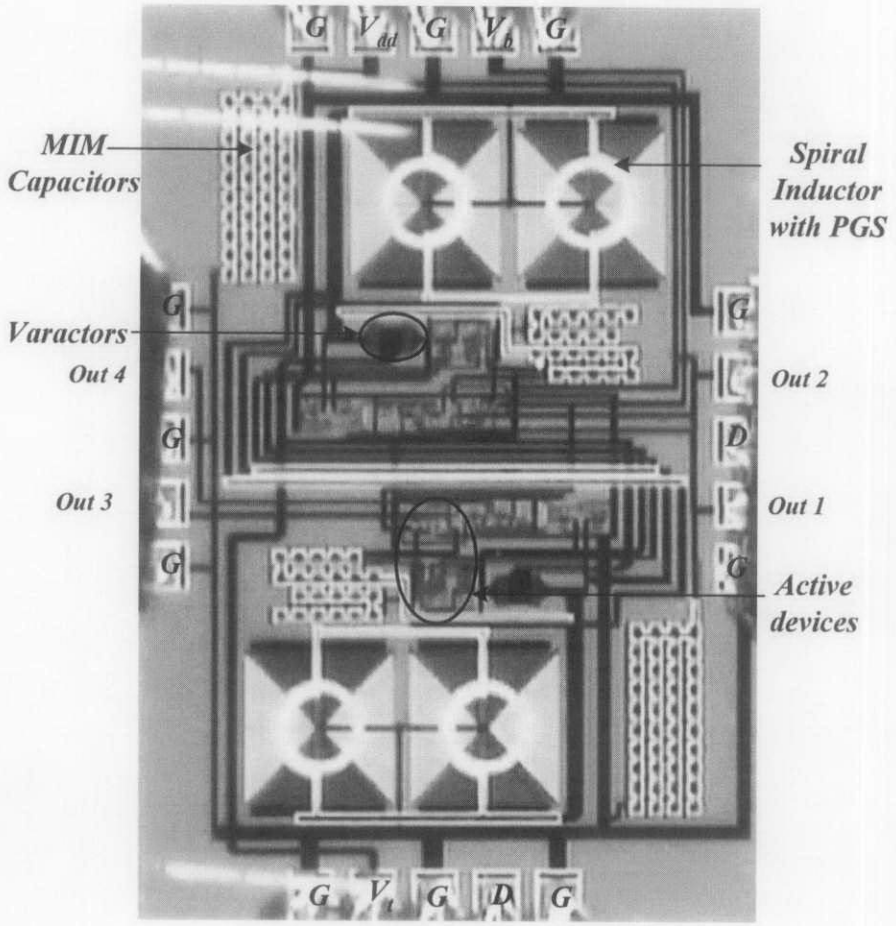


Figure 4.10 Design no. 1. A 2.8 GHz LP³-QVCO magnified micrograph.

contains inductors to avoid unwanted noise signal flow from dc power supply. The MIM capacitors, active device area, pn-junction varactors and spiral inductor with PGS are clearly indicated in Fig. 4.11.

Design no. 3 die magnified micrograph is shown in Fig. 4.12. In this design, the varactors are not used and $LP^3 - QO$ operates at the center frequency of 3.8 GHz. Design no. 2 and 3 consume the same chip area of 5.5 mm^2. Design no. 2 and 3 implementations are carried out using 0.18 μm, 6 metal and 1 poly standard $CMOS$ process technology.

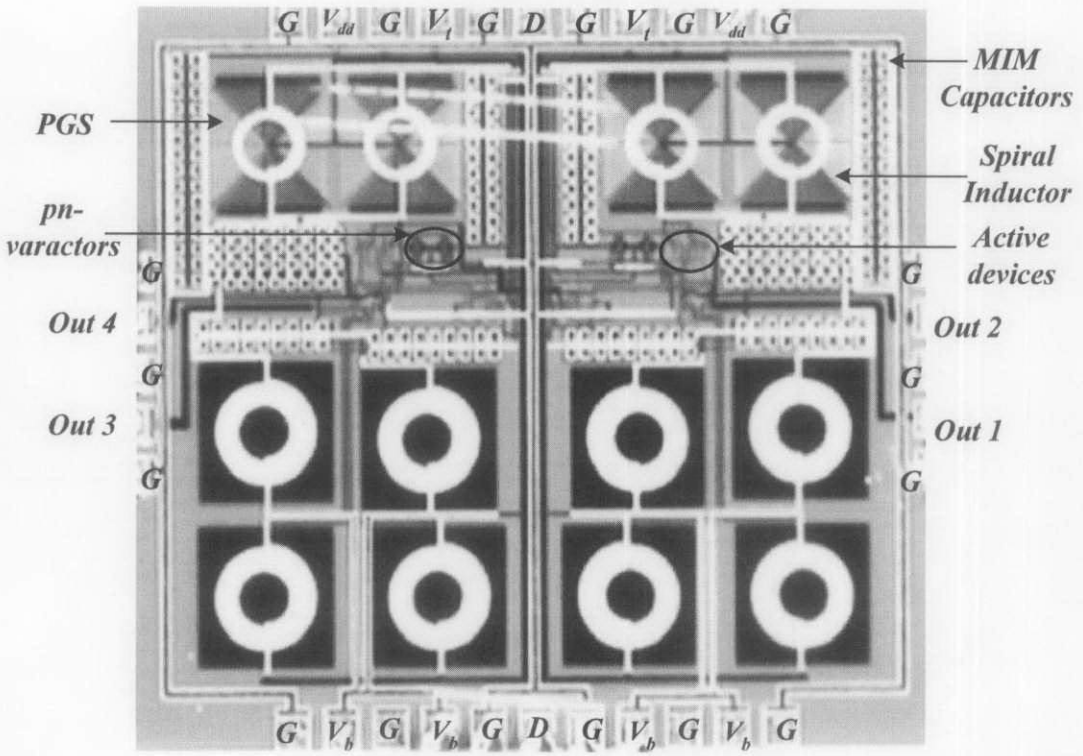


Figure 4.11 Design no. 2. A 3.1 GHz LP^3-QVCO magnified micrograph.

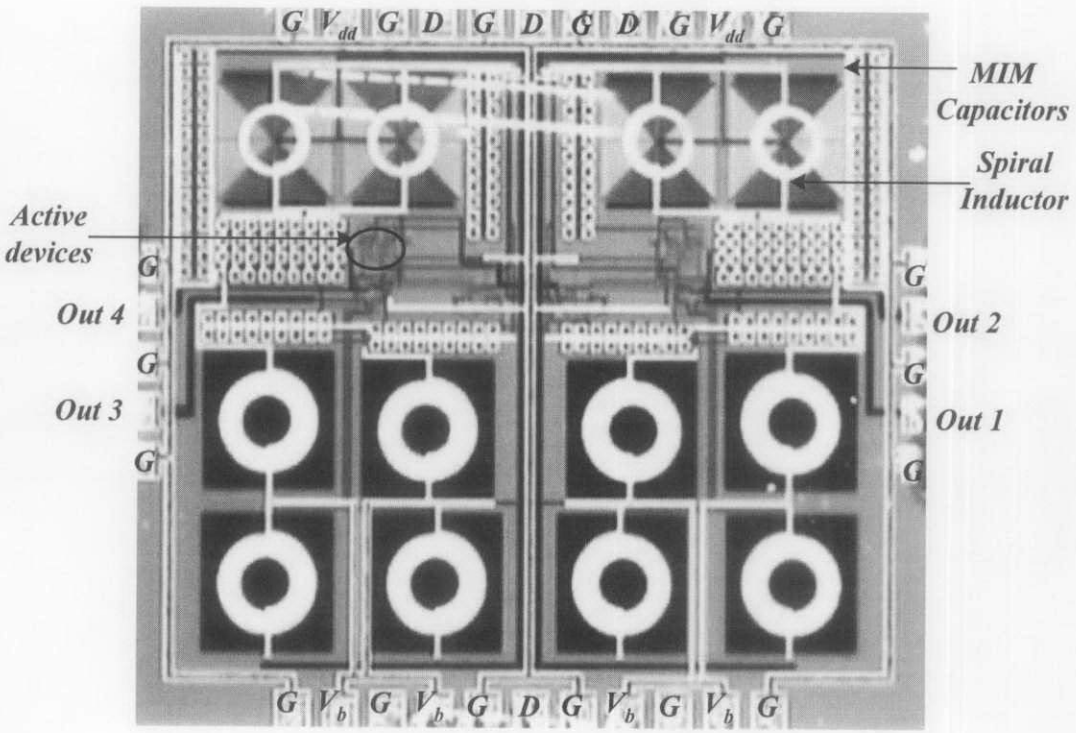


Figure 4.12 Design no. 3. A 3.8 GHz LP³-QVCO magnified micrograph.

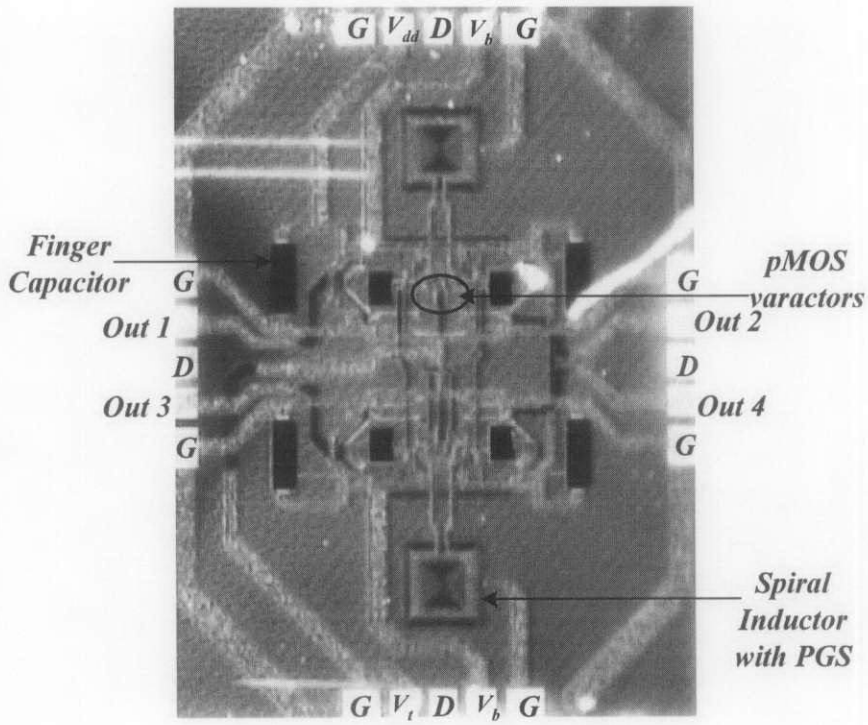


Figure 4.13 Design no. 4. A 4.35 GHz LP³-QVCO magnified micrograph.

4.5.2 LP³-QVCO Fabrication Using 0.13 μm Process

The fabricated $LP^3 - QVCO$ design no. 4 die micrograph is shown in Fig. 4.13. The symmetrical spiral inductor with PGS is implemented in this design. The $pMOS$ based varactors are used to achieve variable capacitance value. This design operates at the center frequency of 4.35 GHz. Fig. 4.13 also shows the finger capacitors ($FM-6$). This $pMOS$ varactor uses smaller finger gate width (3.125 μm) configuration.

The micrograph of design no. 5 is shown in Fig. 4.14. The center frequencies of design no. 4 and 5 are same. The $pMOS$ varactor uses 8 μm finger gate width configuration. The $pMOS$ varactor is square shaped. Design no. 4 and 5 occupy the die area of 2.2 mm^2.

Design no. 6 die micrograph is shown in Fig. 4.15. This $LP^3 - QVCO$ design operates at the center frequency of 5.1 GHz. The symmetrical spiral inductors are

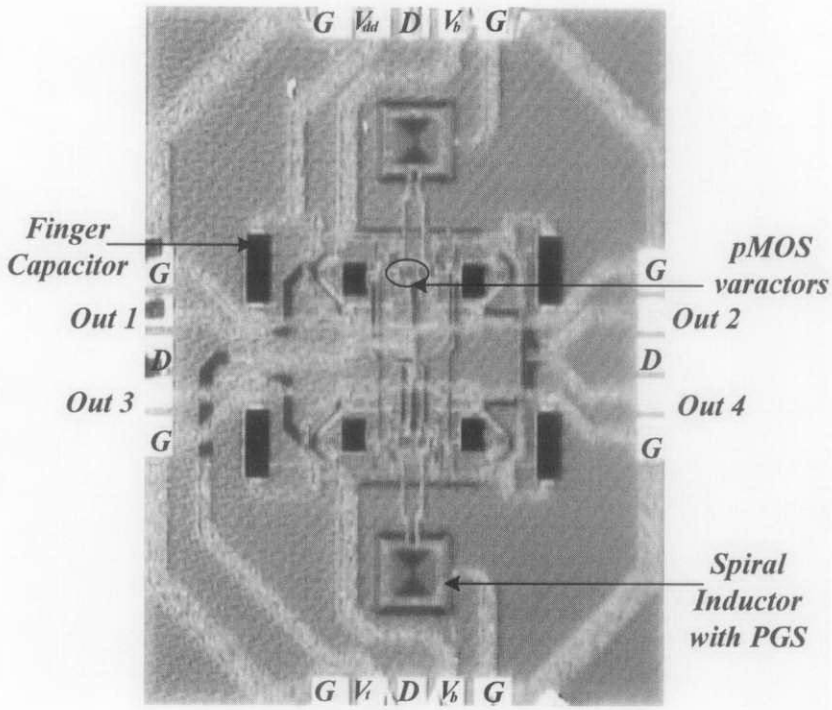


Figure 4.14 Design no. 5. A 4.35 GHz LP^3-QVCO magnified micrograph.

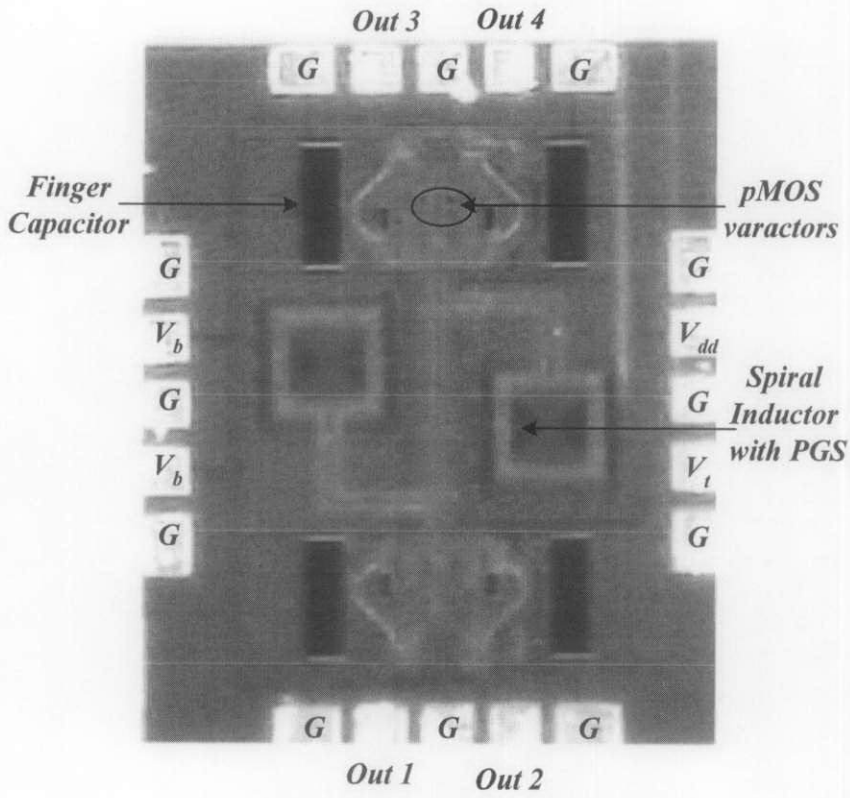


Figure 4.15 Design no. 6. A 5 GHz LP^3-QVCO micrograph.

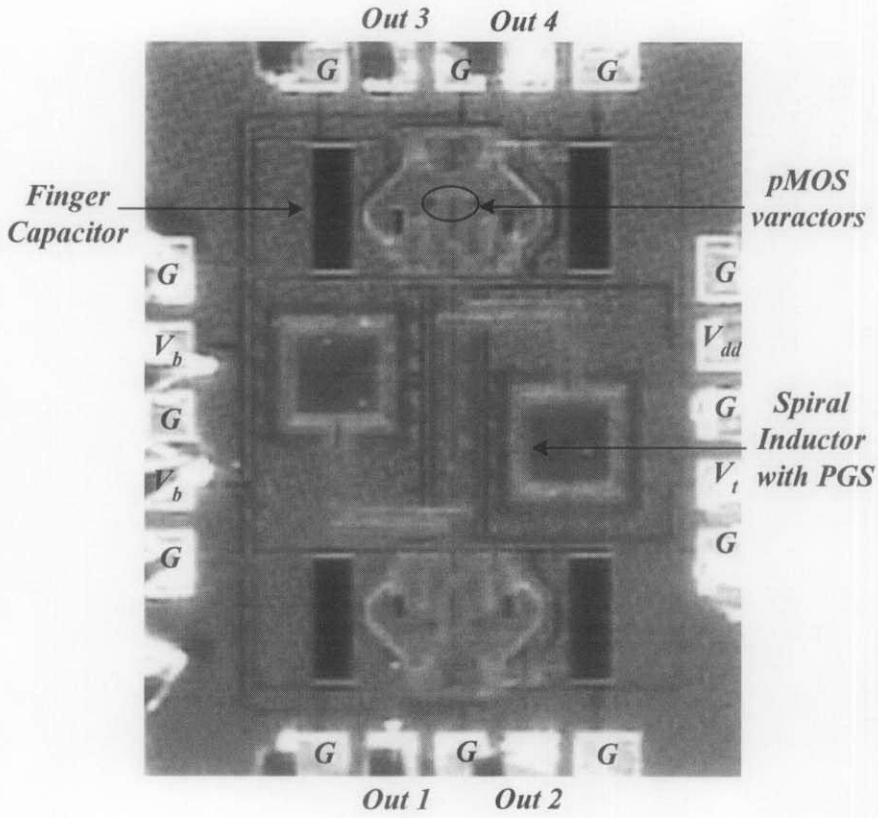


Figure 4.16 Design no. 7. A 5 GHz LP^3-QVCO micrograph.

Table 4.2 Dimensions of fabricated LP^3-QVCO chips.

Design no.	Process (μm)	Dimensions (mm^2)
1	0.18	$2.1 \times 1.5 = 3.3$
2, 3	0.18	$2.5 \times 2.2 = 5.5$
4, 5	0.13	$1.7 \times 1.3 = 2.2$
6, 7	0.13	$1.1 \times 0.87 = 0.95$

integrated in the center of die as compared to design no. 4 and 5. Both designs use different finger gate width configuration of $pMOS$ varactors. Design no. 7 micrograph is shown in Fig. 4.16. The operating frequencies of design no. 6 and 7 are same. The design no. 6 and 7 occupy the die area of 0.95 mm^2. The $LP^3 - QVCO$ design no. 4 to 7 are implemented using 0.13 μm $RF\ CMOS$ process technology with 8 metal and 1 poly.

All fabricated $LP^3 - QVCO$ chip dimensions are summarized in Table 4.2. This table includes the design numbers, process technologies and dimensions of the fabricated $LP^3 - QVCO$ chips. The smallest $LP^3 - QVCO$ design no. 6 and 7 occupy an area of 0.95 mm^2. The difference between design no. 2 and 3 is of varactor circuit. Design no. 4 and 5 also occupy the same chip dimensions.

4.6 Summary

This chapter describes the implementation of seven $LP^3 - QVCO$ designs. The physical realization for $LP^3 - QVCO$ designs are also described with bond pad configurations. The $LP^3 - QVCO$ chip pin configurations, implementation and measurement test setups are described. The measurement setups for phase noise, power dissipation, output frequency spectrum, transient analysis and phase error are also presented. The measurement equipment includes probe station, spectrum analyzer, signal source analyzer, digital oscilloscope and parameter analyzer. The fabricated

$LP^3 - QVCO$ die micrographs with their dimensions are also summarized in this chapter.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Introduction

This chapter presents the simulation and measured results for $LP^3 - QVCO$ designs. The simulation is carried out by using "Cadence-Spectre *RF*" "Analog Design Environment" tools. The designs are measured in laboratory with the measurement setup discussed in the chapter no. 4. This chapter also includes the measured data plots of the $LP^3 - QVCO$ designs. In this chapter, $LP^3 - QVCO$ design no. 4 measurement and simulation results are shown and discussed in detail. The rest of $LP^3 - QVCO$ results are discussed in Appendix C. The implemented $LP^3 - QVCO$ designs are also compared to existing state of the art work in $QVCOs$.

5.2 LP^3-QVCO Simulation and Measurement Results

This section describes the simulation and measurement results for $LP^3 - QVCO$ designs. The $LP^3 - QVCO$ designs are implemented with on-chip common drain buffers using 0.18 μm and 0.13 μm standard $CMOS$ and $RF\ CMOS$ process technologies. The results are measured at the I/O bond pads. The inductors occupy the major area of the chips. The pn-junction and $pMOS$ varactors are also implemented in the $LP^3 - QVCO$ designs.

The source damping resistance is varied and optimum value is selected. The phase noise and R_{dmp} resistor simulation results are plotted. The 40 Ω R_{dmp} shows better phase noise as compared to other values shown in Fig. 5.1. The quadrature phase error accuracy plot is shown in Fig. 5.2. The simulated phase error is plotted against coupling factor. The optimum value of K is selected and implemented in the $LP^3 - QVCO$ design no. 4.

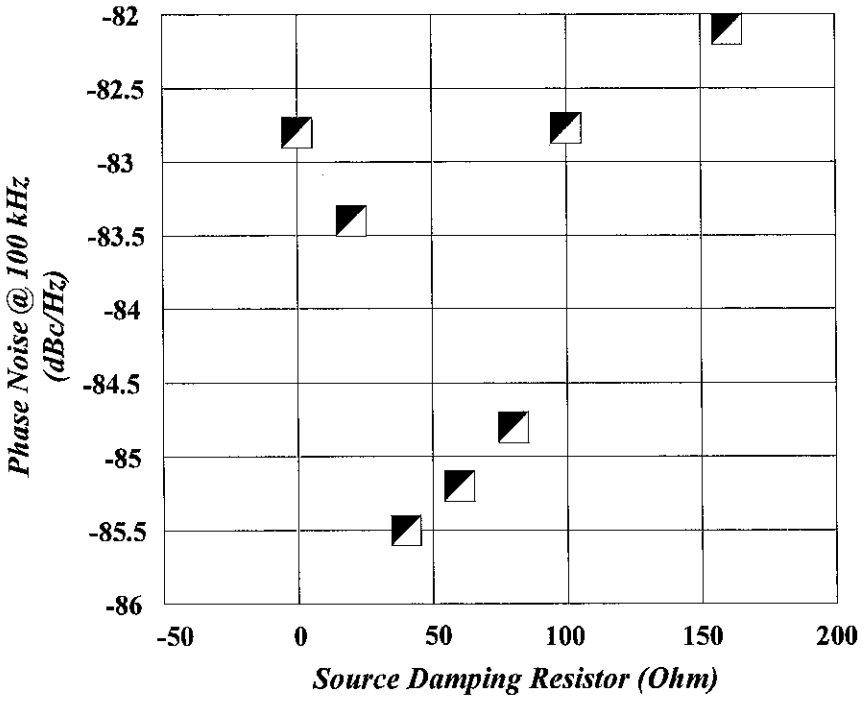


Figure 5.1 Source damping resistor variation against phase noise at the offset frequency of 100 KHz.

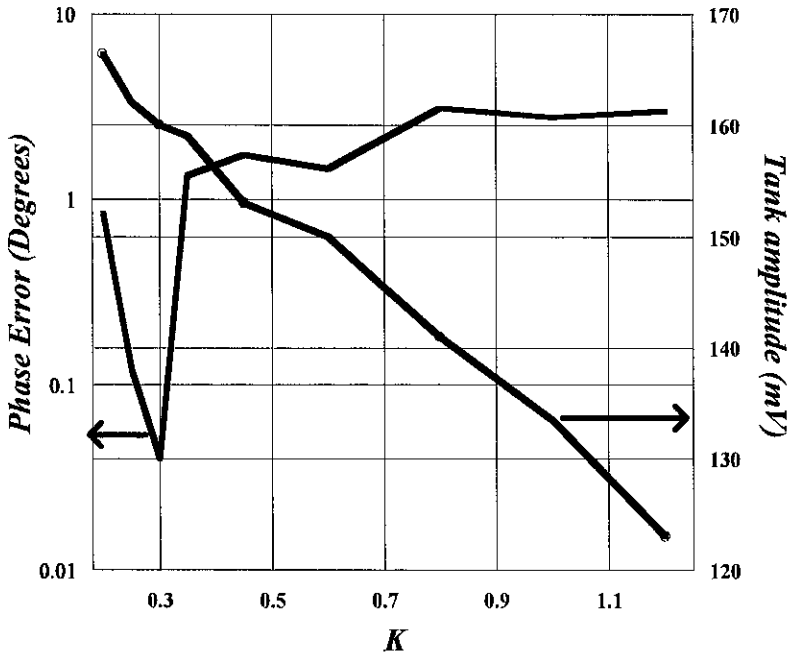


Figure 5.2 Phase error accuracy with coupling factor (K) variations.

The dc analysis, transient analysis and phase noise analysis are carried out for $LP^3 - QVCO$ designs. The transient analysis for $LP^3 - QVCO$ design no. 4 is shown in Fig. 5.3. The transient analysis contains four outputs ($I+$, $I-$) and ($Q+$, $Q-$) signals. Each output waveform exhibits the phase difference of 90° to other waveform. The maximum output voltage V_{p-p} signal is 495 mV. The transient signals are obtained at each output of $LP^3 - QVCO$ buffer. The time period (T) of each sine wave is 208.3 ps. The operating frequency (F) can be calculated by $F = \frac{1}{T}$. The calculated frequency is 4.8 GHz for this design.

The simulation results for $LP^3 - QVCO$ designs are summarized in Table 5.1. This table describes the center frequencies, phase noise, and power dissipation for $LP^3 - QVCO$ designs. The phase noise is measured at the offset frequency of 1 MHz. In Table 5.1, the simulation results for design no. 1 to 3 are the post layout simulation results which are implemented using 0.18 μm $RF\ CMOS$ and $CMOS$ process technology respectively. For the design no. 4 to 7, the results are based on

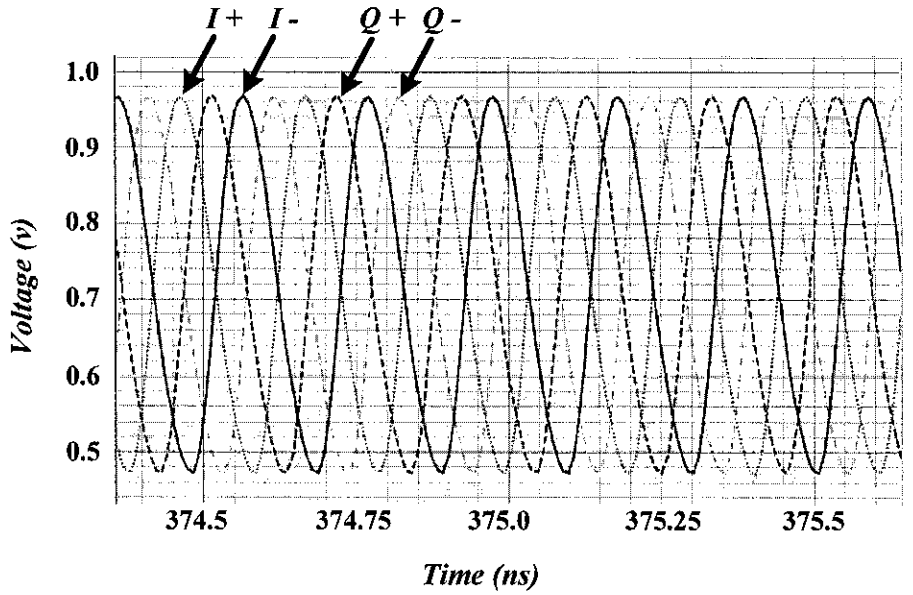


Figure 5.3 Transient analysis of simulated LP^3-QVCO design.

schematic simulations, implemented using 0.13 μm *RF CMOS* process technology. The $LP^3 - QVCO$ design no. 4 measurement results are presented in this section. The remaining $LP^3 - QVCO$ measurement results are shown in appendix C.

The dc bias current of the chip is measured by semiconductor parameter analyzer. The 1.2 V dc voltage is applied at V_{dd} bond pad. The buffer bias voltage of 1.2 V is also applied at the respective bond pads. The total power dissipation for fabricated chip is 10.4 mW. The dc tuning voltage of 0 V to 1.2 V is applied at the respective bond pad and output frequency variation is recorded.

Each output of $LP^3 - QVCO$ exhibits the phase shift of 90°. The phase error is measured using digital oscilloscope and is shown in Fig. 5.4. The phase error is calculated by using Eq. (5.1),

$$\text{Phase Error} = 360° \times f_o \times \Delta \tag{5.1}$$

where f_o is the operating frequency of the oscillator and Δ is the phase shift between

Table 5.1 LP³-QVCO simulation results summary.

Design No	Technology (μm)	Center Frequency f_o (GHz)	Phase Noise @ 1 MHz (dBc/Hz)	Core Power (mW)
1	0.18	3.83	-115.9	6.9
2	0.18	3.84	-115.2	5.2
3	0.18	4.4	-113.6	5.2
4	0.13	4.81	-111.6	2.88
5	0.13	4.81	-110.9	2.88
6	0.13	5.15	-109.3	2.86
7	0.13	5.15	-108.9	2.86

the two corresponding waves. The measured phase error is less than 0.2°.

The output frequency spectrum and RF output power are measured by spectrum analyzer and are shown in the Fig. 5.5. The $LP^3 - QVCO$ exhibits the output frequency of 4.229 GHz at dc tune voltage of 0 V. The $LP^3 - QVCO$ also exhibits output RF power of -15.8 dBm.

The simulated and measured phase noise plots for $LP^3 - QVCO$ are shown in Fig. 5.6. The phase noise plots for conventional simulated $QVCO$, simulated, measured $LP^3 - QVCO$ design no. 4 and measured $LP^3 - QVCO$ design no. 5 are shown clearly in Fig. 5.6. The 3.125 μm finger gate width configuration of $pMOS$ varactor, 40 Ω source damping resistor and tail biasing resistor of 100 Ω are implemented in design no. 4. A $pMOS$ varactor with 8 μm finger gate width configuration, 40 Ω source damping resistor and tail biasing resistor of 100 Ω are implemented in design no. 5. The conventional $QVCO$ contains $pMOS$ varactor with 8 μm gate width configuration and active device based current mirrors. The source damping resistors are removed in conventional $QVCO$. The conventional $QVCO$ and $LP^3 - QVCO$ design no. 4 and 5 dissipate same amount of power.

The phase noise exhibits the slope of $1/f^3$ (30 dB/decade), $1/f^2$ (20 dB/decade) and $1/f$. The averaging is carried out to get the optimized phase noise results from

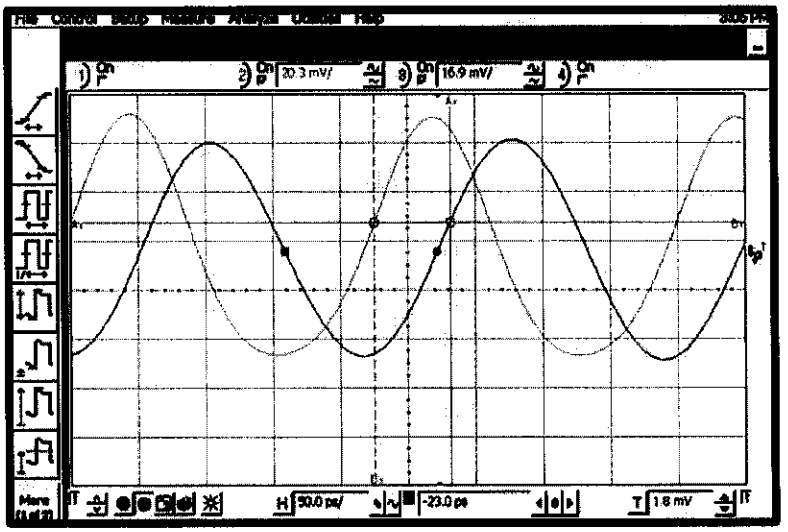


Figure 5.4 Transient output of measured LP^3-QVCO chip.

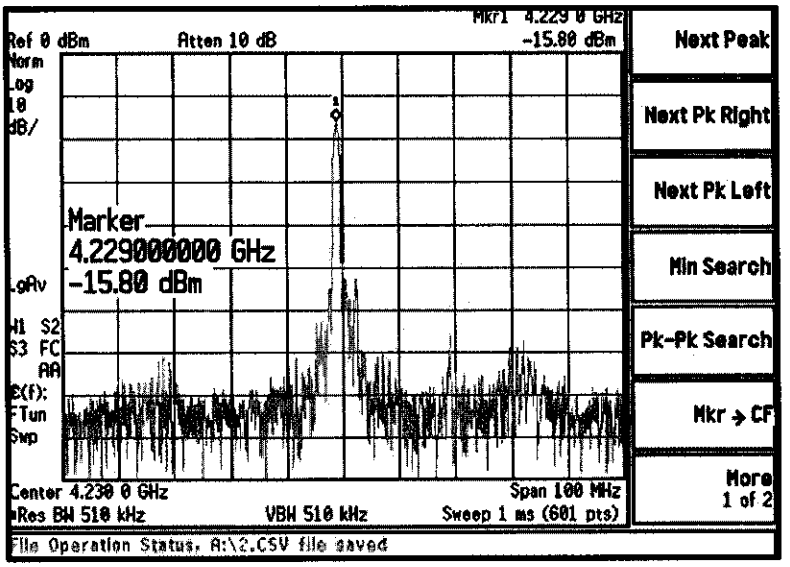


Figure 5.5 Output frequency spectrum of measured LP^3-QVCO chip.

signal source analyzer. Both simulated and measured chips show the significant phase noise improvement at the offset frequencies of 100 KHz, 1 MHz and 3 MHz. The conventional $QVCO$ exhibits the phase noise of -75 dBc/Hz, -104.1 dBc/Hz and -115.1 dBc/Hz at 100 KHz, 1 MHz and 3 MHz offset frequencies, respectively. Next, the measured phase noise for $LP^3 - QVCO$ design no. 5 is presented. The measured $LP^3 - QVCO$ design no. 5 exhibits the phase noise of -72.2 dBc/Hz, -108.5 dBc/Hz and -117.2 dBc/Hz at 100 KHz, 1 MHz and 3 MHz offset frequencies, respectively. The simulated and measured phase noise plots for $LP^3 - QVCO$ design no. 4 are also shown in Fig. 5.6. The simulated phase noise for $LP^3 - QVCO$ design no. 4 is -85.5 dBc/Hz, -112.9 dBc/Hz and -124.5 dBc/Hz at 100 KHz, 1 MHz and 3 MHz offset frequencies, respectively. The measured phase noise for $LP^3 - QVCO$ design no. 4 is -77 dBc/Hz, -110.5 dBc/Hz and -118.0 dBc/Hz at the offset frequencies of 100 KHz, 1 MHz and 3 MHz, respectively. Both $LP^3 - QVCO$ design no. 4 and 5 are similar except gate finger configuration of $pMOS$ varactors. The above discussed phase noise results are summarized in Table 5.2. The measured phase noise for $LP^3 - QVCO$ design no. 4 shows the improvement of 4.5 dB, 1.63 dB and 0.8 dB at the offset frequencies of 100 KHz, 1 MHz and 3 MHz, respectively when compared to the measured $LP^3 - QVCO$ design no. 5. The measured phase noise for $LP^3 - QVCO$ design no. 4 shows the improvement of 2 dB, 6.03 dB and 2.9 dB at the offset frequencies of 100 KHz, 1 MHz and 3 MHz, respectively when compared to the simulated conventional $QVCO$ design. The simulated phase noise for $LP^3 - QVCO$ design no. 4 shows the improvement of 10.5 dB, 8.8 dB and 9.4 dB at the offset frequencies of 100 KHz, 1 MHz and 3 MHz, respectively when compared to the simulated conventional $QVCO$ design.

The $LP^3 - QVCO$ design no. 4 RF output power and tuning sensitivity plot is shown in Fig. 5.7. The frequency tuning range is achieved from 4.21 GHz to 4.44 GHz with the variation of varactor dc tune voltage of 0 V to 1.2 V. The RF output power variation is also shown in Fig. 5.7. The 4.35 GHz center frequency is achieved at 0.6 V dc voltage. The RF output power signal is in the order of -15.8 dBm.

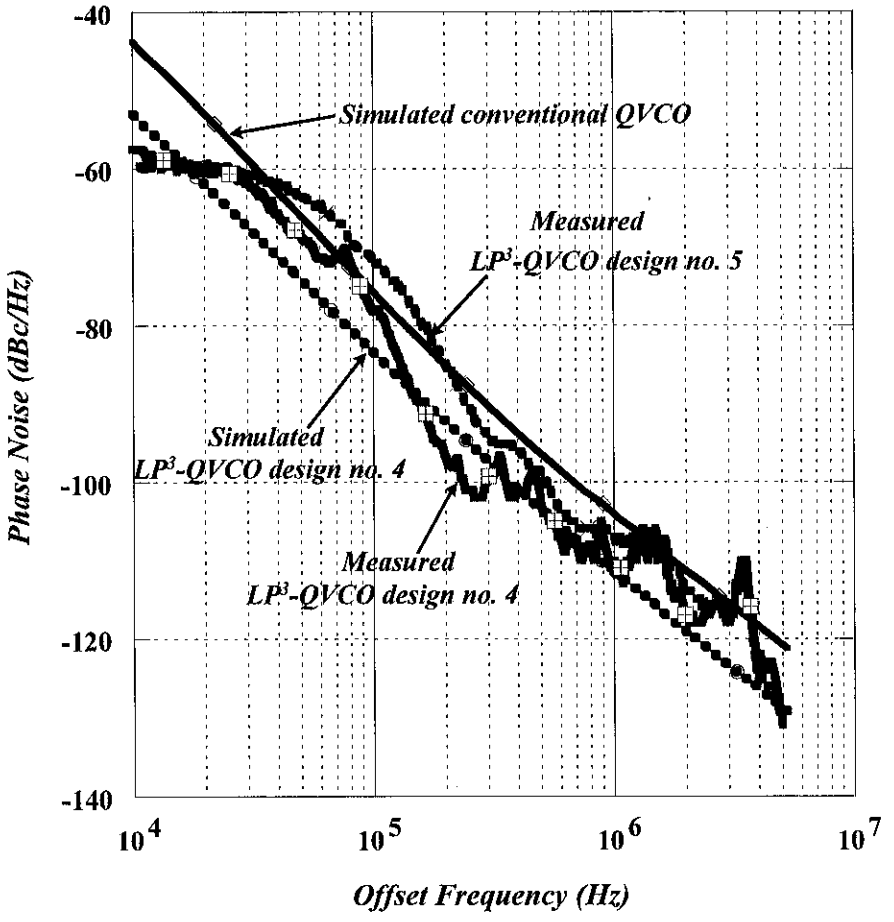


Figure 5.6 Measured phase noise of LP³-QVCO chip.

Table 5.2 LP³-QVCO and conventional QVCO phase noise.

Design	Phase Noise (dBc/Hz)		
No	@ 100 KHz	@ 1 MHz	@ 3 MHz
Simulated Conventional QVCO	-75	-104.1	-115.1
Measured LP³-QVCO design no. 5	-72.5	-108.5	-117.2
Simulated LP³-QVCO design no. 4	-85.5	-112.9	-124.5
Measured LP³-QVCO design no. 4	-77	-110.13	-118

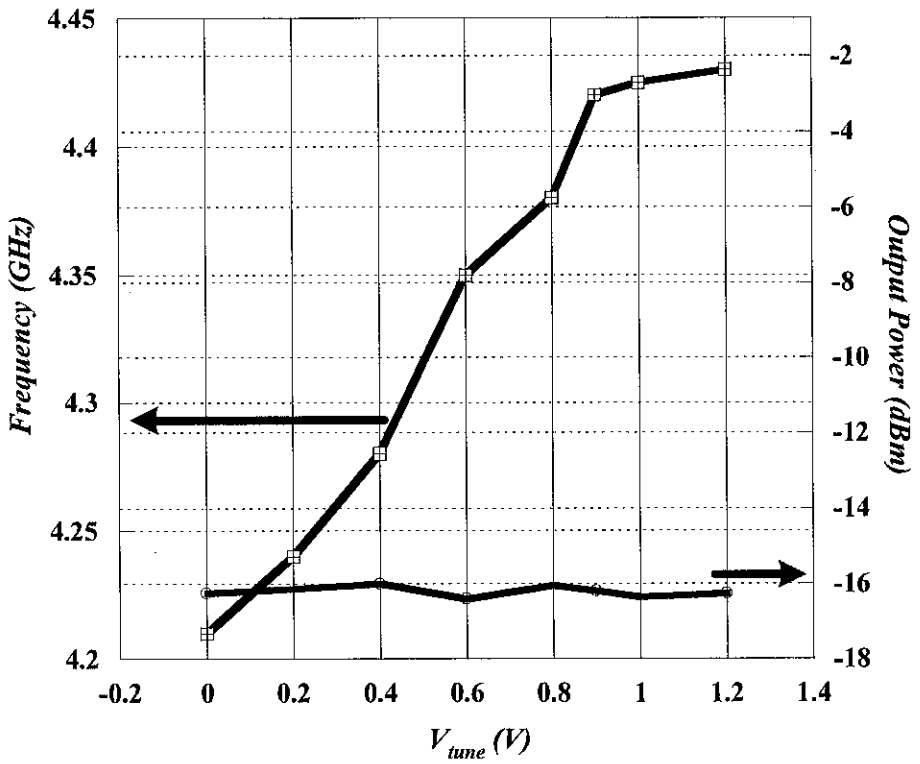


Figure 5.7 Measured frequency tuning range and output power vs varactor dc tune voltage.

The measurement results for $LP^3 - QVCOs$ are summarized in Table 5.3. This table describes the implemented $LP^3 - QVCO$ designs, process technology, frequency sensitivity, RF output power and measured phase noise at offset frequencies of 100 KHz, 1 MHz and 3 MHz, respectively. The frequency sensitivity is calculated with respect to center frequencies. The design no. 2 achieves highest frequency tuning range of 9.03 % implemented using 0.18 μm $CMOS$ process technology. The varactor dc tuning range is 0 V to 1.8 V. The limited frequency tuning range is achieved for the implemented $LP^3 - QVCO$ using 0.13 μm process technology. The maximum frequency tuning range is 6.86 %. The varactor dc tuning range is 0 V to 1.2 V. The FOM is also compared to frequency tuning sensitivity as shown in Fig. 5.8. This shows the FOM $LP^3 - QVCO$ design no. 1 to 7 excluding design no. 3[1]. The $LP^3 - QVCO$ design no. 6 exhibits the highest calculated FOM of -187 dBc/Hz at 1 MHz offset frequency. The frequency sensitivity for the design no. 6 is 6.9 %. The lowest FOM of -165 dBc/Hz is achieved in design no. 1. The maximum frequency sensitivity for design no. 2 is 9.01 % and FOM is -177.5 dBc/Hz at the offset frequency of 1 MHz.

5.3 LP^3-QVCO Results Discussion

In this section, the simulation and measured results for $LP^3 - QVCO$ are discussed. The $LP^3 - QVCO$ simulation and measured results show some discrepancies in the results. However, these differences can be possibly due to following reasons.

The design no. 1, 2 and 3 contain the circular spiral inductors in the LC-tanks. The two inductors are configured in parallel combination to achieve the 1.13 nH inductance value. In the layout designs, the higher metals are not used for the interconnection of components. Metal 1 to metal 3 are used at the output terminals which result in the increased parasitic capacitances. The pn-junction varactors are used without guard rings. The guard rings help to prevent the variation of the capac-

[1]The design no. 3 operates at fixed frequency, the frequency tuning range cannot be achieved as discussed in Chapter 3.

Table 5.3 LP³-QVCO measurement results.

Design No	Process (μm)	Frequency Sensitivity	*RF* Output Power (dBm)	Phase Noise (dBc/Hz) @ 100 KHz	@ 1 MHz	@ 3 MHz
1	0.18	7.51 %	-26.69	-72.71	-104.62	-115.62
2	0.18	9.03 %	-28.65	-70.35	-114.91	-119.71
3	0.18	-	-18.89	-68.5	-115.09	-127.8
4	0.13	5.28 %	-16.1	-78.3	-110.13	-116.87
5	0.13	4.82 %	-17.36	-78.3	-108.54	-117.25
6	0.13	6.86 %	-16.75	-69.41	-118.24	-130.21
7	0.13	6.07 %	-17.72	-68.7	-107.62	-122.3

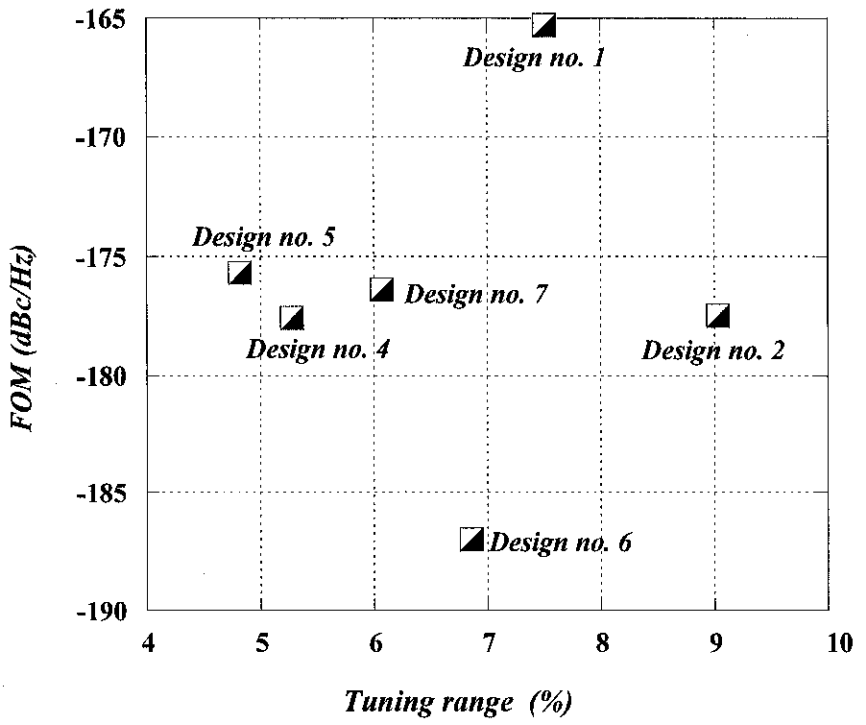


Figure 5.8 Measured FOM against frequency tuning range.

itance value [108]. The total capacitance for design no. 2 is 2.2 pF. The capacitance at each output for $LP^3 - QVCO$ node can be calculated by Eq. (5.2),

$$C_{total} = C_{devices} + C_{inductor} + C_{buffer} + C_{parasitics} \tag{5.2}$$

where $C_{devices}$ is the parasitic capacitance of each transistor in cross-coupled pair, $C_{inductor}$ is the parasitic capacitance of the inductor model, C_{buffer} is the input buffer capacitance and $C_{parasitics}$ represents any additional layout parasitics [109].

The $C_{inductor}$ is 464 fF as four inductors are used in LC-tank of $QVCO$. The C_{buffer} is approximately 100 fF. The other layout parasitic capacitances are 100 fF. The rest of capacitance belongs to the device. The oscillation frequency of 3.1 GHz is achieved with the capacitance of 2.2 pF. The design no. 3 operates at the center frequency of 3.8 GHz. The 630 fF varactor capacitor is removed in design no. 3. In design no. 1, the layout design is carried out with metal 1, 2 and 3. The use of lower metals result in the increase of parasitic capacitance value. Hence, the circuit operates at 2.8 GHz.

The dummy resistor layout structure configuration is to be used to avoid the resistance variation. The layout for $LP^3 - QVCO$ circuit should be as symmetrical as possible, and care must be taken while designing the layout. All of these factors will influence the performance of the $LP^3 - QVCO$ circuits. Hence, the desired oscillation frequency is not achieved as in post layout simulation results. The layout design for $LP^3 - QVCO$ should be symmetrical, second center tapped inductor (CTI) should be used to avoid the inductance variation. The mutual inductance effects should be taken into consideration.

The schematic simulation results for design no. 4 to 7 are also summarized in Table 5.1. The center tapped inductor (CTI) (symmetrical spiral inductor) is extracted using $ASITIC$. Second, the layout design for each component is drawn symmetrically. The layout design for transistors are carefully designed with proper guard rings. The fabricated design no. 4 and 5 operate at the center frequency of 4.35 GHz. The

parasitic capacitances influence the oscillation frequency. The output frequency for design no. 6 and 7 is same when compared to the simulation results for LP^3-QVCO. The $pMOS$ varactors are used in the design no. 4 to 7. The layout of LP^3-QVCO design no. 6 and 7 is different from design no. 4 and 5. In design no. 6 and 7, the symmetrical spiral inductors with PGS are used in the middle of the layouts. The simulated and measured results show symmetry in the operating frequency for LP^3-QVCO design no. 6 and 7.

5.4 LP^3-QVCO Results Comparison

Fig. 5.9 shows the measured phase noise at 1 MHz offset frequency and power dissipation for LP^3-QVCO designs compared to state of the art work. The low power and low phase noise are achieved in LP^3-QVCO design no. 6. The low phase error LP^3-QVCO design no. 4 is compared to the state of the art work [48], [51], [53], [54], [86], [88], [103], [110] and [111].

The phase error comparison to the operating frequency of the $QVCO$ is shown in Fig. 5.10. The low phase error is achieved by [53] and [88] and the operating frequency is in the order of 2.4 GHz. In this work, the LP^3-QVCO design no. 4 exhibits the quadrature phase error of 0.2° with center frequency of 4.35 GHz. The center frequency is high as compared to [53] and [88]. The LP^3-QVCO results are compared to state of the art $QVCO$ works and are summarized in Table 5.4. The center frequencies (f_o), core power dissipation, phase noise and calculated figure of merit (FOM) are compared to state of the art $QVCOs$. The low power dissipation, comparable phase noise and FOM are achieved in design no. 1 to design no. 7. The LP^3-QVCO design no. 2 and 3 exhibit the measured phase noise of -114.9 dBc/Hz and -115.1 dBc/Hz at the offset frequency of 1 MHz, respectively. The calculated FOM for LP^3-QVCO design no. 2 and 3 are -177.5 dBc/Hz and -179.5 dBc/Hz, respectively. The LP^3-QVCO design no. 4 and 5 exhibit the measured phase noise of -110.13 dBc/Hz and -108.5 dBc/Hz at the offset frequency of 1 MHz, respectively. The calculated FOM for LP^3-QVCO design no. 4 and 5 is -177.6 dBc/Hz and

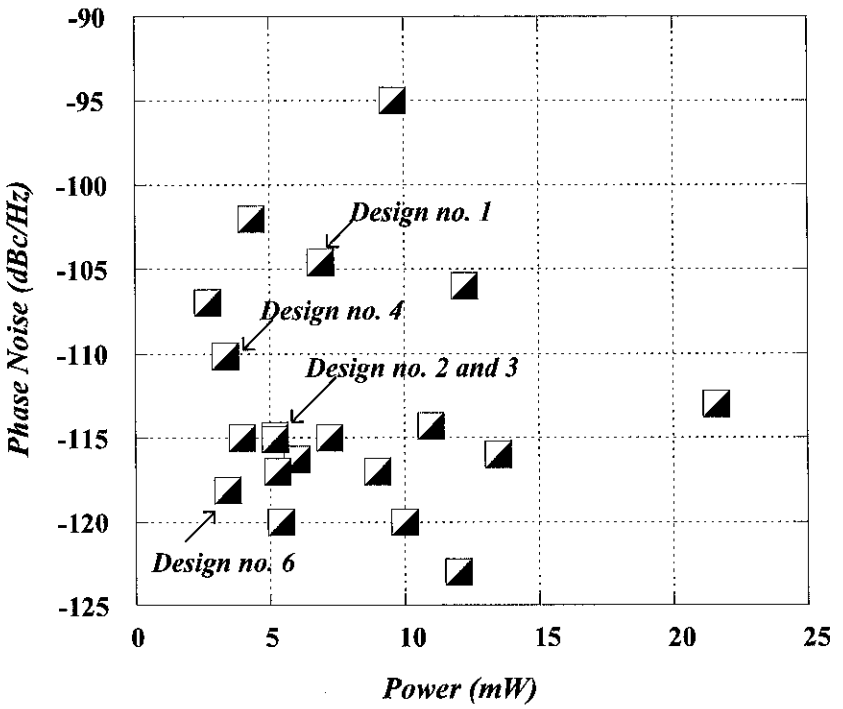


Figure 5.9 LP^3-QVCO phase noise comparison to state of the art work.

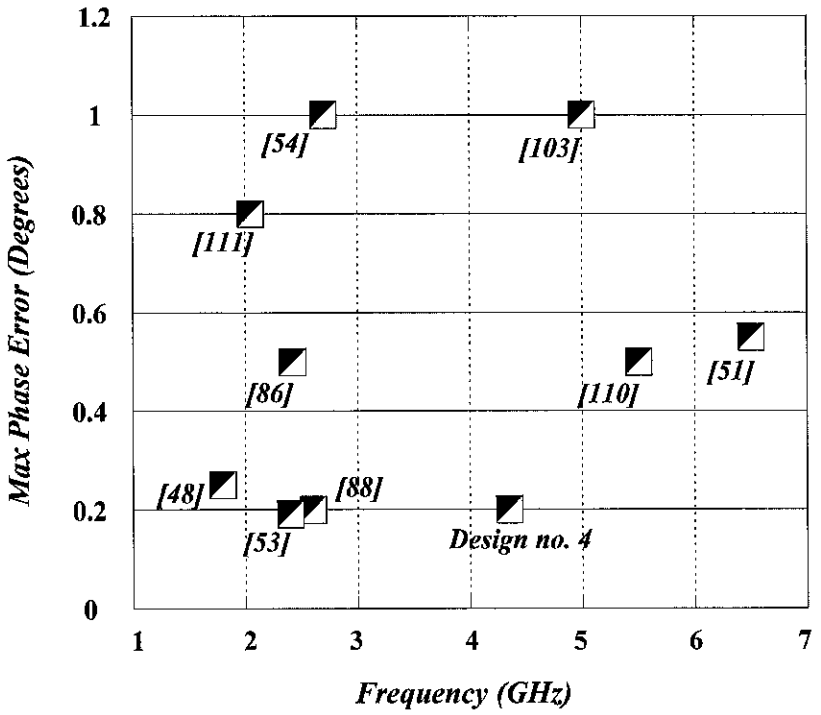


Figure 5.10 LP^3-QVCO phase error comparison to state of the art work.

-175.7 dBc/Hz, respectively. The $LP^3 - QVCO$ design no. 6 exhibits the highest calculated FOM of -187.0 dBc/Hz and phase noise of -118.1 dBc/Hz at the offset frequency of 1 MHz.

The measurement results for design no. 1 to design no. 7 are shown in appendix C. The phase noise results and RF output frequency spectrum for design no. 1 to design no. 7 are shown. The appendix C also contains the transient analysis and frequency tuning range of $LP^3 - QVCO$ designs.

5.5 Summary

This chapter describes the simulation and measurement results for seven $LP^3 - QVCOs$ designed in this thesis work. The results include measured phase noise, frequency spectrum, RF output power, transient analysis, dc current and frequency sensitivity. The phase noise for $LP^3 - QVCO$ design no. 4 is compared to design

Table 5.4 LP^3-QVCO measurement results comparison to state of the art work.

Ref No	Technology (μm)	Frequency $f_\circ$ (GHz)	Core Power (mW)	Phase Noise @ 1 MHz (dBc/Hz)	FOM (dBc/Hz)
[72]	0.18	4.12~4.89	8.6	-115.06	-180.5
[73]	0.18	1.73~2.94	15	-112	-169.6
[73]	0.18	4.13~4.89	15	-101	-163.0
[83]	0.13	3.9	9	-117	-180
[89]	0.18	4.8	12.6	-120	-182.5
[90]	0.18	2.45	7.2	-115	-178
[112]	0.18	4.8	14.4	-127.5 @ 3MHz	-180.2
[113]	0.18	4.2	6	-116.3	-181
[114]	0.18	4.5	3.96	-115	-182.2
[115]	0.13	5.5	5.28	-117	-184.6
[116]	0.25	0.25	5	-124	-184.6
Design 1	0.18	2.81	6.9	-104.6	-165.3
Design 2	0.18	3.15	5.2	-114.9	-177.5
Design 3	0.18	3.8	5.2	-115.1	-179.5
Design 4	0.13	4.35	3.36	-110.13	-177.6
Design 5	0.13	4.35	3.36	-108.5	-175.7
Design 6	0.13	5.1	3.42	-118.1	-187.0
Design 7	0.13	5.1	3.42	-107.6	-176.4

no. 5 and conventional $QVCO$. The $LP^3 - QVCO$ designs are implemented using 0.18 μm and 0.13 μm, $CMOS$ and $RF\ CMOS$ process technologies, respectively. The measured phase noise for $LP^3 - QVCO$ design no. 4 shows an improvement of 4.8 dB, 1.63 dB and 0.8 dB at the offset frequencies of 100 KHz, 1 MHz and 3 MHz, respectively when compared to measured $LP^3 - QVCO$ design no. 5. The measured phase error is less than 0.2°. In the results discussion, the possible justification of the results is also explained. The $LP^3 - QVCO\ FOM$ is also compared to the frequency sensitivity. The $LP^3 - QVCO$ results are also compared to the state of the art quadrature voltage controlled oscillators. The lowest phase error achieved for $LP^3 - QVCO$ design no. 4 is also compared to the state of the art $QVCOs$. The $LP^3 - QVCO$ design no. 6 exhibits the highest measured phase noise of -118.1 dBc/Hz and FOM of -187 at the offset frequency of 1 MHz.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Introduction

The quadrature oscillator circuit plays an important role in the performance of the RF radio transceivers. The quadrature signal accuracy, low phase noise and low power are key performance factors for the design of $QVCO$ circuits. In this thesis work, the design evolution and optimizations for $LP^3 - QVCOs$ are presented. This chapter summarizes the design and outcome of $LP^3 - QVCO$ designs for the wireless applications.

6.2 Conclusion

In this work, the low power, low phase noise and low phase error $LP^3 - QVCO$ designs are described. The $LP^3 - QVCO$ designs are implemented for wireless applications. The proposed $LP^3 - QVCO$ implementation is carried out using 0.13 μm, $RF\ CMOS$ with 8 metal and 1 poly layer. The remaining implementations are carried out using 0.18 μm standard $CMOS$ and $RF\ CMOS$ process technology with 6 metal and 1 poly layer. The $LP^3 - QVCO$ provides the low cost and fully integrated single chip solution.

Different $QVCO$ design structures are studied and parallel coupled fully differential $LP^3 - VCOs$ are suitable candidate for the $LP^3 - QVCO$ architectures in this work. The coupling transistors also play an important role in the accuracy of the phase error as well as phase noise of the circuit. The proper coupling transistor ratio is chosen which provides better compromise between quadrature accuracy and phase noise. The resonator Q factor and oscillator output amplitude also influence the performance of the $LP^3 - QVCO$. The symmetrical layout design for $LP^3 - QVCO$ is

another challenge in circuit implementation. The proper design approach has been adopted and suggested in this work.

The $LP^3 - QVCOs$ are designed with tail biasing resistor (R_{tail}) instead of active device based current biasing circuitry. The source damping resistor (R_{damp}) is also used to achieve low $1/f$ noise. The multifinger gate structure of the MOS device and $pMOS$ varactors are used in this design.

The $LP^3 - QVCO$ design no. 4 uses the (R_{damp}) resistor of 40 Ω, (R_{tail}) of 102 Ω and multifinger gate width configuration of 3.125 μm $\times$ 64 = 200 μm. This $LP^3 - QVCO$ exhibits the measured phase noise of -110.13 dBc/Hz at the offset frequency of 1 MHz. The calculated figure of merit is -177.6 dBc/Hz. The measured phase error is less than 0.2°. The core power dissipation for $LP^3 - QVCO$ design is 3.36 mW from 1.2 V dc power supply. The $pMOS$ varactors and symmetrical spiral inductors are used in LC-tanks of $LP^3 - QVCO$. The $LP^3 - QVCO$ exhibits the measured frequency tuning range of 4.21 GHz to 4.44 GHz (230 MHz) with the variation of 0 V to 1.2 V dc control voltage of varactors. The 1.12 nH symmetrical spiral inductor with PGS is used with the quality factor of 18.6. The center frequency for $LP^3 - QVCO$ is 4.35 GHz with maximum supply voltage of 1.2 V. The $LP^3 - QVCO$ design no. 6 exhibits the measured phase noise of -118.1 dBc/Hz at the offset frequency of 1 MHz and calculated FOM is -187.1 dBc/Hz.

The remaining $LP^3 - QVCO$ designs (1, 2, 3, 5, 6 and 7) are also implemented and measured. The $LP^3 - QVCO$ design no. 4, 5, 6 and 7 are implemented using $pMOS$ varactors and symmetrical spiral inductors. The $LP^3 - QVCO$ design no. 4, 5, 6 and 7 are implemented using 0.13 μm $RF\ CMOS$ process technology. The pn-junction varactors are also used in $LP^3 - QVCO$ design no. 1, 2 and 3. $LP^3 - QVCO$ design no. 1, 2 and 3 contain the circular spiral inductors and implementations are carried out using 0.18 μm $CMOS$ and $RF\ CMOS$ process technology. The $LP^3 - QVCOs$ are designed, implemented and measured. A significant improvement in the phase noise and phase errors have been reported. The proper care must be taken into consideration while designing the symmetrical layout for $LP^3 - QVCO$ structures.

The parasitics of the layout design have proven to optimum phase accuracy and better phase noise.

6.3 Future Work

The most interesting and important thing is to complete the Ph.D studies. The research is the endless ocean one can never ever completely gain all knowledge in the research. There are many areas which still need attention and further research. There are many research areas in the field of $RFIC$ design.

There are many building blocks of RF wireless transceivers such as LNA, mixer, PLL, frequency dividers and power amplifiers. An enhanced investigations are required to achieve better performance parameters and improved architectures for these building blocks. In todays communication system, oscillators are one of the key building blocks in realizing a single-chip radio. Advanced $RF\ CMOS$ technology has been implemented to solve various problems related to the conductive substrate and operation speed of active devices. The inherent 1/f noise is still a bottleneck to the design of integrated low phase noise oscillators. Fully integrated $VCOs$ and $QVCOs$ are one of the major bottleneck in $RFIC$ design wireless transceivers. The $CMOS$ processes are attractive due to the highest integration level achievement and cost effective solution.

The wide tuning range, low phase noise achievement and low phase error are key parameters which influence the overall performance of wireless transceiver system. However, unfortunately still we have to compromise at optimum phase noise and wide tuning range of the circuit. The inductor and varactors are also one of the major blocks in the VCO and $QVCO$ design. The Q factor of the on-chip inductor is limited and influences the performance of the oscillator system. The center tapped inductors (CTI) are potential candidates for fully integrated on-chip $VCOs$ and $QVCOs$. There are various types of the varactors such as pn-junction diodes and MOS varactors. This also motivates that the research should be carried out in the area of the passive devices. $RF - MEMS$ may also provide better solution for the

existing on-chip passive components. The oscillator phase noise is also limited due to power supply reduction as technology scales down in $CMOS$ process. The parasitic capacitance are also increased due to technology scales down. The frequency tuning range of VCO and $QVCO$ is limited due to the limitations of dc power supply. Therefore, the only way to get better phase noise results is to achieve better Q factor of the device. The process variations in temperature and power supply should also be considered for the fabrication of the circuits. In oscillator circuits, the use of $MEMS$ resonator structure, achievement of wide frequency tuning range and high Q factor of resonator circuit are the areas for future exploration.

REFERENCES

[1] B. Razavi, *RF Microelctronics* (Prentice Hall, London, UK, 1999).

[2] T. H. Ning, "Silicon Technology Directions in the New Millennium," In *IEEE 38th Annual International Reliability Physics Symposium*, **13,** 1–6 (San Jose, CA, USA, 2000).

[3] A. E. Husscin and M. I. Elmasry, "A Fractional-N Frequency Synthesizer For Wireless Communications," In *IEEE International Symposium on Circuits and Systems*, **4,** IV–513–IV–516 (2002).

[4] S. J. Yun, C. Y. Cha, H. C. Choi, and S. G. Lee, "RF CMOS LC-Oscillator With Source Damping Resistors," In *IEEE International Solid-State Circuits Conference*, **16,** 511–513 (2006).

[5] A. Abidi and P. Andreani, "CMOS Wireless Transceivers: The New Wave," IEEE Communication Magazine **37,** 119–124 (1999).

[6] A. J. Joseph *et al.*, "Product Applications and Technology Directions With SiGe BiCMOS," IEEE Journal of Solid State Circuits **38,** 1471–1478 (2003).

[7] B. U. H. Klepser and J. Kucera, "A Fully Integrated SiGe Bipolar 2.4 GHz Bluetooth Voltage Controlled Oscillator," In *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 61–64 (Infineon Technologies, Munich, Germany, 2000).

[8] S. Zafar, *Design of a Low Phase Noise Voltage Controlled Oscillator with On-Chip vs Off-Chip Passive Components* (Masters Dissertation submitted to the faculty of Royal Institute of Technology, Stockholm,Sweden, 2003), No. IMIT/LECS/2003-04.

[9] S. Malevsky and J. R. Long, "CMOS Receiver Frontends for mm-Wave Short Range Gigabit Communication," http://domino.watson.ibm.com/acas/w3www_acas.nsf/images/projects_03.04/$FILE/kornegay.pdf pp. 55–59 (Accessed at June, 2009).

[10] J. J. Kucera, "Wideband BiCMOS VCO for GSM/UMTS Direct Conversion Receivers," IEEE International Solid-State Circuits Conference, Digest of Technical Papers pp. 374–375 (2001).

[11] W. A. Wieder and F. Neppl, "CMOS Technology Trends and Economics," In *Micro, IEEE*, **12**, 10–19 (Munich, Germany, 1992).

[12] B. Razavi, *Design of Integrated Circuits for the Optical Communications*, 1st ed. (McGraw-Hill, New York, USA, 2003).

[13] K. H. D-Mcnaught and E. D. Fague, "Performance evaluation of a single chip radio transceiver," In *IEEE 46th Vehicular Technology Conference, Mobile Technology for the Human Race*, **2**, 1048–1051 (Atlanta, GA, 1996).

[14] Z. Pala and N. Inanc, "Smart Parking Applications Using RFID Technology," In *RFID Eurasia, 2007 1st Annual*, **2**, 1048–1051 (Istanbul, 2007).

[15] T. E. V. der Velde, E. D. Atsma, R. Hoekema, E. J. Luijten, I. C. Buddelmeijer, J. H. Spruijt, and J. J. H. N. V. der Putten, "A Multicentre PDA Project to Support the Clinical Decision Process," In *Computers in Cardiology*, pp. 177–179 (Netherlands, 2007).

[16] P. Wambacq, S. Donnay, H. Zaid, M. Engles, H. D. Man, and I. Bolsens, "A Single-Package Solution for Wireless Transceivers," In *Design, Automation and Test in Europe Conference and Exhibition. Proceedings*, pp. 425–429 (Munich, Germany, 1999).

[17] M. Dobers, M. Seyffert, D. F. Hauschild, and P. C. Czaya, "Low Cost Multi Chip Modules," In *Proceedings of Sixteenth IEEE/CPMT International Electronics*

Manufacturing Technology Symposium, Low-Cost Manufacturing Technologies for Tomorrow's Global Economy, **1**, 340–343 (La Jolla, CA, 1994).

[18] H. C. Luong and G. C. T. Leung, *Low-Voltage CMOS RF Frequency Synthesizers* (Cambridge University Press, Cambridge, UK, 2004).

[19] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits **33,** 179–194 (1998).

[20] M. Tiebout, *Low Power VCO Design in CMOS* (Springer, 2006).

[21] A. Ravi, K. Soumyanath, R. E. Bishop, B. A. Blocechel, and L. R. Carley, "An optimally transformer coupled, 5 GHz Quadrature VCO in a 0.18 μm digital CMOS process," In *IEEE VLSI Circuits Symposium*, **2,** 141– 144 (2003).

[22] A. Hajimiri and T. H. Lee, "Corrections to: A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits **33,** 928 (1998).

[23] P. Andreani and S. Mattison, "On the Use of MOS Varactors in RF VCOs," IEEE Journal of Solid-State Circuit **35,** 905–910 (2000).

[24] L. E. Larson, "Silicon Technology Tradeoffs for Radio-Frequency/Mixed-Signal System-on-a-Chip," IEEE Transactions on Electron Devices **50,** 683–699 (2003).

[25] A. Abidi, "Direct Conversion Radio Transceivers for Digital Communications," IEEE Journal of Solid-State Circuits **30,** 1399–1409 (1995).

[26] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8-dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz for GPS Receiver," IEEE Journal of Solid-State Circuits **37,** 760–765 (2002).

[27] S. I. Ahmed and R. D. Mason, "Improving the Acquisition Time of a PLL-based, Integer-N Frequency Synthesizer," In *Proceedings of International Symposium on Circuits and Systems, (ISCAS)*, **4,** 365–368 (2004).

[28] S. Cheng, K. Zhang, W. Lu, Y. Liu, S. Cao, X. Zhou, and D. Zhou, "A 2.4 GHz Spur-Cancelled Fractional-N Frequency Synthesizer with PFD/DAC Structure for WSN Application," In *7th International Conference on ASIC, (ASICON)*, pp. 696–699 (2007).

[29] M. Gupta and B. S. Song, "A 1.8 GHz Spur-Cancelled Fractional-N Frequency Synthesizer With LMS-Based DAC Gain Calibration," IEEE Journal of Solid-State Circuit **41**, 2842–2851 (2006).

[30] T. Musch and B. Schiek, "Measurement of the Ramp Linearity of Extremely Linear Frequency Ramps Using a Fractional Dual Loop Structure," IEEE Journal of Solid-State Circuit **50**, 389–392 (2001).

[31] H. Zhang and G. Chen, "A Monolithic Fast-Hopping Frequency Synthesizer for MB-OFDM UWB," In *Asia-Pacific Microwave Conference (APMC)*, **2**, 4–7 (2005).

[32] B. Razavi, *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, New York, US, 2001).

[33] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits* (John Wiley and Sons, Inc, New York, US, 2001).

[34] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge University Press, New York, US, 1998).

[35] A. M. Niknejad and R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF ICs," IEEE Journal of Solid-State Circuits **33**, 1470–1481 (2003).

[36] L. V. Belini and A. M. Romero, "Design of Active Inductors using CMOS Technology," In *15th Symposium on Integrated Circuits and Systems Design*, **2**, 296–301 (2002).

[37] E. C. Park, Y. S. Choi, J. B. Yoon, S. Hong, and E. Yoon, "Fully Integrated Low Phase-Noise VCOs with On-Chip MEMS Inductors," IEEE Transactions on Microwave Theory and Techniques **51,** 289–296 (2003).

[38] G. P. T. Mayuga and M. D. Rosales, "Inductor Modeling Using 3D EM Design Tool for RF CMOS Process," In *Proceedings of Progress In Electromagnetics Research Symposium,* pp. 216–221 (The Electromagnetics Academy, Cambridge, USA, 2008).

[39] *Agilent Technologies* (Santa Clara, CA, USA, 2007).

[40] D. T. S. Cheung, J. R. Long, and R. A. Hadaway, "Monolithic Transformers for Silicon RFIC Design," In *IEEE Bipolar/BiCMOS Circuits and Technology Meeting,* pp. 105–108 (1998).

[41] P. Andreani, "A Comparison Between two 1.8 GHz CMOS VCOs Tuned by Different Varactors," In *IEEE 24th European Conference on Solid-State Circuits,* **35,** 380–383 (1998).

[42] D. Ham and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," IEEE Journal of Solid-State Circuits **36,** 896–909 (2001).

[43] N. M. Nguyen and R. G. Meyer, "Start-up and Frequency Stability in High-Frequency Oscillators," IEEE Journal of Solid-State Circuits 27 (1992).

[44] D. Ham and A. Hajimiri, "Virtual Damping In Oscillators," In *CICC,* (2002).

[45] A. Hajimiri and T. Lee, "Design Issues in CMOS Differential LC Oscillators," IEEE Journal of Solid-State Circuits **34,** 717–724 (1999).

[46] A. Fard, T. Johnson, M. Linder, and D. Aberg, "A Comparative Study of CMOS LC VCO Topologies for Wide-Band Multi-Standard Transceivers," In *IEEE 47th Midwest Symposium on Circuits and Systems,* **3,** 17–20 (2004).

[47] H. Ramiah and T. Z. A. Zulkifli, "Design of 3-4 GHz Tunable Low Noise LC QVCO for IEEE 802.11a WLAN Application," In *IEEE Asia Pacific Conference on Circuits and Systems (APPCAS)*, **3,** 507–510 (2006).

[48] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and Design of a 1.8 GHz CMOS LC Quadrature VCO," IEEE Journal of Solid-State Circuits **37,** 1737–1747 (2002).

[49] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," In *43rd International Solid-State Circuits (ISSC) Conference Digest of Technical Papers*, pp. 392–393 (1996).

[50] I. R. Chamas and S. Raman, "A Comprehensive Analysis of Quadrature Signal Synthesis in Cross-Coupled RF VCOs," IEEE Transactions on Ciruits and System **54,** 689–704 (2007).

[51] M. Chu and D. J. Allstot, "A 6 GHz low-noise quadrature Colpitts VCO," In *Proceedings of IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 21–24 (Washington, Seattle, 2004).

[52] H. Ramiah and T. Z. A. Zulkifli, "Design of Low Noise SIPC LC-QVCO for IEEE 802.11a Application in 0.18 μm CMOS Technology," International Journal of Electronics, Circuits and Systems **1,** 48–53 (2007).

[53] H. Gao, Z. Q. Lu, and F. C. Lai, "Design of Low-Phase-Noise Low-Phase-Error CMOS Quadrature VCO," In *Proceedings of International Conference on Microwave and Millimeter Wave Technology*, pp. 1–4 (China, 2007).

[54] S. Byun, K. W. Kim, D. H. Lee, J. Laskar, and C. S. Kim, "A Self-Calibrated LC Quadrature VCO in a Current-Limited Region," In *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 379–382 (2008).

[55] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," IEEE Journal of Solid-State Circuits **31,** 331–343 (2001).

[56] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a Tutorial," IEEE Journal of Solid-State Circuits **35,** 326–336 (2000).

[57] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," IEEE Proc. Letters **54,** 329–330 (1966).

[58] J. J. Rael and A. A. Abidi, "Physical Processes of Phase Noise in Differential LC Oscillators," in IEEE Custom Integrated Circuit Conference (2000).

[59] E. Hegazi, H. Sjoland, and A. Abidi, "A Filtering Technique to Lower Oscillator Phase Noise," In *IEEE Solid-State Circuits Conference,* pp. 364–365 (2001).

[60] C. Samori, A. L. Lacaita, A. Zanchi, S. Levantino, and F. Torrisi, "Frequency Dependence on Bias Current in 5 GHz CMOS VCOs," In *IEEE Solid-State Circuits Conference,* pp. 202–205 (1999).

[61] S. Levantino, C. Samori, A. Bofanti, S. L. J. Gierkink, A. L. Lacaita, and V. Boccuzzi, "Impact of Indirect Stability on Phase Noise Performance of Fully-Integrated LC Tuned VCOs: Impact on Tuning Range and Flicker Noise Up-conversion," In *IEEE European Solid-State Circuits Conference,* **37,** 1003–1011 (2002).

[62] S. Gagliolo, G. Pruzzo, and D. D. Caviglia, "Phase Noise Performance of a Cross-Coupled CMOS VCO with Resistor Tail Basing," In *SBCCI,* **37,** 1003–1011 (2005).

[63] C. C. Ho, G. H. Liang, C. Huang, Y. J. Chan, C. S. Chang, and C. P. Chao, "VCO Phase Noise Improvement by Gatefinger Configuration of 0.13 μm CMOS Transistors," IEEE Electron Device Letters **26,** 258–260 (2005).

[64] C. Y. Cha, H. C. Choi, H. T. Kim, and S. G. Lee, "RF CMOS Differential Oscillator With Source Damping Resistors," In *IEEE Radio Frequency Integrated Circuits Symposium,* **37,** 399–402 (2005).

[65] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators* (Kluwer Academic Publishers, Boston/Dorrdrecht/London, 1999).

[66] P. Kinget, *Integrated GHz Voltage Controlled Oscillators* (Kluwer Publish, Norwell, 1999).

[67] M. A. Do, R. Y. Zhao, K. S. Yeo, and J. G. Ma, "New Wideband/Dualband CMOS LC Voltage-Controlled Oscillator," In *IEE Proceedings Circuits, Devices and Systems*, **150,** 453–459 (2003).

[68] W. Y. Chung and Y. Y. Chi, "A 0.8 V 5.9 GHz Wide Tuning Range CMOS VCO Using Inversion-Mode Bandswitching Varactors," In *IEEE International Symposium on Circuits and Systems, (ISCAS)*, **5,** 5079 – 5082 (2005).

[69] X. Chao, W. Sargeant, K. Laker, and J. V. der Spiegel, "An Extended Frequency Range CMOS Voltage-Controlled Oscillator," In *9th International Conference on Electronics, Circuits and Systems*, **2,** 425–428 (2002).

[70] W. C. Chien, C. C. Hsien, and F. S. Wu, "An Ultra-Wideband CMOS VCO With 3-5 GHz Tuning Range," In *IEEE International Workshop on Radio-Frequency Integration Technology: Integrated Circuits for Wideband Communication and Wireless Sensor Networks*, pp. 87–90 (2005).

[71] Y. Yoshihara, H. Sugawara, H. Ito, K. Okada, and K. Masu, "A Wide Tuning Range CMOS VCO Using Variable Inductor," In *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 278–281 (2004).

[72] C. H. Kim, S. H. Shin, and H. J. Yoo, "A Low Phase Noise and Low Power Series Coupled Quadrature VCO Using Reconfigurable LC Tank," In *IEEE Custom Intergrated Circuits Conference (CICC)*, **1,** 395–398 (2007).

[73] J. H. Kim and H. J. Yoo, "Multi-standard CMOS LC QVCO with Reconfigurable LC Tank and Low Power Low Phase Noise Quadrature Generation Method," In *IEICE Trans. Fundamentals*, **E89-A,** 1547–1551 (2006).

[74] J. H. C. Zhan, J. S. Duster, and K. T. Kornegay, "A Comparative Study of Common MOS VCO Topologies," http://domino.watson.ibm.com/acas/w3www_acas.nsf/images/projects_03.04/$FILE/kornegay.pdf (Accessed at November, 2008).

[75] P. Andreani, W. Xiaoyan, L. Vandi, and A. Fard, "A Study of Phase Noise in Colpitts and LC-Tank CMOS Oscillators," IEEE Journal of Solid State Circuits **40,** 1107–1118 (2005).

[76] H. K. Chiou, H. J. Chen, H. Y. Liao, S. G. Lin, and Y. C. Chang, "Design Formula For Band-Switching Capacitor Array in Wide Tuning Range Low-Phase-Noise LC-VCO," Microelectronics Journal, Elsevier pp. 1–6 (2008).

[77] M. D. Tsai, Y. H. Cho, and H. Wang, "A 5 GHz Low Phase Noise Differential Colpitts CMOS VCO," IEEE Microwave Wireless Components Letters pp. 327–329 (2005).

[78] D. Guermandi, P. Tortori, E. Franchi, and A. Gundi, "A 0.75 to 2.2 GHz Continuously-Tunable Quadrature VCO," IEEE Journal of Solid-State Circuits **1,** 536–615 (2005).

[79] O. Frioui, L. Zaid, W. Rahajandraibe, and F. Haddad, "A Very Low Phase Noise Fully Integrated CMOS Quadrature LC Oscillator for 2.4 GHz Bluetooth/WLAN Applications," In *International Symposium on communication and Information Technologies (ISCIT)*, pp. 55–60 (2007).

[80] C. T. Fu and H. C. Luong, "A 0.8 V CMOS Quadrature LC VCO Using Capacitive Coupling," In *IEEE Asian Solid-State Circuits Conference*, pp. 436–439 (2007).

[81] Y. H. Cho, F. C. Chang, M. F. Lei, and M. D. Tsai, "A low noise Bulk-coupled colpitts CMOS Quadrature VCO," In *Proceedings of Asia-Pecific Microwave Conference*, pp. 997–1000 (2006).

[82] H. M. Chen, Y. D. Jhuang, J. C. Lin, and S. L. Jang, "A 5.6 GHz Balanced Colpitts QVCO With Back-Gate Coupling Technique," In *IEEE Conference on Electron Devices and Solid-State Circuits, (EDSSC)*, pp. 965–967 (2007).

[83] C. T. Fu and H. C. Luong, "A 1V CMOS Quadrature LC VCO Using Diode Coupling," In *IEEE Radio and Wireless Symposium*, pp. 167–170 (2008).

[84] Z. Li, W. Zhihua, and C. Hongyi, "A 5 GHz CMOS VCO for the IEEE 802.11a WLAN Application," In *7th International Conference on Solid-State and Integrated Circuits Technology*, **2**, 1311– 1314 (2004).

[85] N. J. Oh and S. G. Lee, "Current Resused LC VCOs," IEEE Microwave Wireless Component Letters 15 (2005).

[86] S. M. Moon, M. Q. Lee, and B. S. Kim, "Design of Quadrature CMOS VCO Using Source Degeneration Resistor," In *Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 535–538 (2005).

[87] R. B. Jackson and E. C. Saavedra, "A 3 GHz CMOS Quadrature Oscillator Using Active Superharmonic Coupling," In *European Microwave Conference*, pp. 1109–1112 (2007).

[88] J. Y. Chang, C. H. Wu, and S. I. Liu, "A Low-Phase-Noise Low-Phase-Error 2.4 GHz CMOS Quadrature VCO," In *European Microwave Conference*, pp. 281–284 (2005).

[89] S. L. Jang, Y. H. Chuang, C. F. Lee, and S. H. Lee, "A 4.8 GHz Low Phase Noise Quadrature Colpitts VCO," In *International Symposium on VLSI Design, Automation and Test*, pp. 1–4 (2006).

[90] D. Leenaerts, C. Dijkmans, and M. Thompson, "A 0.18 μm CMOS 2.45 GHz, Low-Power Quadrature VCO With 15 percent Tuning Range," In *Radio Frequency Integrated Circuits (RFIC) Symposium*, **1**, 67–70 (2002).

[91] H. R. Kim, C. Y. Cha, S. M. Oh, M. S. Yang, and S. G. Lee, "A Very Low-Power Quadrature with Back-Gate Coupling," IEEE Journal of Solid-State Circuit **39,** 952–955 (2004).

[92] H. Shin, Z. Xu, and M. F. Chang, "A 1.8 V 6/9 GHz Switchable Dual-Band Quadrature LC VCO in SiGe BiCMOS Technology," In *IEEE Radio Frequency Integrated Circuits Symposium,* pp. 71–74 (2002).

[93] Y. C. Tsai, Y. S. Shen, and C. F. Jou, "A Low-Power Quadrature VCO Using Current-Reused Technique and Back-gate Coupling," In *Progress In Electromagnetics Research Symposium,* pp. 192–195 (2007).

[94] B. D. Muer, M. Borremans, M. Steyaert, and G. L. Puma, "A 2 GHz Low-Phase-Noise Integrated LC-VCO Set with Flicker-Noise Upconversion Minimization," IEEE Journal of Solid-State Circuit 35 (2000).

[95] S. Zafar, T. Z. A. Zulkifli, and M. Awan, "Design of Voltage Controlled Oscillator (VCO) for Ultra Wideband (UWB) CMOS Frequency Synthesizer," In *International Conference On Intelligent and Advanced Systems, (ICIAS),* pp. 1383–1386 (2007).

[96] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF ICs," IEEE Journal of Solid-State Circuits **33,** 743–751 (1998).

[97] D. Roberts *et al.*, "Application of On-Chip MIM Decoupling Capacitor for 90nm SOI Microprocessor," IEEE International Electron Devices Meeting, (IEDM) Technical Digest pp. 72–75 (2005).

[98] *Cadence Design Environment, Version 5.1.41* (San Jose, CA, USA :Cadence Design Systems, 2007).

[99] R. M. Svitek, *SiGe BiCMOS RF ICs and Components for High Speed Wireless Data Networks* (P.hD Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University, Blacksburg, Virginia, 2005).

[100] S. Zafar, T. Z. A. Zulkifli, and M. Awan, "Design of the Low Power 2.8 GHz LC QVCO in 0.18 μm RF CMOS Technology," International Journal of Electronics, Taylor and Francis (Submitted) (2008).

[101] S. Zafar, T. Z. A. Zulkifli, and M. Awan, "Design and Measurement of 3.1 GHz Low Phase Noise Quadrature VCO," In *IEEE Circuits and System, International Conference on Testing and Diagnostics, (ICTD), (Accepted)*, (China, 2009).

[102] S. Zafar, T. Z. A. Zulkifli, and M. Awan, "5 GHz Low Phase Noise Quadrature VCO in 0.13 μm RF CMOS Process Technology," In *IEEE Wireless and Micrwave Technology Conference, (WAMICON)(Accepted)*, (FL, USA, 2009).

[103] Y. C. Chang, Y. C. Chiu, S. G. Lin, Y. Z. Juang, and H. K. Chiou, "High Phase Accuracy On-Wafer Measurement for Quadrature Voltage-Controlled Oscillator," In *Proceedings of the 37th European Microwave Conference*, pp. 340–343 (2007).

[104] M. Burns and G. W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement* (Oxford Series, 2001).

[105] T. E. Kolding, "General Accuracy Considerations of Microwave on Wafer Silicon Device Measurements," In *IEEE International Microwave Symposium Digest, (MTT-S)*, pp. 1839–1842 (2000).

[106] K. B. Schaub, *Production Testing of RF and System-on-a-Chip Devices for Wireless Communications*, 1st ed. (Artech House, Inc, London, 2004), No. 272.

[107] *Calibre nmDRC and Calibre nmLVS* (Mentor Graphics, Wilsonville, OR, 2007).

[108] K. J. Koh, M. Y. Park, C. S. Kim, and H. K. Yu, "Subharmonically Pumped CMOS Frequency Conversion (Up and Down) Circuits for 2 GHz WCDMA Direct-Conversion Transceiver," IEEE Journal of Solid-State Circuits **39,** 871–884 (2004).

[109] N. M. Pletcher, *Micro Power Radio Frequency Oscillator Design* (University of California, Berkeley, USA, 2004).

[110] J. H. Chang and C. K. Kim, "A Symmetrical 6 GHz Fully Integrated Cascode Coupling CMOS LC Quadrature VCO," IEEE Microwave Wireless Component Letters **15,** 389–392 (2005).

[111] C. Y. Wu and H. S. Kao, "A 2-V Low-Power CMOS Direct-Conversion Quadrature Modulator with Integrated Quadrature Voltage-Controlled Qscillator and RF Amplifier for GHz RF Transmitter Appllications," In *IEEE Trans. On Circuits and System-II: Analog and Digital Signal Process*, **49,** 123–134 (2002).

[112] A. Fard and P. Andreani, "A Low-Phase-Noise Wide-Band CMOS Quadrature VCO For Multi-Standard RF Front-Ends," In *IEEE Radio Frequency Integrated Circuit (RFIC) Symposium*, pp. 539–542 (2005).

[113] S. Rong and H. C. Luong, "A 1 V 4 GHz and 10 GHz Transformer Based Dual Band Quadrature VCO in 0.18 μm CMOS," In *IEEE Custom Intergrated Circuits Conference (CICC)*, **1,** 817–820 (2007).

[114] S. L. Jang, Y. H. Chuang, Y. C. Wang, S. H. Lee, and J. F. Lee, "A Low Power and Low Phase Noise Complementary Colpitts Quadrature VCO," http://140.117.166.1/cchome/ISCOM2005/SubmitPaper/UploadPapers/ISCON05_00125.pdf (Accessed at November, 2008).

[115] C. Y. Jeong and C. Yoo, "5 GHz Low Phase Noise CMOS Quadrature VCO," IEEE Microwave and Wireless Components Letters **16,** 609–611 (2006).

[116] S. L. J. Gierkink, "A Low-Phase-Noise 5 GHz CMOS Quadrature VCO Using Superharmonic Coupling," IEEE Journal of Solid-State Circuits **38,** 1148–1154 (2003).

Appendix A

Inductor Design

This chapter describes the physical realization of patterned ground shield (PGS) and the spiral inductor design parameters.

The patterned ground shield (PGS) is designed using 0.18 μm $CMOS$ process technology. The polysilicon width is 2 μm. The metal 1 strips are used to provide ground. The PGS is shown in Fig. A.1.

$ASITIC$ is used to design symmetrical spiral inductor. The symmetrical spiral inductor is designed for $LP^3 - QVCO$ designs. The implementation is carried out using 0.13 μm RF $CMOS$ process technology. The inductor design parameters are summarized in Table A.1. The inductor output results are discussed in Chapter 3, previously.

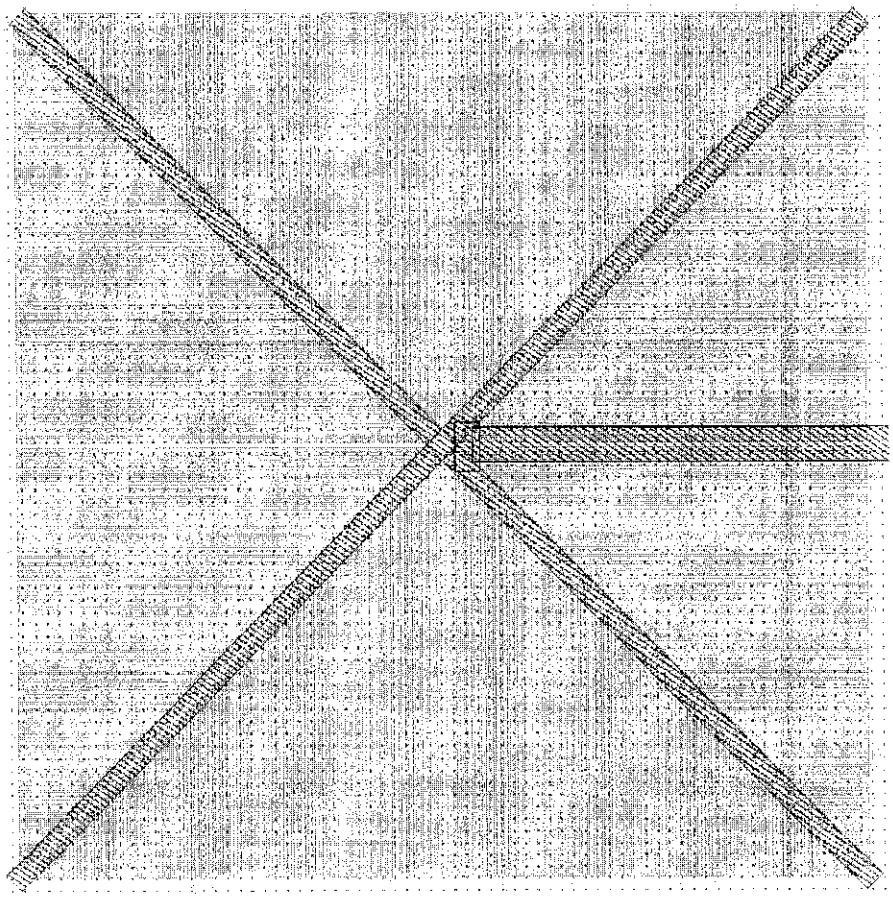


Figure A.1 Patterned ground shield used in LP^3-QVCO design no. 1, 2 and 3

Table A.1 Symmetrical spiral inductor design parameters using ASITIC.

Parameter Names	Inductor Parameter Values
SYMSQ Name	L1
Length (LEN)	160
Width (W)	8
Spacing (S)	2
Inner Length (ILEN)	17
Number of turns (N)	2
Origin of spiral center (XOR)	100
Origin of spiral center (YOR)	100
Metal Layer	UTM (Met 8)

Appendix B

Physical Realization of pMOS Varactor

This chapter contains the physical realization of $pMOS$ varactors. The $pMOS$ varactors are used in $LP^3 - QVCO$ design no. 4 to 7 and implementation is carried out using 0.13 μm $RF\ CMOS$ process technology. The multifinger gate width structure of a $pMOS$ varactors are used in $LP^3 - QVCO$ designs. The $pMOS$ varactors with multifinger gate width configuration are shown in Fig. B.1 and Fig. B.2. The $pMOS$ varactors with multifinger gate width configuration used in $LP^3 - QVCO$ design no. 6 and 7 are shown in Fig. B.3 and Fig. B.4, respectively.

Fig. B.1 and Fig. B.3 show the (3.125 μm $\times$ 64 = 200 μm) multifinger gate width configuration of $pMOS$ varactor used $LP^3 - QVCO$ design no. 4 and 6, respectively. Fig. B.2 and Fig. B.4 show the (8 μm $\times$ 25 = 200 μm) multifinger gate width configuration of $pMOS$ varactor used in $LP^3 - QVCO$ design no. 5 and 7, respectively.

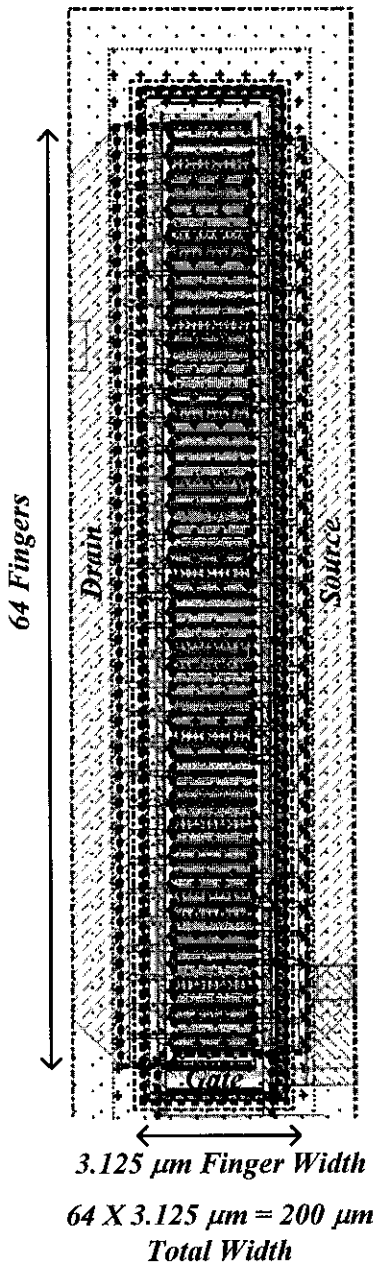


Figure B.1 A pMOS varactor layout of LP^3-QVCO design no. 4

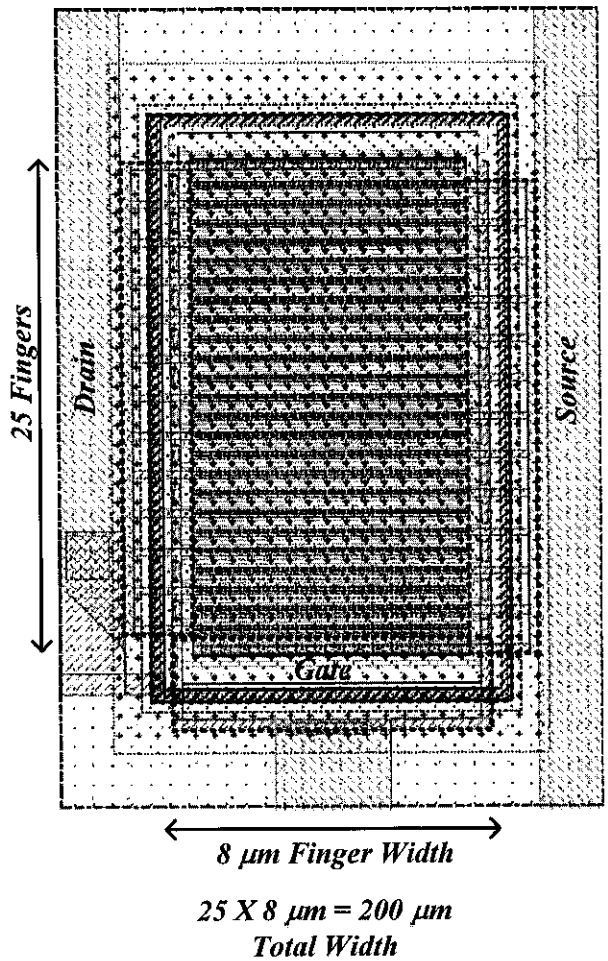


Figure B.2 A pMOS varactor layout of LP^3-QVCO design no. 5

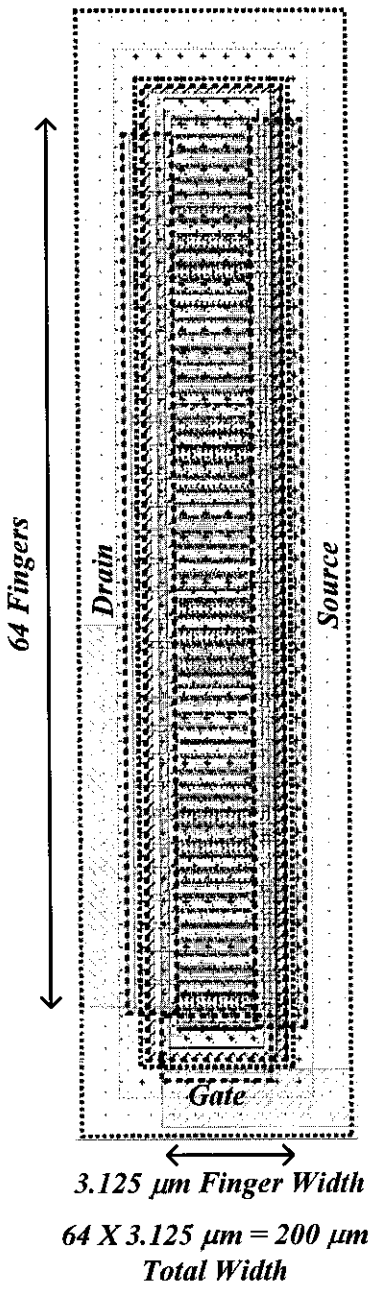


Figure B.3 A pMOS varactor layout of LP^3-QVCO design no. 6

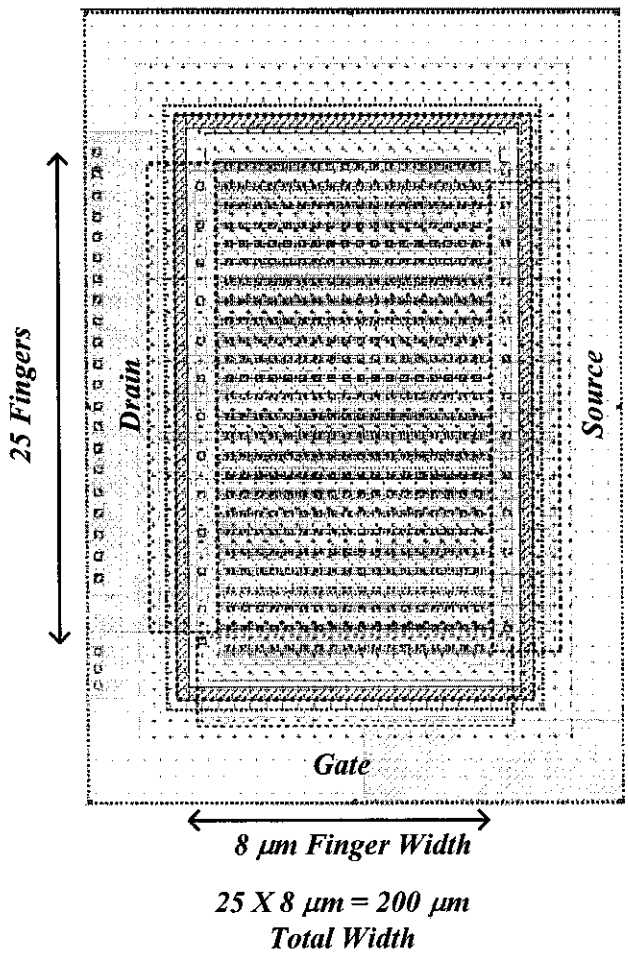
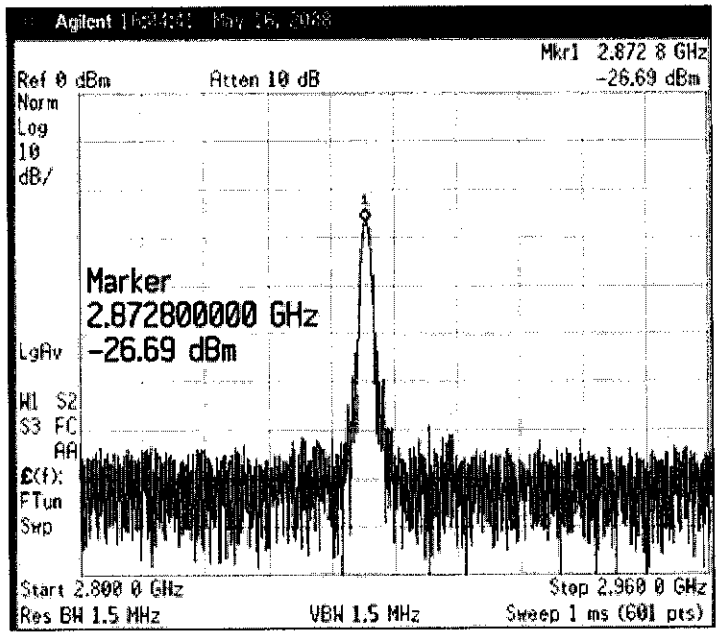


Figure B.4 A pMOS varactor layout of LP^3-QVCO design no. 7

Appendix C

LP^3-QVCO Measurement Results

The measured results for $LP^3 - QVCO$ designs are shown in this chapter. The frequency spectrum, phase noise, frequency sensitivity and transient analysis of $LP^3 - QVCO$ design no. 1 to design no. 7 are presented. The phase noise results for $LP^3 - QVCO$ designs are measured at the offset frequencies of 100 KHz, 1 MHz and 3 MHz from the carrier signal. The frequency spectrum also shows the output RF power for $LP^3 - QVCO$ designs.



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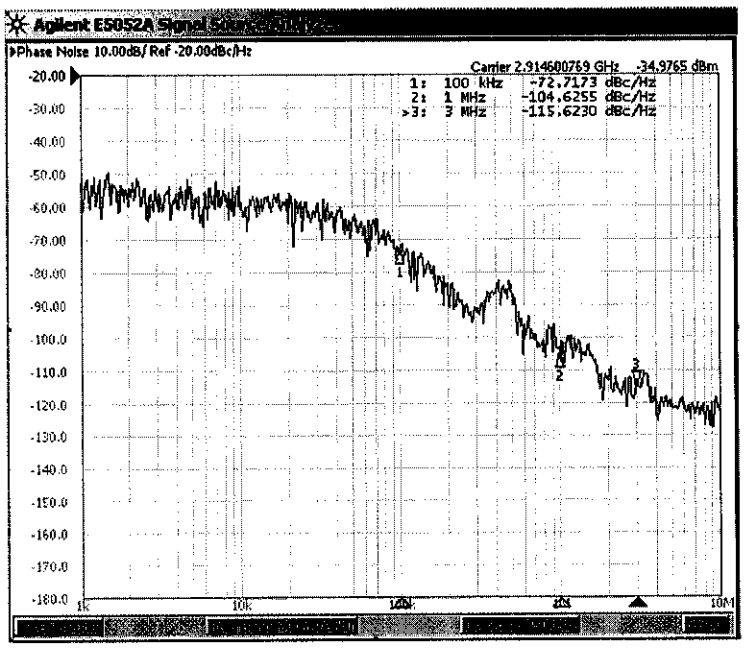
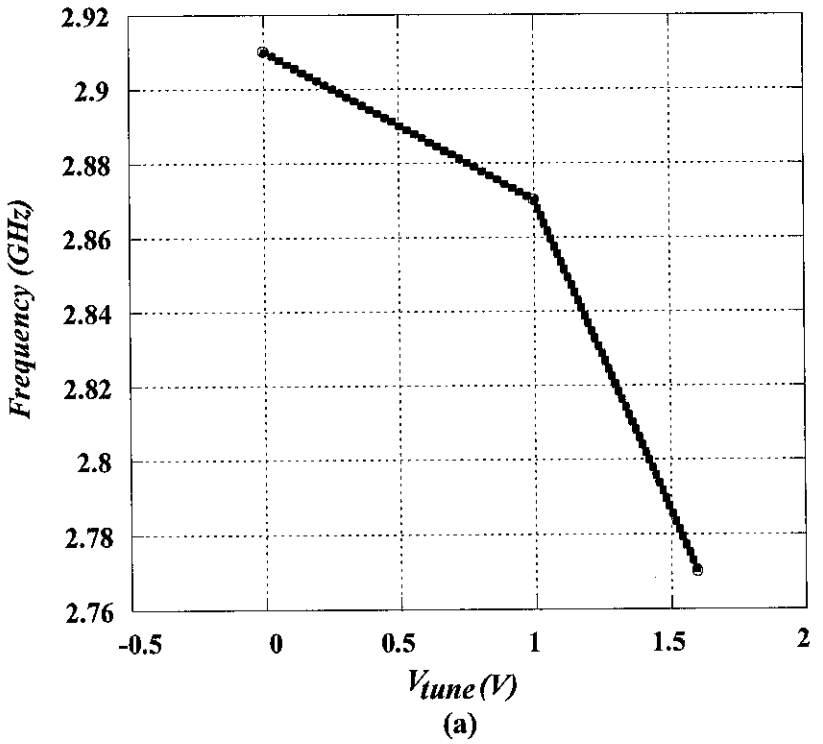


(b)

Figure C.1 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 1



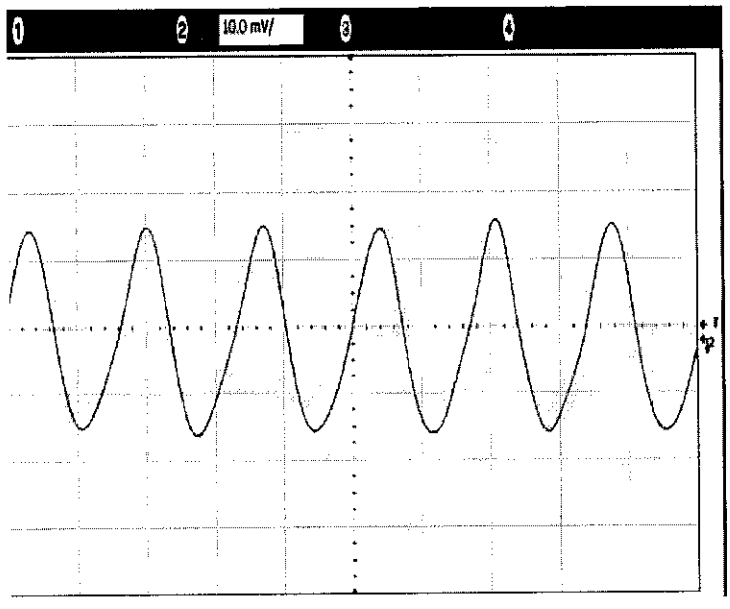
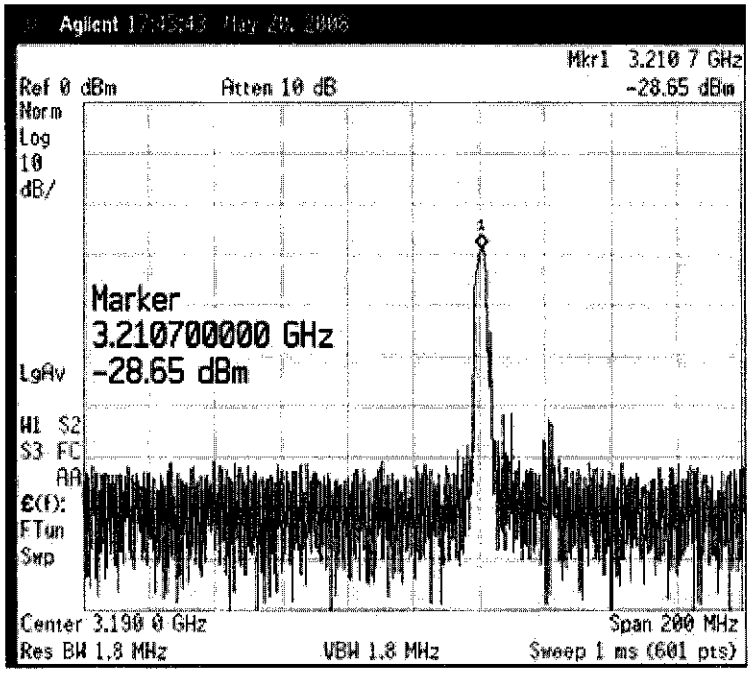
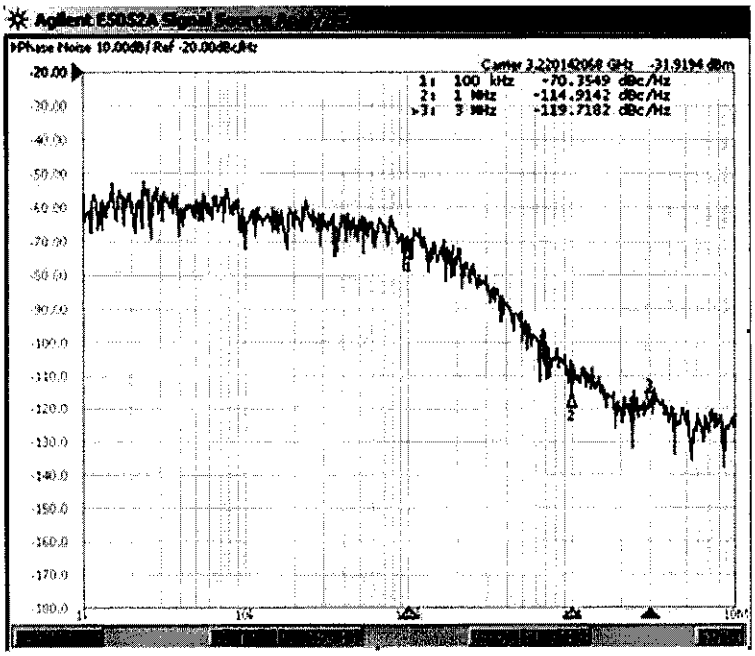


Figure C.2 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 1

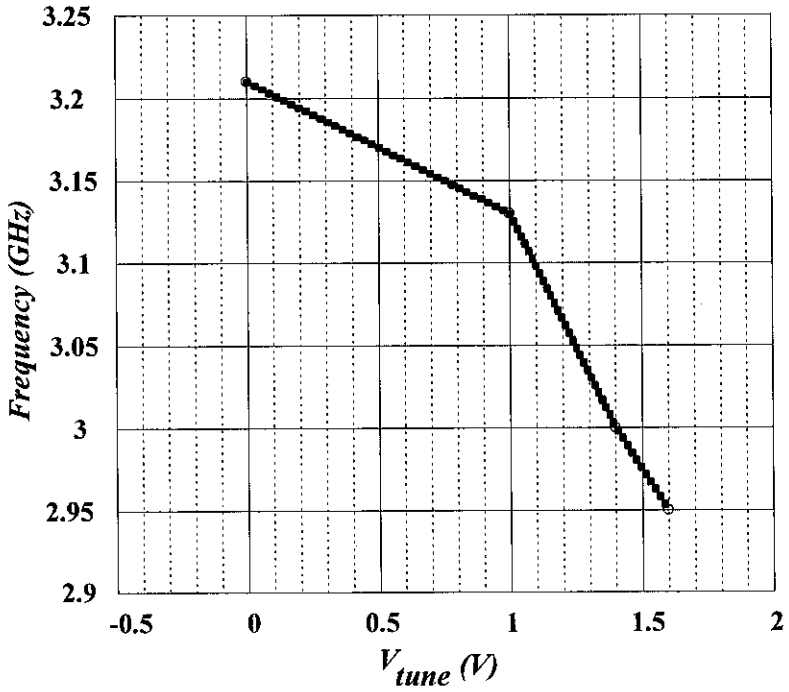


(a)



(b)

Figure C.3 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 2



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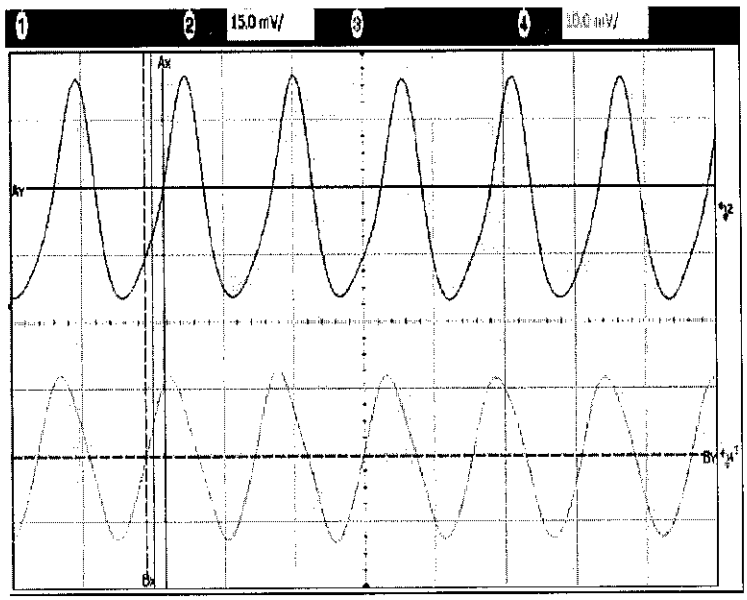

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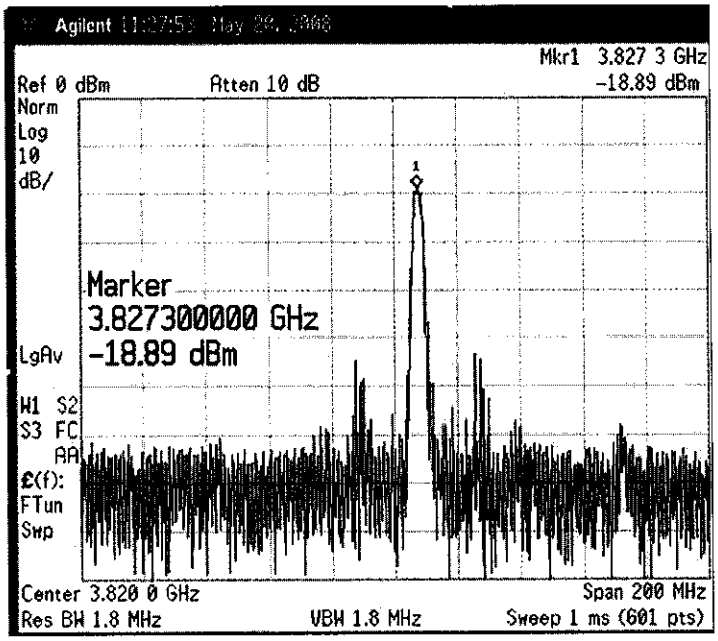
Figure C.4 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 2



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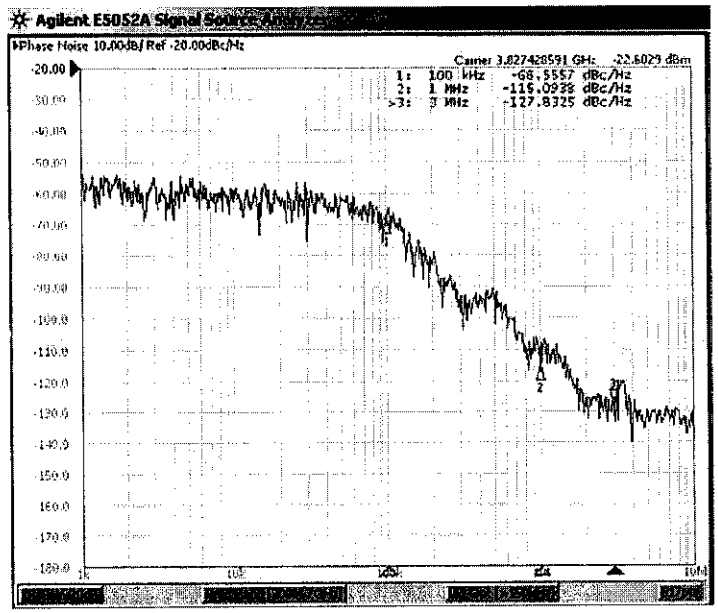


(b)

Figure C.5 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QO design no. 3

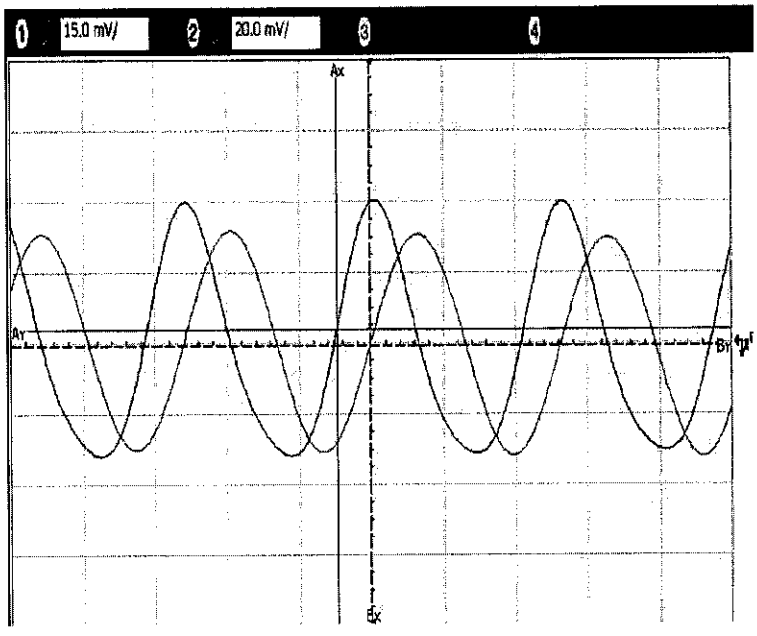
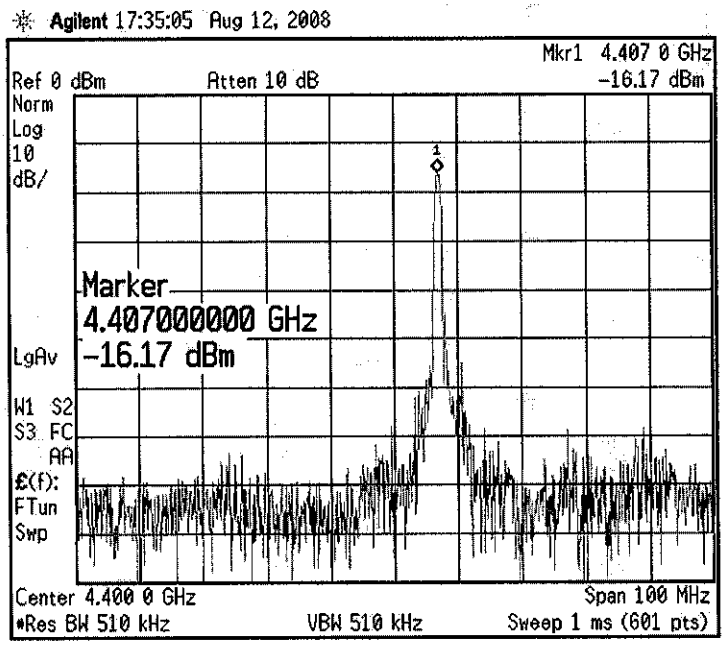


Figure C.6 Transient analysis of measured LP^3-QO design no. 3



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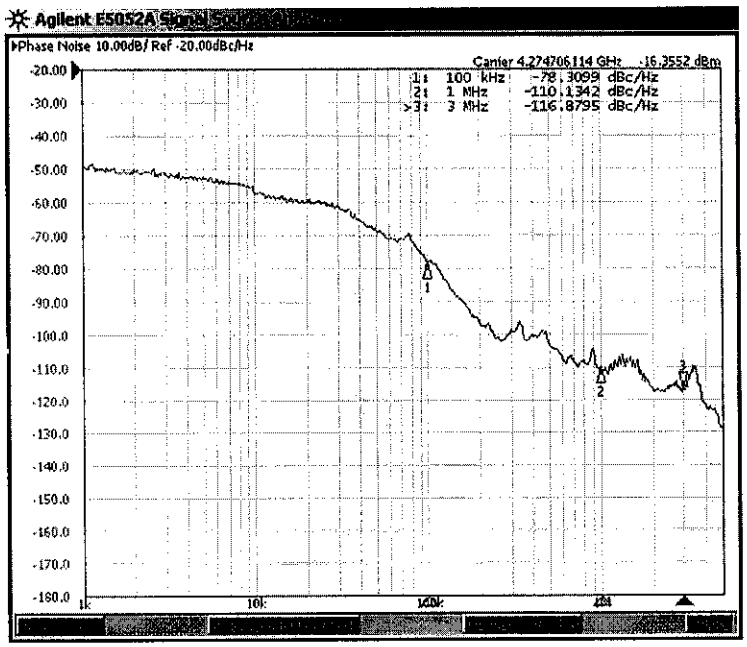

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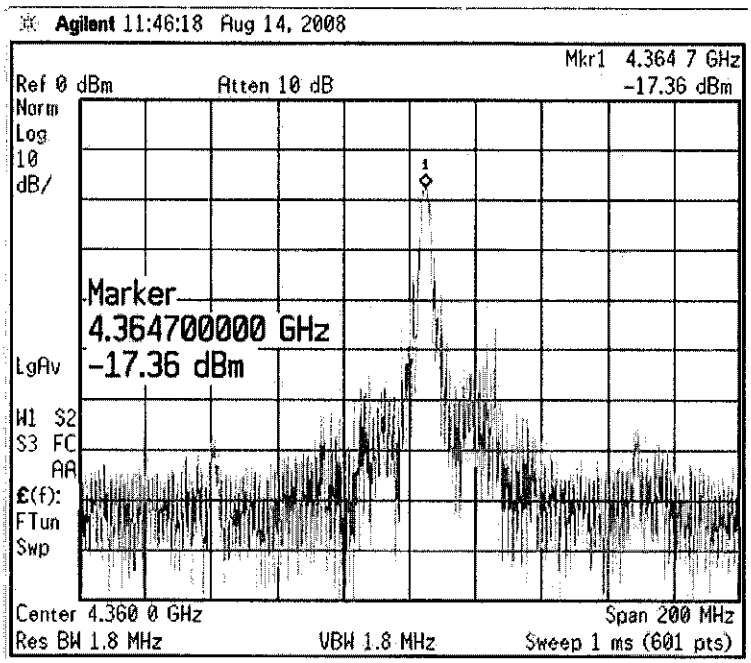
Figure C.7 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 4



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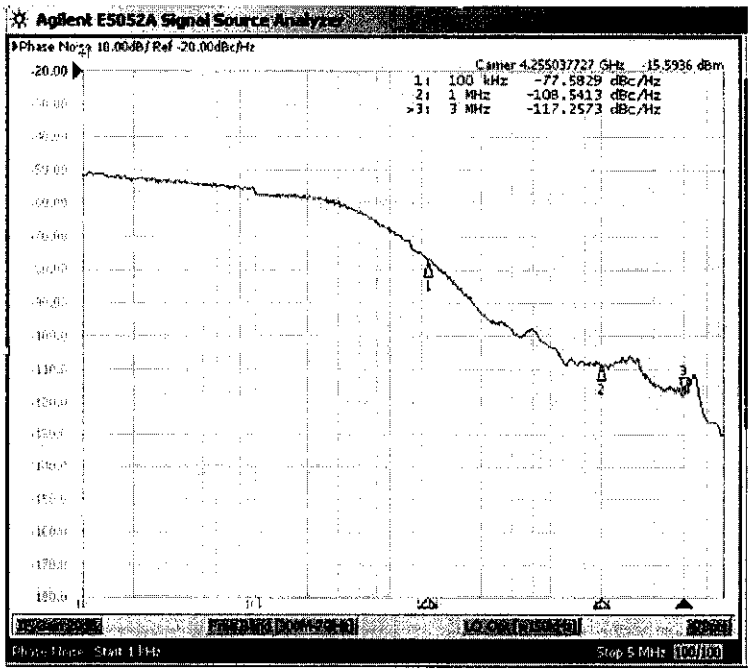

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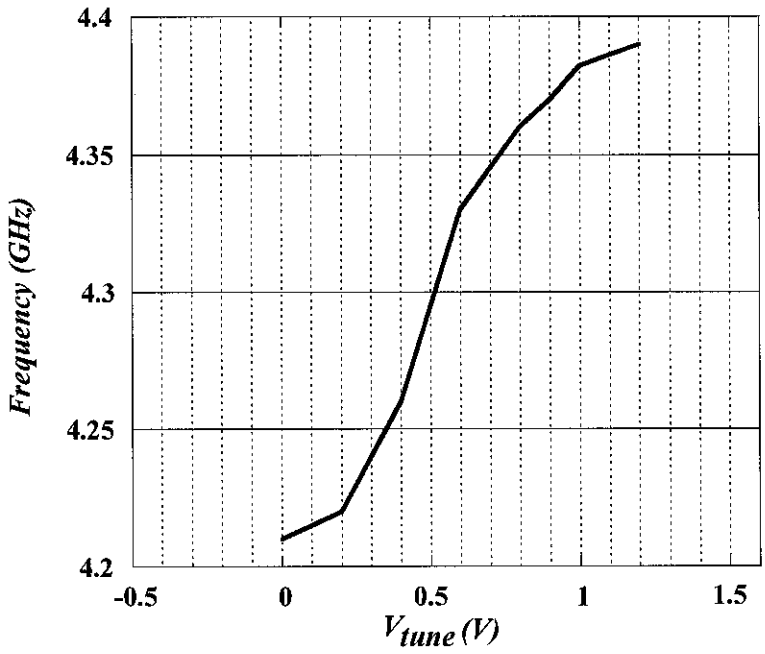
Figure C.8 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 5



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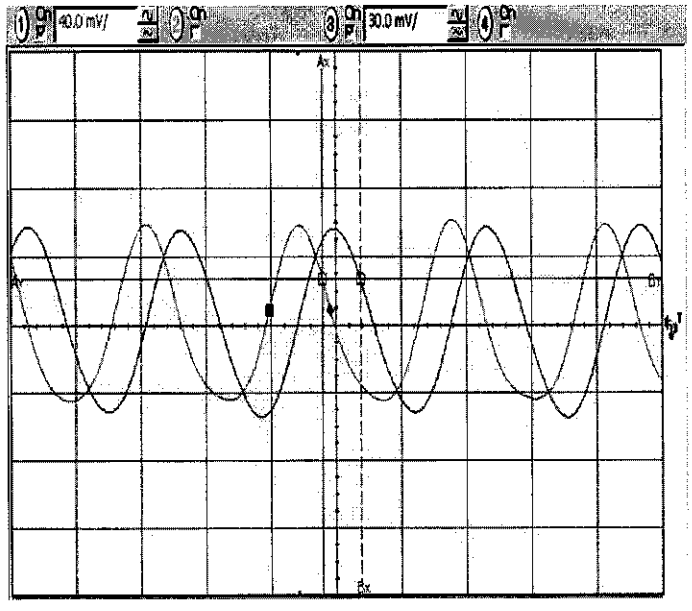

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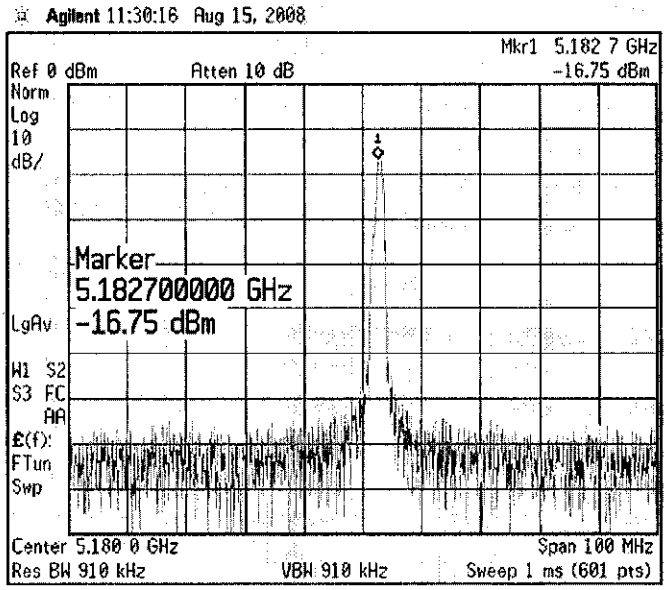
Figure C.9 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 5



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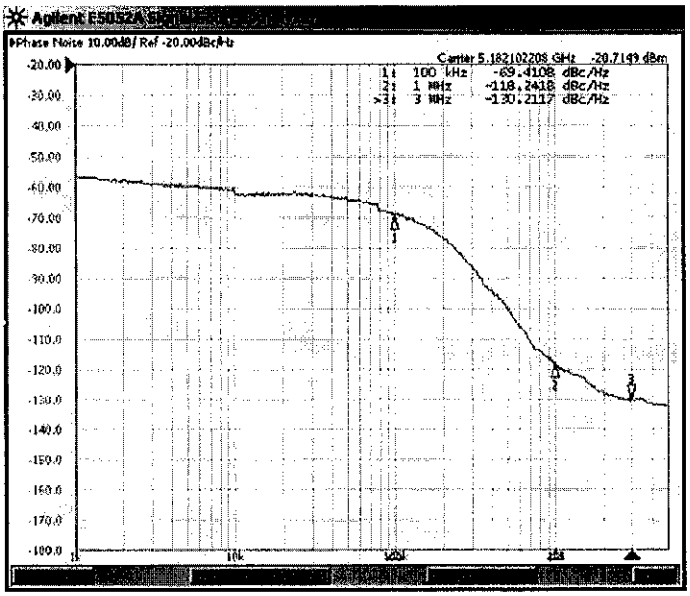

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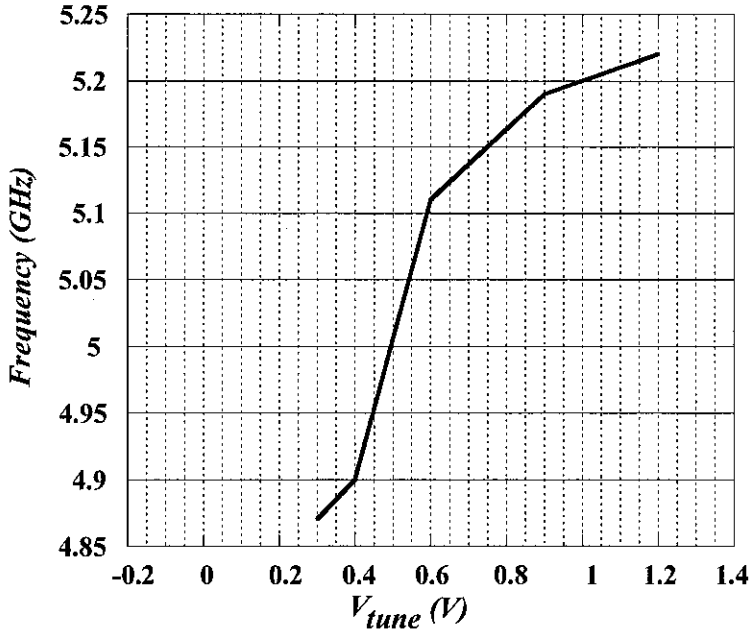
Figure C.10 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 6



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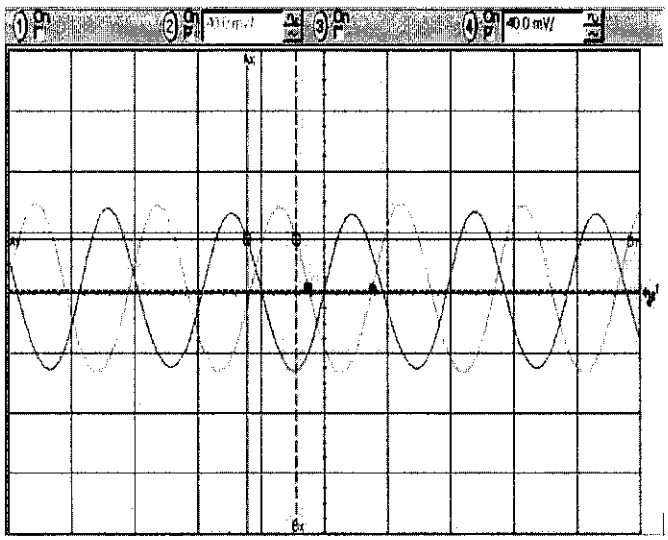

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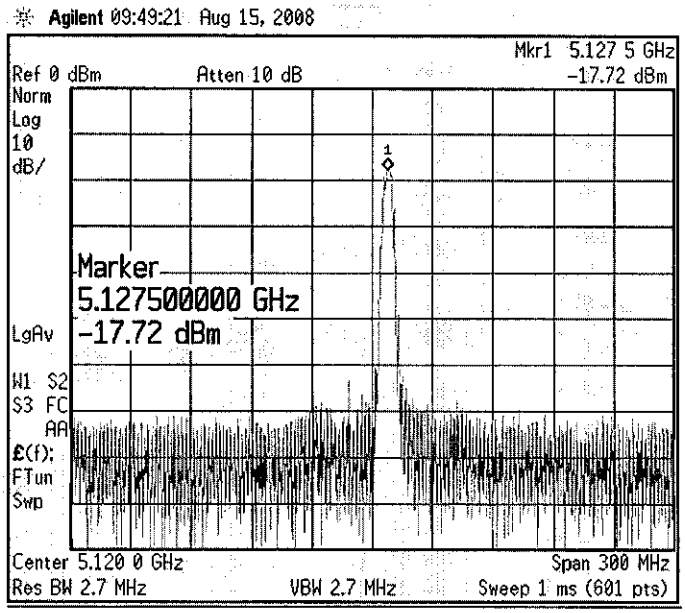
Figure C.11 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 6



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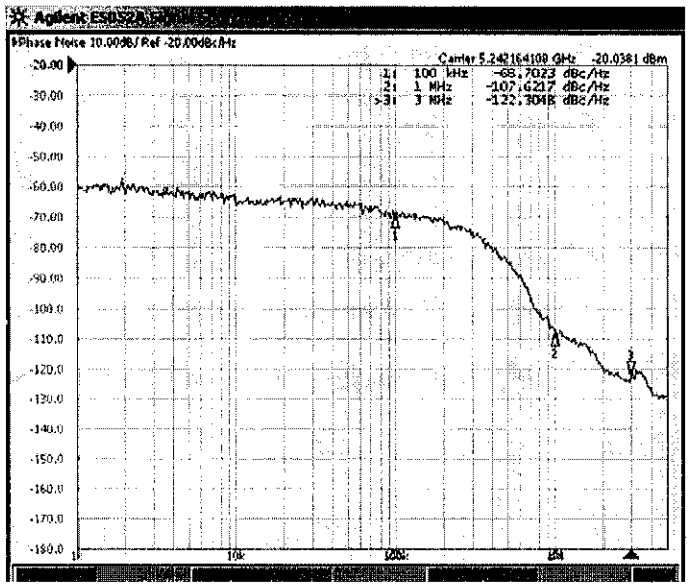

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Figure C.12 (a) Output frequency spectrum and (b) phase noise of the measured LP^3-QVCO design no. 7

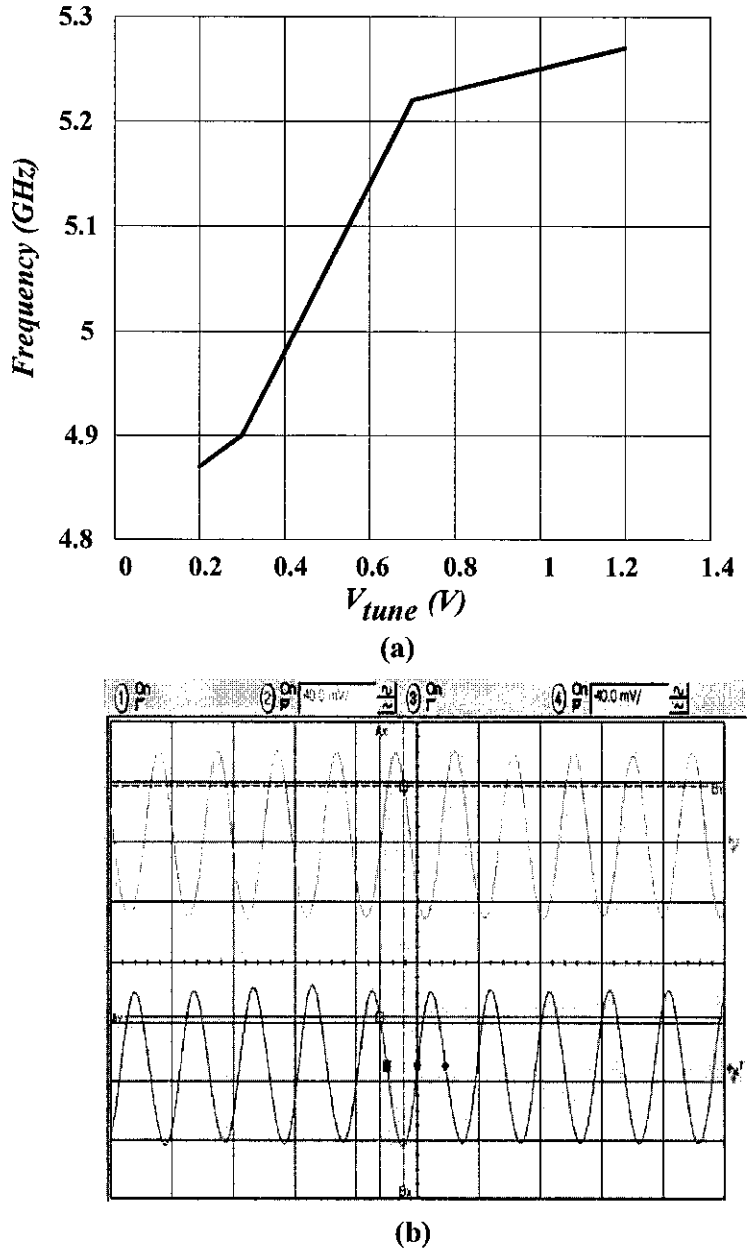

Figure C.13 (a) Frequency sensitivity and (b) transient analysis of measured LP^3-QVCO design no. 7

INDEX

RF CMOS, 5, 64, 126, 127
0.13 μm *CMOS* process, 47
0.13 μm RFCMOS process, 5, 6, 89, 93, 95, 99
0.18 μm *CMOS* process, 47, 64
0.18 μm CMOS process, 5, 6, 88, 99, 100
0.18 μm RFCMOS process, 5, 84, 95
1/f noise, 40, 42, 55
50 Ω resistor, 64

active device, 55
ADS, 18
Agilent signal source analyzer, 96
ASITIC, 18, 56, 144

Barkhausen criteria, 14
Bias-Tee, 96
BiCMOS, 2
boltzman's constant, 38
Bond pad, 84
Bond pads, 64, 69, 83, 88, 89, 93, 107, 109, 112
buffer, 63

Cadence, 62
Cadence-SpectreRF, 109
chapter no. 2 summary, 47
Chip area, 100
Circular spiral inductors, 118
closed-loop poles, 26
CMOS, 2, 58, 64, 125
CMOS oscillator types, 13
CMOS VCO topologies, 30
CMOS-VCO, 45
Colpitts oscillator, 49
colpitts oscillator, 15, 27, 28
colpitts oscillators, 27
Common drain buffer, 63, 64
Common-drain buffer, 64
conclusion, 126
coupling factor, K, 35
cross coupled oscillators, 24
cross-coupled oscillator, 24
crystal oscillators, 14
CTI, 120
current mirrors, 64
cyclostationary noise, 40

DS-VCO, 32, 52–54

electromagnetic energy, 19
Electromagnetic loss, 60
electron mobility, 30
EM modulator, 18

FastHenry, 18
figure of merit, 44
filters, 11
flicker noise, 54, 55
FOM, 44, 47
frequency synthesizers, 1
frequency tuning range, 45
future work, 128

GaAs, 2

heterodyne receiver, 9, 10
homodyne receivers, 9, 10

IC, 62
ideal oscillator, 37
Implementation introduction, 83
inductor design, 56
integrated capacitors, 60
Introduction, 50
Introduction of chapter 1, 9
ISF, 41, 43

layout, 83
Layout of Design No. 1, 84
Layout of Design No. 2 and 3, 84
Layout of Design No. 4 and 5, 88
Layout of Design No. 6 and 7, 93
LC, 45
LC oscillator, 20

LC-tank, 5, 14, 19–21, 23, 24, 30, 33, 35, 40, 49, 50, 52, 54, 62, 66
Leeson's equation, 37–39, 54
LNA, 1, 11
LP^3-QVCO results discussion, 118
LP^3-QVCO, 4, 6–8, 69, 79, 107, 126
LP^3-QVCO chip dimensions, 107
LP^3-QVCO component parameters, 78
LP^3-QVCO design, 66
LP^3-QVCO design no. 1, 71
LP^3-QVCO design no. 2, 71
LP^3-QVCO design no. 4 - 5, 76
LP^3-QVCO design no. 4 micrograph, 103
LP^3-QVCO design no. 5 micrograph, 103
LP^3-QVCO design no. 6 - 7, 78
LP^3-QVCO design no. 6 micrograph, 103
LP^3-QVCO design no. 7 micrograph, 107
LP^3-QVCO design summary, 81
LP^3-QVCO fabricated chips, 99
LP^3-QVCO fabricated chips using 0.13 μm process, 103
LP^3-QVCO fabricated chips using 0.18 μm process, 99
LP^3-QVCO implementation summary, 107
LP^3-QVCO measurement setup, 96, 99
LP^3-QVCO results comparison, 121
LP^3-QVCO results summary, 123
LP^3-QVCO test results, 109
LP^3-QVCO with nMOS coupling, 67
LP^3-VCO, 56
LP^3 – *QO* design no. 3, 73
LP^3 – *QVCO* design flow, 79
LTI, 7, 9, 44
LTV, 7, 9, 44, 49
LTV system, 40

magnetic coupling, 16
MCM, 3
Metal 1, 60
metal top, 58
MIM, 62
MIM capacitors, 60
mixer, 1, 11
modern RF communication system, 9
MOS varactors, 20
MOSFET, 30
multifinger gate structure, 39, 55
mutual inductance, 16

negative (-Gm) oscillators, 29
nMOS, 52
noise figure, 11

objectives, 4
on-chip, 18
oscillation amplitude, 26
oscillator center frequency, 52
oscillator design techniques, 52
oscillator frequency spectrum, 37
oscillator performance parameters, 36
oscilloscope, 96
oxide capacitance, 30
oxide layer, 17

parameter analyzer, 96
parasitic capacitance, 17, 56
Parasitics capacitance, 120
Parseval's theorem, 42
patterned ground shield, 60
PGS, 60
phase noise, 9, 11, 14, 15, 30–32, 35–37, 39, 42, 44, 54, 55, 66, 69, 78, 96, 99, 113
Physical Realization of pMOS Varactor, 147
pi model, 18
pi model for spiral inductors, 58
pMOS varactor, 62
pMOS varactors, 20
pn-junction, 128
pn-junction varactor, 62
pn-junctions, 20
Polysilicon, 60
polysilicon-based capacitors, 60
power amplifier, 11
probe station, 96
process technology, 18

Q factor, 15
Q-factor, 58
quadrature voltage controlled oscillator, 32
QVCO, 1, 3, 4, 33, 47, 128
QVCO chip pins, 93

Research Scope, 5
Resistance variation, 120
RF, 1, 10, 125
RF circuits, 37
RF communication system, 50
RF output power, 113
RF transceivers, 10
RFIC, 2, 15
RFID, 3

s-parameters, 58
s-plane, 26
self resonance frequency, 18
Si, 2
Si-bipolar, 2
simulation transient output, 111
skin effect, 16
small signal model, 24
SNR, 53
SOC, 3, 47
source damping resistor, 55
Spectrum analyzer, 113
spectrum analyzer, 96
spiral inductor, 15
SS-VCO, 31
state of the art oscillators, 46
system-on-chip, 47

tail biasing, 54
thesis organization, 6
transconductance, 52
transconductances, 35
transient output, 112
tuning sensitivity, 115

UTM, 58
UWB frequency synthesizer architecture, 13

varactor, 15, 19, 62
VCO, 3, 4, 45, 47, 49, 52, 56
VCO design, 50, 51
VCO sensitivity, 46

wireless communication, 4

y-parameters, 18

zero-IF, 1, 10