APPLICATION OF BIFURCATION THEORY TO CURRENT MODE CONTROLLED PARALLEL-CONNECTED BOOST DC-DC CONVERTERS

By

ISLAM ISGENDEROV

PROJECT DISSERTATION

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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Certification of Approval

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Certification of Originality

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgments, and that the original work contained herein have not been undertaken or done by unspecified sources or persons

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ABSTRACT

This project is to design a circuit which will guarantee stable operation at switching frequencies, and any quasi-periodic or chaotic operation is regarded as being undesirable and should be avoided. This project focuses in particular on the application of bifurcation theory to parallel-input / parallel-output two-module current-programmed DC-DC converters. Besides, this project describes the operation of Current Mode Controlled Parallel-Connected Boost DC-DC Converters and basically defines chaos, bifurcation and quasi-periodic distortion of the circuit by varying the reference current and comparing it with inductor output current. Within specific ranges of reference current the circuit operates without any distortion. The design includes the simulation of any bifurcation within the intended operation range by using PSpice, Multisim and EWB software. The inductor current output waveforms obtained and compared at different levels of reference currents. There are few ways to improve the output waveforms such as connecting freewheeling diode with parallel to inductor, using combination of triple input/triple output Current Mode Controlled converter or just using parallel input/series output configuration. Parallel-input / parallel-output are the most common configuration that can be used in current mode control DC-DC converters. Simulation and calculation results shows that capacitor voltage ripple factor reduced from 30% to 3%(actual) and output current ripple from 20% to 3%. Improvement in this type of converter will open up new applications in datacommunication, telecommunication, power-supply in PC and inside the notebook, industrial automation and so forth. The core of the project work focuses on simulating the entire process and later building the prototype.

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ABBREVIATION AND NOMENCLATURES

FYP1	Final Year Project, Phase 1
FYP2	Final Year Project, Phase 2
PWM	Pulse Width Modulation
PCB	Printed Circuit Board
CMC	Current Mode Controller
VMC	Voltage Mode Controller
CCM	Continuous Conduction Mode
DCM	Discrete Conduction Mode
%OS	Percentage Overshoot
T_p	Peak Time
T_r	Rise Time
T_s	Settling Time
G(s)	Defined as open loop transfer function at s-plane
T(s)	Defined as close loop transfer function at s-plane

ACKNOWLEDGMENT

First and foremost, I would like to thank my supervisor, Mr. Zaihar Yahaya. Without his guidance, feedback and encouragement, this project would not have been possible. It has been valuable experience to work with him.

I would like to express my gratitude to Mr. Noridin Saad, lecturer at Electrical & Electronics Department of UTP for additional guidance and outstanding motivation to work on this project. His advices and support are greatly appreciated.

Special thanks to laboratory technicians at Electrical & Electronics Department of UTP, to Mr. Musa for his help with experiments when the project circuits were tested and to Ms. Siti Hawa for the time she invested in teaching the soldering techniques.

CHAPTER 1
INTRODUCTION

Bifurcation theory is introduced into nonlinear dynamics by a French man named Poincare. Bifurcation is used to indicate a qualitative change in features of the system, such as the number and the type of solutions, under the variation of one or more parameters on which the considered system depends.

This project uses reference current as variable parameter. Current Mode Controlled (CMC) converter becomes unstable at certain operating conditions, which causes unusual vibrations in the dc motor driving systems. Instability phenomena in power electronic motor driving systems are investigated from the point of view of bifurcation theory. It is known that CMC converter produces some kinds of bifurcations at the output which effects stable operation of dc motor driving systems. This project proposes method which makes it possible not only to determine instability regions of system parameters but also to investigate qualitative properties of the instability phenomena. These measurements and simulations can be done by using PSpice, EWB and Multisim electronic software packages. These software packages help us to visualize the performance and effect of the auxiliary circuit on converter systems.

The choice of whether to implement Current Mode Control (CMC) or Voltage Mode Control (VMC) as the feedback control method in a boost dc-dc converter is based on a number of considerations. While the perceived advantage of CMC is better feedback loop response, today high-frequency VMC converters closely rival their CMC counterparts. Beside this CMC control to output gain is higher at low frequencies and has a zero gain crossover frequency much higher than the VMC counterpart has. From a signal path standpoint in VMC, a load current change must first have an effect on the output voltage before the voltage amplifier can react and make a correction. CMC on the other hand sense a change in load current directly so the voltage amplifier does not need to react in order for the loop to make a correction. This cause and then react approach makes VMC slower to response than CMC with very high speed load transients. Because of these significant points I prefer to work on CMC rather than VMC converters.

Applications of boost CMC DC-DC converters:

- To control dc motor
- To control fan drive
- To boost the current inside the notebook or in PC power supply
- In industrial Automation such as PLC
- Single solenoid controllers
- Dual solenoid drivers for proportional and directional valves.

These are just a few applications of dc-dc boost converters but in real life it can be found more than these.

1.2 Problem Statement

In Current Mode Controlled Parallel-Connected Boost DC-DC Converter was observed to behave in a chaotic manner. Beside, this converter was encountered nonlinear behaviors, such as subharmonics and a period-doubling route to chaos. At some reference current levels, the output signal getting distorted and unstable. The design should have been in subharmonics and/or chaotic-free operation mode. From this it will help us to solve/improve stable operation performance of the output device that is connected to dc-dc boost converter.

1.3 Objectives and Scope of Study

The final year project (FYP) at University Technology Petronas covers period of 30 weeks starting from July 2005 to May 2006. Final year project can be divided into two phases, such as FYP 1 and FYP 2. The first phase requires working on research and finding out alternative solutions on a purposed topic. Beside this, all output simulation results of the project must be provided on this phase. Design implementation and final simulation on printed circuit board will be conducted on second phase. Moreover, scope of work includes some improvement on working project by applying suitable theories from Control Systems, Analogue Electronics and Power Electronics subjects.

The main objectives are:

- To demonstrate ability to integrate fundamental knowledge in developing techniques, methods and analysis.
- To be more attentive and initiative such as proposing a title for their project on their own.
- To work independently through exercising self-discipline, self-management and job co-ordination while undertaking the project.
- To enhance skills in the process of applying knowledge, expanding thoughts, solving problems independently and presenting findings through minimum guidance and supervision.

CHAPTER 2
LITERATURE REVIEW

The modern nonlinear theory is used such as, bifurcation theory and chaos theory, to analyze the two-module parallel-input / parallel-output boost DC-DC converter using peak current-control. This topology is known as a boost converter since the output voltage is higher than input. The converter circuits that are used in power electronics systems to change the system voltages from one dc level to another dc level. These devices normally operated at much higher frequencies than the line frequency, reaching as high as a few hundred kilo-hertz. This is why such converter circuits are known as high-frequency dc-to-dc switching converters or regulators.

The name "chaos theory" comes from the fact that the systems that the theory describes are apparently disordered, but chaos theory is really about finding the underlying order in apparently random data. The first true experimenter in chaos was a meteorologist, named Edward Lorenz. In 1960, he was working on the problem of weather prediction. He had a computer set up, with a set of twelve equations to model the weather. It didn't predict the weather itself. However this computer program did theoretically predict what the weather might be. One day in 1961, he wanted to see a particular sequence again. To save time, he started in the middle of the sequence, instead of the beginning. He entered the number off his printout and left to let it run. When he came back an hour later, the sequence had evolved differently. Instead of the same pattern as before, it diverged from the pattern, ending up wildly different from the original. (See Figure 1.) Eventually he figured out what happened. The computer stored the numbers to six decimal places in its memory. To save paper, he only had it printed out three decimal places. In the original sequence, the number was .506127, and he had only typed the first three digits, .506. [1]

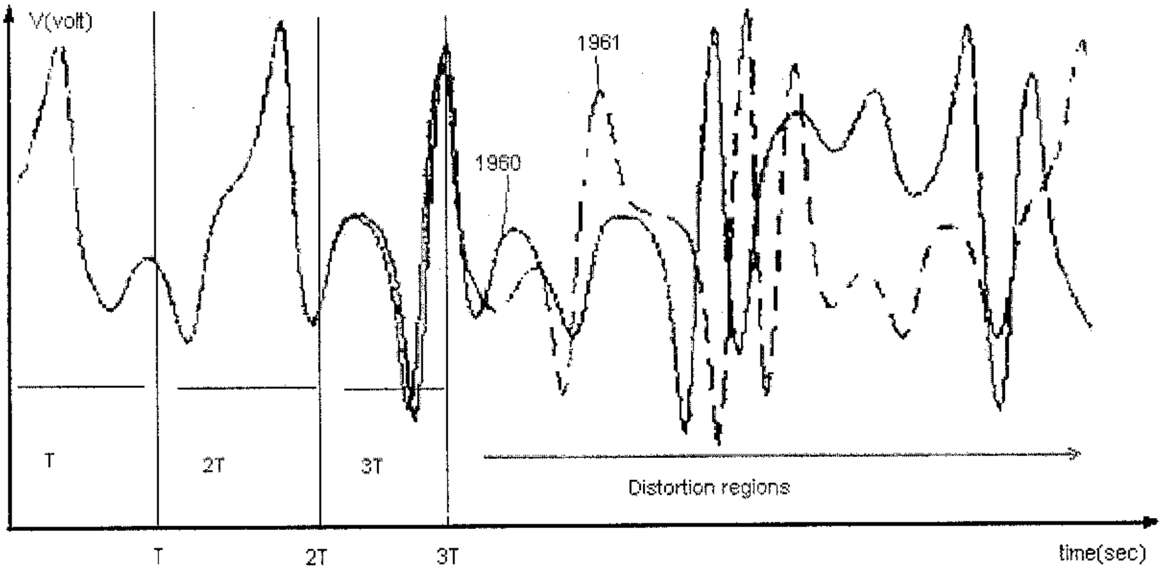


Figure 1: The difference between the start of these curves in only .000127[1]

From above information it is noticed that as soon as the period passes 3, the line breaks in two. Instead of settling down to a single line value, it would jump between two different values. Raising the reference current a little more causes it to jump between four different values. As the parameter rose further, the line bifurcated (doubled) again. The bifurcations came faster and faster until suddenly, chaos appeared. Past a certain increase in reference current, it becomes impossible to predict the behavior of the equation. However, upon closer inspection, it is possible to see white strips. Looking closer at these strips reveals little windows of order, where the equation goes through the bifurcations again before returning to chaos. This self-similarity, the fact that the graph has an exact copy of itself hidden deep inside, came to be an important aspect of chaos. It will give an ease to visualize the order and difference between chaos and bifurcation by looking at the graph provided in Figure 2.

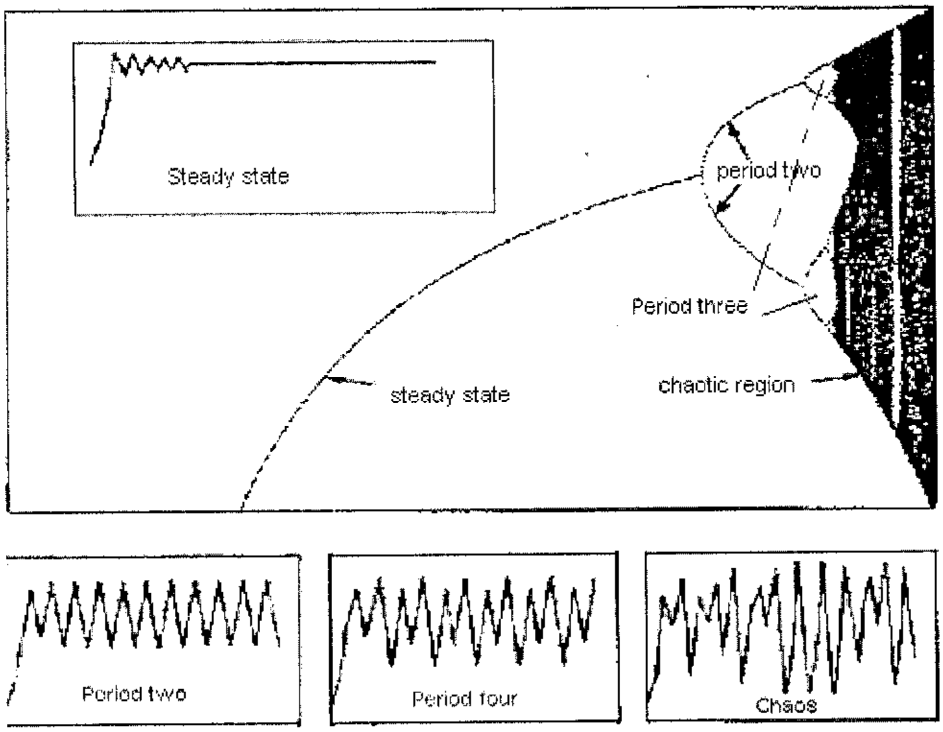


Figure 2: Bifurcation diagram for the quadratic map.[1]

Poincare used the term bifurcation to describe the "splitting" of asymptotic states of a dynamical system. As we examine Figure 2, several different types of changes can be occurred. These bifurcations should be analyzed and classified. At a bifurcation value, the qualitative nature of the solution changes. It can change to, or from, an equilibrium, periodic, or chaotic state. It can change from one type of periodic state to another or from one type of chaotic state to another. [1]

According to authors (Professor Al-Mothafar, and Professor A. Natsheh), initial studies on DC-DC converters' chaos and subharmonics instability were observed by Deane and Hamill [2] and Chan and Tse [3]. Their works illustrate how chaos can occur in current-programmed boost DC-DC converters operating in the continuous conduction mode. Chaos was also studied for a voltage-mode PWM buck DC-DC switching converter operating in the continuous conduction mode by Brockett and Wood [2], Deane and Hamill [5] and Al-Fayyoumi [6].

In the aforementioned studies, the analyses were limited to a single boost converter. The first the small signal and transient behavior of two-module parallel-input/series-output

DC-DC converters with mutually coupled inductor was investigated by Professor Al-Mothafar but in his studies bifurcation analysis were not addressed.

The last study on parallel input/parallel output dc-to-dc converter was done by authors in 2002 (Professor Al-Mothafar, and Professor A. Natsheh). They could manage to find out chaos, bifurcation and steady state regions of the system. Except the authors nobody studied on parallel input/parallel output dc-dc converters. But on their work they did not mention how to reduce or cancel the distortion on boost converter. This project paper will further investigate on chaos and bifurcation distortions by designing auxiliary circuit which will reduce or even cancel the output distortion in dc-dc converter.

CHAPTER 3
METHODOLOGY

3.1 Basic Operation

3.1.1. DC-DC Boost Converter.

Parallel-input / parallel-output two-module current-programmed boost DC-DC converter circuit (Figure 3) consists of two controlled switches S_1 and S_2, two uncontrolled switches D_1 and D_2, two inductors L_1 and L_2, two capacitors C_1 and C_2, and a load resistor R. The switching of each converter is controlled by a feedback path consisting of a comparator and a flip-flop.

Each comparator compares the respective current through the inductor with a reference current. It is assumed that the converter is operating in continuous conduction mode, so that the inductor currents never fall to zero.

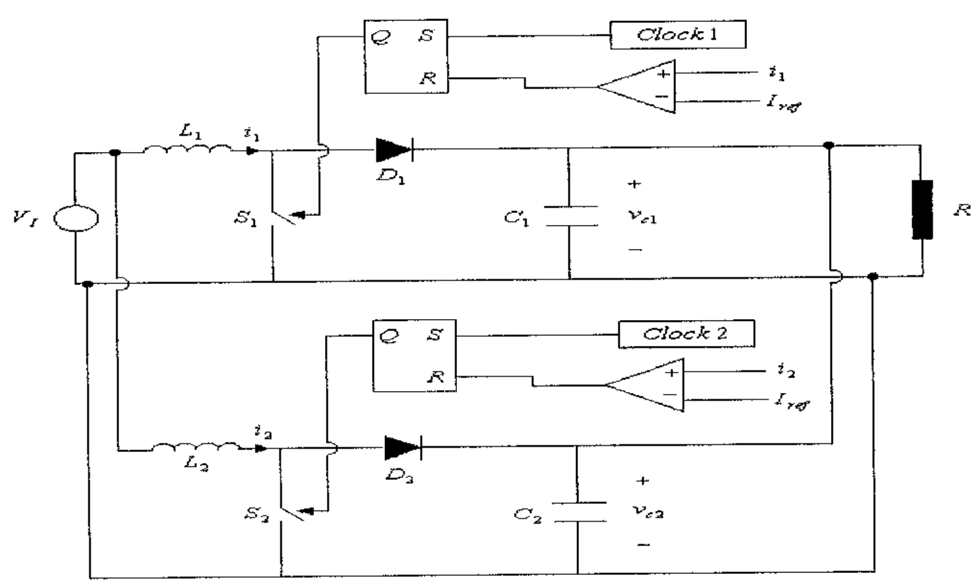


Figure 3: Bifurcation diagram for the quadratic map.

There are two states of the circuit depending on whether the controlled switches S_1 and S_2 are open or closed. When switches S_1 and S_2 are closed, the currents through the inductors rise and any clock pulses arriving during that period are ignored. The switches S_1 and S_2 become open when i_1 and i_2 reach the reference current. When switches S_1 and S_2 are open, the currents i_1 and i_2 fall. The switches S_1 and S_2 close again upon the arrival of the next clock pulses. The significance of reference current is to determine the allowed operation range of the dual input – dual output boost converter. In this circuit the reference current range is from 500 mA to 1.5 mA. Increase in reference current raise the conduction time of the inductor. As result output voltage and output current level increases.

3.1.2 Remote Control for Power Supply

Connect this circuit to any of your home appliances (lamp, fan, radio, etc) to make the appliance turn on/off from a TV, VCD or DVD remote control. The circuit can be activated from up to 10 meters. The 38 kHz infrared (IR) rays generated by the remote control are received by IR receiver module TSOP1738 of the circuit. Pin 1 of TSOP1738 is connected to ground, pin 2 is connected to the power supply through resistor R5 and the output is taken from pin 3. The output signal is amplified by transistor T1 (BC558). (see figure 4).

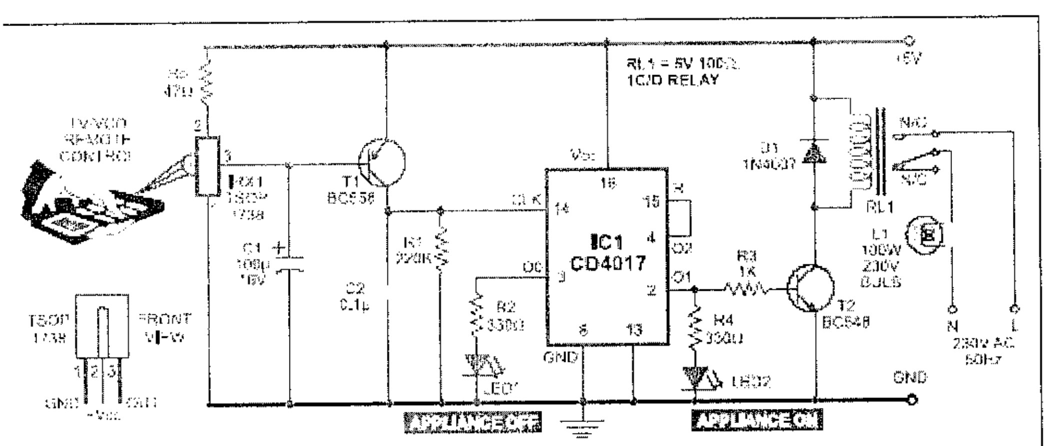


Figure 4: Receiver and transmitter schematic diagram

The amplified signal is fed to clock pin 14 of decade counter IC CD4017 (IC1). Pin 8 of IC1 is grounded, pin 16 is connected to V_{cc} and pin 3 is connected to LED_1 (red), which glows to indicate that the appliance is "off". The output of IC1 is taken from its pin 2. LED_2 (green) connected to pin 2 is used to indicate the 'on' state of the appliance. Transistor T_2 (BC548) connected to pin 2 of IC_1 drives relay RL_1. Diode 1N4007 (D_1) acts as a freewheeling diode. The appliance to be controlled is connected between the pole of the relay and neutral terminal of mains. It gets connected to live terminal of AC

Mains via normally opened (N/O) contact when the relay energizes. This circuit configuration can be applied to turn on / off dc-dc boost converter. At the output of the converter dc motor can be used as example of digital tape which controlled by remote control.

3.2 Derivation of the Iterative Map

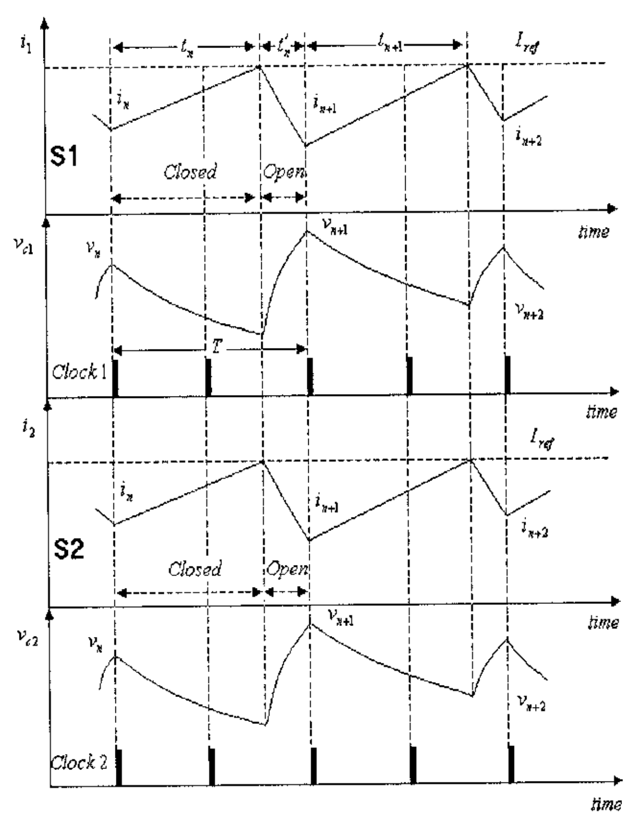


Figure 5: Sketch of current and voltage waveforms appearing in the circuit of Figure 3 [7]

Where:

i_1, i_2 are the currents through inductors L_1 and L_2, respectively.

v_{c1}, v_{c2} are voltages across capacitors C_1 and C_2, respectively.

There are two circuit configurations, according to whether S_1 and S_2 are closed or open. It is assumed that they are closed initially. The currents i_1 and i_2 through inductors L_1 and L_2 then rise linearly until $i_1 = I_{ref}$ and $i_2 = I_{ref}$. Any clock pulses arriving during this time are ignored. When $i_1 = I_{ref}$ and $i_2 = I_{ref}$, S_1 and S_2 open, and remain open until the arrival of the next clock pulse, whereupon they close again. The waveforms appearing in the circuit are sketched in Figure 4.

3.3 Circuit Simulation and Results

The circuit was simulated by using PSpice software. The most important parameters are inductor current and capacitor voltage behaviors. Slight change in reference current influences the output operation of DC-DC converter circuit. Figure 5 shows the inductor current waveform at I_{ref}= 0.7 A.

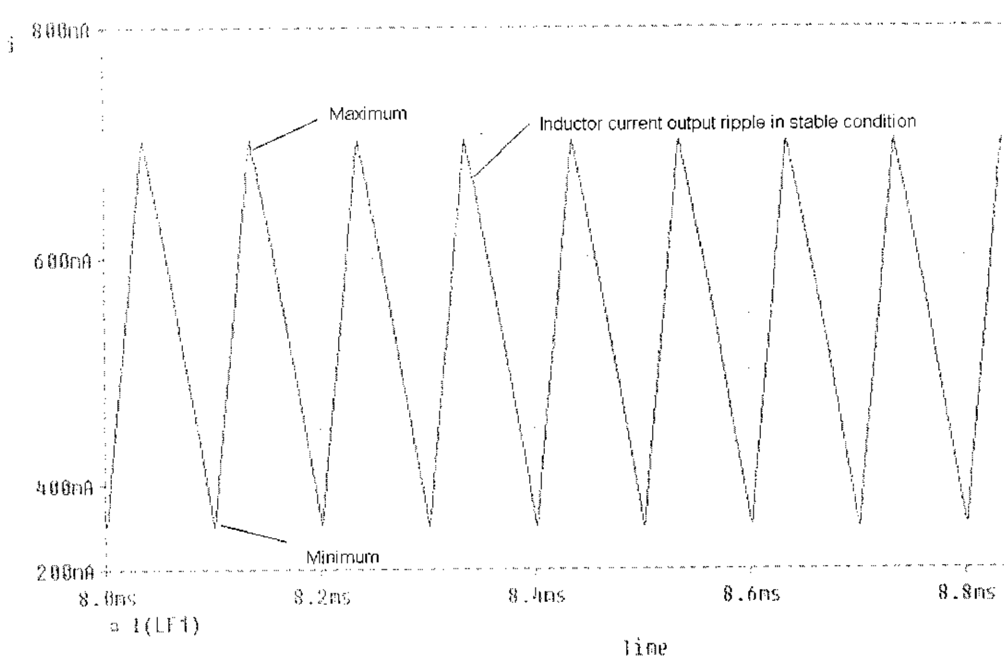


Figure 6: Inductor current response at I_{ref}=0.7 A.

Continuous conduction waveform in Figure 5 represents the output waveform of the inductor current in DC-DC boost converter. At this level of reference current neither vibration nor distortion can be found in the given circuit design. The output waveform operates in periodical mode, because the current repeats itself at each period.

Now, let's consider that the reference current changed to 5.5 A. At this magnitude of reference current the chaos operation can be observed. Because output waveform of the inductor current is totally distorted, this represents instable operation mode of the system. Figure 6 shows the output waveform of the inductor current.

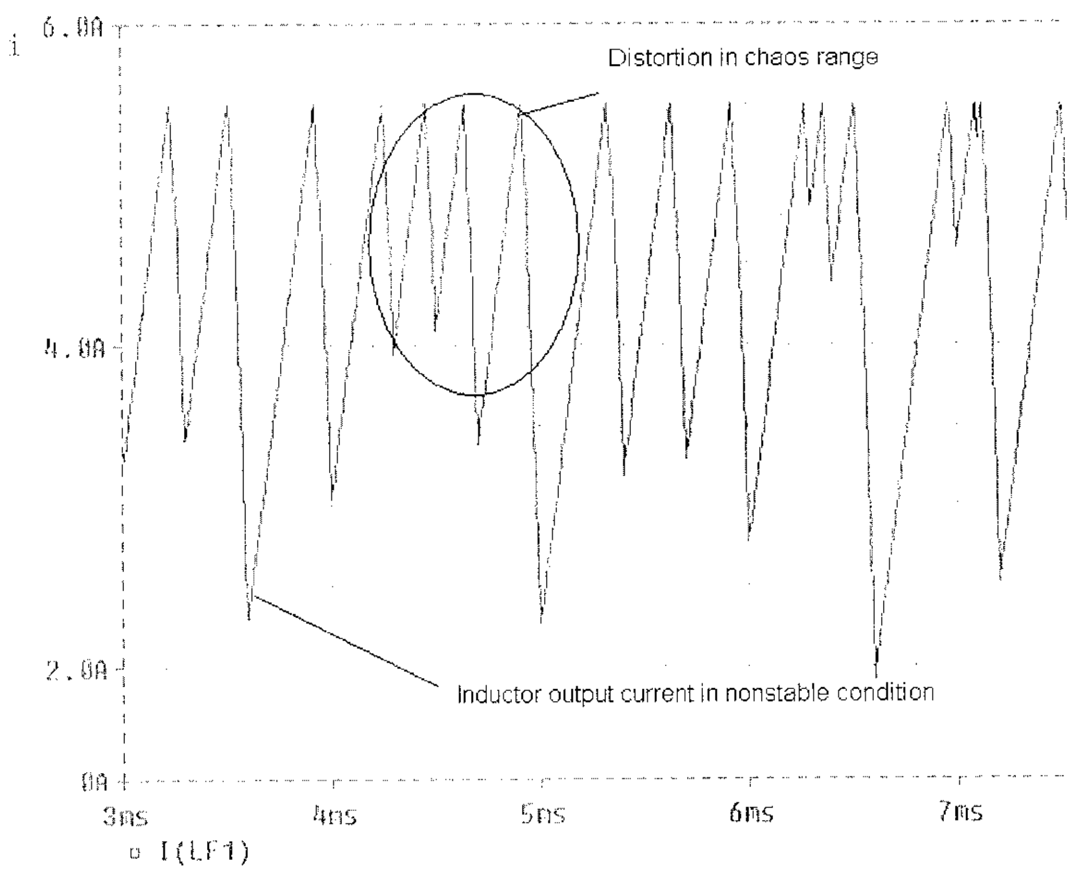


Figure 7: Inductor current response at I_{ref}=5.5 A

From inductor output waveform response (Figure 6), we can see that the system is in unstable operation mode. Because it is non-periodic and the current peak levels are vary with the time. At this reference current level we can find vibration and distortion in dc motor driving systems. This is undesirable condition in power electronics circuitry. This project focuses on cancellation of this distortion by using auxiliary circuit which will improve the operation mode of DC-DC boost converter. If we are going to compare these to output graphs; first we have to mention the current level of the waveforms, the second why this current level changes when reference current varies. These questions can be easily answered by looking and understanding the operation concept of the boost converter. When I reference current increases, it raises the conduction period of the inductor, as result inductor having more current charged. The output current and voltage levels vary according proportionally to reference current.

3.4 Printed Circuit Board Design

Short for Printed Circuit Board, PCB is a board made of plastic or fiberglass designed to hold electronic circuits, ICs, switches and other components. A good example of a PCB found in all computers today is the computer motherboard. It is required to examine every step of the design process; including schematic packaging, component placement, interconnect routing and manufacturing data generation. PSpice simulation software was used for this design.

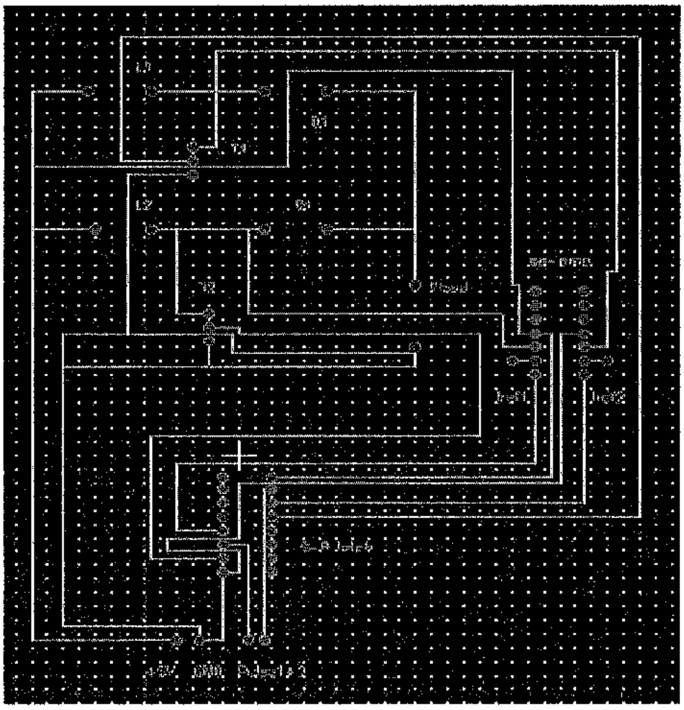


Figure 8: PCB outline for the DC-DC Boost Converter

DC-DC Boost converter PCB (Printed Circuit Board) outline is given in the Figure 7. This is initial design of this project if any changes or modifications occurred during soldering process this circuit might change. Besides, this project also includes receiver and transmitter circuit boards. Transmitter can be used as remote control because it has fixed 38 Mhz frequency. Receiver circuit board designed by using PSpice software program. The main problem in this design is a lack of components in the electronics store. Therefore it was required to buy all the components from the Ipoh electronics shops.

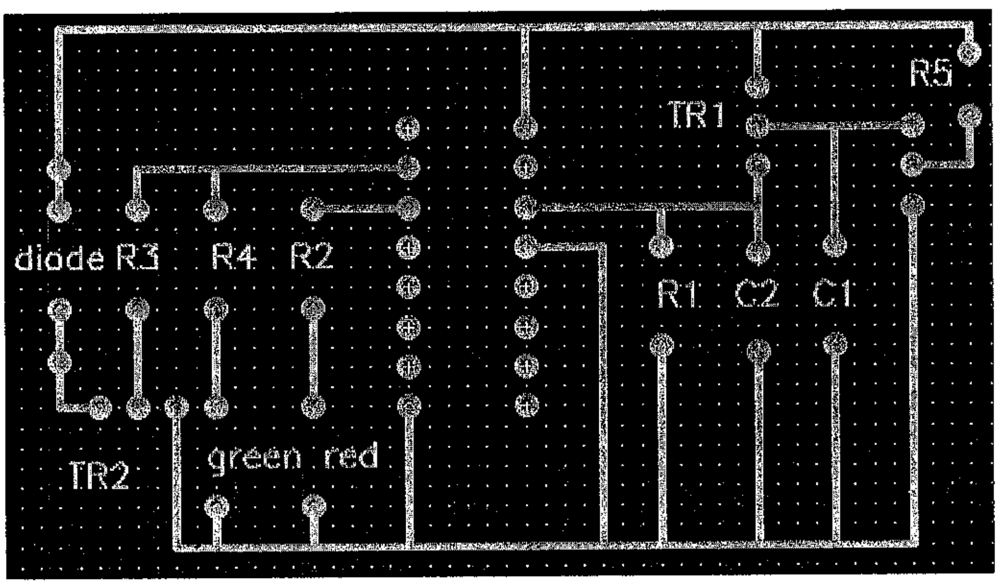


Figure 9: Receiver Printed Circuit Board outline.

As it can be seen form Figure 9, receiver printed circuit board pin layout was obtained by using PSpice software. Receiver and Transmitter circuit combination can be bought as a ready kit from electronics shops, but it will not be beneficial for personal skill performances.

CHAPTER 4

CALCULATION AND RESULTS

This section shows the steps and mathematical expressions to design a single input and single output Boost Converter which is in Continuous Conduction Mode. Since the input here is dc, which comes from voltage generator, these devices are normally operated at much higher frequency than the line frequency, reaching as high as a few hundred kilo-hertz. This calculation section consists of two parts. The first part is to design boost converter and the second part to investigate whether system is stable or not.

The main steps for the first part; to get right L and C components to control the capacitor voltage ripple.

Given:

$V_{in} = 5Volts;$

$V_{out} = 8Volts$

$\frac{\Delta V_c}{V_0} = 3\%$

$R = 20ohm$

$f_s = 40kHz$

Design CCM (Continuous Conduction Mode) Boost Converter.

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \qquad \text{......... (Equation 1)}$$

$$\frac{8}{5} = \frac{1}{1-D}$$

$$1-D = \frac{5}{8}$$

$$D = 0.375 = 37.5\%$$

$$L_{crit} = \frac{RT}{2}(1-D)^2 D$$ .... (Equation 2)

$$L_{crit} = \frac{20 \times 25\mu}{2}(1-0.375)^2 0.375$$

$$L_{crit} = 36.62\,\mu H$$

To satisfy Continuous Conduction Mode DC-DC boot converter property, L_{used} must be larger than L_{crit} value. Therefore, L_{used} equals to hundred times L_{crit} value. Otherwise, it will operate as Discrete Conduction Mode which is out of project objectives.

$$L_{used} = L_{crit} \times 100 = 3.662mH$$

$$I_{L\min} = V_{in}\left[\frac{1}{R(1-D)^2} - \frac{DT}{2L}\right] = 5[0.128 - 1.28m]$$ .... (Equation 3)

$$I_{L\min} = 0.633A$$

$$I_{L\max} = V_{in}\left[\frac{1}{R(1-D)^2} + \frac{DT}{2L}\right] = 5[0.128 + 1.28m]$$ .... (Equation 4)

$$I_{L\max} = 0.646A$$

For the positive values of $I_{L\max}$ and $I_{L\min}$, the converter will operate in the Continuous Conduction Mode and the given system is stable.

The voltage ripple is given by

$$\frac{\Delta V_c}{V_o} = 3\% = \frac{D}{RCf}$$ .... (Equation 5)

$$0.03 = \frac{0.375}{20 \times C \times 40\ kHz}$$

$$C = 15.62\ \mu F$$

$$I_0 = \left[\frac{I_{L\max} + I_{L\min}}{2}\right](1-D) = \frac{0.6464 + 0.633}{2}(1-0.375) = 0.3998A$$ .... (Equation 6)

$$I_{in} = \left[\frac{I_{L\max} + I_{L\min}}{2}\right] = \frac{0.6464 + 0.633}{2} = 0.6397A$$ .... (Equation 7)

Inductor ripple is given by

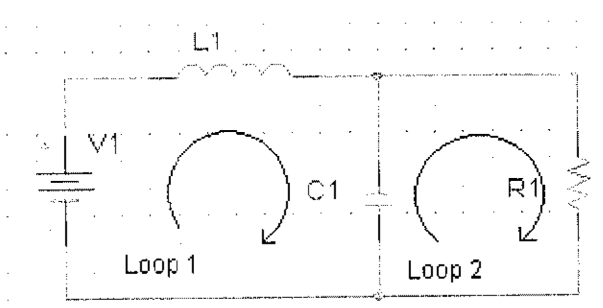
$$\Delta I = \frac{1}{L} V_{in} DT = \frac{1}{2.92m}(5)(0.375)(25\mu) = 0.016A$$

Table 1: Designed Boost Converter components.

Circuit Components	Values
Switching period T	25 μs
Input voltage V_1	5 V
Inductance L_1	3.662mH
Inductance L_2	3.662mH
Capacitance C_1	15.62 μF
Capacitance C_2	15.62 μF
Load Resistance R	20 Ω

Boost Converter Configuration

As it was mentioned before, this is a stable system. This calculation conducted to prove the stability of this system. Stability is the most important system specification. If a system is unstable, transient response and steady state errors are moot points. An unstable system can not be designed for a specific transient response or steady state error requirement. This is very important to achieve stable operation of the system.



Two loops were obtained by using the Mesh's loop method;

$$V(s) = LsI_1(s) + \frac{1}{Cs}I_1(s) - \frac{1}{Cs}I_2(s) ----loop1$$

$$0 = \frac{1}{Cs}I_2(s) + RI_2(s) - \frac{1}{Cs}I_1(s) ----loop2$$

$$V(s) = (Ls + \frac{1}{Cs})I_1(s) - \frac{1}{Cs}I_2(s) ----loop1$$

$$0 = (\frac{1}{Cs} + R)I_2(s) - \frac{1}{Cs}I_1(s) ----loop2$$

Both loops in the matrix form;

$$\begin{bmatrix} (Ls + \frac{1}{Cs}) & -\frac{1}{Cs} \\ -\frac{1}{Cs} & (\frac{1}{Cs} + R) \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = \begin{bmatrix} V(s) \\ 0 \end{bmatrix}$$

$$\Delta = (Ls + \frac{1}{Cs})(\frac{1}{Cs} + R) - (\frac{1}{Cs})(\frac{1}{Cs}) = \frac{L}{C} + LsR + \frac{1}{C^2s^2} + \frac{R}{Cs} - \frac{1}{C^2s^2}$$

$$\Delta = \frac{Ls + Ls^2CR + R}{Cs}$$

$$\Delta_1 = \begin{bmatrix} V(s) & -\frac{1}{Cs} \\ 0 & \frac{1}{Cs} + R \end{bmatrix} = V(s)(\frac{1}{Cs} + R)$$

$$\Delta_2 = \begin{bmatrix} (Ls + \frac{1}{Cs}) & V(s) \\ -\frac{1}{Cs} & 0 \end{bmatrix} = \frac{V(s)}{Cs}$$

$$I_1 = \frac{\Delta_1}{\Delta} = \frac{V(s)(\frac{1}{Cs} + R)(Cs)}{Ls^2CR + Ls + R}$$

$$I_2 = \frac{\Delta_2}{\Delta} = \frac{V(s)}{\frac{Cs(Ls^2CR + Ls + R)}{Cs}} = \frac{V(s)}{Ls^2CR + Ls + R}$$

V(s) is the input voltage

I_2 is the output of the system

Open loop Transfer function G(s) is given by

$$G(s) = \frac{I_2(s)}{V(s)} = \frac{1}{Ls^2CR + Ls + R}$$

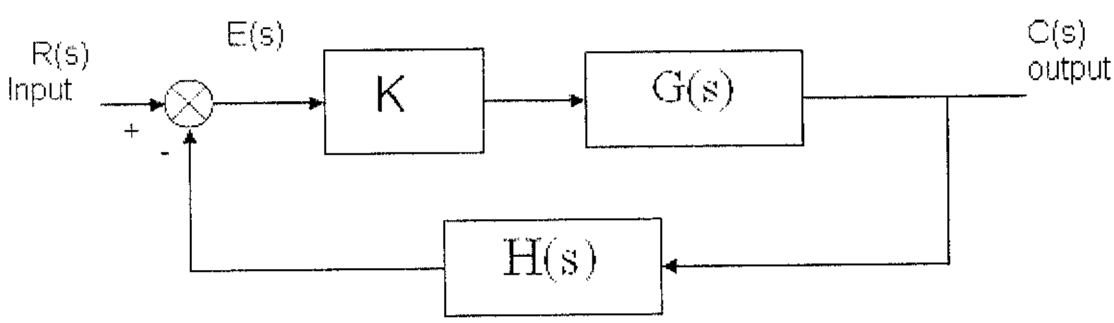


Figure 10: Close loop with unity feedback system

The close loop with unity feedback system is shown in figure 7. K is the gain factor of the system and H(s) is the feedback loop of the system. Furthermore, it is required to calculate the value for gain (K) and show the poles locations by indicating the stability of the system.

$$G(s)=\frac{1}{s^2(3.662m)(15.62u)(20)+(3.662m)s+20}$$

$$G(s)=\frac{1}{s^2(1.444u)+(3.662m)s+20}$$

Thus, Close Loop Transfer Function T(s) of the system is

$$T(s)=\frac{G(s)}{1+G(s)H(s)}=\frac{1}{(1.144\mu)s^2+(3.662m)s+21}$$

Table 2: Stability verification

S^2	**1.144u**	**21**
S^1	**3.662m**	**0**
S^0	**21**	**0**

Closed loop transfer function has all poles in the left half of the s-plane, the system is stable. Thus, a system is stable if there are no sign changes in the first column of the Routh table. The system can not have jw poles since a row of zeros did not appear in the Routh table.

From second order general equation

$$G(s)=\frac{W_n^2}{s^2+2(\zeta W_n)s+W_n^2}$$

$K=4181^2=W_n^2$

$W_n=4181$

Damping Ratio:

$$\zeta=\frac{\frac{2536}{2}}{41810}=0.3032$$

$0<\zeta<1$ System is Underdamped

$\sigma = -\zeta W_n = -1267.6$ **Real axis**

$jWn\sqrt{1-\zeta^2} = 3984j$ **Imaginary axis**

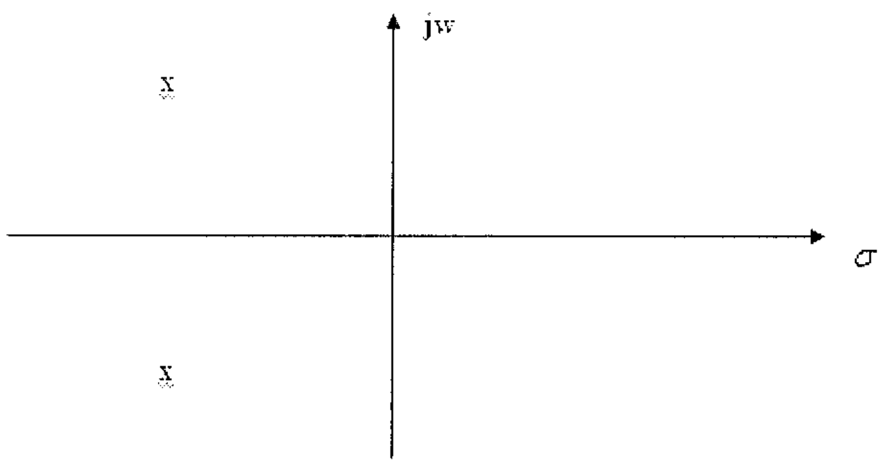


Figure 11: Underdamped system poles location

Location of the poles clearly indicated in the figure 8. It can be concluded that the system is stable and having overshoot at the output waveform which satisfy to underdamped system operation.

Peak Time

$$T_p = \frac{\pi}{W_n\sqrt{1-\zeta^2}} = 788\mu\sec \qquad \text{......... (Equation 8)}$$

Settling Time

$$T_s = \frac{-\ln(0.02\sqrt{1-\zeta^2})}{(\zeta)(W_n)} = 3.123m\sec \qquad \text{......... (Equation 9)}$$

System Percentage Overshoot

$\%OS = e^{-(\pi\zeta/\sqrt{1-\zeta^2})}x100 = 36.82\%$ .... (Equation 10)

Calculation results show that our designed boost converter satisfies stability aspect of the system. For this reason we can confidently use these parameters in designing boost converter. After proving the stability of the system, now we can proceed with simulation of the system.

Simulation Results

As it was mentioned before, this project operates in CCM (Continuous Conduction Mode). This can be seen from Figure 7., which provides output current ripple waveform of the inductor. Neither minimum nor maximum points are distorted which clearly correspond CCM mode operation of the designed circuit. Besides, maximum and minimum points are 693.734 mA and 684.015mA respectively.

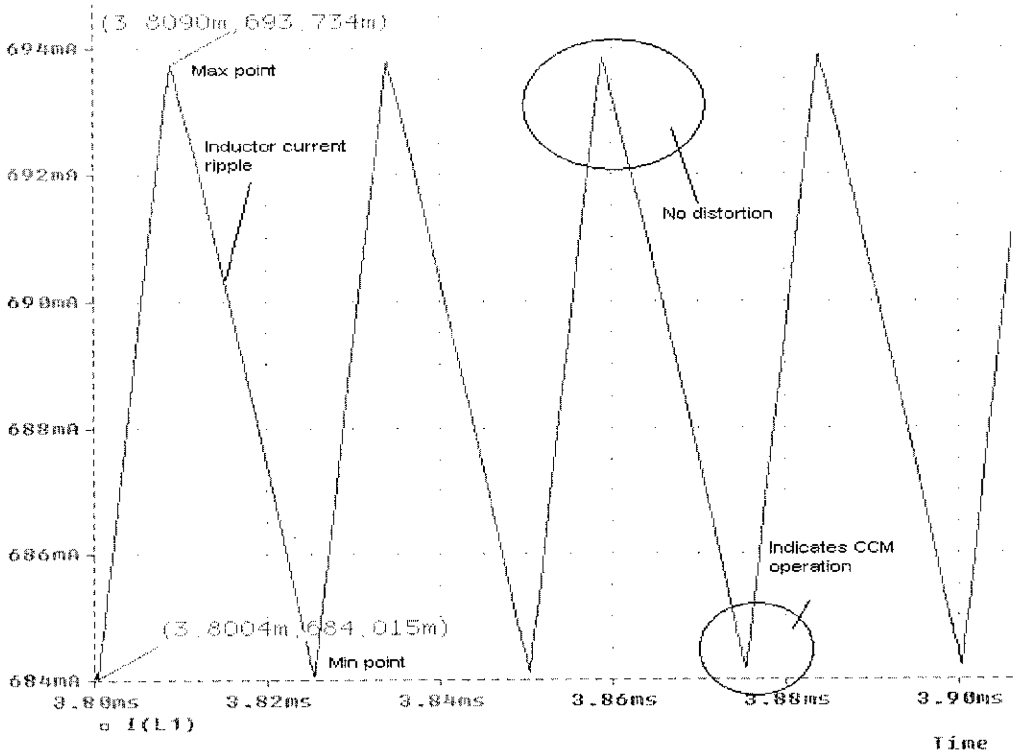


Figure 12: Inductor current ripple in actual design (I_{ref}=700mA)

This type configuration and parameter values reduces output current ripple from 64% (authors) [7] to 5 % (actual). It is important to mention that author uses high voltage boost converter system where input voltage 10 V boosted up to 60 V. Whereas, this project uses low voltage system, input 5 V boosted up to 8 V.

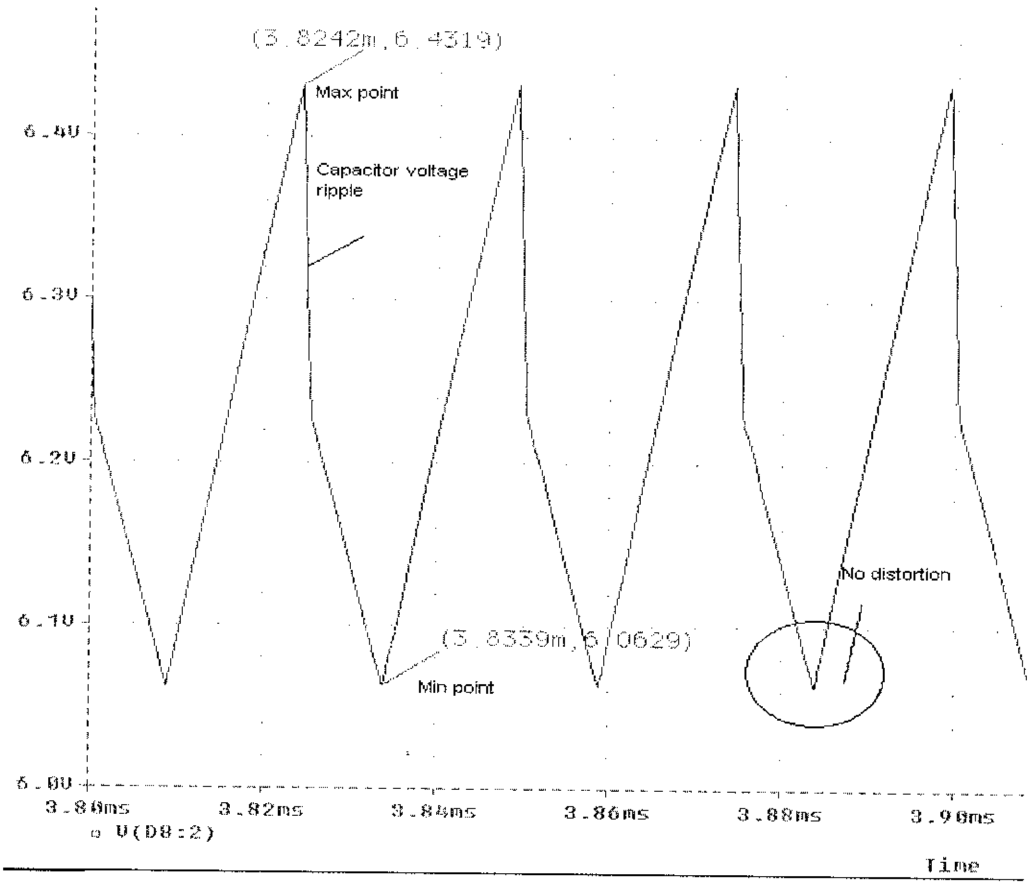


Figure 13: Capacitor output voltage ripple in actual design.(I_{ref}= 700 mA)

Capacitor output voltage ripple waveform is shown in Figure 8. above. The maximum and minimum points are 6.4319 V. and 6.0629 V. respectively. Shaded area indicates distortion less minimum and maximum output waveform ripple. The capacitor voltage ripple factor reduced from 30 % (authors) [7] to 3 % (actual). Reduction in output ripple gives good efficiency and better performance of the converter circuit. According to the theory of dual input-dual output boost converter the output voltage raises as reference current increases. Figure 13 shows that nominal voltage is at 6.25V for I_{ref} = 700 mA. According to our calculation output voltage should be 8 Volts but because of the wide range of reference current (500 mA - 1.5 A) and considering voltage drop on components we could not achieve in the simulation.

Experimentation Results

This section focuses on difference between theoretical and experimental results. The project implementation uses different parameters than calculated ones. The lack of components in the market gave us no choice but use close parameters for the inductor, transistor, and capacitor in the boost converter circuit. Alternative selection of the project components are shown in the Table 3.

Table 3: Difference between theoretical and experimental parameters

Circuit Components	Theoretical	Experimental
Inductance L_1	3.662mH	4.2mH
Inductance L_2	3.662mH	4.2mH
Capacitance C_1	15.62 μF	32 μF
Capacitance C_2	15.62 μF	32 μF

Regardless to components changes the system stability and continuous conduction mode of boost converter still maintained as before. Table 4. shows the load voltage response to different values of reference current. The load voltage must show increasing response. This verifies the correct operation of Current Controlled Boost converter.

Table 4: Boost converter load voltage response.

Applied Voltage Level (V)	$R_{reference}$ (ohms)	$I_{1reference}$ (mA)	$I_{2reference}$ (mA)	Load Voltage (V)
3	1000	3	3	9.780
3.5	1000	3.5	3.5	9.784
4	1000	4	4	9.786
4.5	1000	4.5	4.5	9.903
5	1000	5	5	9.955

The experimentation results shows that slight increase in reference current will affect the output of the system at the load. The voltage at the load should increasingly rise (see Table 4). Theoretically maximum output should be 8 V. but due to some components parameter changes the output of the system reaches around 10 V.

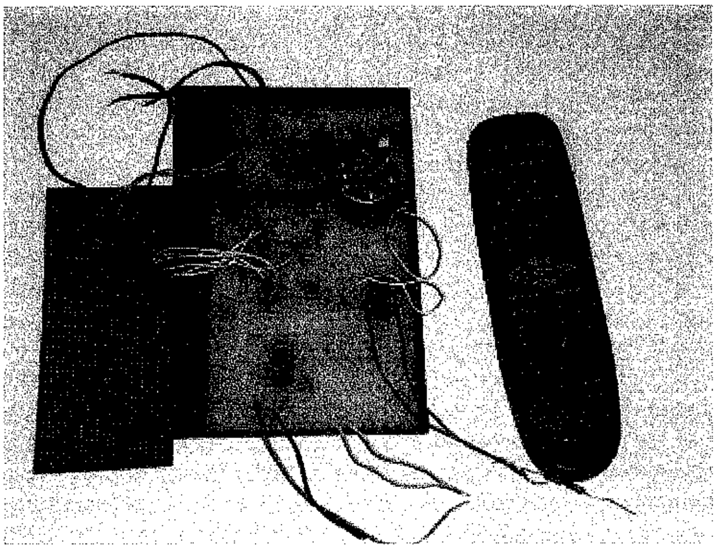


Figure 14: Project Printed Circuit Board Implementation

As it was mentioned before the project consists of two parts.

- Receiver and Transmitter
- Current Controlled Boost Converter.

Receiver and Transmitter

The main objective of this circuit is to activate the boost converter circuit. Infrared Remote controller used as transmitter circuit which can initiate process within 7 meter radius. IR controller uses 38 MHz frequency (see Figure 14).

Current Controlled Boost Converter.

This is the main and significant part of the project. Where input 5 V. increase or boosted until 8 V. it is also important to note that this circuit controlled and varied by reference current level.

CHAPTER 5
DISCUSSION

For the proposed system shown in Figure 3, the switching is controlled by a feedback path consisting of a comparator and a flip-flop. Each comparator compares the corresponding current through the inductor with a reference current I_{ref}. The mapping is a function that relates the voltage and current vector (v_{n+1}, i_{n+1}) sampled at one instant, to the vector (v_n, i_n) at a previous instant; the instants in question are the arrival of a triggering clock pulse. For the proposed converter, calculated values for inductor (L) and capacitor (C) are different from the author's circuit design parameters (refer to table 1). These two component parameters deeply effect the boost converter operation. For example, CCM (Continuous Conduction Mode) and DCM (Discrete Conduction Mode) and output ripple of the inductor current depends on inductor parameter. This design concentrates on CCM operation rather than DCM. This can be seen from figure 7., which is indicated with circle. In CCM operation minimum current value can not be zero whereas in DCM operation the minimum current level at zero. Beside this, the capacitor voltage factor can be manipulated by varying the capacitor parameter. According to Al-Mothofar M.R.[7] circuit configuration, the large voltage ripple at the capacitor and inductor were achieved. The author's component parameters (see Appendix-B) give large ripple at the output waveforms for the inductor current and capacitor voltage. The capacitor voltage ripple factor reduced from 30%(authors) to 3%(actual) and output current ripple from 20%(Al Mothofar M.R.[7]) to 3%(according to my calculation).

To check the validity of the theoretical modeling, PSpice circuit analysis program has been employed. In the inductor current and capacitor voltage output waveforms for different values of control parameter I_{ref} = 0.7, 1.3, 1.5, and 5.5 A. To compare different regulator systems with different compensation networks, the control (design) parameter should be independent from the compensator design. A good choice would be either the input voltage V_I or the load resistance R. Hence we repeated the calculations for the same feedback system with the input voltage as the control parameter.

CHAPTER 6
CONCLUSION

This project is to design a circuit which will guarantee stable operation at switching frequencies, and any quasi-periodic or chaotic operation is regarded as being undesirable and should be avoided. This project has focused in particular on the application of bifurcation theory to parallel-input / parallel-output two-module current-programmed DC-DC converters. The nonlinear mapping that describes the boost converter under current-mode control in continuous conduction mode has been derived. Beside this project paper describes the operation of Current Mode Controlled Parallel-Connected Boost DC-DC Converters and basically defines chaos, bifurcation and quasi-periodic distortion of the circuit by varying the reference current and comparing it with inductor output current. Within specific ranges of reference current the circuit operates without any distortion.

The design includes the simulation of any bifurcation within the intended operation range by using PSpice, Multisim and EWB software. The inductor current output waveforms obtained and compared at different levels of reference currents. From output waveforms I observe that at fundamental frequency designed circuit operates in stable mode which is periodic. But changing reference current magnitude to 5.5 amp causes chaos in output waveform of the inductor current. In chaos operation peak of the inductor current are changing with the time which shows the unstable behavior and non-periodic output waveform. There are a few ways to improve the output waveforms such as connecting freewheeling diode with parallel to inductor, using combination of triple input/triple output Current Mode Controlled converter or just using parallel input/series output configuration. Each of these configurations must be investigated in this project paper to come out with the final DC-DC boost converter.

Much of the work in the study of nonlinear phenomena of power electronics circuits and systems has been focused on basic research into the bifurcation and chaotic behavior of power converters under variation of some selected parameters. Parallel-input / parallel-output are the most common configuration that can be used in current mode control DC-DC converters. Simulation results shows that capacitor voltage ripple factor reduced from 30% to 3%(actual) and output current ripple from 20% to 3%. Improvement in this type of converter will open up new applications in datacommunication, telecommunication, power-supply in pc and inside the notebook, industrial automation and so forth. The core of the project work focuses on simulating the entire process and later building the prototype. The design performance will also be evaluated based on output results.

REFERENCES

[1] Deane, Jonathan H.B., and David C. Hamill, Instability, Subharmonics, and Chaos in Power Electronic Systems, PESC'89, IEEE Power Electronics Specialists Conference, 1989, pp. 34-42.

[2] Deane, J. H. B. and Hamill, D. C., "Chaotic Behavior In Current Mode Controlled DC-DC Converter, "Electronics Letters", Vol. 27, No. 13, 20th June 1991, pp. 1172-1173.

[3] Iu, H. H. C., and Tse, C. K., "Bifurcation Behavior in Parallel-Connected Buck Converters," IEEE Transactions on Circuits and systems-1: Fundamental Theory and Applications, Vol. 48. No. 2, February 2001, pp. 2

[4] Brocket, R. W. and wood, J. R., "Understanding power converter chaotic behavior mechanisms in protective and abnormal modes," Proceedings of the Powercon, Vol. 11, No. 4, 1984, pp. 1-15.

[5] Deane, J. H. B. and Hamill, D. C., "Instability, Subharmonics and Chaos in PE circuits," IEEE Transactions on Power Electronics, Vol. 5, 1990, pp. 260 – 268.

[6] Al-Fayyoumi, M., "Nonlinear Dynamics and Interactions in Power Electronic systems," M. E. dissertation Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Virginia, 1998.

[7] Al-Mothafar, M. R., "Small-Signal and Transient Behavior of Two-Module DC-DC Converter Using Mutually Coupled Output Filter Inductors," Int. J. Electronics, Vol. 79, No. 6, 1995, pp. 917-932.

[8] http://www.ibiblio.org/e-notes/MSet/Orbit2.htm Internet web page. Theory of period doubling bifurcation.

APPENDICES

Appendix –A: Chronological list of the activities

FYP1

a. Assess and select the software best suited for the project.
b. Study the software manuals/documentation, focusing on simulation exercises.
c. Prepare and write the progress report.
d. Simulate the current controlled dc/dc converter of the project.
e. Run and troubleshoot the simulation.
f. Research/Decide component parameters based on simulation output.
g. Research on how to select the right component for a particular process.
h. Perform design calculations for subharmonics, quasi-periodic or chaotic operation.
i. Specify and order parts for the prototype.
j. Prepare and write the interim report.
k. Prepare for an oral presentation.

FYP2

l. Prepare and write the progress report 1.
m. Test the validity of the design and the accuracy of the operation
n. Finalize the project PCB Gerber files
o. Build the prototype.
p. Prepare and write the progress report 2.
q. Interface the with the prototype
r. Test and troubleshoot the prototype
s. Exhibition.
t. Prepare and write the dissertation.
u. Prepare for an oral presentation.

Appendix –B: Tools and Materials Required

The following is list of initial materials and tools necessary to complete the project. Note that the materials are mentioned without detailed purchasing data. This data will be provided at a later stage, after design calculations.

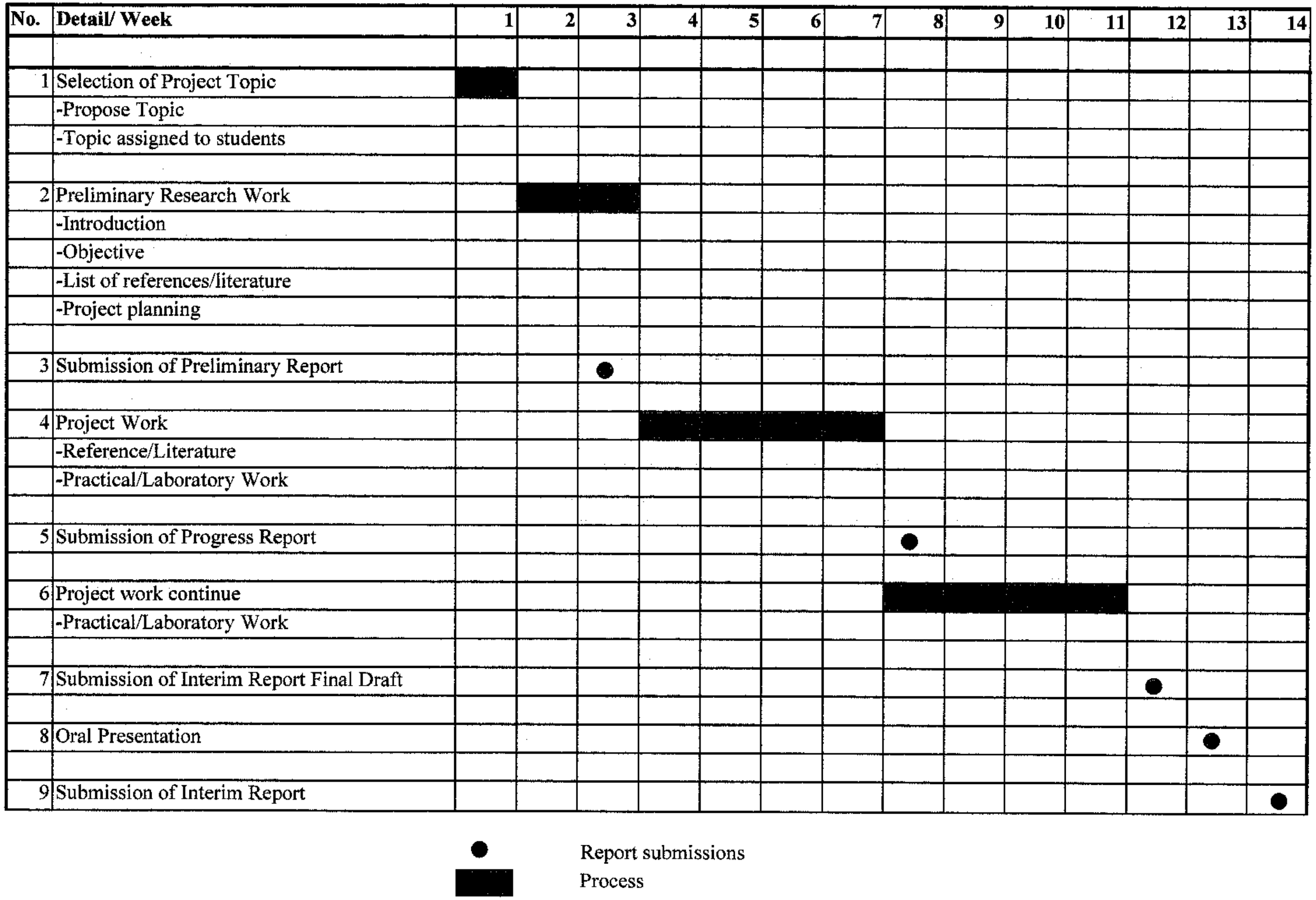
a. Simulation software for design simulation.
b. A personal computer that can support the software in (a).
c. Two flip-flops
d. Two inductors
e. Two capacitors
f. Two comparators
g. Diodes

Circuit Components	Values
Switching period T	100 μs
Input voltage V_1	10 V
Inductance L_1	1mH
Inductance L_2	1mH
Capacitance C_1	10 μF
Capacitance C_2	10 μF
Load Resistance R	20 Ω

Table 5: Circuit components and values

Appendix C: Gantt Charts

Gantt chart for the First Semester of 2 Semester Final Year Project



Gantt chart for the Second Semester of 2 Semester Final Year Project

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Project Work Continue		■	■											
	-Practical/Laboratory Work														
2	Submission of Progress Report 1			●											
3	Project Work Continue				■	■	■	■							
	-Practical/Laboratory Work														
4	Submission of Progress Report 2								●						
5	Project work continue								■	■	■	■			
	-Practical/Laboratory Work														
6	Submission of Dissertation Final Draft												●		
7	Oral Presentation													●	
8	Submission of Project Dissertation														●

● Report submissions

■ Process

Appendix D: Data sheets

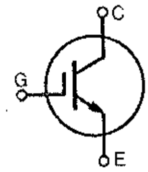
IXYS Advance Technical Data

liPerFAST™ IGBT

IXGH 40N60B2
IXGT 40N60B2

V_{CES}	=	600 V
I_{C25}	=	75 A
$V_{CE(sat)}$	<	1.7 V
$t_{fi\,typ}$	=	82 ns

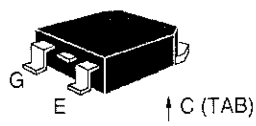
ptimized for 10-25 KHz hard vitching and up to 150 KHz sonant switching



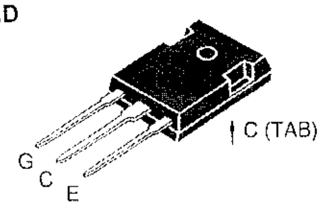
'mbol	Test Conditions	Maximum Ratings	
:ES	T_J = 25°C to 150°C	600	V
:GR	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
;ES	Continuous	±20	V
;EM	Transient	±30	V
5	T_C = 25°C (limited by leads)	75	A
10	T_C = 110°C	40	A
1	T_C = 25°C, 1 ms	200	A
3OA :BSOA)	V_{GE} = 15 V, T_{VJ} = 125°C, R_G = 10 Ω Clamped inductive load @ ≤ 600 V	I_{CM} = 80	A
:	T_C = 25°C	300	W
I		-55 ... +150	°C
IM		150	°C
tg		-55 ... +150	°C
aximum lead temperature for soldering 6 mm (0.062 in.) from case for 10 s		300	°C
d	Mounting torque (M3)	1.13/10 Nm/lb.in.	
/eight	TO-247 AD	6	g
	TO-268 SMD	4	g

ymbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
GE(th)	I_C = 250 μA, V_{CE} = V_{GE}		3.0		5.0	V
:ES	V_{CE} = V_{CES} V_{GE} = 0 V	T_J = 25°C T_J = 150°C			50 1	μA mA
;ES	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
CE(sat)	I_C = 30 A, V_{GE} = 15 V	T_J = 25°C			1.7	V

TO-268 (IXGT)



TO-247 AD (IXGH)



G = Gate, C = Collector,
E = Emitter, TAB = Collector

Features

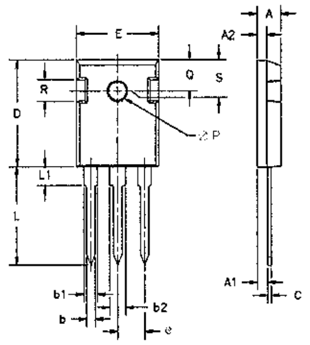
- Medium frequency IGBT
- Square RBSOA
- High current handling capability
- MOS Gate turn-on
  - drive simplicity

Applications

- PFC circuits
- Uninterruptible power supplies (UPS)
- Switched-mode and resonant-mode power supplies
- AC motor speed control
- DC servo and robot drives
- DC choppers

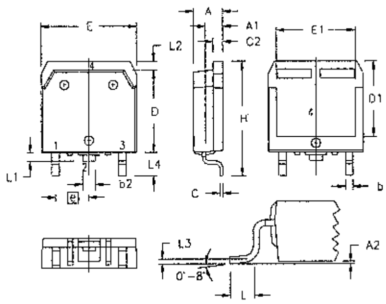
Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_C = 30 A; V_{CE} = 10 V, Pulse test, t ≤ 300 µs, duty cycle ≤ 2 %	20	36		S
V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		2560		pF
		180		pF
		54		pF
I_C = 30 A, V_{GE} = 15 V, V_{CE} = 300 V		100		nC
		15		nC
		36		nC
Inductive load, T_J = 25°C I_C = 30 A, V_{GE} = 15 V V_{CE} = 400 V, R_G = 3.3 Ω		18		ns
		20		ns
		130	200	ns
		82	150	ns
		0.4	0.8	mJ
Inductive load, T_J = 125°C I_C = 30 A, V_{GE} = 15 V V_{CE} = 400 V, R_G = 3.3 Ω		18		ns
		20		ns
		0.3		mJ
		240		ns
		150		ns
		1.10		mJ
			0.42	K/W
(TO-247)		0.25		K/W

TO-247 AD Outline



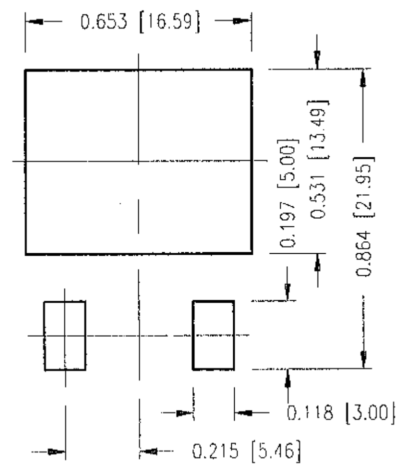
Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

TO-268 Outline



SYM	INCHES MIN	MAX	MILLIMETERS MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

ommended Footprint
ons in inches and mm)



'ves the right to change limits, test conditions, and dimensions.

's and IGBTs are covered by one or more U.S. patents: 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343

Fig. 1. Output Characteristics @ 25 Deg. C

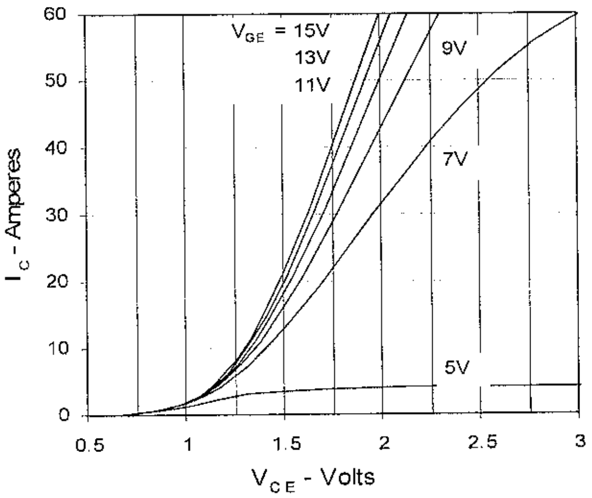


Fig. 2. Extended Output Characteristics @ 25 deg. C

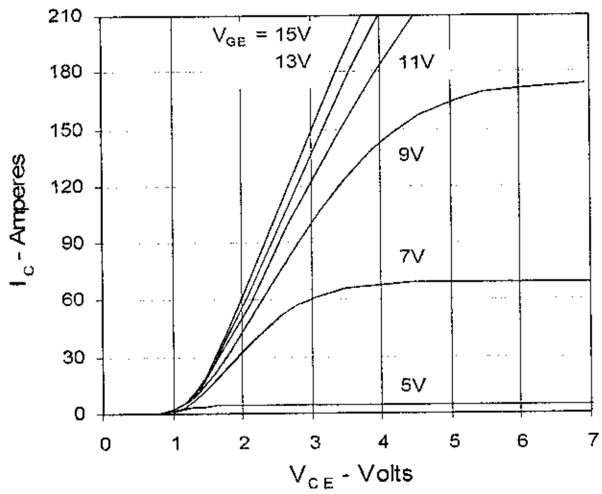


Fig. 3. Output Characteristics @ 125 Deg. C

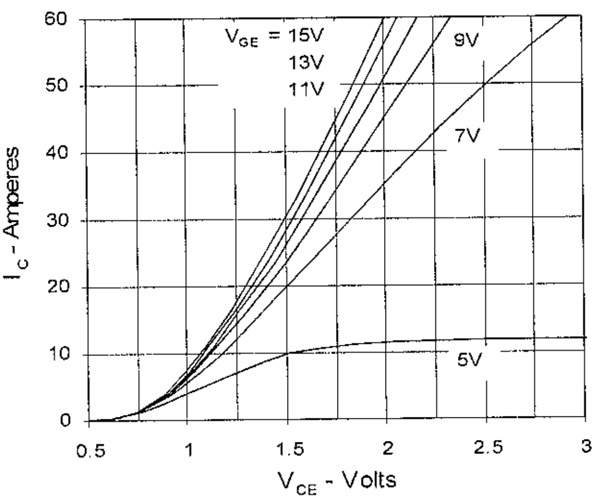


Fig. 4. Dependence of $V_{CE(sat)}$ on Temperature

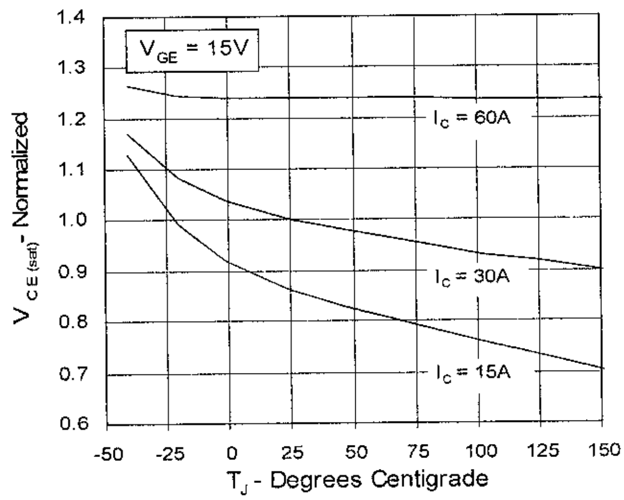


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter voltage

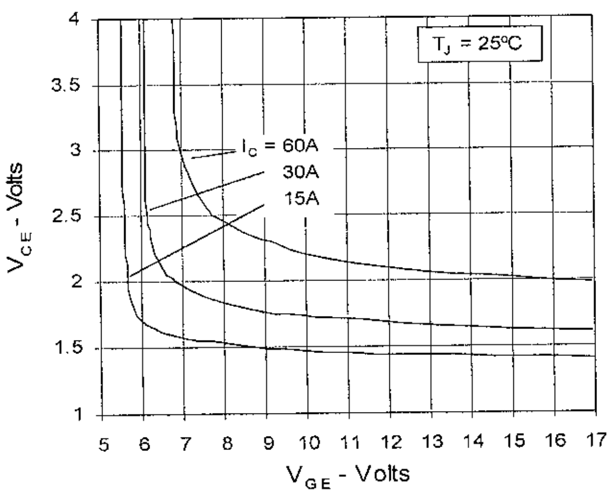


Fig. 6. Input Admittance

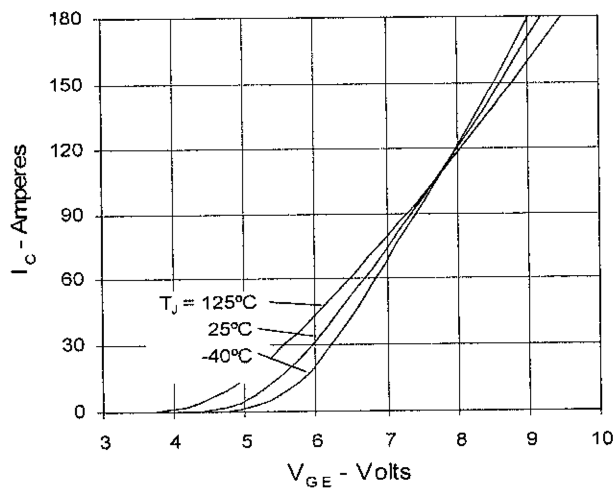


Fig. 7. Transconductance

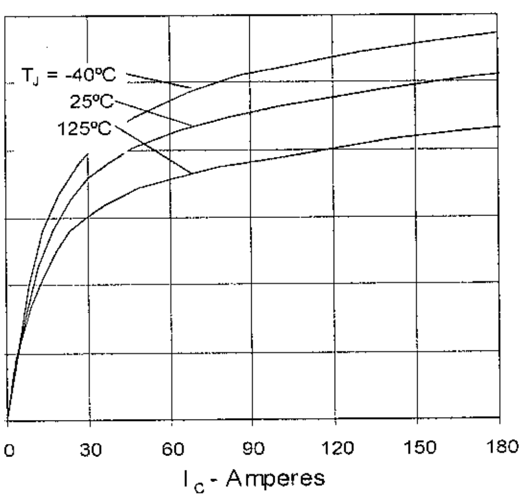


Fig. 8. Dependence of Turn-Off Energy on R_G

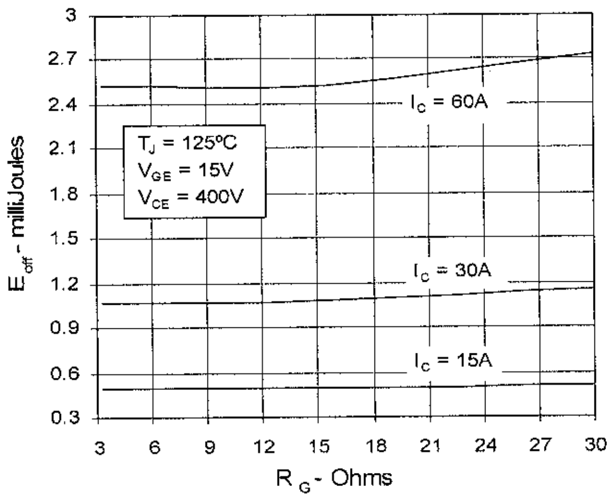


Fig. 9. Dependence of Turn-Off Energy on I_c

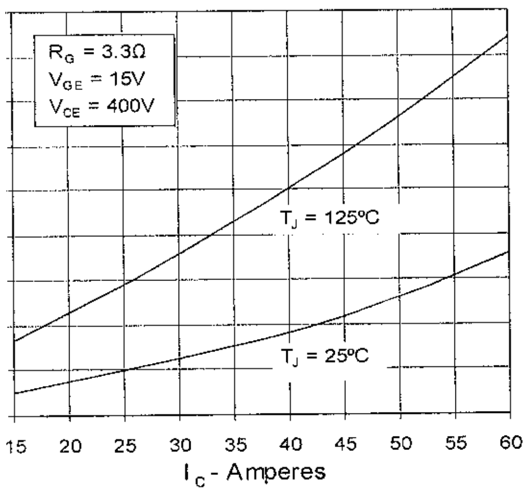


Fig. 10. Dependence of Turn-Off Energy on Temperature

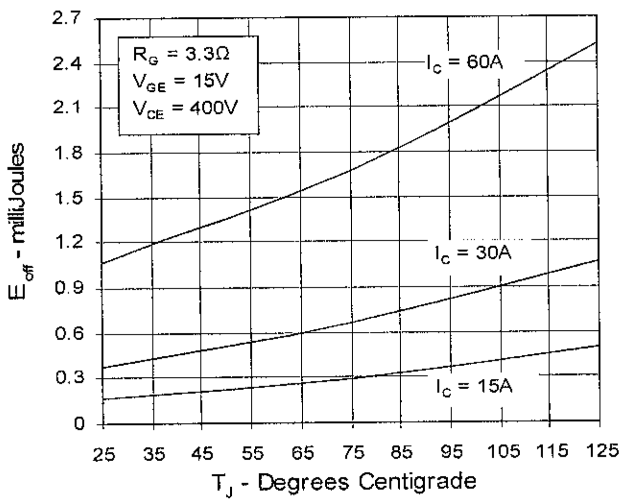


Fig. 11. Dependence of Turn-Off Switching Time on R_G

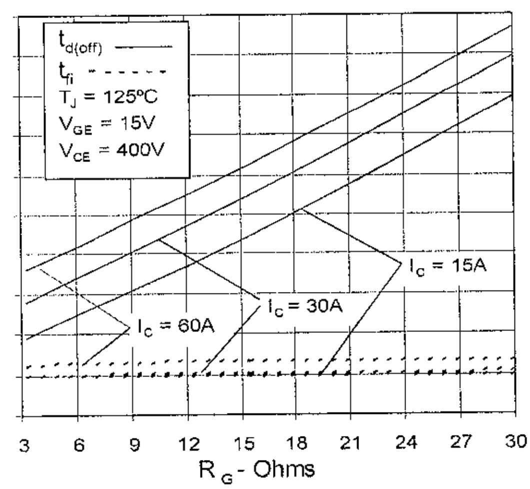


Fig. 12. Dependence of Turn-Off Switching Time on I_c

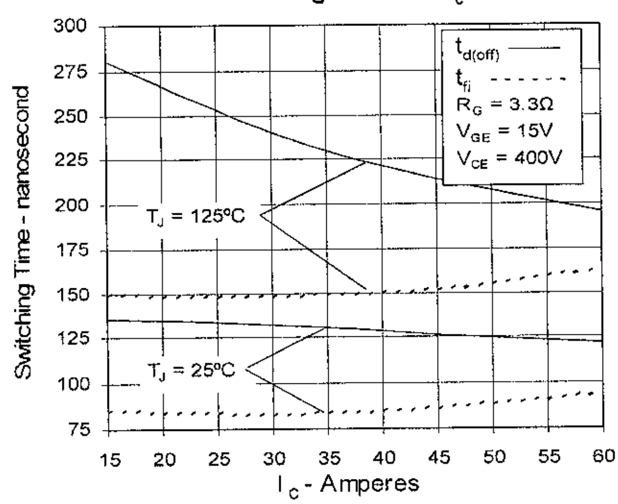


Fig. 13. Dependence of Turn-Off Switching Time on Temperature

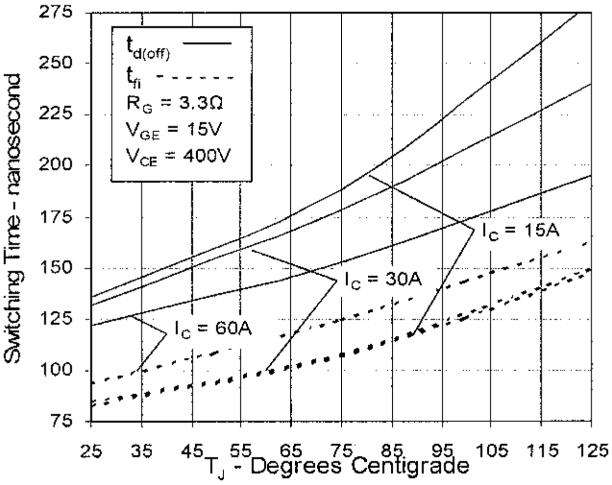


Fig. 14. Gate Charge

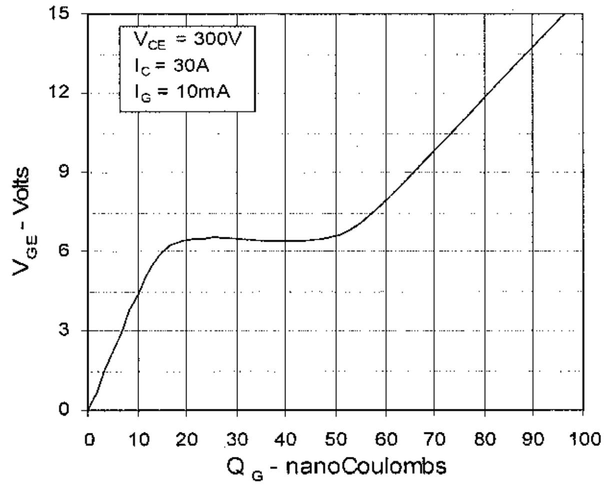


Fig. 15. Capacitance

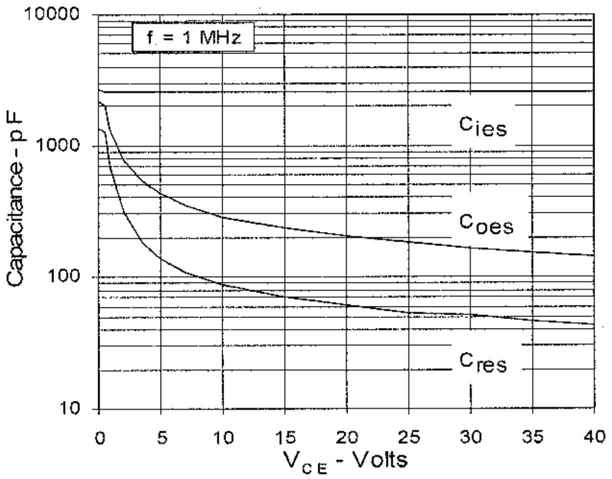
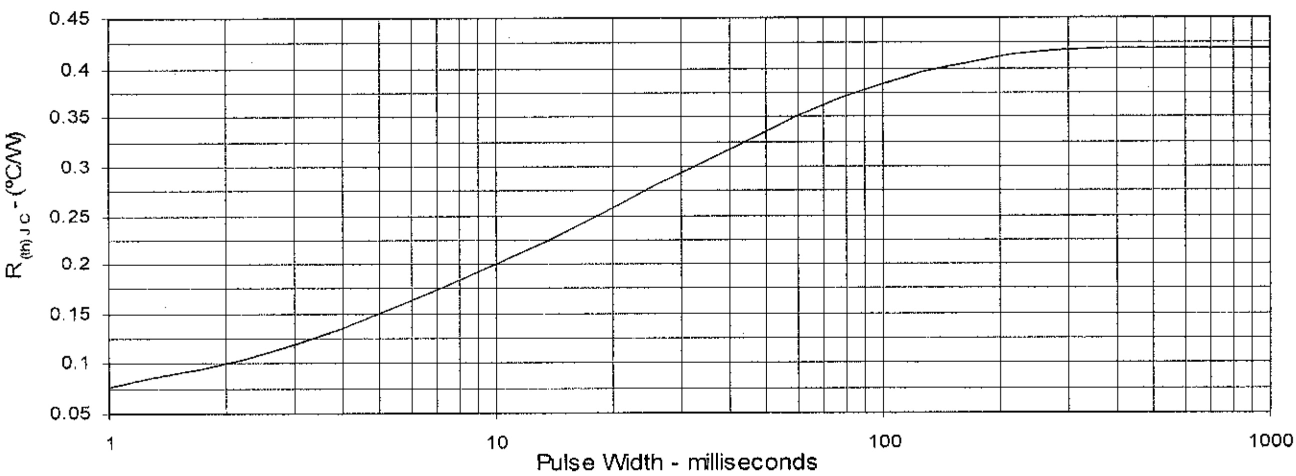
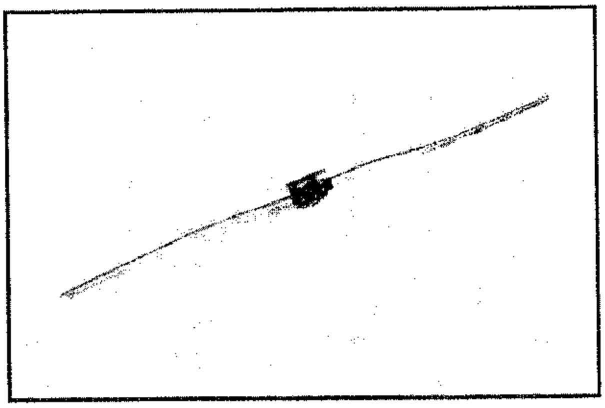


Fig. 16. Maximum Transient Thermal Resistance



1N4001 Thru 1N4007

AMP PLASTIC SILICON RECTIFIER

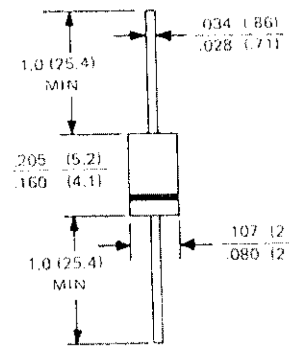


FEATURES

- Rating to 1000V PRV
- Low cost
- Diffused junction
- Low leakage
- Low forward voltage drop
- High current capability
- Easily cleaned with freon, alcohol, chlorothene and similar solvents
- UL recognized 94V-O plastic material

Outline Drawing

DO-41



Dimensions in inches and (millimeters)

Mechanical Data

- Case: JEDEC DO-41
- Terminals: Axial leads, solderable per MIL-STD-202, Method 208
- Polarity: Color band denotes cathode
- Weight: 0.012 ounce, 0.3 grams
- Mounting Position: Any

Maximum Ratings & Characteristics

- Ratings at 25° C ambient temperature unless otherwise specified
- Single phase, half wave, 60Hz, resistive or inductive load
- For capacitive load, derate current by 20%

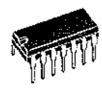
		1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Units
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	V_{RMS}	35	70	140	280	420	560	700	V
Maximum DC Blocking Voltage	V_{DC}	50	100	200	400	600	800	1000	V
Maximum Average Forward Rectified Current .375 (9.5mm) Lead Lengths @ T_A = 75° C	$I_{(AV)}$	1.0							A
Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave Superimposed On Rated Load	I_{FSM}	40							A
Maximum Forward Voltage At 1.0A DC	V_F	1.0							V
Maximum DC Reverse Current @ T_A = 25°C At Rated DC Blocking Voltage @ T_A = 100°C	I_R	5 50							μA
Typical Junction Capacitance (Note 1) T_A = 25° C	C_J	15							pF
Typical Thermal Resistance (Note 2)	R_{thJA}	26							°C/W
Operating Temperature Range	T_J	-65 to +175							°C
Storage Temperature Range	T_{STG}	-65 to +175							°C

Notes. 1. Measured at 1.0 MHz and applied reverse voltage of 4.0V DC

LM124
LM224 - LM324

LOW POWER QUAD OPERATIONAL AMPLIFIERS

- WIDE GAIN BANDWIDTH : 1.3MHz
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LARGE VOLTAGE GAIN : 100dB
- VERY LOW SUPPLY CURRENT/AMPLI : 375µA
- LOW INPUT BIAS CURRENT : 20nA
- LOW INPUT OFFSET VOLTAGE : 5mV max. (for more accurate applications, use the equivalent parts LM124A-LM224A-LM324A which feature 3mV max.)
- LOW INPUT OFFSET CURRENT : 2nA
- WIDE POWER SUPPLY RANGE :
  SINGLE SUPPLY : +3V TO +30V
  DUAL SUPPLIES : ±1.5V TO ±15V



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

P
TSSOP14
(Thin Shrink Small Outline Package)

DESCRIPTION

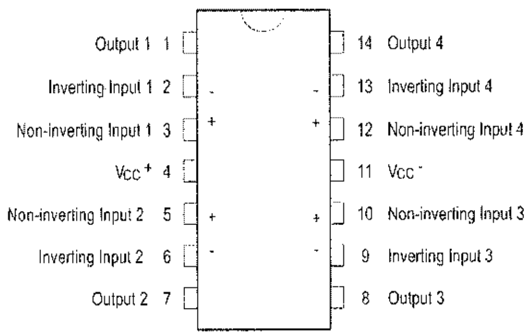
These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

ORDER CODE

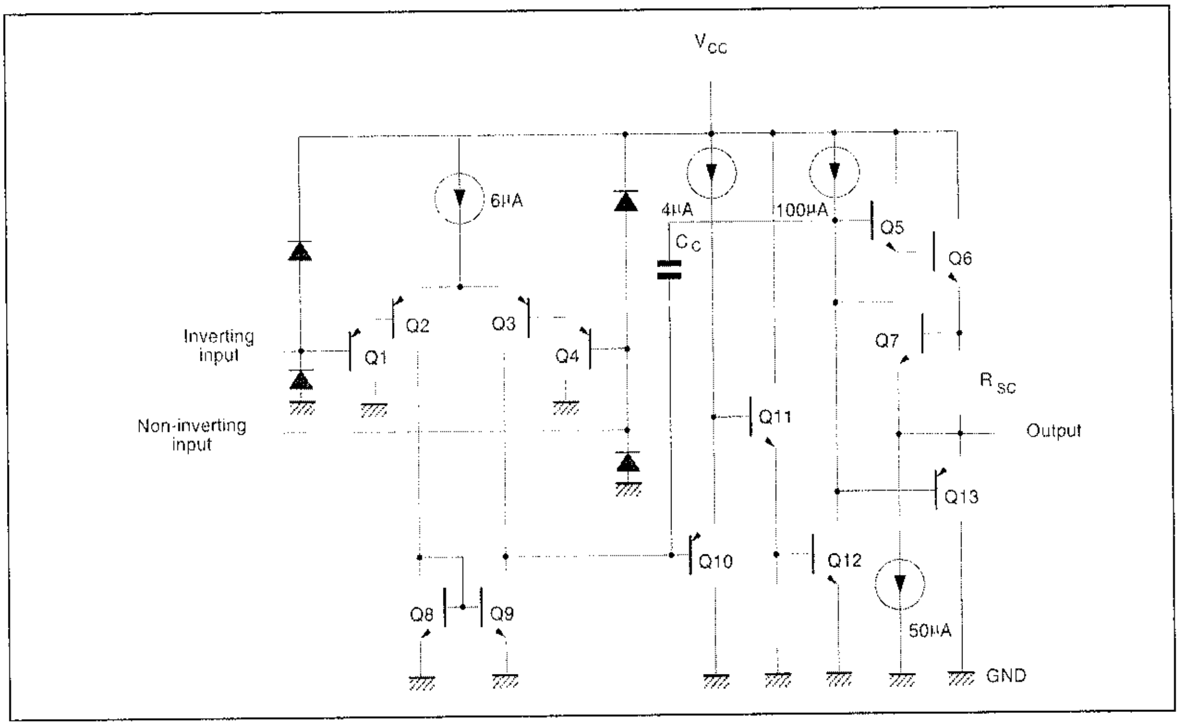
Part Number	Temperature Range	Package		
		N	D	P
LM124	-55°C, +125°C	•	•	•
LM224	-40°C, +105°C	•	•	•
LM324	0°C, +70°C	•	•	•
Example : LM224N				

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape &Reel (PT)

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM (1/4 LM124)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	LM124	LM224	LM324	Unit
V_{CC}	Supply voltage	±16 or 32			V
V_i	Input Voltage	-0.3 to +32			V
V_{id}	Differential Input Voltage 1)	+32			V
P_{tot}	Power Dissipation N Suffix D Suffix	500	500 400	500 400	mW mW
	Output Short-circuit Duration 2)	Infinite			
I_{in}	Input Current 3)	50	50	50	mA
T_{oper}	Opearting Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-.
2. Short-circuits from the output to VCC can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. this transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3V.

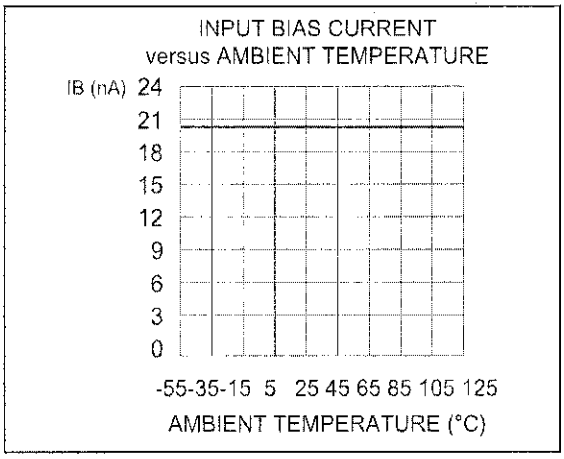
ELECTRICAL CHARACTERISTICS

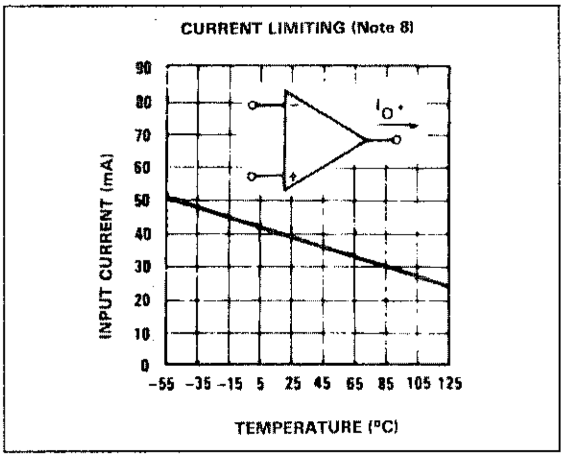
V_{CC}^+ = +5V, V_{CC}^-= Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

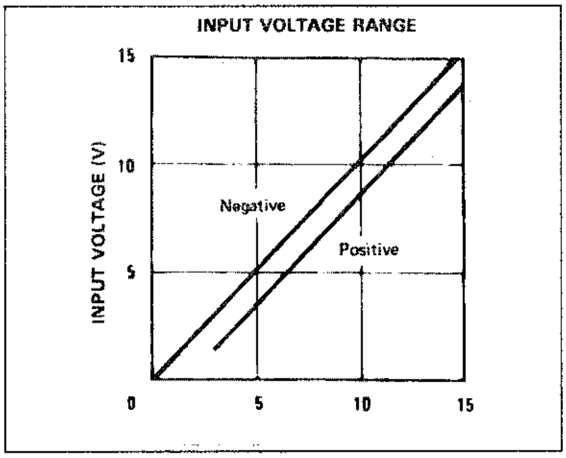
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - note [1] T_{amb} = +25°C LM324 T_{min} • T_{amb} • T_{max} LM324		2	5 7 7 9	mV
I_{io}	Input Offset Current T_{amb} = +25°C T_{min} • T_{amb} • T_{max}		2	30 100	nA
I_{ib}	Input Bias Current - note [2] T_{amb} = +25°C T_{min} • T_{amb} • T_{max}		20	150 300	nA
A_{vd}	Large Signal Voltage Gain V_{CC}^+ = +15V, R_L = 2kX -!V_o = 1.4V to 11.4V T_{amb} = +25°C T_{min} • T_{amb} • T_{max}	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio (R_s • 10kX) V_{CC}^+ = 5V to 30V T_{amb} = +25°C T_{min} • T_{amb} • T_{max}	65 65	110		dB
I_{CC}	Supply Current, all Amp, no load T_{amb} = +25°C V_{CC} = +5V V_{CC} = +30V T_{min} • T_{amb} • T_{max} V_{CC} = +5V V_{CC} = +30V		0.7 1.5 0.8 1.5	1.2 3 1.2 3	mA
V_{icm}	Input Common Mode Voltage Range V_{CC} = +30V - note [3] T_{amb} = +25°C T_{min} • T_{amb} • T_{max}	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common Mode Rejection Ratio (R_s • 10kX) T_{amb} = +25°C T_{min} • T_{amb} • T_{max}	70 60	80		dB
I_{source}	Output Current Source (V_{id} = +1V) V_{CC} = +15V, V_o = +2V	20	40	70	mA
I_{sink}	Output Sink Current (V_{id} = -1V) V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		mA nA
V_{OH}	High Level Output Voltage V_{CC} = +30V T_{amb} = +25°C R_L = 2kX T_{min} • T_{amb} • T_{max} T_{amb} = +25°C R_L = 10kX T_{min} • T_{amb} • T_{max} V_{CC} = +5V, R_L = 2kX T_{amb} = +25°C T_{min} • T_{amb} • T_{max}	26 26 27 27 3.5 3	27 28		V

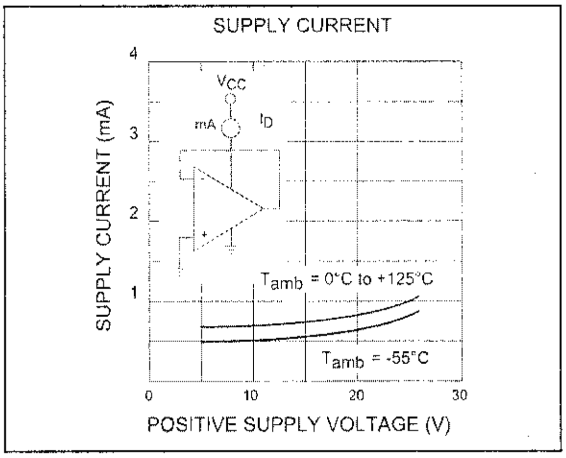
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage (R_L = 10kX) T_{amb} = +25°C T_{min} • T_{amb} • T_{max}		5	20 20	mV
SR	Slew Rate V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kX, C_L = 100pF, unity Gain		0.4		V/ns
GBP	Gain Bandwidth Product V_{CC} = 30V, f =100kHz,V_{in} = 10mV, R_L = 2kX, C_L = 100pF		1.3		MHz
THD	Total Harmonic Distortion f = 1kHz, A_v = 20dB, R_L = 2kX -!V_o = 2V_{pp}-!C_L = 100pF, V_{CC} = 30V		0.015		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100X - V_{CC} = 30V		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	30	nV/°C
DI_{Iio}	Input Offset Current Drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel Separation - note 4) 1kHz • !f • !20kHZ		120		dB

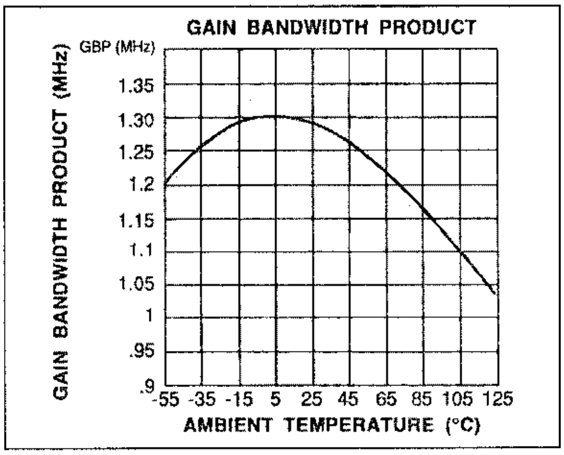
1. V_o = 1.4V, R_s = 0X, 5V < V_{CC}^+ < 30V, 0 < V_{ic} < V_{CC}^+ - 1.5V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.

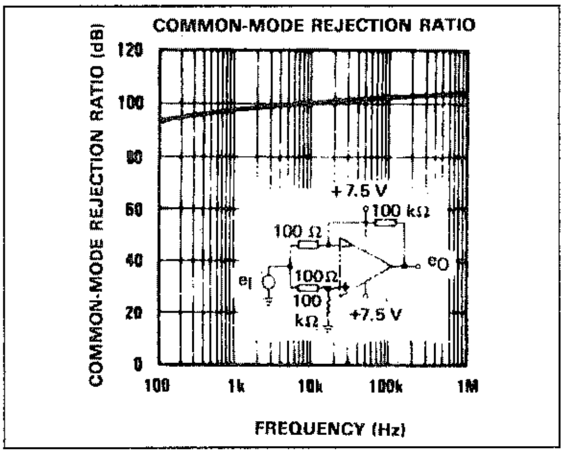

INPUT BIAS CURRENT
versus AMBIENT TEMPERATURE
IB (nA)
24
21
18
15
12
9
6
3
0
-55 -35 -15 5 25 45 65 85 105 125
AMBIENT TEMPERATURE (°C)


CURRENT LIMITING (Note 8)
INPUT CURRENT (mA)
90
80
70
60
50
40
30
20
10
0
I_O
-55 -35 -15 5 25 45 65 85 105 125
TEMPERATURE (°C)

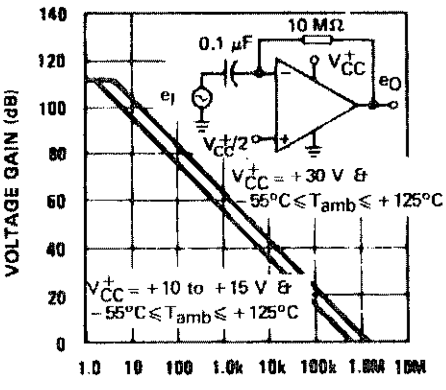

INPUT VOLTAGE RANGE
INPUT VOLTAGE (V)
15
10
5
0
Negative
Positive
5
10
15


SUPPLY CURRENT
SUPPLY CURRENT (mA)
4
3
2
1
V_{CC}
mA
I_D
T_{amb} = 0°C to +125°C
T_{amb} = -55°C
0
10
20
30
POSITIVE SUPPLY VOLTAGE (V)


GAIN BANDWIDTH PRODUCT
GAIN BANDWIDTH PRODUCT (MHz)
GBP (MHz)
1.35
1.30
1.25
1.2
1.15
1.1
1.05
1
.95
.9
-55 -35 -15 5 25 45 65 85 105 125
AMBIENT TEMPERATURE (°C)

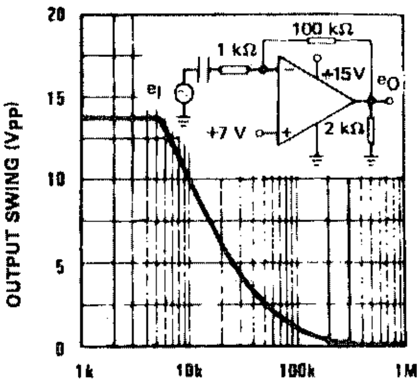

COMMON-MODE REJECTION RATIO
COMMON-MODE REJECTION RATIO (dB)
120
100
80
60
40
20
0
+7.5 V
100 kΩ
100 Ω
100 Ω
e_O
e_I
100 kΩ
+7.5 V
100
1k
10k
100k
1M
FREQUENCY (Hz)

OPEN LOOP FREQUENCY RESPONSE



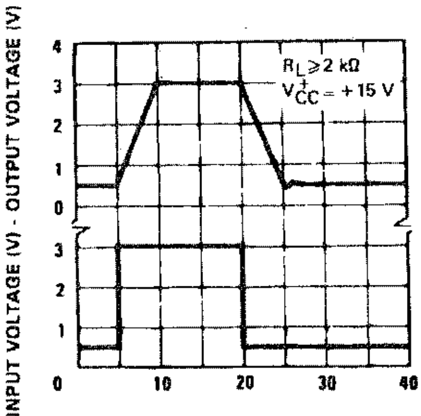
FREQUENCY (Hz)

LARGE SIGNAL FREQUENCY RESPONSE



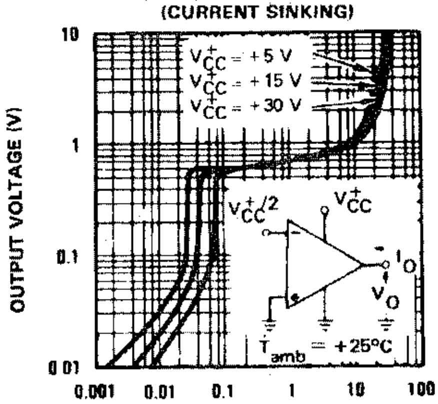
FREQUENCY (Hz)

VOLTAGE FOLLOWER PULSE RESPONSE



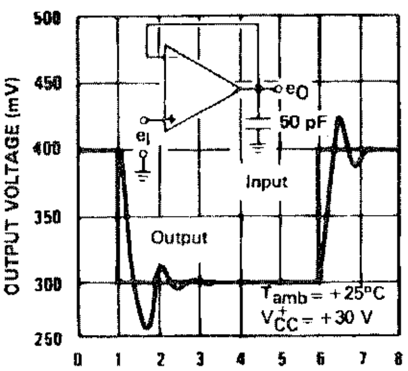
TIME (μs)

OUTPUT CHARACTERISTICS
(CURRENT SINKING)



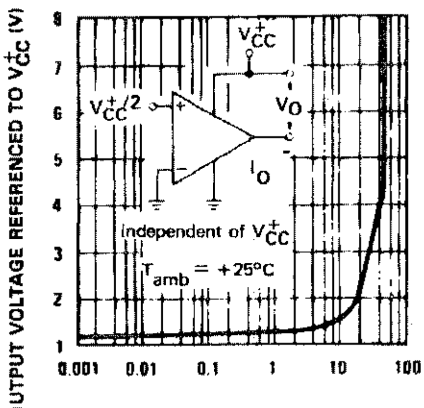
OUTPUT SINK CURRENT (mA)

VOLTAGE FOLLOWER PULSE RESPONSE
(SMALL SIGNAL)

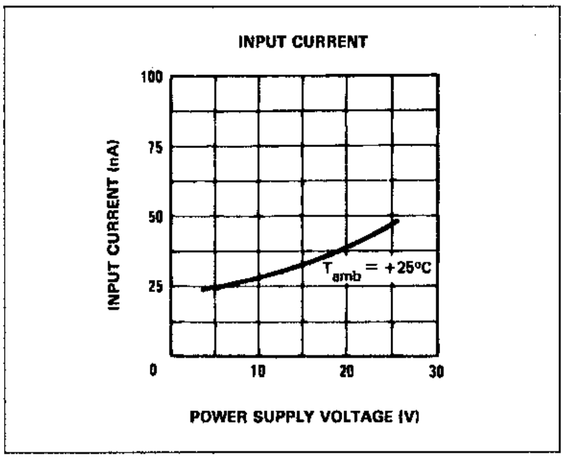


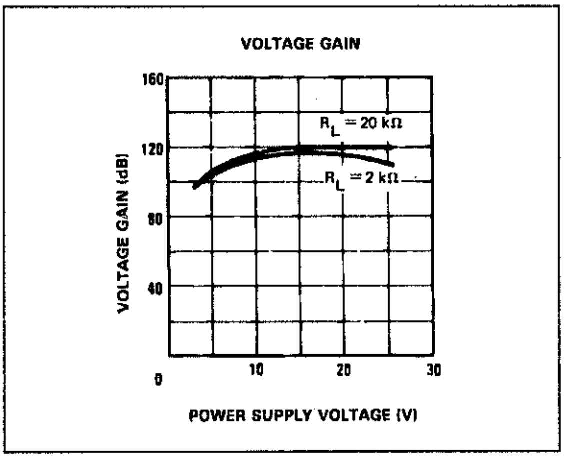
TIME (μs)

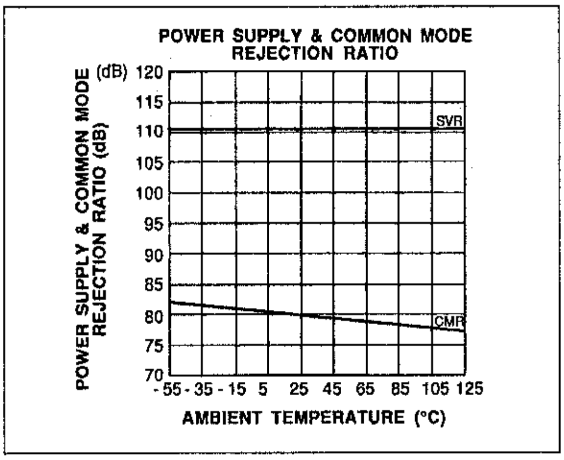
OUTPUT CHARACTERISTICS
(CURRENT SOURCING)

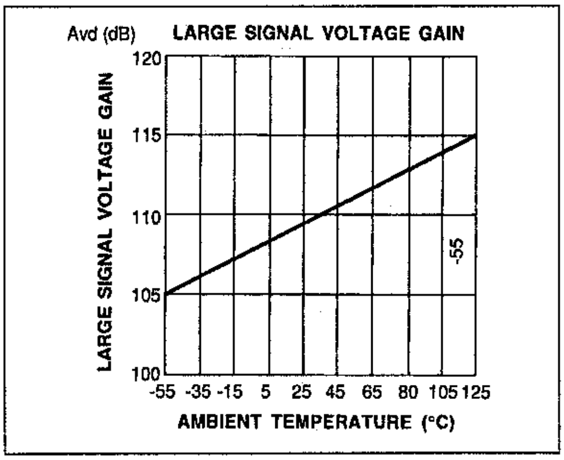


OUTPUT SOURCE CURRENT (mA)



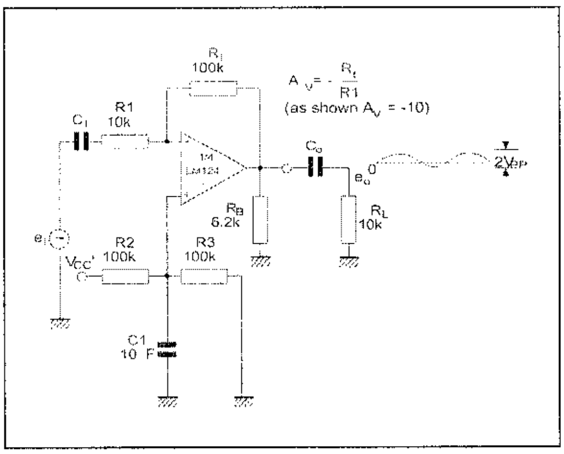




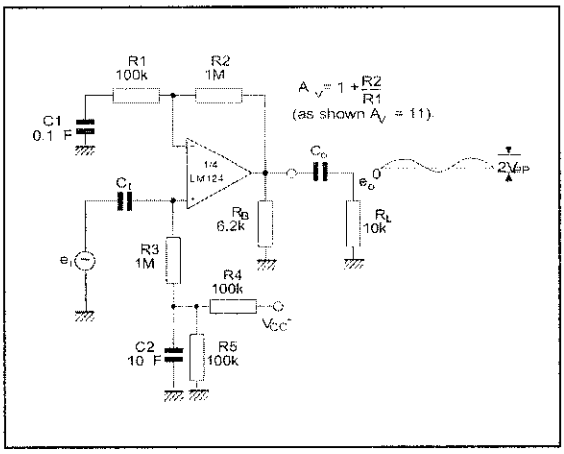


TYPICAL SINGLE - SUPPLY APPLICATIONS

AC COUPLED INVERTING AMPLIFIER

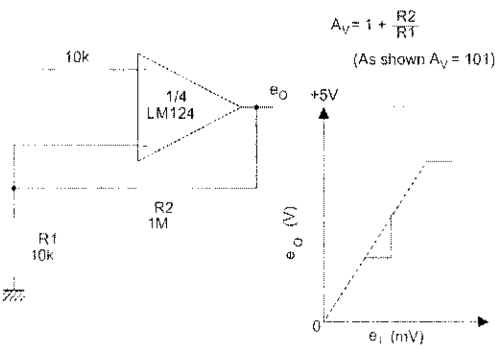


AC COUPLED NON INVERTING AMPLIFIER

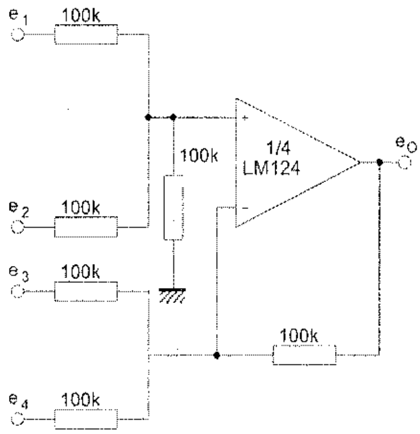


TYPICAL SINGLE - SUPPLY APPLICATIONS

NON-INVERTING DC GAIN

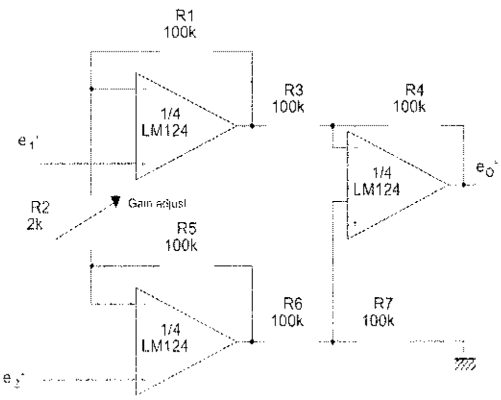


DC SUMMING AMPLIFIER



$e_0 = e_1 + e_2 - e_3 - e_4$
Where $(e_1 + e_2)$ μ $(e_3 + e_4)$
to keep e_0 μ 0V

HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

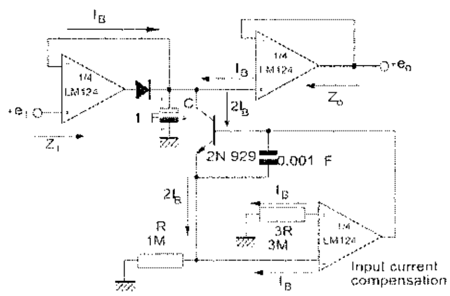


if R1 = R5 and R3 = R4 = R6 = R7

$$e_0 = \left[1 + \frac{2R_1}{R_2}\right](e_2 - e_1)$$

As shown $e_0 = 101\ (e_2 - e_1)$.

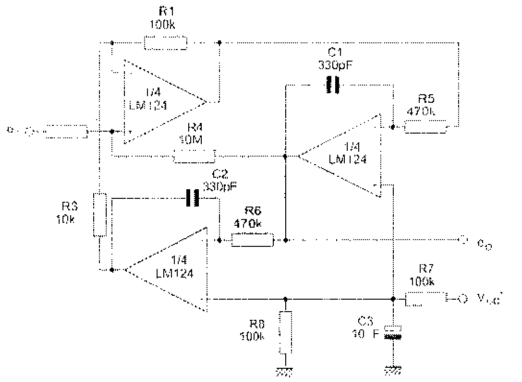
LOW DRIFT PEAK DETECTOR



* Polycarbonate or polyethylene

TYPICAL SINGLE - SUPPLY APPLICATIONS

ACTIVER BANDPASS FILTER



F_o = 1kHz

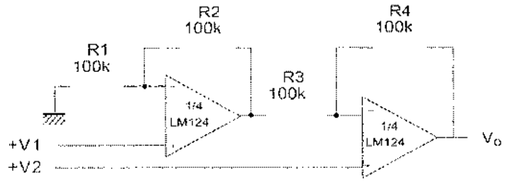
Q = 50

A_v = 100 (40dB)

HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$

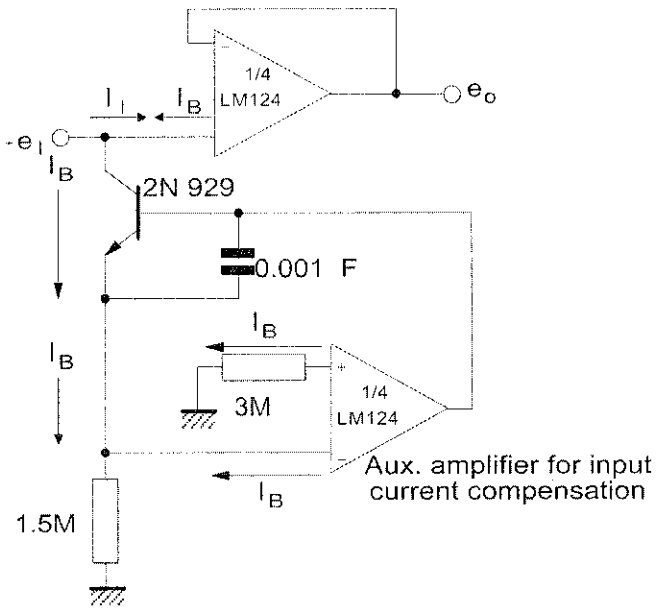
(CMRR depends on this resistor ratio match)



$e_0 = \left(1 + \frac{R_4}{R_3}\right)(e_2 - e_1)$

As shown $e_0 = (e_2 - e_1)$

USING SYMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (GENERAL CONCEPT)



MACROMODEL

**** Standard Linear Ics Macromodels, 1993.**

```
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT LM124 1 3 2 4 5 (analog)
*******************************************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15
CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

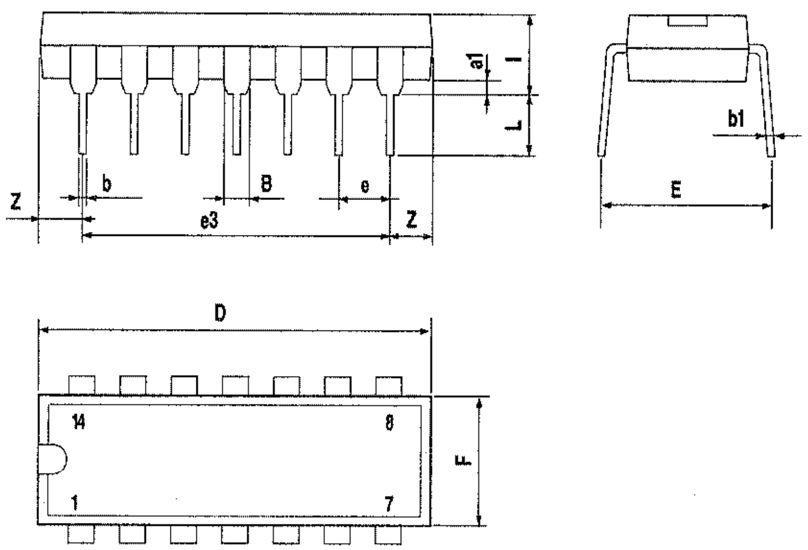
ELECTRICAL CHARACTERISTICS

V_{cc}^{+} = +15V, V_{cc}^{-} = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 2kX	100	V/mV
I_{cc}	No load, per amplifier	350	nA
V_{icm}		-15 to +13.5	V
V_{OH}	R_L = 2kX !(V_{CC}^{+}=15V)	+13.5	V
V_{OL}	R_L = 10kX	5	mV
I_{os}	V_o = +2V, V_{CC} = +15V	+40	mA
GBP	R_L = 2kX-!C_L = 100pF	1.3	MHz
SR	R_L = 2kX-!C_L = 100pF	0.4	V/ns

PACKAGE MECHANICAL DATA

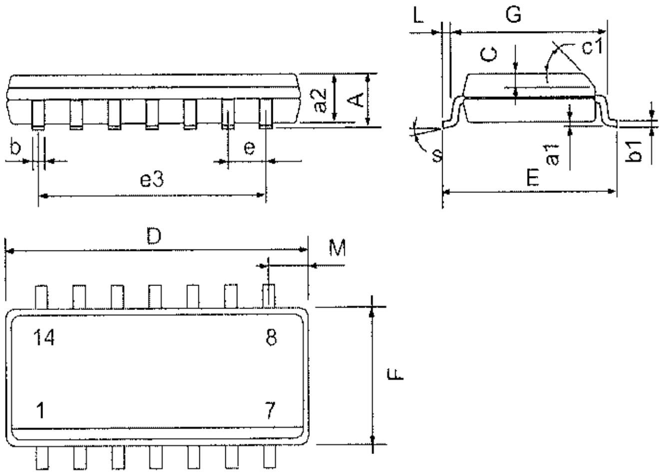
14 PINS - PLASTIC DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)

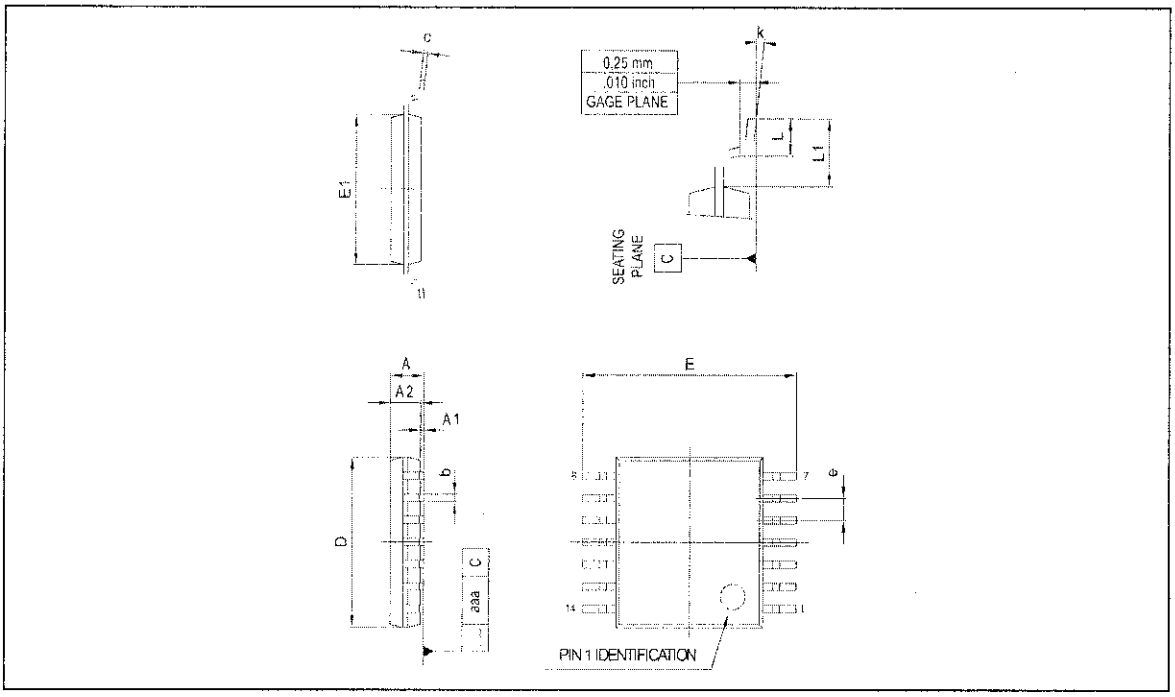


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

Note : (1) D and F do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.066 inc) ONLY FOR DATA BOOK.

PACKAGE MECHANICAL DATA

14 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	4.90	5.00	5.10	0.192	0.196	0.20
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.00			0.039	
aaa			0.100			0.004

STMicroelectronics GROUP OF COMPANIES

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Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States

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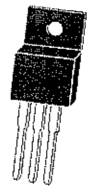
Standard

TO-220

Optional



TO-220FP Full Pak

Power Transistors
TO-220 Case

TYPE NO.		I_C	P_D	BV_{CBO}	BV_{CEO}	h_{FE}		@ I_C	$V_{CE(SAT)}$	@ I_C	f_T
NPN	PNP	(A) MAX	(W)	(V) MIN	(V) MIN	MIN	MAX	(A)	(V) MAX	(A)	(MHz) MIN
2N5294		4.0	36	80	70	30	120	0.5	1.0	0.5	0.8
2N5296		4.0	36	60	40	30	120	1.0	1.0	1.0	0.8
2N5298		4.0	36	80	60	20	80	1.5	1.0	1.5	0.8
2N5490		7.0	50	60	40	20	100	2.0	1.0	2.0	0.8
2N5492		7.0	50	75	55	20	100	2.5	1.0	2.5	0.8
2N5494		7.0	50	60	40	20	100	3.0	1.0	3.0	0.8
2N5496		7.0	50	90	70	20	100	3.5	1.0	35	0.8
2N6043	2N6040	10	75	60	60	1,000	20,000	4.0	2.0	4.0	4.0
2N6044	2N6041	10	75	80	80	1,000	20,000	4.0	2.0	4.0	4.0
2N6045	2N6042	10	75	100	100	1,000	20,000	3.0	2.0	3.0	4.0
2N6099		10	75	70	60	20	80	4.0	2.5	10	5.0
2N6101		10	75	80	70	20	80	5.0	2.5	10	5.0
2N6103		16	75	45	40	15	80	8.0	2.5	16	5.0
2N6121	2N6124	4.0	40	45	45	25	100	1.5	0.6	1.5	2.5
2N6122	2N6125	4.0	40	60	60	25	100	1.5	0.6	1.5	2.5
2N6123	2N6126	4.0	40	80	80	20	80	1.5	0.6	1.5	2.5
2N6129	2N6132	7.0	50	40	40	20	100	2.5	1.4	7.0	2.5
2N6130	2N6133	7.0	50	60	60	20	100	2.5	1.4	7.0	2.5
2N6131	2N6134	7.0	50	80	80	20	100	2.5	1.8	7.0	2.5
2N6288	2N6111	7.0	40	40	30	30	150	2.0	3.5	7.0	4.0
2N6290	2N6109	7.0	40	60	50	30	150	2.5	3.5	7.0	4.0
2N6292	2N6107	7.0	40	80	70	30	150	3.0	3.5	7.0	4.0
2N6386	2N6666	8.0	65	40	40	1,000	20,000	3.0	2.0	3.0	20
2N6387	2N6667	10	65	60	60	1,000	20,000	5.0	2.0	5.0	20
2N6388	2N6668	10	65	80	80	1,000	20,000	5.0	2.0	5.0	20
2N6473	2N6475	4.0	40	110	100	15	150	1.5	1.2	1.5	4.0
2N6474	2N6476	4.0	40	130	120	15	150	1.5	1.2	1.5	4.0
2N6486	2N6489	15	75	50	40	20	150	5.0	1.3	5.0	5.0
2N6487	2N6490	15	75	70	60	20	150	5.0	1.3	5.0	5.0
2N6488	2N6491	15	75	90	80	20	150	5.0	1.3	5.0	5.0

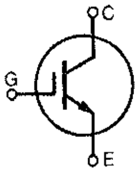
Shaded areas indicate Darlington.
Available in TO-220FP Full Pak upon request.

iPerFAST™ IGBT

IXGH 40N60B2
IXGT 40N60B2

V_{CES} = 600 V
I_{C25} = 75 A
$V_{CE(sat)}$ < 1.7 V
$t_{fi\,typ}$ = 82 ns

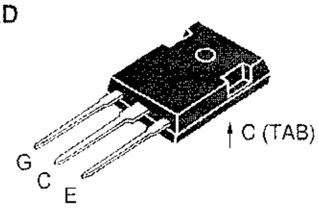
)timized for 10-25 KHz hard /itching and up to 150 KHz sonant switching



mbol	Test Conditions	Maximum Ratings	
:S	T_J = 25°C to 150°C	600	V
3R	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
:S	Continuous	±20	V
:M	Transient	±30	V
	T_C = 25°C (limited by leads)	75	A
0	T_C = 110°C	40	A
	T_C = 25°C, 1 ms	200	A
OA 3SOA)	V_{GE} = 15 V, T_{VJ} = 125°C, R_G = 10 Ω Clamped inductive load @ ≤ 600 V	I_{CM} = 80	A
	T_C = 25°C	300	W
		-55 ... +150	°C
		150	°C
t		-55 ... +150	°C
ximum lead temperature for soldering mm (0.062 in.) from case for 10 s		300	°C
	Mounting torque (M3)	1.13/10 Nm/lb.in.	
ight	TO-247 AD TO-268 SMD	6 4	g g

TO-268 (IXGT)

TO-247 AD (IXGH)



G = Gate, C = Collector,
E = Emitter, TAB = Collector

Features

- Medium frequency IGBT
- Square RBSOA
- High current handling capability
- MOS Gate turn-on
  - drive simplicity

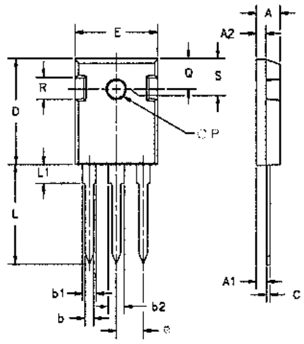
Applications

- PFC circuits
- Uninterruptible power supplies (UPS)
- Switched-mode and resonant-mode power supplies
- AC motor speed control
- DC servo and robot drives
- DC choppers

mbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
:(th)	I_C = 250 µA, V_{CE} = V_{GE}		3.0		5.0	V
:	V_{CE} = V_{CES} V_{GE} = 0 V	T_J = 25°C T_J = 150°C			50 1	µA mA
;	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
:(sat)	I_C = 30 A, V_{GE} = 15 V	T_J = 25°C			1.7	V

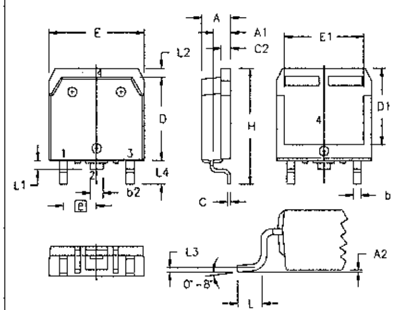
Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
= 30 A; V_{CE} = 10 V, ulse test, t ≤ 300 µs, duty cycle ≤ 2 %	20	36		S
		2560		pF
V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		180		pF
		54		pF
		100		nC
I_C = 30 A, V_{GE} = 15 V, V_{CE} = 300 V		15		nC
		36		nC
		18		ns
Inductive load, T_J = 25°C		20		ns
I_C = 30 A, V_{GE} = 15 V		130	200	ns
V_{CE} = 400 V, R_G = 3.3 Ω		82	150	ns
		0.4	0.8	mJ
		18		ns
Inductive load, T_J = 125°C		20		ns
I_C = 30 A, V_{GE} = 15 V		0.3		mJ
V_{CE} = 400 V, R_G = 3.3 Ω		240		ns
		150		ns
		1.10		mJ
			0.42	K/W
(TO-247)		0.25		K/W

TO-247 AD Outline



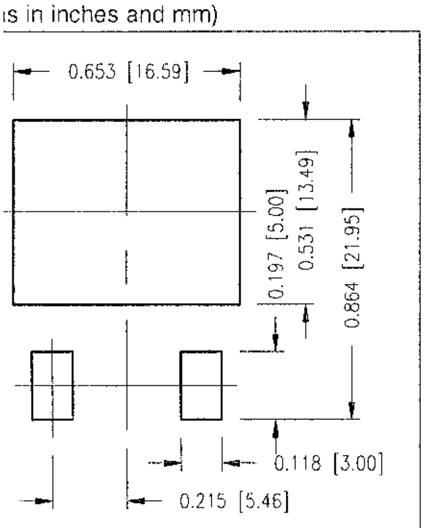
Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

TO-268 Outline



SYM	INCHES MIN	MAX	MILLIMETERS MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

mmended Footprint
ıs in inches and mm)



es the right to change limits, test conditions, and dimensions.

and IGBTs are covered by one or more
S. patents

4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343

Fig. 1. Output Characteristics @ 25 Deg. C

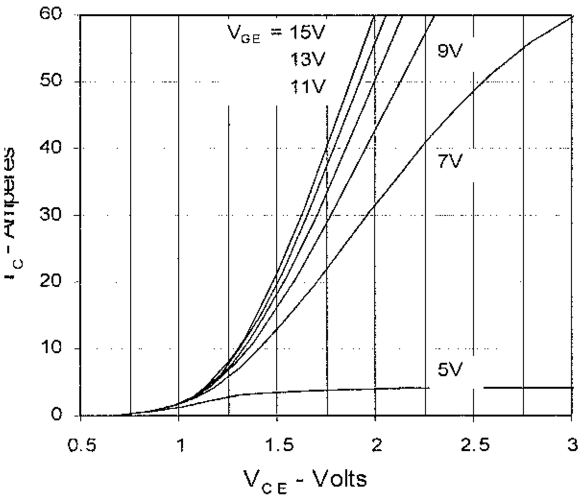


Fig. 2. Extended Output Characteristics @ 25 deg. C

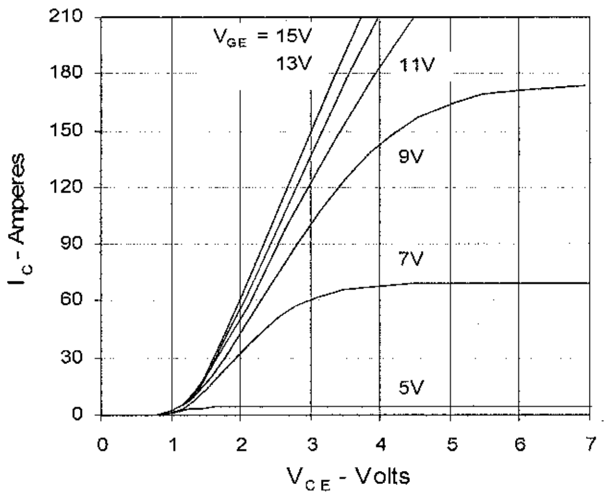


Fig. 3. Output Characteristics @ 125 Deg. C

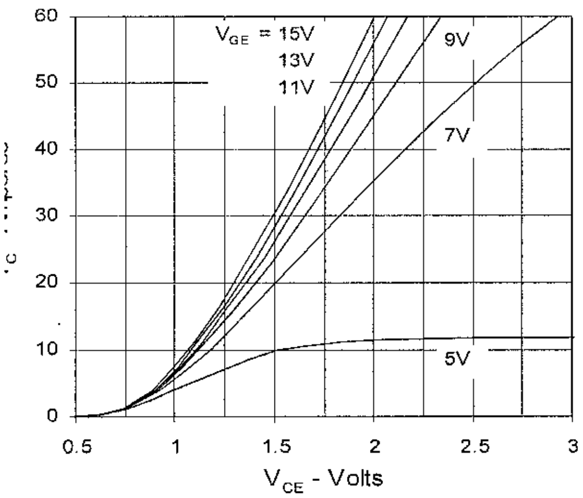


Fig. 4. Dependence of $V_{CE(sat)}$ on Temperature

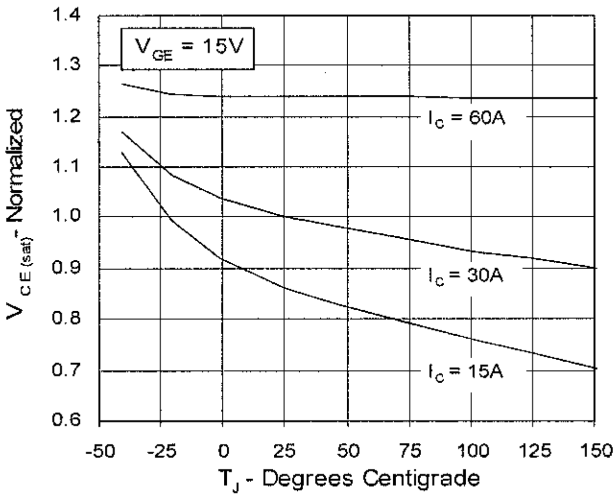


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter voltage

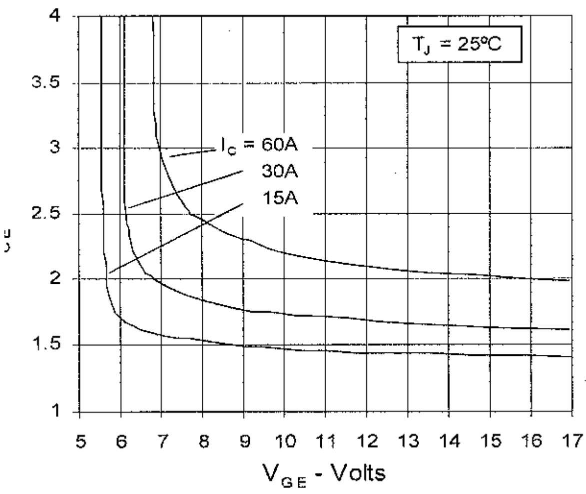


Fig. 6. Input Admittance

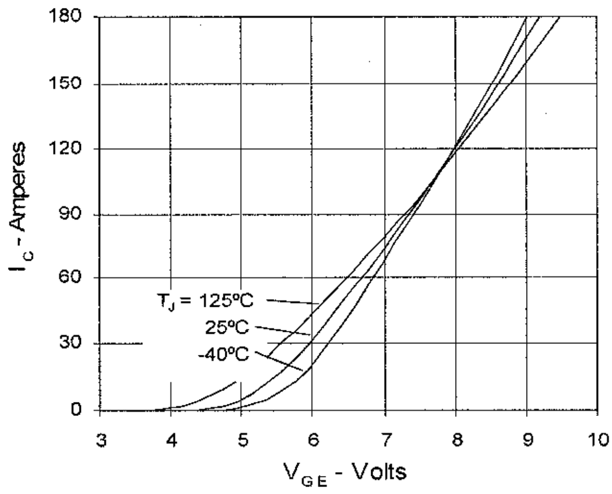


Fig. 7. Transconductance

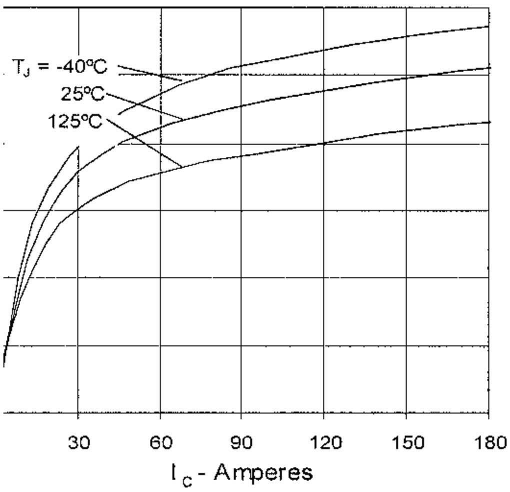


Fig. 8. Dependence of Turn-Off Energy on R_G

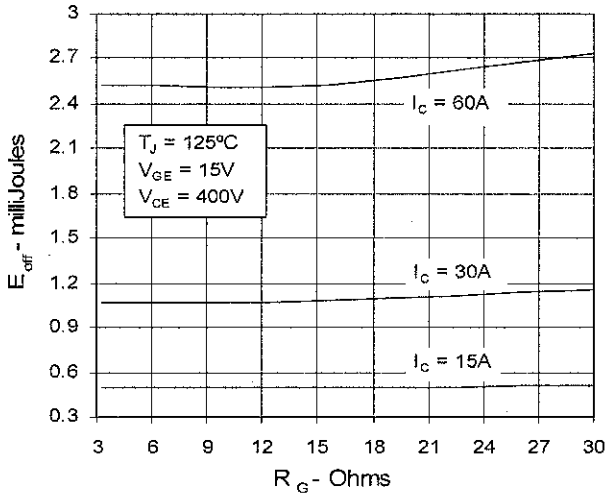


Fig. 9. Dependence of Turn-Off Energy on I_c

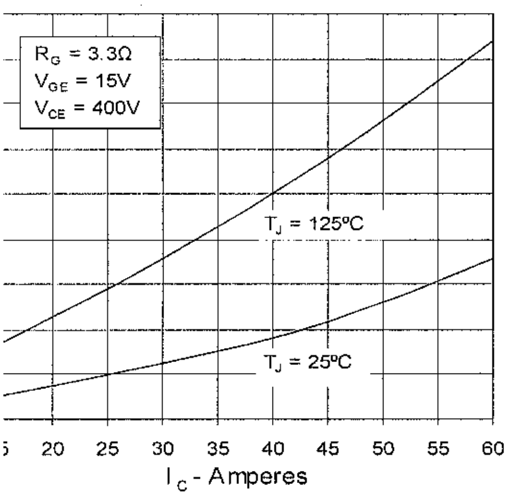


Fig. 10. Dependence of Turn-Off Energy on Temperature

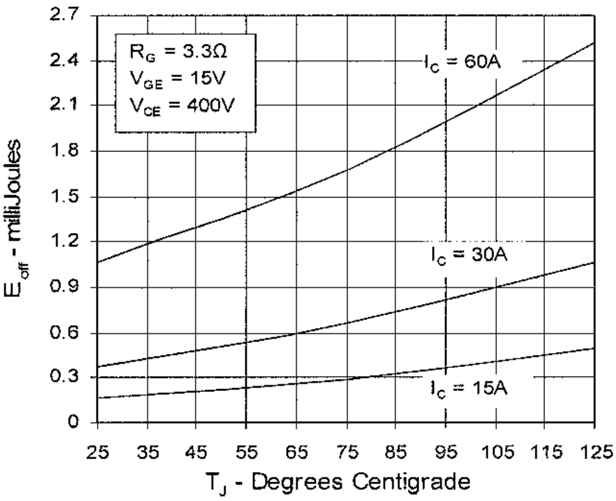


Fig. 11. Dependence of Turn-Off Switching Time on R_G

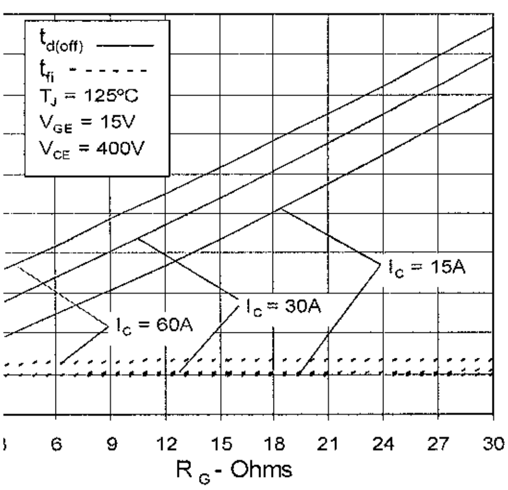


Fig. 12. Dependence of Turn-Off Switching Time on I_c

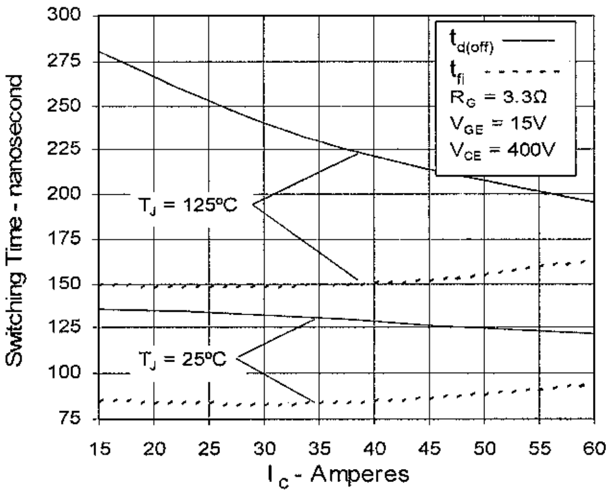


Fig. 13. Dependence of Turn-Off Switching Time on Temperature

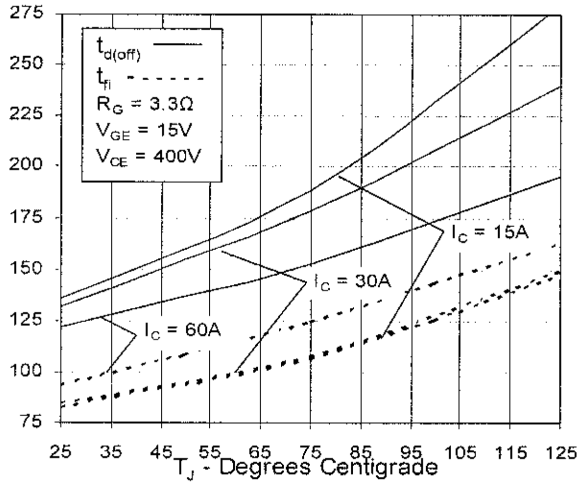


Fig. 14. Gate Charge

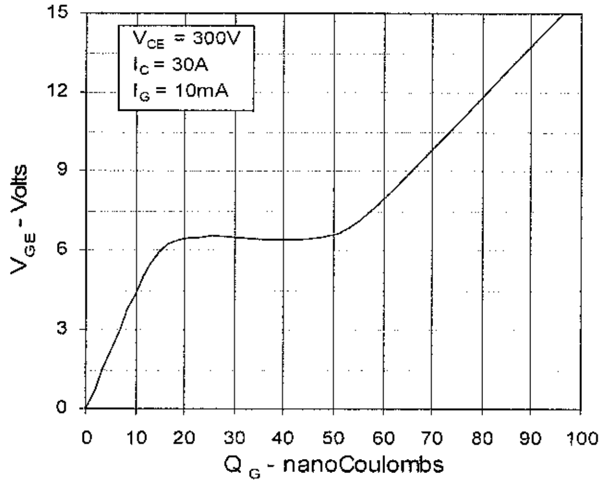


Fig. 15. Capacitance

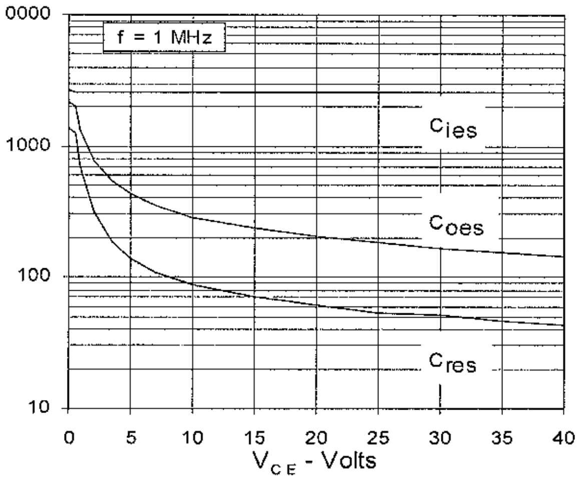
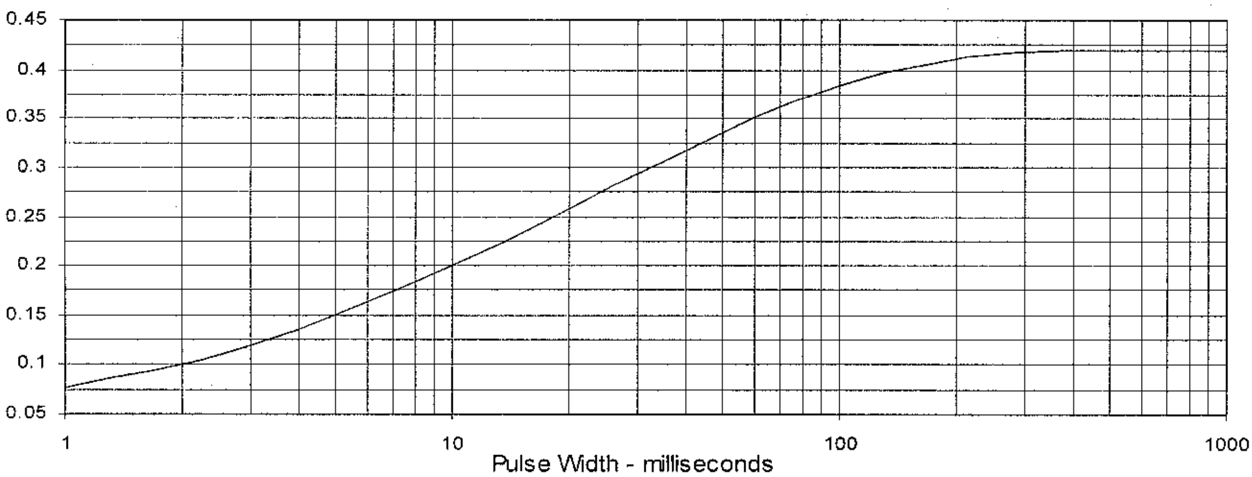


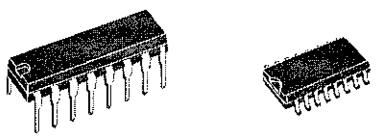
Fig. 16. Maximum Transient Thermal Resistance



HCF4017B

DECADE COUNTER WITH 10 DECODED OUTPUTS

- MEDIUM SPEED OPERATION :
  10 MHz (Typ.) at V_{DD} = 10V
- FULLY STATIC OPERATION
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
  I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP SOP

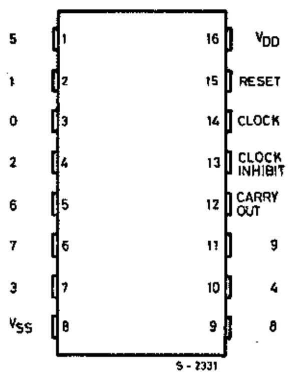
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4017BEY	
SOP	HCF4017BM1	HCF4017M013TR

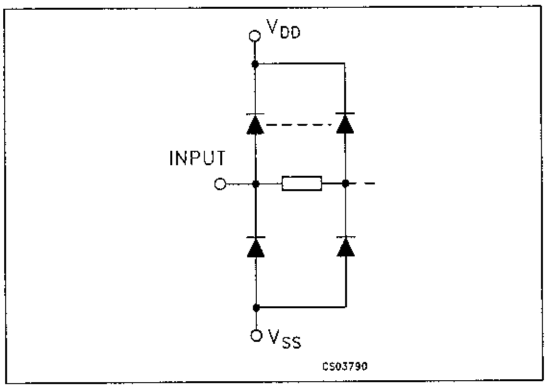
DESCRIPTION

The HCF4017B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4017B is 5-stage Johnson counter having 10 decoded outputs. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the clock input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. This counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advanced via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high speed operation, 2-input decimal decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY - OUT signal completes one cycle every 10 clock input cycles and is used to ripple-clock the succeeding device in a multi-device counting chain.

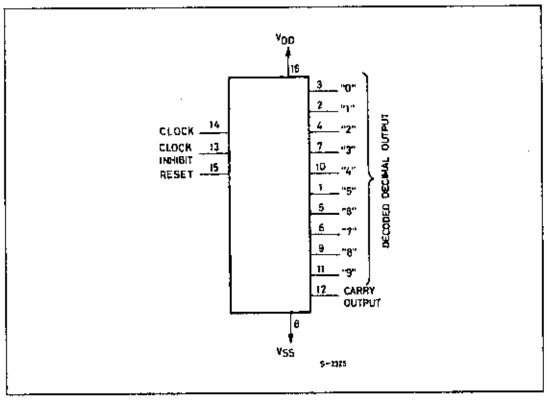
PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



FUNCTIONAL DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	0 to 9	Decoded Decimal Output
14	CLOCK	Clock Input
13	CLOCK INHIBIT	Clock Inhibit Input
15	RESET	Reset Input
12	CARRY OUT	Carry Output
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

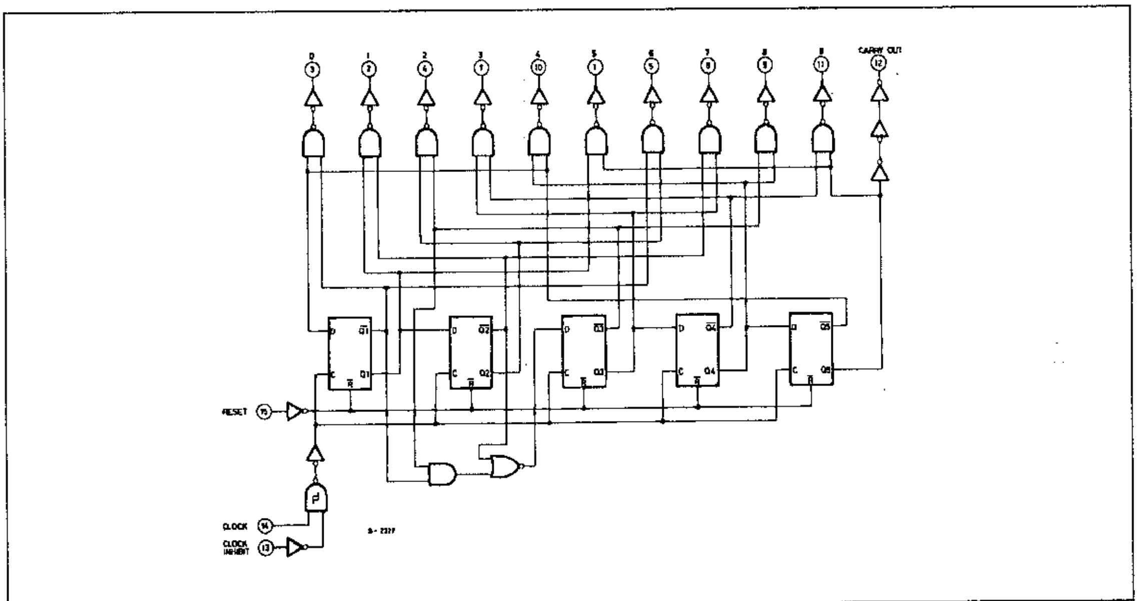
TRUTH TABLE

CLOCK	CLOCK INHIBIT	RESET	DECODED OUTPUT
X	X	H	Q_0
L	X	L	Q_n
X	H	L	Q_n
↑	L	L	Q_{n+1}
↓	L	L	Q_n
H	↑	L	Q_n
H	↓	L	Q_{n+1}

X : Don't Care

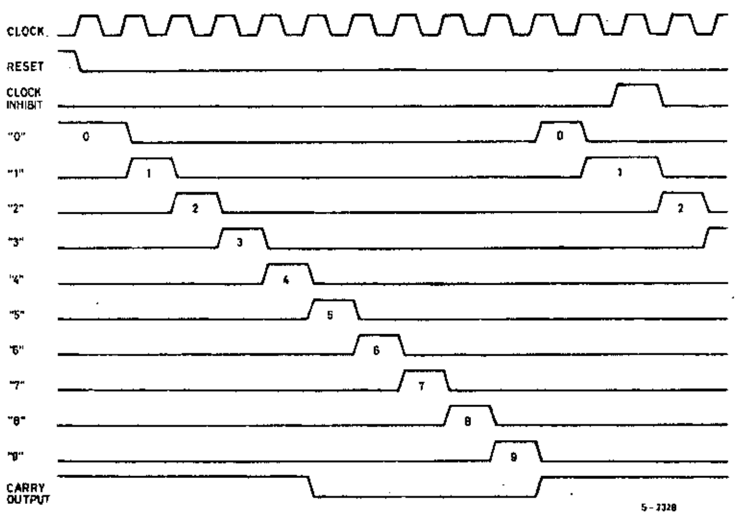
Qn : No Change

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	≥ 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (nA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	nA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\geq 10^{-5}$	≥0.1		≥1		≥1	nA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

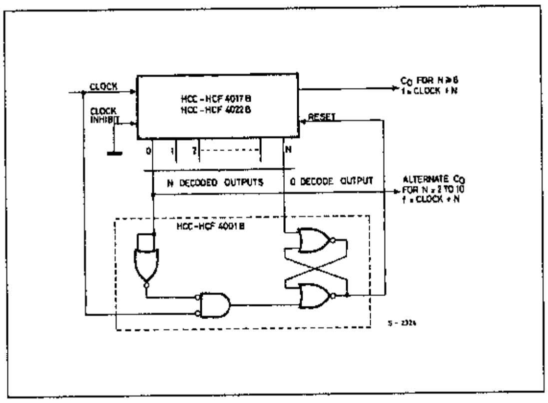
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, t_r = t_f = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
CLOCKED OPERATION							
t_{PLH} t_{PHL}	Propagation Delay Time (decode out)	5			325	650	ns
		10			135	270	
		15			85	170	
	Propagation Delay Time (carry out)	5			300	600	ns
		10			125	250	
		15			80	160	
t_{THL} t_{TLH}	Transition Time (carry out or decoded out lines)	5			100	200	ns
		10			50	100	
		15			40	80	
f_{CL} (1)	Maximum Clock Input Frequency	5		2.5	5	5	MHz
		10		5	10		
		15		5.5	11		
t_W	Minimum Clock Pulse Width	5			100	200	ns
		10			45	90	
		15			30	60	
t_r, t_f	Clock Input Rise or Fall Time	5			unlimited		ns
		10					
		15					
t_{setup}	Data Setup Time Minimum Clock Inhibit	5			115	230	ns
		10			50	100	
		15			35	75	
RESET OPERATION							
t_{PLH}, t_{PHL}	Propagation Delay Time (carry out or decoded out lines)	5			265	530	ns
		10			115	230	
		15			85	170	
t_W	Minimum Reset Pulse Width	5			130	260	ns
		10			55	110	
		15			30	60	
t_{REM}	Minimum Reset Removal Time	5			200	400	ns
		10			140	280	
		15			75	150	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) Measured with respect to carry out line.

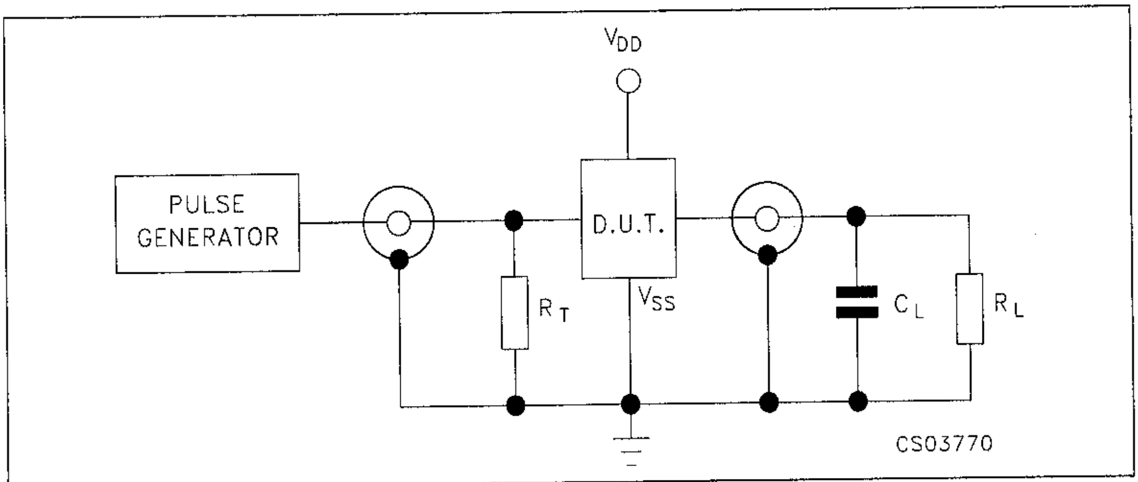
TYPICAL APPLICATIONS

DIVIDE BY N COUNTER(N ≤ 10) WITH DECODED OUTPUTS



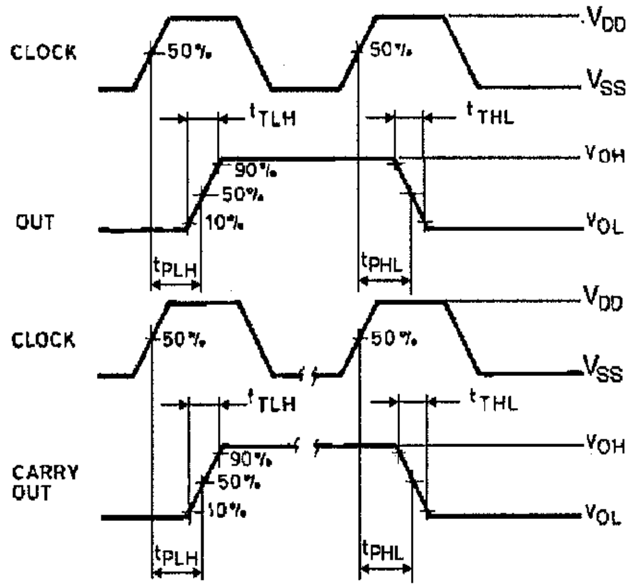
When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip-flop (constructed from two NOR gates of the HCF4001B) generates a reset pulse which clears the HCF4017B to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next HCF4017B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output high resets the S-R flip-flop to enable the HCF4017B. If the N^{th} decoded output is less than 6, the COUT line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

TEST CIRCUIT

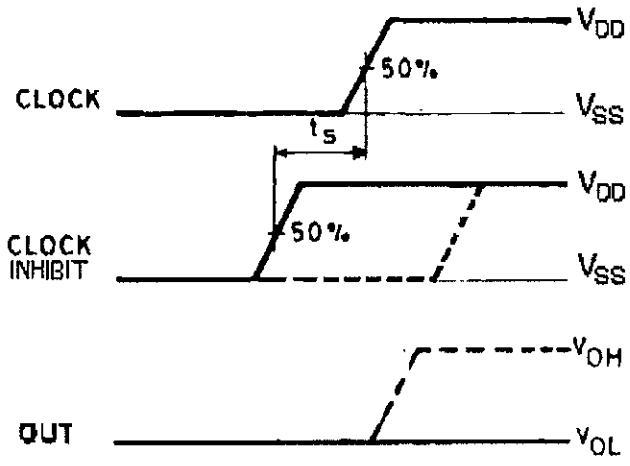


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KX
R_T = Z_{OUT} of pulse generator (typically 50X)

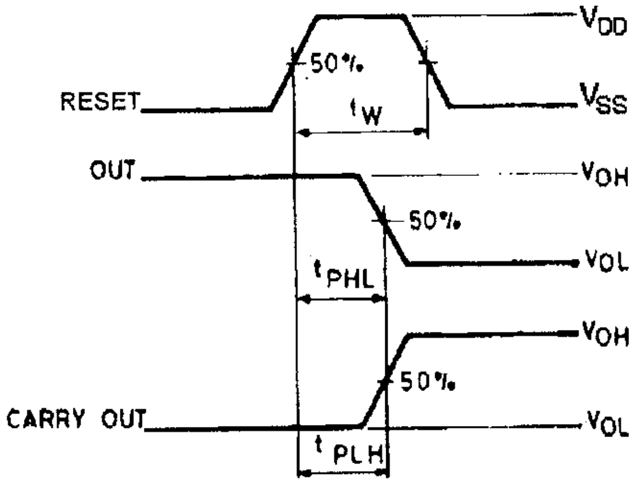
WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



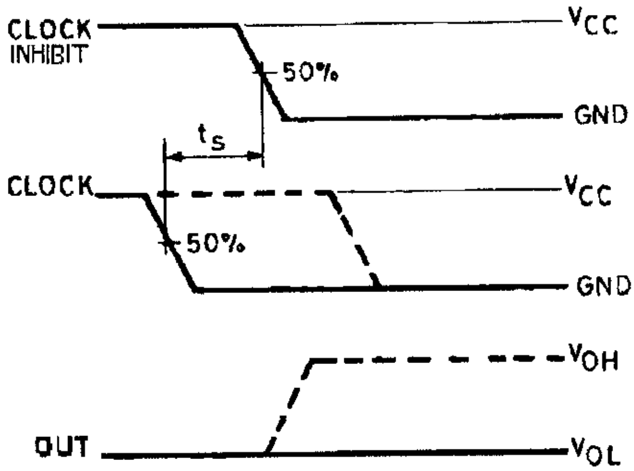
WAVEFORM 2 : MINIMUM SETUP TIME (CLOCK INHIBIT TO CLOCK) (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAY TIMES, MINIMUM RESET PULSE WIDTH (f=1MHz; 50% duty cycle)

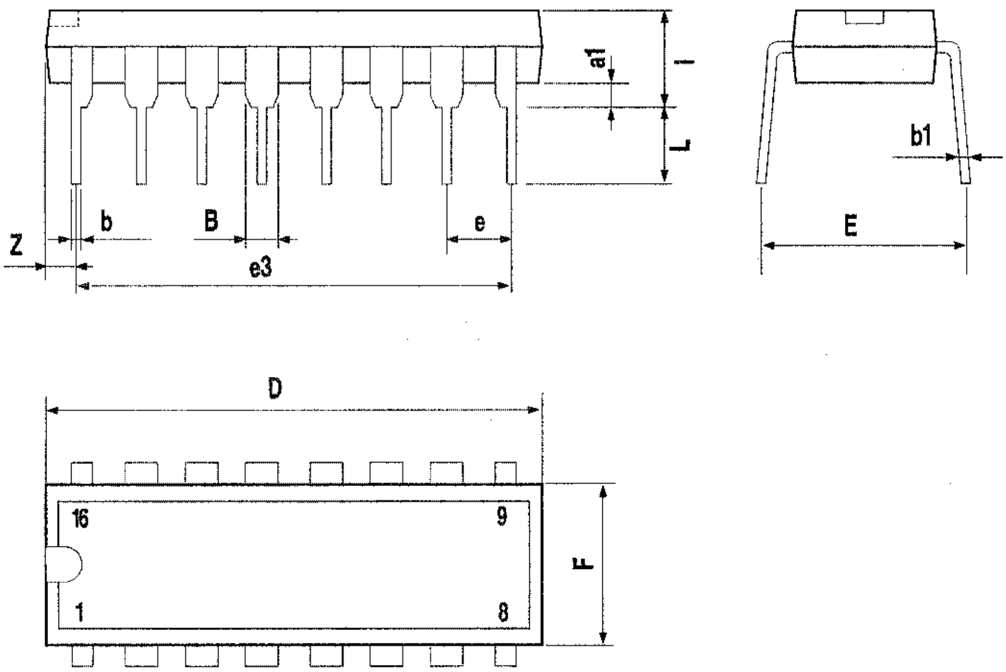


WAVEFORM 4 : MINIMUM SETUP TIME (CLOCK TO CLOCK INHIBIT) (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

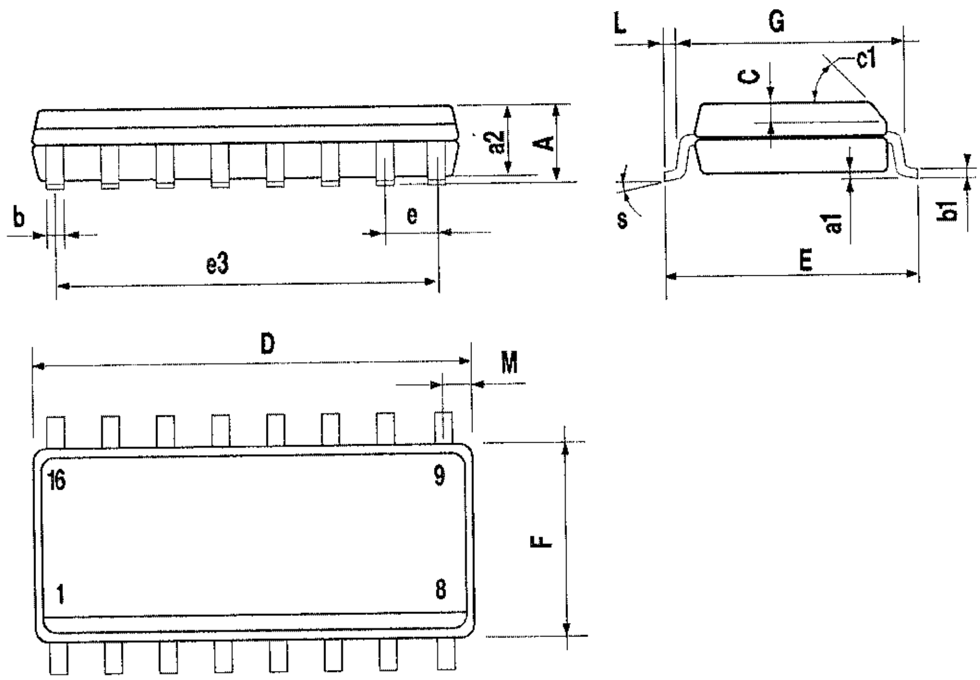
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

IS1U60/IS1U60L

Sensors with 1-Package Design of Remote Control Detecting Functions owing to OPIC

■ Features

1. 1-package design owing to adoption of OPIC
2. Compact
   (Volume : About 1/8 compared with **GP1U58X**)
3. B.P.F. (Band Pass Frequency) : (TYP. 38kHz)
4. Aspherical lens

■ Applications

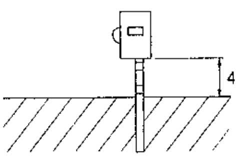
1. Audio equipment
2. Cameras

■ Absolute Maximum Ratings

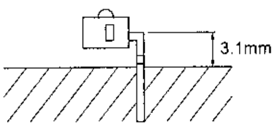
(Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	0 to 6.0	V
*1 Operating temperature	T_{opr}	- 10 to + 60	°C
Storage temperature	T_{stg}	- 20 to + 70	°C
*2 Soldering temperature	T_{sol}	260	°C

*1 No dew condensation is allowed.
*2 For 5 seconds



Soldering area

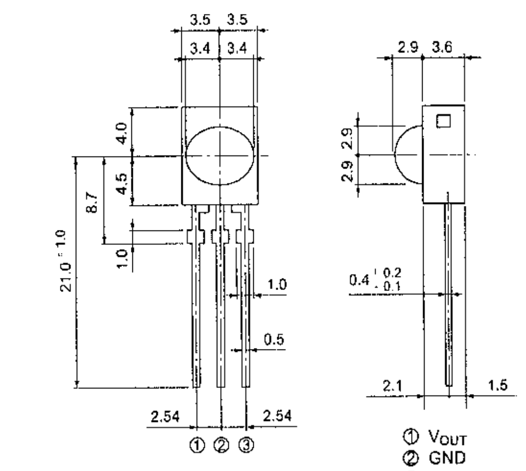


Soldering area

■ Outline Dimensions

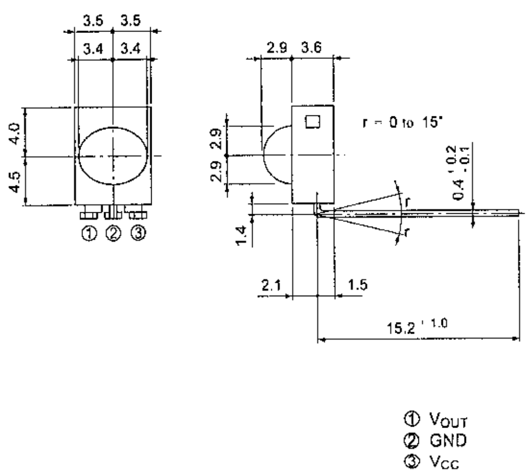
(Unit : mm)

IS1U60



* Tolerance : ± 0.2

IS1U60L



* Tolerance : ± 0.2

* "OPIC" (Optical IC) is a trademark of the SHARP Corporation.
An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Recommended Operating Conditions

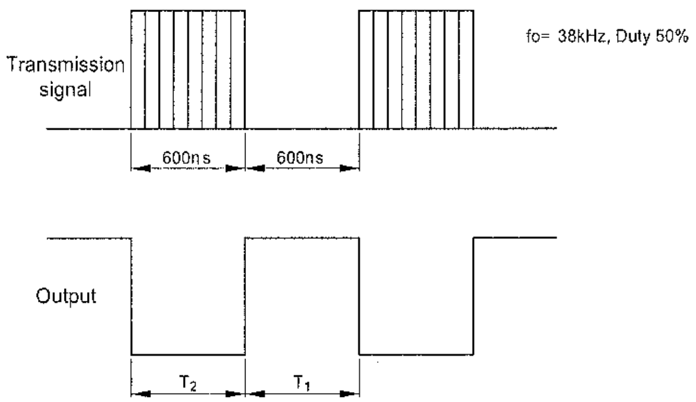
Parameter	Symbol	Recommended operating conditions	Unit
Operating supply voltage	V_{CC}	4.7 to 5.3	V

Electrical Characteristics

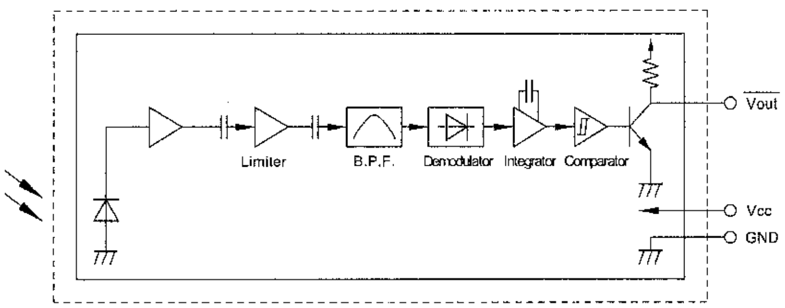
(Ta=25°C, V_{CC} =+5V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Dissipation current	I_{CC}	No input light	-	2.8	4.5	mA
High level output voltage	V_{OH}	*3, Output terminal OPEN	V_{CC} - 0.2	-	-	V
Low level output voltage	V_{OL}	*3, *4	-	0.45	0.6	V
High level pulse width	T_1	*3	400	-	800	ns
Low level pulse width	T_2		400	-	800	ns
B.P.F. center frequency	f_O		-	38	-	kHz
Linear ultimate distance	L	g , r = 0°, E_e < 10 lx	5.0	-	-	m
Linear ultimate distance	L_1	g = ± 30° (r = 0°) r = ± 15° (g = 0°) E_e < 10 lx	3.0	-	-	m

3 The burst wave as shown in the following figure shall be transmitted.
4 Pull-up resistance : 2.2kX
5 By SHARP transmitter



Internal Block Diagram



I Performance

sing the transmitter shown in Fig. 1, the output signal of the light detecting unit is good enough to meet the following items in the standard optical system in Fig. 2.

:) Linear reception distance characteristics

When L=0.2 to 5 m, Ee < 10 lx (*4) and g =0° in Fig. 2, the output signal shall meet the electrical characteristics in the attached list.

2) Sensitivity angle reception distance characteristics

When L=0.2 to 3 m, Ee < 10 lx (*4) and g<= 30 ° in the direction X and r =0° in the direction Y in Fig. 2, the output signal shall meet the electrical characteristics in the attached list Further, the electrical characteristics shall be met when L=0.2 to 5 m. Ee < 10 lx (*4) and g =0° in the direction X and r<= 15° in the direction Y.

*4 It refers to detector face illuminance.

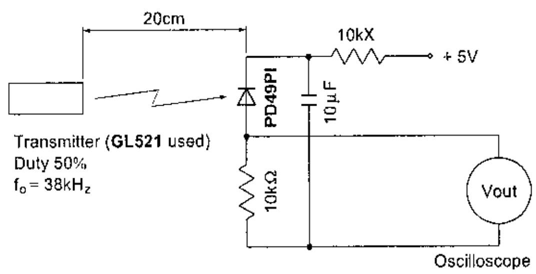


Fig. 1 Transmitter

n the above figure, the transmitter should be set so that the output Vout can be 40mV$_{P-P}$.
lowever, the **PD49PI** to be used here should be of the short-circuit current I_{SC}=2.6 nA at Ev=100 lx.
Ev is an illuminance by CIE standard light source A (tungsten lamp).)

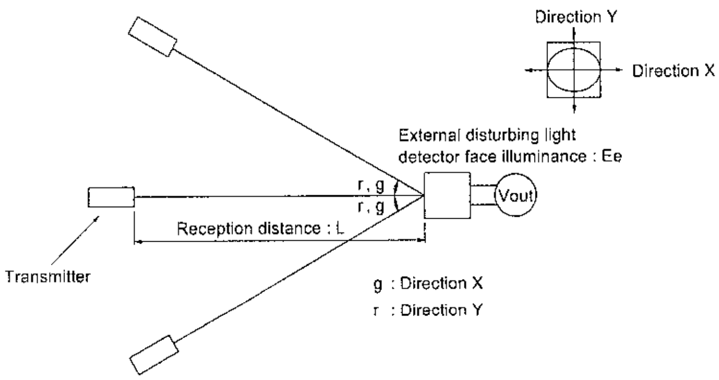


Fig. 2 Standard optical system

IS1U60/IS1U60L

Sensors with 1-Package Design of Remote Control Detecting Functions owing to OPIC

■ Features

1. 1-package design owing to adoption of OPIC
2. Compact
   (Volume : About 1/8 compared with **GP1U58X**)
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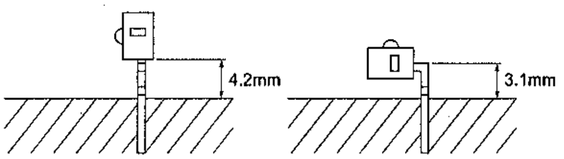
*2 Soldering temperature	T_{sol}	260	°C

*1 No dew condensation is allowed.
*2 For 5 seconds

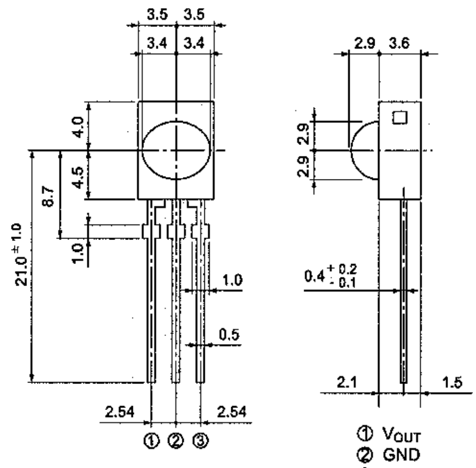


Soldering area　　Soldering area

■ Outline Dimensions

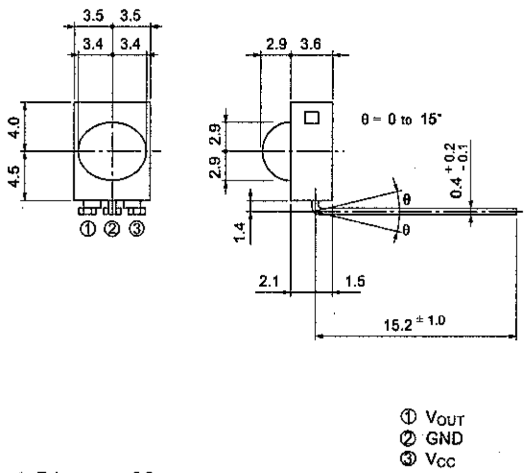
(Unit : mm)

IS1U60



* Tolerance : ± 0.2

IS1U60L



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An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Recommended Operating Conditions

Parameter	Symbol	Recommended operating conditions	Unit
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■ Electrical Characteristics

(Ta=25°C, V_{CC}=+5V)

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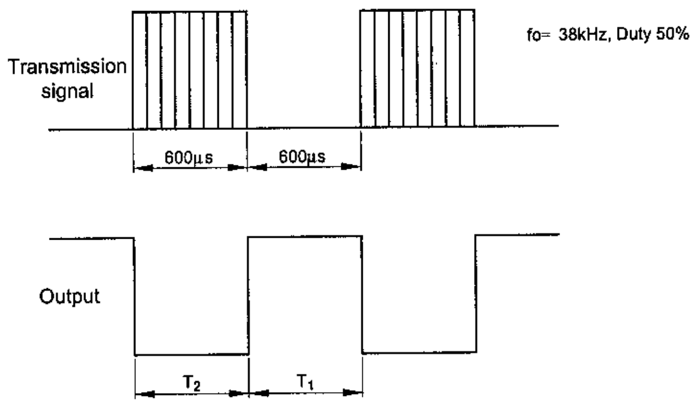
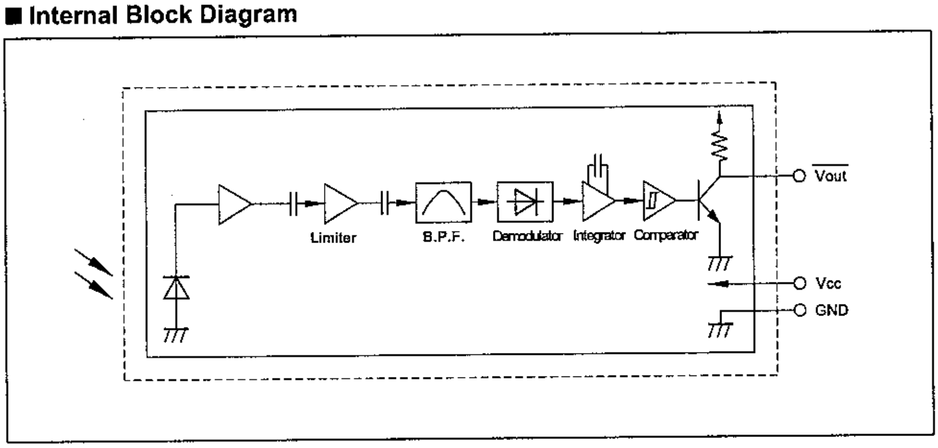
High level output voltage	V_{OH}	*3, Output terminal OPEN	Vcc- 0.2	-	-	V
Low level output voltage	V_{OL}	*3, *4	-	0.45	0.6	V
High level pulse width	T_1	*3	400	-	800	μs
Low level pulse width	T_2		400	-	800	μs
B.P.F. center frequency	fo		-	38	-	kHz
Linear ultimate distance	L	$\phi, \theta = 0°, E_e < 10$ lx	5.0	-	-	m
Linear ultimate distance	L_l	$\phi = \pm 30°$ ($\theta = 0°$) $\theta = \pm 15°$ ($\phi = 0°$) $E_e < 10$ lx	3.0	-	-	m

*3 The burst wave as shown in the following figure shall be transmitted.
*4 Pull-up resistance : 2.2kΩ
*5 By SHARP transmitter



■ Internal Block Diagram



■ Performance

Using the transmitter shown in Fig. 1, the output signal of the light detecting unit is good enough to meet the following items in the standard optical system in Fig. 2.

(1) Linear reception distance characteristics

When L=0.2 to 5 m, Ee < 10 lx (*4) and ϕ =0° in Fig. 2, the output signal shall meet the electrical characteristics in the attached list.

(2) Sensitivity angle reception distance characteristics

When L=0.2 to 3 m, Ee < 10 lx (*4) and ϕ<= 30 ° in the direction X and θ =0° in the direction Y in Fig. 2, the output signal shall meet the electrical characteristics in the attached list Further, the electrical characteristics shall be met when L=0.2 to 5 m, Ee < 10 lx (*4) and ϕ =0° in the direction X and θ<= 15° in the direction Y.

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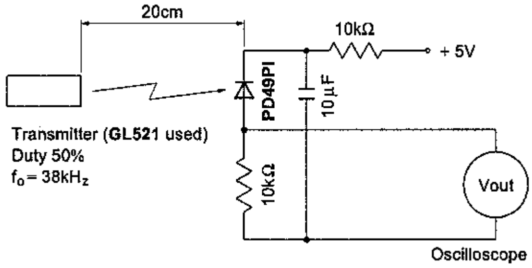


Fig. 1 Transmitter

In the above figure, the transmitter should be set so that the output Vout can be 40mV$_{P-P}$.
However, the **PD49PI** to be used here should be of the short-circuit current I_{SC}=2.6μ A at Ev=100 lx.
(Ev is an illuminance by CIE standard light source A (tungsten lamp).)

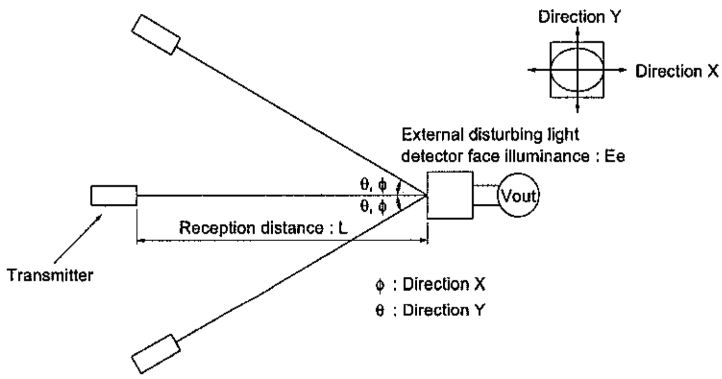


Fig. 2 Standard optical system

Fig. 1 B.P.F. Frequency Characteristics (TYP.)

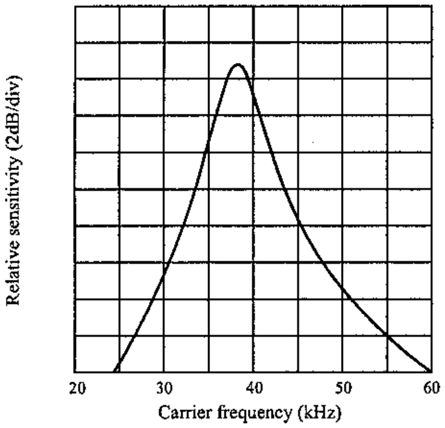


Fig. 2 Sensitivity Angle (Direction X) Characteristics (TYP.) for Reference

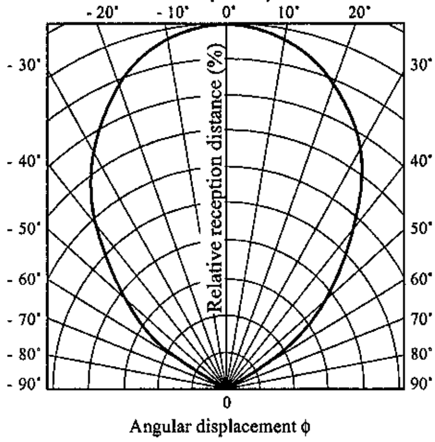


Fig. 3 Sensitivity Angle (Direction Y) Characteristics (TYP.) for Reference

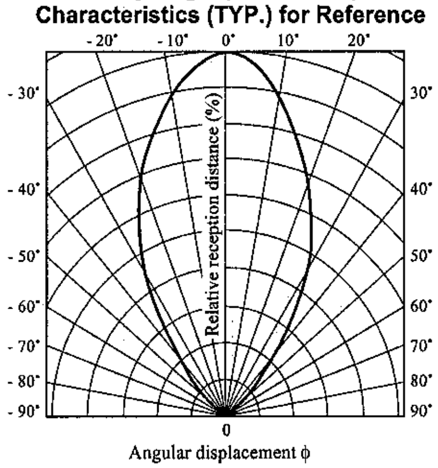


Fig. 4 Relative Reception Distance vs. Ambient Temperature (TYP.) for Reference

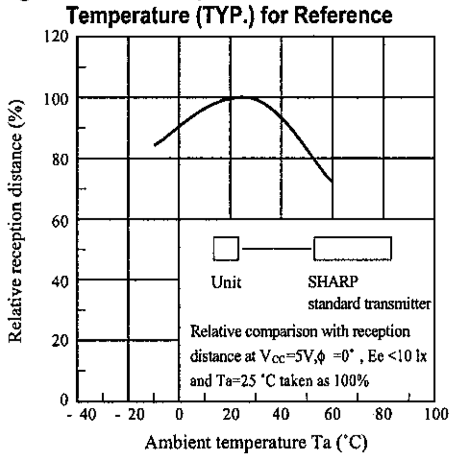
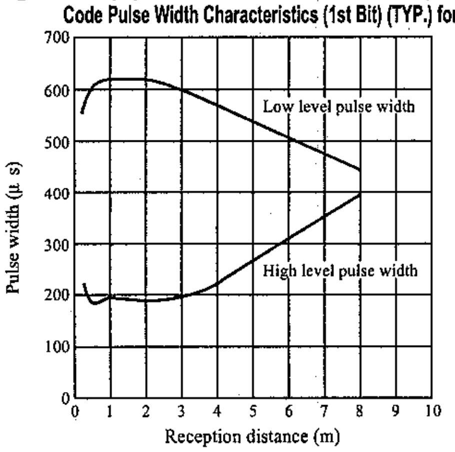
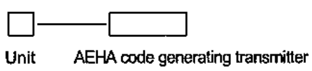


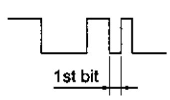
Fig. 5 AEHA (Japan Association of Electrical Home Appliances) Code Pulse Width Characteristics (1st Bit) (TYP.) for Reference



(Conditions)

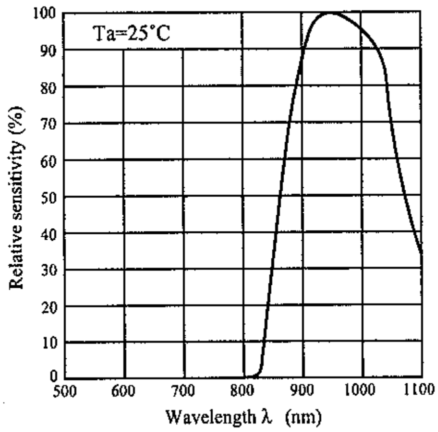


V_{CC}=5V, Ta=RT, ϕ =0° , Ee < 10 lx



T= 430µs

Fig. 6 Spectral Sensitivity for Reference



■ Precautions for Operation

(1) Use the light emitting unit (remote control transmitter), in consideration of performance, characteristics, operating conditions of light emitting device and the characteristics of the light detecting unit.

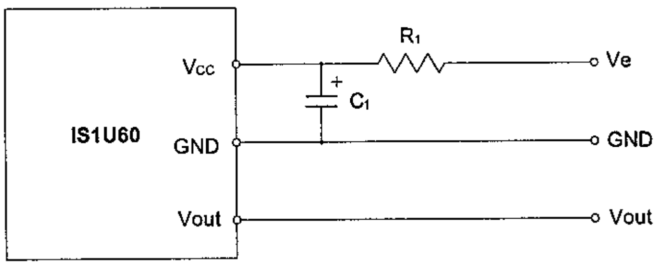
(2) Pay attention to a malfunction of the light detecting unit when the surface is stained with dust and refuse.
Care must be taken not to touch the light detector surface.
- Conduct cleaning as follows.

(3) Cleaning
Solvent dip cleaning : Solvent temperature of 45 °C max., dipping time : Within 3 minutes
Ultrasonic cleaning : Elements are affected differently depending on the size of cleaning bath, ultrasonic output, time, size of PWB and mounting method of elements.
Conduct trial cleaning on actual operating conditions in advance to make sure that no problem results.
- Use the following solvents only.
Solvents : Ethyl alcohol, methyl alcohol or isopropyl alcohol

(4) To avoid the electrostatic breakdown of IC, handle the unit under the condition of grounding with human body, soldering iron, etc.

(5) Do not apply unnecessary force to the terminal.

(6) Example of recommended external circuit (mount outer mounting parts near the sensor as much as possible.)



(Circuit constant)
$R_1 = 47\Omega \pm 5\%$
$C_1 = 47\mu F$

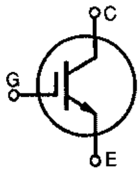
Advance Technical Data

PerFAST™ IGBT

IXGH 40N60B2
IXGT 40N60B2

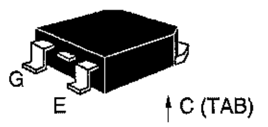
V_{CES}	=	600 V
I_{C25}	=	75 A
$V_{CE(sat)}$	<	1.7 V
$t_{fi\,typ}$	=	82 ns

:imized for 10-25 KHz hard
tching and up to 150 KHz
onant switching

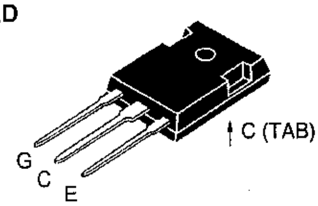


ıbol	Test Conditions	Maximum Ratings	
	T_J = 25°C to 150°C	600	V
	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
	Continuous	±20	V
	Transient	±30	V
	T_C = 25°C (limited by leads)	75	A
	T_C = 110°C	40	A
	T_C = 25°C, 1 ms	200	A
ıA 3OA)	V_{GE} = 15 V, T_{VJ} = 125°C, R_G = 10 Ω Clamped inductive load @ ≤ 600 V	I_{CM} = 80	A
	T_C = 25°C	300	W
		-55 ... +150	°C
		150	°C
		-55 ... +150	°C
imum lead temperature for soldering ım (0.062 in.) from case for 10 s		300	°C
	Mounting torque (M3)	1.13/10	Nm/lb.in.
ght	TO-247 AD TO-268 SMD	6 4	g g

TO-268
(IXGT)



TO-247 AD
(IXGH)



G = Gate, C = Collector,
E = Emitter, TAB = Collector

Features

- Medium frequency IGBT
- Square RBSOA
- High current handling capability
- MOS Gate turn-on
  - drive simplicity

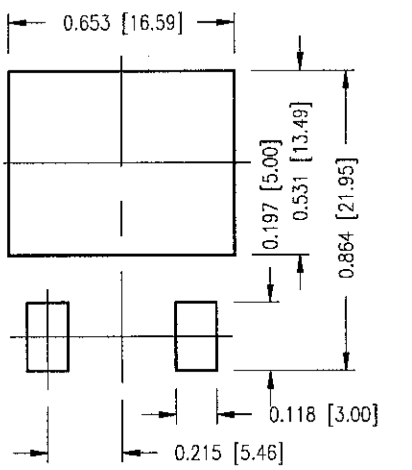
Applications

- PFC circuits
- Uninterruptible power supplies (UPS)
- Switched-mode and resonant-mode power supplies
- AC motor speed control
- DC servo and robot drives
- DC choppers

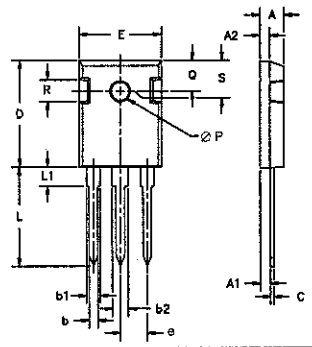
ıbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
h)	I_C = 250 µA, V_{CE} = V_{GE}		3.0		5.0	V
	V_{CE} = V_{CES} V_{GE} = 0 V	T_J = 25°C T_J = 150°C			50 1	µA mA
	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
sat)	I_C = 30 A, V_{GE} = 15 V	T_J = 25°C			1.7	V

Test Conditions	Characteristic Values (T$_J$ = 25°C, unless otherwise specified) min.	typ.	max.	
= 30 A; V_{CE} = 10 V, ılse test, t ≤ 300 µs, duty cycle ≤ 2 %	20	36		S
		2560		pF
V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		180		pF
		54		pF
		100		nC
I_C = 30 A, V_{GE} = 15 V, V_{CE} = 300 V		15		nC
		36		nC
		18		ns
Inductive load, T_J = 25°C		20		ns
I_C = 30 A, V_{GE} = 15 V		130	200	ns
V_{CE} = 400 V, R_G = 3.3 Ω		82	150	ns
		0.4	0.8	mJ
		18		ns
Inductive load, T_J = 125°C		20		ns
I_C = 30 A, V_{GE} = 15 V		0.3		mJ
V_{CE} = 400 V, R_G = 3.3 Ω		240		ns
		150		ns
		1.10		mJ
			0.42	K/W
(TO-247)		0.25		K/W

nmended Footprint
s in inches and mm)

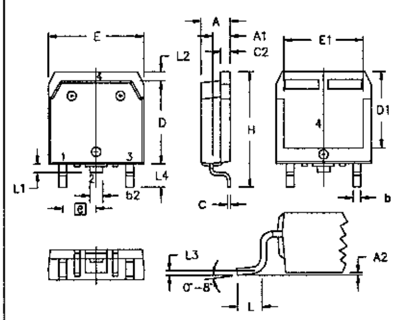


TO-247 AD Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

TO-268 Outline



SYM	INCHES MIN	MAX	MILLIMETERS MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

ɜs the right to change limits, test conditions, and dimensions.

Fig. 1. Output Characteristics @ 25 Deg. C

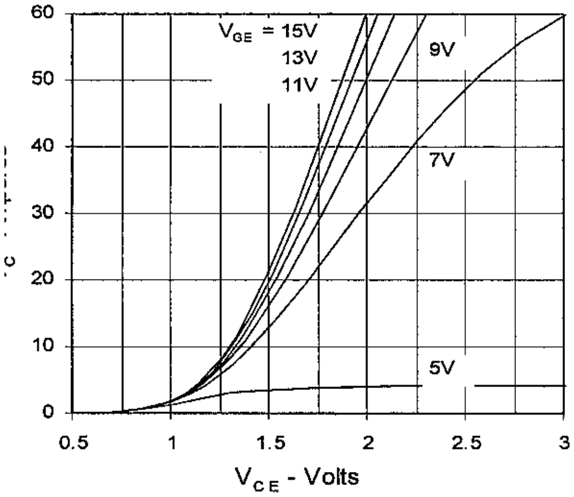


Fig. 2. Extended Output Characteristics @ 25 deg. C

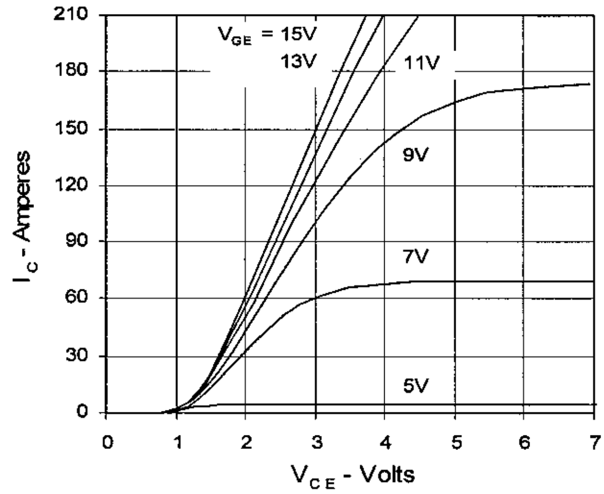


Fig. 3. Output Characteristics @ 125 Deg. C

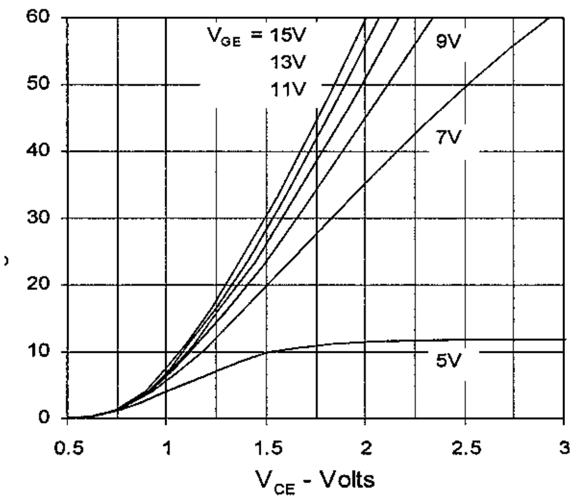


Fig. 4. Dependence of $V_{CE(sat)}$ on Temperature

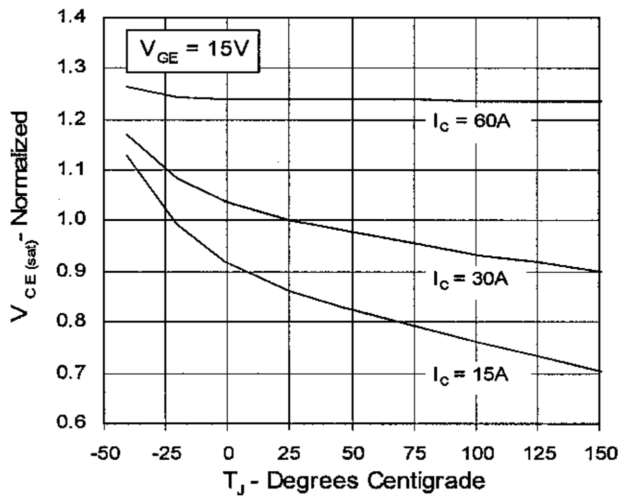


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter voltage

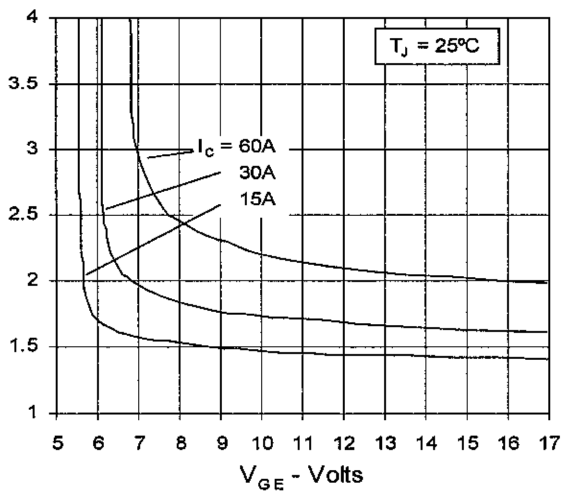


Fig. 6. Input Admittance

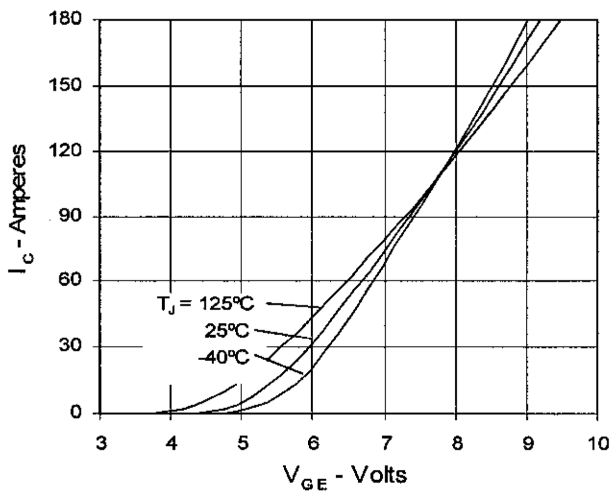


Fig. 7. Transconductance

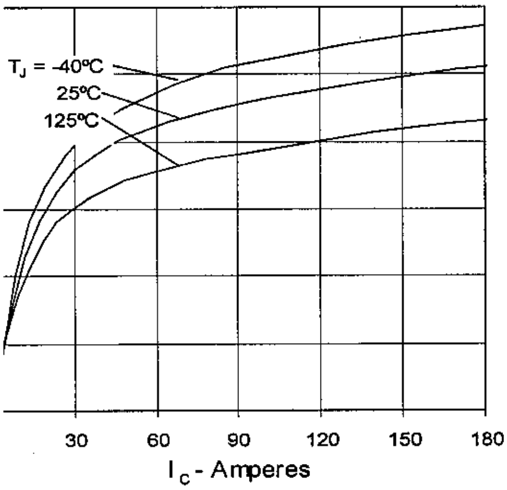


Fig. 8. Dependence of Turn-Off Energy on R_G

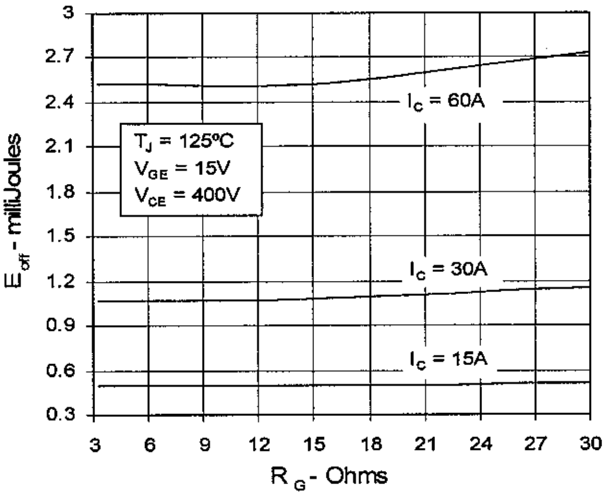


Fig. 9. Dependence of Turn-Off Energy on I_c

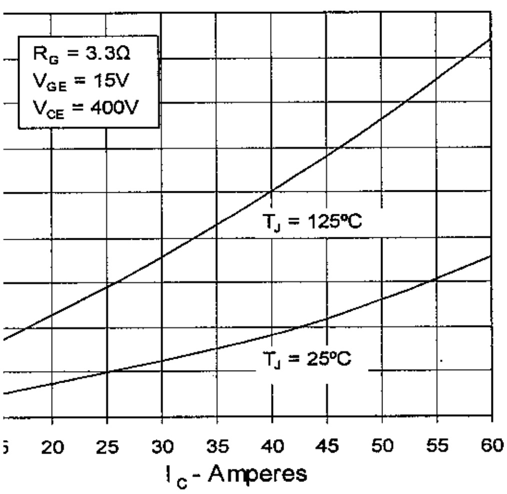


Fig. 10. Dependence of Turn-Off Energy on Temperature

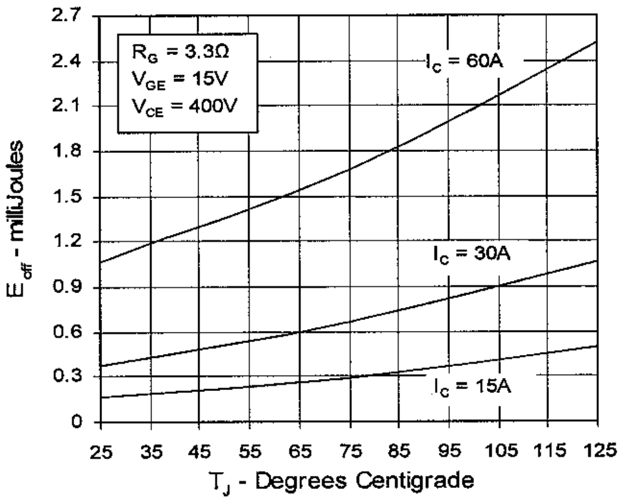


Fig. 11. Dependence of Turn-Off Switching Time on R_G

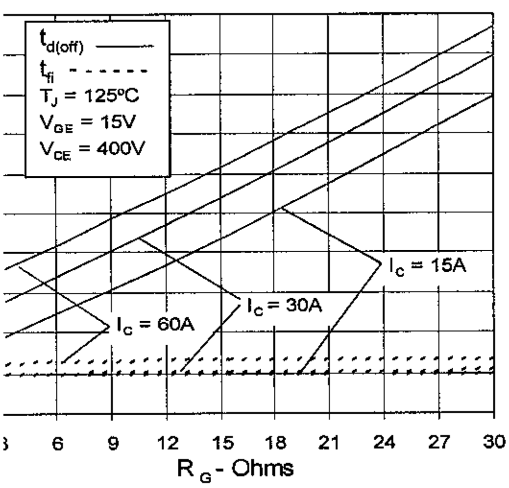


Fig. 12. Dependence of Turn-Off Switching Time on I_c

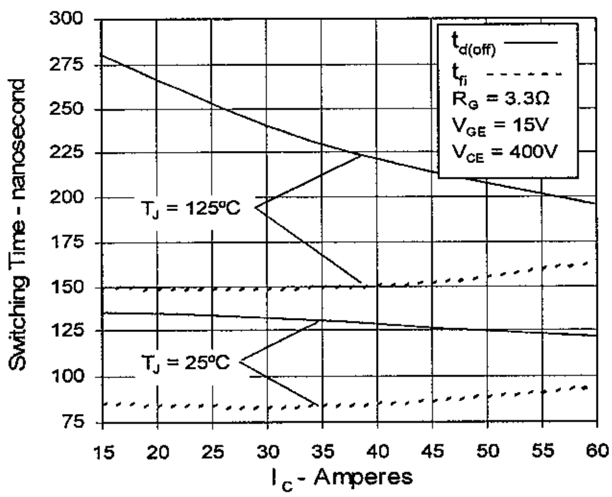


Fig. 13. Dependence of Turn-Off Switching Time on Temperature

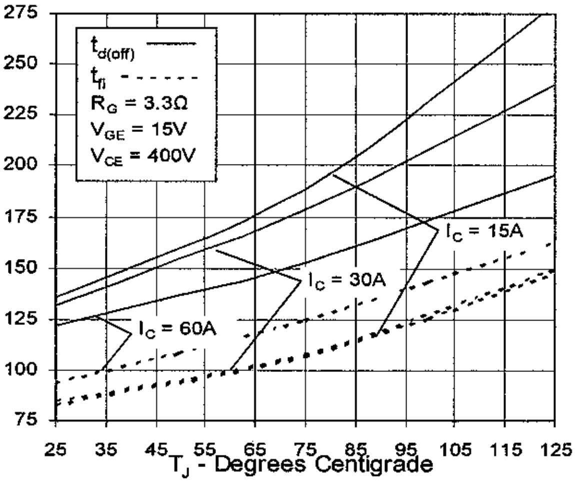


Fig. 14. Gate Charge

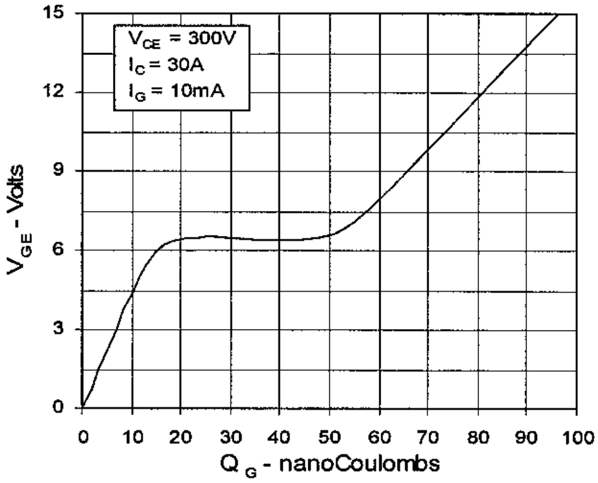


Fig. 15. Capacitance

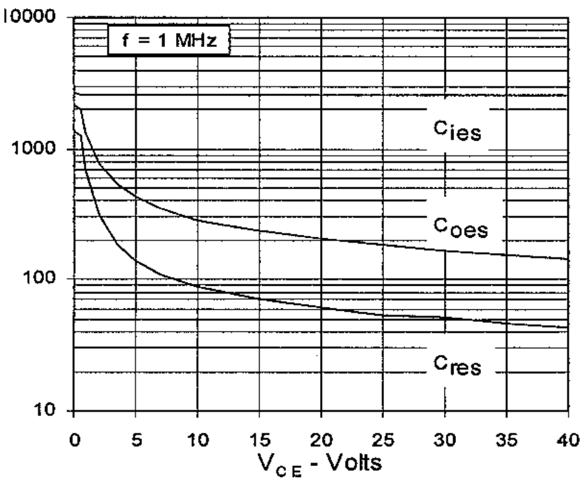
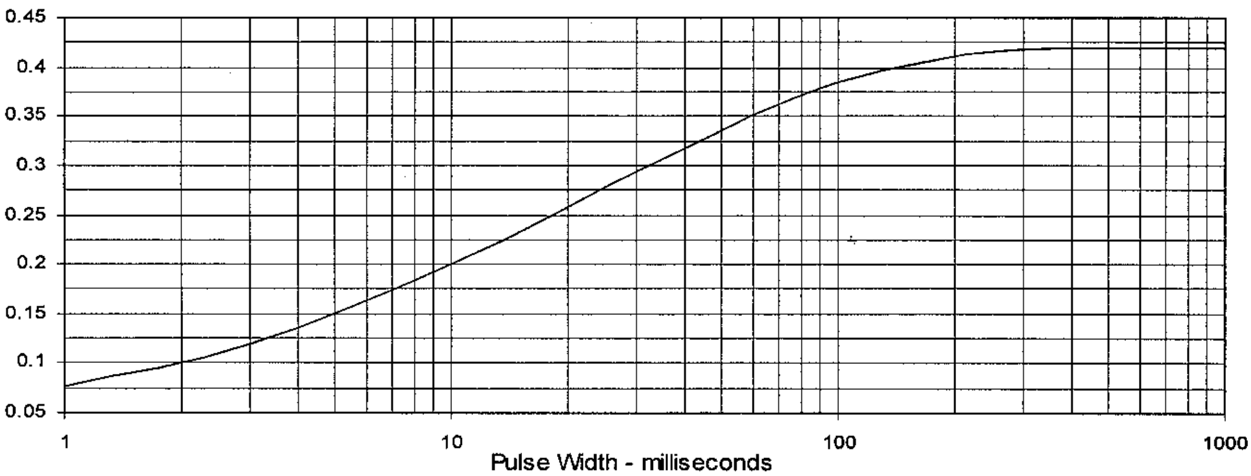


Fig. 16. Maximum Transient Thermal Resistance



FAIRCHILD
SEMICONDUCTOR™

BC556/557/558/559/560

BC556/557/558/559/560

Switching and Amplifier

- High Voltage: BC556, V_{CEO}= -65V
- Low Noise: BC559, BC560
- Complement to BC546 ... BC 550

1 TO-92

1. Collector 2. Base 3. Emitter

PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Capacitance		
	: BC556	-80	V
	: BC557/560	-50	V
	: BC558/559	-30	V
V_{CEO}	Collector-Emitter Voltage		
	: BC556	-65	V
	: BC557/560	-45	V
	: BC558/559	-30	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current (DC)	-100	mA
P_C	Collector Dissipation	500	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{CBO}	Collector Cut-off Current	V_{CB}= -30V, I_E=0			-15	nA
h_{FE}	DC Current Gain	V_{CE}= -5V, I_C=2mA	110		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C= -10mA, I_B= -0.5mA		-90	-300	mV
		I_C= -100mA, I_B= -5mA		-250	-650	mV
V_{BE} (sat)	Collector-Base Saturation Voltage	I_C= -10mA, I_B= -0.5mA		-700		mV
		I_C= -100mA, I_B= -5mA		-900		mV
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}= -5V, I_C= -2mA	-600	-660	-750	mV
		V_{CE}= -5V, I_C= -10mA			-800	mV
f_T	Current Gain Bandwidth Product	V_{CE}= -5V, I_C= -10mA, f=10MHz		150		MHz
C_{ob}	Output Capacitance	V_{CB}= -10V, I_E=0, f=1MHz			6	pF
NF	Noise Figure : BC556/557/558	V_{CE}= -5V, I_C= -200μA		2	10	dB
	: BC559/560	f=1KHz, R_G=2KΩ		1	4	dB
	: BC559	V_{CE}= -5V, I_C= -200μA		1.2	4	dB
	: BC560	R_G=2KΩ, f=30~15000MHz		1.2	2	dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

Typical Characteristics

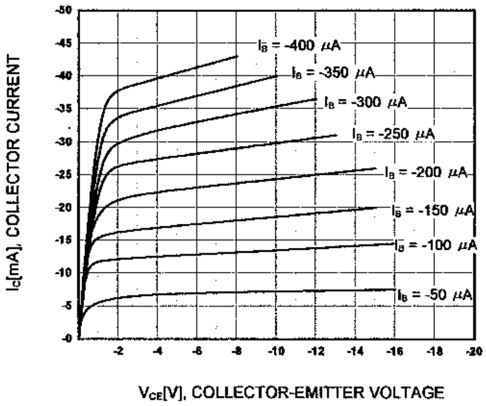


Figure 1. Static Characteristic

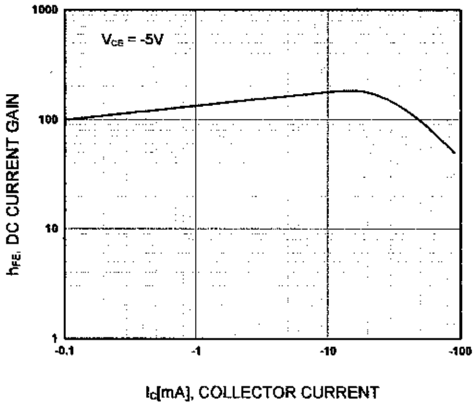


Figure 2. DC current Gain

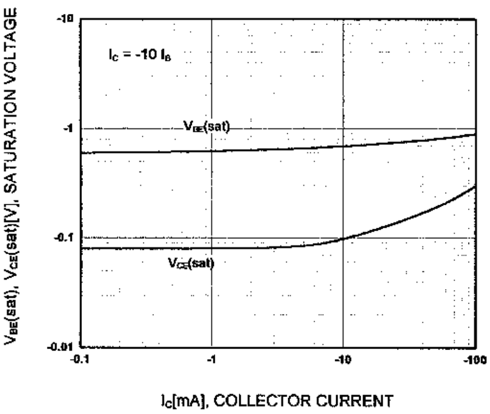


Figure 3. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

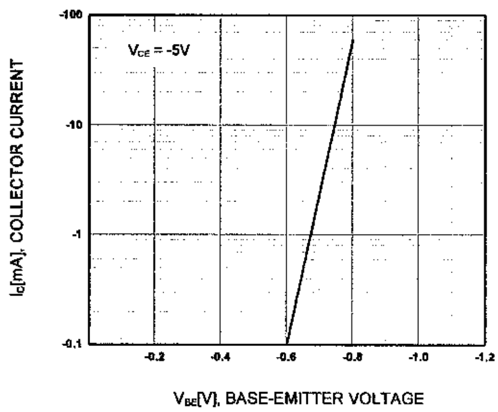


Figure 4. Base-Emitter On Voltage

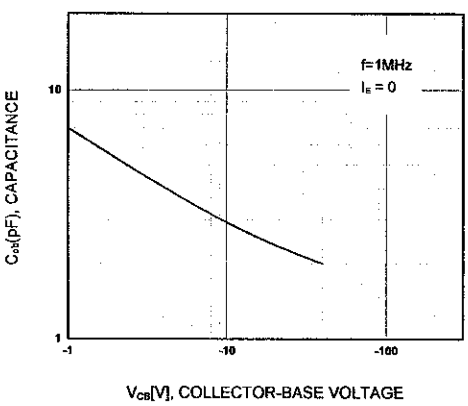


Figure 5. Collector Output Capacitance

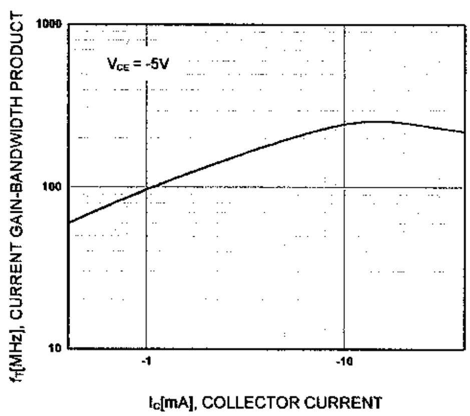
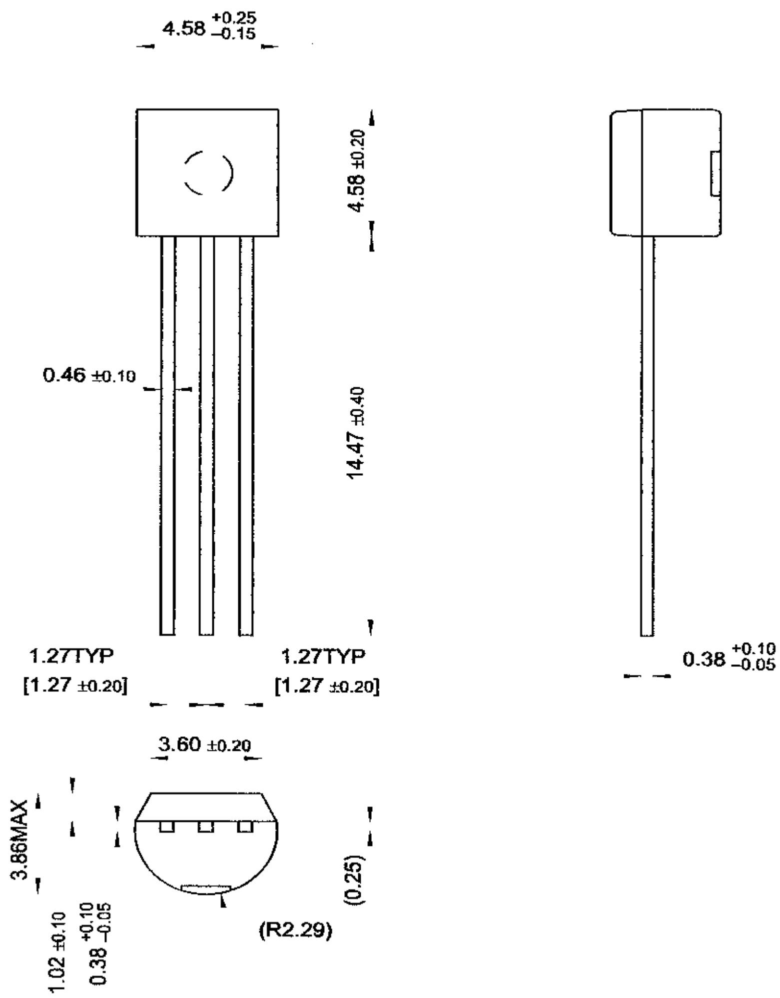


Figure 6. Current Gain Bandwidth Product

Package Demensions

TO-92



Dimensions in Millimeters

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Bottomless™
CoolFET™
CROSSVOLT™
E^{2}CMOS™
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench®
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic™
UHC™
VCX™

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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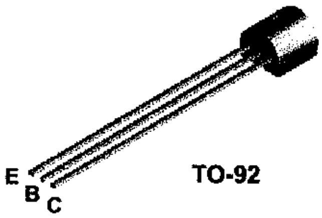
BC548B
BC548C



TO-92

NPN General Purpose Amplifier

This device is designed for use as general purpose amplifiers and switches requiring collector currents to 300 mA. Sourced from Process 10. See PN100A for characteristics.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	30	V
V_{CES}	Collector-Base Voltage	30	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	500	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

TA = 25°C unless otherwise noted

Symbol	Characteristic	Max	Units
		BC548 / A / B / C	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	°C/W

NPN General Purpose Amplifier
(continued)

Electrical Characteristics
TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0	30		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	30		V
$V_{(BR)CES}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	30		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 30 V, I_E = 0 V_{CB} = 30 V, I_E = 0, T_A = +150 °C		15 5.0	nA μA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain	V_{CE} = 5.0 V, I_C = 2.0 mA **548** **548A** **548B** **548C**	110 110 200 420	800 220 450 800	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 0.5 mA I_C = 100 mA, I_B = 5.0 mA		0.25 0.60	V V
$V_{BE(on)}$	Base-Emitter On Voltage	V_{CE} = 5.0 V, I_C = 2.0 mA V_{CE} = 5.0 V, I_C = 10 mA	0.58	0.70 0.77	V V
SMALL SIGNAL CHARACTERISTICS					
h_{fe}	Small-Signal Current Gain	I_C = 2.0 mA, V_{CE} = 5.0 V, f = 1.0 kHz	125	900	
NF	Noise Figure	V_{CE} = 5.0 V, I_C = 200 μA, R_S = 2.0 kΩ, f = 1.0 kHz, B_W = 200 Hz		10	dB