DEVELOPMENT OF ELECTRICAL CAPACITANCE TOMOGRAPHY SYSTEM DATA ACQUISITION SYSTEM FOR NON-CONDUCTIVE MULTIPHASE PROCESSES

By

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FINAL REPORT

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CERTIFICATION OF APPROVAL

Development of Electrical Capacitance Tomography Data Acquisition System for Non-Conductive Multiphase Processes

By

Muhammad Sufi bin Mansor

A project dissertation submitted to the

Electrical and Electronics Engineering Programme

Universiti Teknologi PERTONAS

In partial fulfilment of the requirement for the

Bachelor of Engineering (Hons)

(Electrical & Electronics Engineering)

Approved by:

……..

(DR. IR IDRIS ISMAIL)

Project Supervisor

CERTIFICATION OF ORIGINALITY

I hereby verify that this report was written by me, Muhammad Sufi bin Mansor (12084). I am responsible for the work that I have submitted in this project. The procedures and results achieved throughout the project were conducted with my own effort except as specified in the reference and acknowledgement.

……**.....**

(MUHAMMAD SUFI BIN MANSOR)

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Abstract

Electrical Tomography System has gained much attention these recent years as the ultimate solution of multiphase flow analysis and multiphase level analysis. It offers a Non-Destructive Testing (NDT) method that produces real-time images of cross-sectional area of an enclosed space. This provides the solution to problems involving non-conductive processes where hydrocarbon-based environment are of interest. Problems ranges from variation in the velocity profile, uneven phase distribution and flow characterization and by analyzing the multiphase flow patterns and multiphase level patterns, an accurate model of the fluid transportation could be attained. Distribution profile of the different phases are present in the multiphase transportation system can be determined across the cross sectional area during the transportation process at varying velocity and pressure. The chosen Electrical Tomography System to be developed in the project is the Electrical Capacitance Tomography System (ECT) as it has no hazardous radiation emission, low cost, able to be used in high temperature and pressure environment and its high accuracy [13]. The system is also very advantageous to be used in the measurements involving non-conducting processes and it have been proven to be very stable and accurate [13, 14]. The project will focus on the development of ECT system with some additional improvement made based on the current development of the technology. The main focus of the project is to develop a Data Acquisition System for UTP's own Electrical Capacitance System. Major focus will be given in increasing the efficiency of the Data Acquisition System by having to implement several techniques that suppress the common problems faced by the conventional Electrical Capacitance Tomography. Associated issues include the existence of stray capacitances, switching problems and speed of the system. The research will first proceeds with a comparison profile of all prior conventional Data Acquisition System developed for Electrical Capacitance Tomography and then a newer Data Acquisition System layout have been designed based on prior systems. Several test measurements involving multiphase flow analysis will be done in order to justify the accuracy and reliability of the ECT system developed. Finally, a profile of the accuracy and the reliability of the ECT system developed will be tabulated to be compared with other current developments of the system.

CHAPTER 1

INTRODUCTION

1.1 Project Introduction

Tomographic imaging system is one of the many mechanisms of modern imaging systems whereby the system allows the user to analyze the structure and composition of an enclosed space by capturing multiple sectioning or plane images of the object with the help of the numerous penetrating waves or radiation. By measuring the parameters of the penetrating waves and radiation patterns following certain measurement protocols, these signals are then treated with scientifically-derived algorithm to come up with the final image or more-accurately a vivid representation of the spatial distribution of the area of interest [3, 4].

These modern imaging systems are used pervasively in many industries such as medical industry (Cancer Detection, Brain Scans, and Preventative Medicine), continuous surveillance purposes (for industries such as Oil and Gas (OnG) Industry and Mining Industry) and fault detection purposes (Micro-crack Detection, Non-Destructive Testing (NDT)) [3].

As to date, many technologies have been developed in the domain of tomographic imaging systems. The main technologies include Optical Tomography System, Synchrotron Tomography System, Computed Tomography (CT) System and Electrical Tomography System. Electrical Tomography System can be further divided into numerous classes such as Electrical Capacitance Tomography (ECT), Electrical Resistive Tomography (ERT) and Electrical Impedance Tomography (EIT).

In petroleum industry, the transport of well products usually involves a mixture of products from different phases. These multiphase products such as hydrocarbons (methane, ethane, natural gases), water and carbon dioxide are usually send to the separator unit to determine the percentage of each product with reference of the other products extracted with it. This could range from hydrocarbon-to-water production ratio to water-to-natural gas production ratio. These products that have coexists from the underground will be extracted in such a high pressure and relatively-high temperature could pose some negative effects to the transportation system.

The existence of the multiphase nature of the products will force each individual product to interact with each other causing unexpected phase combination and uneven phase distribution. As the system is also very sensitive with pressure, temperature and the flow condition of the internal vessels, it is very important to perform measurements on these non-conductive processes in order to monitor the performance of the transport system. The solution proposed is the implementation of Electrical Capacitance Tomography (ECT) system. The system allows the user to analyze the internal multiphase flow conditions, the multiphase level conditions and to monitor any foreign formation inside the transport system itself such as the formation of hydrates and accumulation of sand particles.

In this project, an Electrical Capacitance Tomography (ECT) Data Acquisition System (DAQ) System is build to enhance the performance of the current implementation of DAQ system. Special focus is given in overcoming the common problems faced by the current system implementation. The circuit is also designed as such it could provides the flexibility of multiple electrode readings and it also provides a very stable and accurate measuring platform for the purpose of Electrical Capacitance Tomography.

1.2Problem Statement

1.2.1 Problem Identification

The extraction of hydrocarbon from oil wells poses many difficulties and one of them is the relatively-unknown end products conditions that have been obtained from the extraction process. Predictions made by geologists could not have forecast in specifics the ratio of end products, the output phase ratio and the flow condition of the end products that are obtained in the process. The products are then send to a separator unit where they will be separated to their respective types of usability and further treated properly.

Though the system seems stable and efficient, there are many flaws in the system. First and foremost, the separators are usually located far from the drilling well that makes it susceptible to disturbances and without a proper knowledge of the flow condition of the end products; it could bring adverse effects such as clogging and cracks in the system. If an efficient flow monitoring system is introduced, a real-time flow representation of the pipes could be constructed and these will give the operators a first idea of the multiphase product and it could also be used to determine the block profile of the piping systems as flow condition could differs according to the type of blockages present in a system. The flow condition analysis also eases the transportation system as piping blockage monitoring could be done via a computer and little manpower is needed on the job.

There is also a need for an accurate and continuous surveillance of the products extracted as to determine the percentage of each kind of products so that appropriate measures can be taken to the system given unexpected things happen such as a sudden surge in water inflow, sudden change in hydrocarbon throughput and formation of hydrates [1]. These fallacies could cost the production line to come to a halt and damage the instruments [5, 6]. These in turn could cost millions of dollars and use up a lot of unnecessary manpower.

Apart from that, the current Data Acquisition System that have been developed for Electrical Capacitance Tomography do posses certain number of fallacies such as low switching speed, inefficient switching mechanism and less flexible. By having an improper switching mechanism, the image reconstructed from the system would not be ideal to represent the imaging area of interest. Switch drifting is also another major problem as drifting leads to incorrect data.

Another interesting aspect of the project is the manipulation of the system implementation itself. The current Data Acquisition System is very rigid in terms of its excitation and measurement cycles. It only offers a one-excitation-one-measurement scheme where multiple electrode readings are absent. This inhibits the research development in the areas of multiple electrode readings scheme where improvements could be analyzed from. Thus, the rigidity of the system needs improvement as it will leads to a much better Data Acquisition System in the future.

1.2.2 Significant of Project

In this project, an accurate and continuous surveillance imaging system is proposed. Using Electrical Capacitance Tomography, a multiphase flow analysis could be done real-time in order to monitor any significant changes in the products of the drilling system. By analyzing the distribution of the product flow in the pipeline, appropriate changes in the treatment could be improvised real-time to further increase the quality of the product [1].

Apart from that, the formation of hydrates in the pipeline system could also be supervised as the formation takes up some time to build up in the pipes. As the imaging system detects the real-time density distribution of the pipes, appropriate treatments to the system can be made upfront to counter back the formation of the hydrates [5, 8].

The system could show the behavior of the products obtained from a well and characteristics of the well can be formulated. The flow analysis could then allow the user to observe the flow condition of the system (turbulent flow or laminar flow) and these measures can be taken to counter the effects of flow stability issues such as flow oscillations and flow reversals. The system could also be used to monitor the performance of the tubing and the casings [7].

With the development of an accurate and continuous surveillance system, the pipelines could be carefully monitored and changes can be made to regulate the maintenance of the pipelines. By implementing ECT system, blockage and hydrates formation could be monitored properly and the early counter-measures can be taken to save up hundreds of manpower and resources.

After the project is successfully completed, the system could also be used in Desalter units in oil refineries. The system could be used to effectively determine the multiphase level of the products and this will allow better control to the separation of the salt from crude oil. With the implementation of electrically-aided separators, the level of the products (water, crude oil, and emulsion layer) are important as to properly induce the separators at the appropriate levels to increase the efficiency of the system.

The project also offers a better implementation of the Data Acquisition System by having a much better efficiency in term of excitation and measurement cycles. The system also offers certain flexibility where readings from different electrodes could be taken simultaneously and more data could be extracted to come up with a better representation of the imaging area.

1.3 Objective and Scope of Project

1.3.1 Main Objective

In this project, the main objective is to develop an accurate and precise Electrical Capacitance Tomography Data Acquisition System. The new system should be able to overcome certain problems that have been faced by the prior Data Acquisition System. The development of the Data Acquisition System comprises of:

1) An efficient switching circuit that is capable in providing appropriate excitation to the electrodes and also are able to extract data from the electrodes during their measurement cycles.

2) An effective measurement layout where control units are needed to determine the switching sequences of all electrodes and also to initiates all excitation and measurement cycles for all electrodes.

3) A reliable switching conditioning circuit that could provides a stable excitation signals to the excitation electrodes and smoothes up the process of electrode measurements.

Major attention shall be given in overcoming the common problems of any Electrical Capacitance Tomography Data Acquisition System such as stray capacitances, switching drifts and low switching speeds.

1.3.2 Scope of the Project

In this project, the tomographic imaging system will be developed for the use in petroleum industry. The main scope of the project is the multiphase flow analysis for the non-conductive processes and transport part of the oil and gas industry. Special attention will be given to the analysis of the flow itself which revolves around its spatial distribution representation. These representations which are then converted to a cross-sectional image of the system will then be used to detect the flow condition, phase distribution and hydrate formation.

The project revolves around the development of an efficient, effective and high speed Data Acquisition System for Electrical Capacitance Tomography. The project would starts with a development of a comparison profile of prior Data Acquisition System associated to the project. Major attention is given to the hardware selection for the project as proper instruments and devices are needed in handling such measurements. Software development revolves around the interfacing between the measurement environment and the computer unit.

1.4 Relevancy of the Project

In this project, the main target of utilization is the petroleum industry even though it can be used pervasively in other industries such as mining industry, power generation industry and energy industry. As the need for a stable continuous surveillance system is escalating, the project is very relevant to the industry nowadays. The ECT developed could improve the multiphase flow analysis in the industry and it could significantly benefits the industry in term of proper monitoring system for fault detection and maintenance purposes. It can also be used for tubing selection and to perform tests to determine the maximum flow rates of the system.

Moreover, ECT system also offers an efficient way to observe the formation of hydrates. In the industry, hydrates have been clogging pipelines and vessels and with this efficient imaging system, the condition of the pipeline could be monitored and proper maintenance of the pipelines could be regulated better.

Apart from that, the current implementation of Data Acquisition System for Electrical Capacitance Tomography poses flaws that needed improvements and by developing a better Data Acquisition System, these flaws could be overcome and a better ECT system would be developed.

1.5 Feasibility of the Project

The duration of this project is for two semesters and this gives the author ample time to work on the development of the Data Acquisition System. In the first half of the project duration, the author would first have to perform extensive research on the subject matter as the system is foreign to the author prior to the project. The author then would come up with the comparison study of the current Data Acquisition System for Electrical Capacitance Tomography. The comparison study will consist of comparison in term of system implementation, hardware utilization and the software usage.

In the second half of the project duration, the author will come up with an extensive measurement protocol of the new Data Acquisition System. The protocol should include a measurement layout, hardware structure and software utilization. The author then would proceed in building the appropriate circuitry to perform the measurements efficiently. Several test measurements would then performed and compared to the recent literature to confirm the efficiency of the system.

CHAPTER 2

LITERATURE REVIEW

In many industries particularly the petroleum industry, many problems arise from the multiple phase nature of the product extracted from oil wells [1]. These products can range from solid-phases products such as sand, liquid-phase products such as hydrocarbons (ethane, propane) and gaseous-phase products such as natural gas, nitrogen gas and hydrogen sulfide. The production and transportation of these end-products involves multiphase flow environment where problems such as phase distribution and variation in velocity profile could severely slow down the production line [9]. Prior to the project, several methods of analyzing the multiphase analysis are proposed. Discussions involving the methods are tabulated as follows:

Suggested Methods	Advantage	Disadvantage
X-ray	• Gives a very good representation of the internal vessels • Fast response time	• Gives out radiation • Bulky in size • Impractical in its logistics
Computed Tomography (CT)	• Produces very accurate results in term of density and spatial distributions	• Bad performance for imaging dynamic systems • Bulky and logistically impractical

2.1 Electrical Tomography

In the light of recent years, attention is given to Electrical Tomography as a solution to the problem of non-conductive multiphase transport as it offers a Non-Destruction Testing (NDT) imaging method that shows promising results [10, 11]. The method can be further classified into three major classes namely; Electrical Impedance Tomography (EIT), Electrical Resistive Tomography (ERT) and Electrical Capacitance Tomography (ECT). All three measurement systems utilizes the concept of electrode-based measurements where the system would be given an input excitation and measurements between the electrodes are done to calculate the permittivity of the specimen in real-time. These data would then be processed to produce a representation of the permittivity distribution inside the experimental channel.

2.2 Comparison of EIT, ERT and ECT

EIT method was considered the most generic tool to be used in this domain especially because it measures the concentration distribution by implementing current-based measurements. Compared to the others, this method is the most simple and the lowest in term of installation cost. In reverse, the method would not yield a good representation for stratified flow or intermittent flow in a channel or in the event of foams and large bubble formation inside the experiment channel. This is caused when some of the electrodes in the system lose contact with the fluid flowing through the system [12].

The development of another method, the ERT does not completely abolish the drawbacks of EIT. ERT also does not yield a good representation of the system as the precision is usually low. However, ERT method is able to represent the system in 2-D or 3-D representation on two-phase flow [13]. Another advantage of the method is that the method allows distribution of phases to be build at various times. These advantages besides the poor throughput representation, makes ERT overrides EIT in term of NDT imaging methods.

At the same time, many researchers have been focusing on ECT. It has many advantages such as relatively low cost, absence of radiation in the system, fast response time, non-intrusive and non-invasive nature of the system [13, 14]. Apart from that, ECT systems have the advantage of being non-intrusive and non-invasive which isolates the system and the imaging area. The isolation allows its own advantage as the electrodes does not interfere with the product flow inside the area of interest. Even with the extensive advantages, ECT has a very high stray capacitance element which at times, could actually be larger than the value of the capacitance of the specimen. Thus, a lot of researches are done in order to suppress the effect of these stray capacitances to further increase the accuracy and sensitivity of the system.

2.3 Choice of Method

Based on the reviews of the three methods, the project will proceed with the use of ECT as the solution to the problem of multiphase flow analysis as it poses a wide range of advantages especially no emission of radiation as these concerns on the safety of the workforce on the oil rigs themselves. The system is also very reliable and being non-intrusive and non-invasive in nature, the method will not tarnish or affect the product flow while implemented. This is very essential as if the method used is intrusive and invasive in nature, clogs and unwanted deposits will accumulate inside the pipelines and this could lead to a major blockage. It will also tarnish the quality of the product and even affect the performance of the overall imaging system.

After reviewing all the possible solutions and comparing them to obtain the most optimal method to be used to solve the existing problem, the development of the method itself are now in focus. The design that have been developed will then be fabricated, tested and verified for their accuracy and reliability.

2.4 Capacitive Sensor Element

Capacitance is a measure of the capacity of a body to store electrical charge either positive or negative. Anything that is able to be charged will exhibit capacitance. This includes parallel-plate capacitors, ceramic capacitors and touch-screens. It is formed when conducting bodies are separated by a medium and a voltage is applied across the conductors. An accumulation of equal but opposite in polarity of charges will be deposited at the surface of the two separated bodies. The charges are distributed evenly throughout the body and each point on the body has the same relative ground voltage.

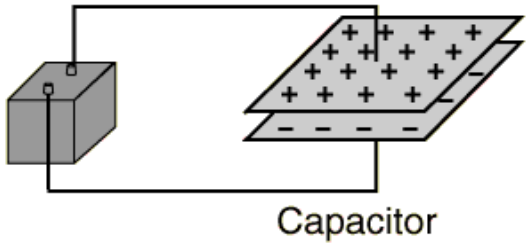


Figure 1: A typical capacitance phenomenon

When a voltage is applied across the plate structure, the plates will be having an electric field connection between them. If an insulator is to be put in the middle of the plates, the value of the capacitance will increase by a particular value. Permittivity is a measure of the ability of the material to allow electric fields interaction. The same concept is applied in ECT where by measuring the voltage and the capacitance between the electrodes (analogous to the plates), a permittivity and density distribution graph could be attained by implementing special mathematical formulae for the tomographic reconstruction algorithm.

Based on the same principle, an ECT sensor system utilizes the concept of capacitance to attain the needed representation of permittivity distribution. The typical structure of an ECT sensor system is shown in Figure 2 [1].

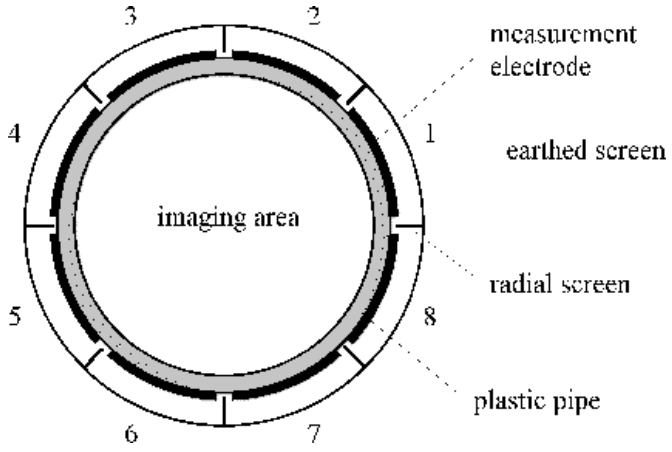


Figure 2: Typical Set-up for ECT Sensor

The main component of the sensor system is the Electrode which the medium for the accumulation of electrical charge and it is essential as the point of measurement to detect the capacitance of the system. The capacitance in ECT system will be measured in between any two combinations of the electrodes by inferring one of the electrodes as the main input electrode [13]. The input electrode hence is called the excitation electrode, bearing the excitation signal to the system and the other electrode is called the measurement electrode conveying the signal level it's detected to the consequent part of the system. The earthed screen functions as a barrier that separates the signal from the sensors and any nearby source of interference such as any devices that utilizes electromagnetic waves and these can induce the presence of interference to the system and any deviation of results would leads to inaccurate representation of the tomographic images. This in turn suppresses noise presence in the system and increases the system's efficiency. The function of the radial screen unit is to suppress the effect of stray capacitance interactions between the electrodes [15].

Another interesting aspect of the build-up of the sensor system is the number of electrodes used in the system. ECT systems usually use eight or twelve number of electrodes systems though it is not rare to find other number of electrodes such as four electrode systems and thirty two electrode systems. Naturally, the more electrodes used in the system, the more

accurate the resultant representation will be. Bear in mind that for a similar dimension unit, more number of electrodes will forces the electrodes to be smaller which in term does not yield a good result [33]. Several optimization researches have been done on the subject and ultimately, the most recommended and preferable number of electrodes to be used in an ECT system is twelve electrode systems [15] as it yields the most optimal representation of the flow condition in most cases.

There are also other benefits of keeping the number of electrodes to a twelve as fewer electrode systems will further simplify the data acquisition system design needed to accommodate such number of electrode systems. The systems are simplified in term of fewer channel are to be used for data collection, less complicated switching circuits and reduces the number of coaxial cables and Sub-Miniature Version B (SMB) plugs used in the system [14, 15].

Sensor placement design also plays a part on the end representation of the internal condition of the measurement area. Logically, a more thorough coverage of the sensor would yield a better representation [22]. Several other arrangements for the ECT Sensor System include:

1) Two paralleled metal plates attached to the interior of a pipe or placed at the exterior of the pipe wall.

2) Two concave metal plate attached to the interior of the pipe or placed at the exterior pipe wall

3) Several concave metal plates attached spirally in stair-like fashion surrounding the exterior pipe wall.

The accepted design for the project is chosen to be the typical ECT Sensor System arrangement where copper plates are placed at specific intervals surrounding only a plane of the whole pipe. The design is chosen because there is no need for a multi-plane image representation. The one-plane image representation has proved to be sufficient to be used in the analysis of multiphase issues. The design is also chosen as to simplify the software algorithm used in the project as the usual Mixture Model Correlation could not be used in this case.

Sensor application to the system also could vary from system to system. Naturally, a thinner pipe or enclose wall layer is preferred than thick wall layer as it will yield a better result [14]. The differences in sensor system application can be divided into two main classes; invasive sensor system or non-invasive sensor system. Invasive sensor application is applied in the interior part of the enclosed wall and this method has gained its popularity by yielding a better representation and more accurate results from its measurements [16].

This is due to the direct contact of the electrodes with the measurement area at test and errors derived from the wall layer capacitance are suppressed completely. The disadvantage of this system implementation is that the sensor itself is in the way of the flow inside the measurement area which would affect the real flow of the fluids in the measurement area.

Inversely, the direct contact makes the system susceptible to other disadvantages such as material deposits can attach to the electrodes making it inaccurate and these depositions could also blocks the flow in the wall layers. Non-invasive sensor application is implemented by attaching the sensors along the exterior layer of the wall layer. This method does not involve direct contact between the electrodes and the measurement area. Even though it is not as accurate as Invasive method offers, it relieves the system from regular maintenance of the electrodes and the probability of blocking the wall layers itself. Also, as it does not involve direct contact with the measurement area, fluid-based measurements can be performed more accurately as the method does not interrupt the real flow condition of the measurement area.

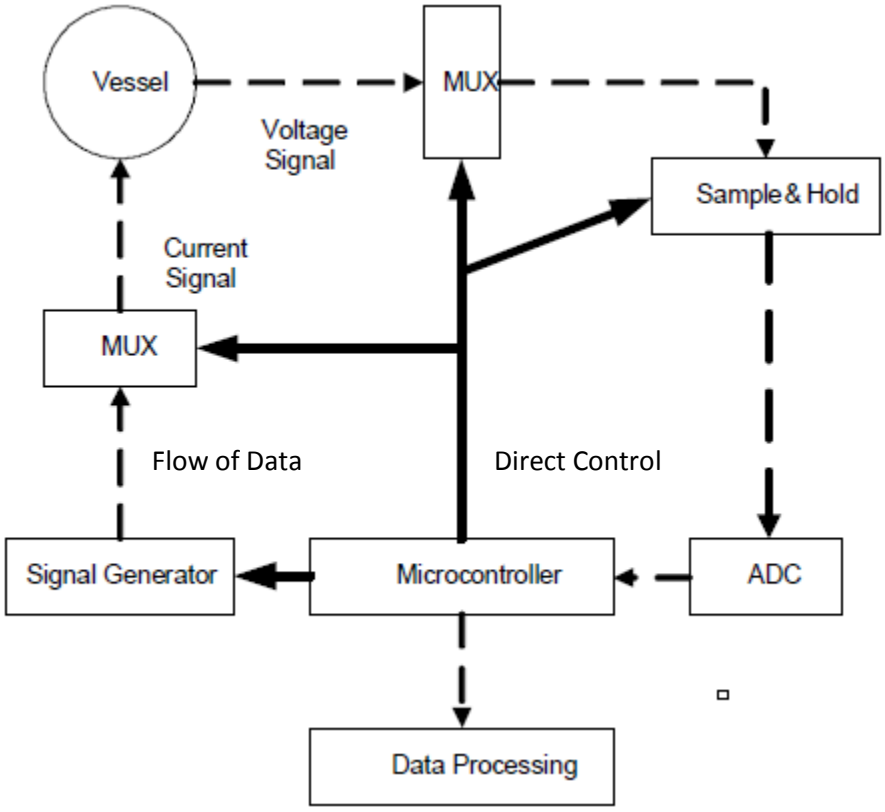
2.5 Data Acquisition System Element

In order to communicate between the sensor element and the computer implementation element, an effective Data Acquisition System (DAS) is to be developed. Several models of Data Acquisition Models have been studied and their pros and cons are determined. The results are tabulated below:

Contributor	DAS Remarks	Advantage(s)	Disadvantage(s)
Baloch, T.M et al. [17]	Microcontroller-centralized system to control switching and flow control of the system. An AC-Based DAS utilization.	• Simple circuitry with centralized control • Relatively easy to be executed	• End image is not accurate and reliable.
Yang, W.Q. [28]	PGA-centralized system that uses Direct-Digital Synthesizer (DDS) units.	• A more complex circuitry approach • Acceptable speed at 100 frames per second	• The effect of stray capacitance is too significant • Limited frequency range of excitation signal
Ying, J [29]	Another microcontroller-utlized circuitry with external program storage and control chips	• Yields a good results • Fast speed at more than 100 frames per second	• No centralization of the control mechanism • Complicated architecture

In the initial part of the project, the first model is first deemed to be used is the microcontroller- centered Data Acquisition System [17]. The choice is made as the system layout provides a complementary system where any changes can be made through the microcontroller and this saves up time if any change in the system is required. The fast speed, ample resources and sufficient accuracy for the project are also the factors that lead to the choice. Thus, the basic ECT Data Acquisition System used in this project should composed of a signal generator block, switching circuit block, sample &hold block, Analogue to Digital Converter block and a main controller block [17]. The following flow diagram shows the operation of a complete and functioning ECT Data Acquisition System.

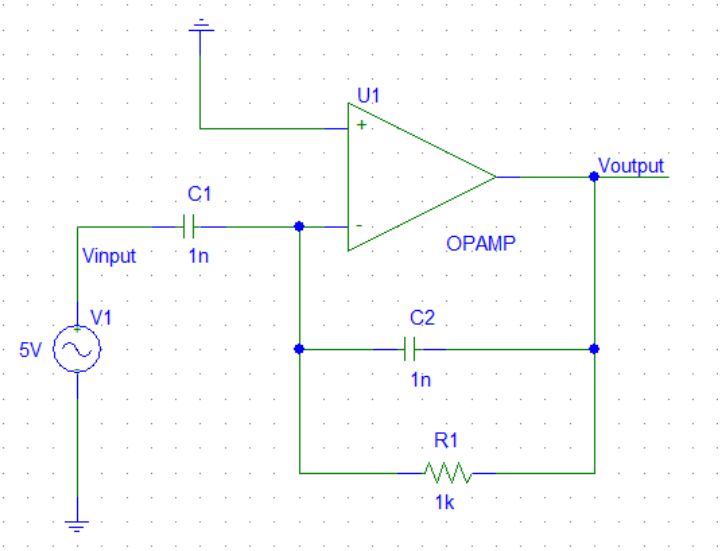
The basic ECT Data Acquisition System should composed of a signal generator block, switching circuit block, sample &hold block, Analogue to Digital Converter block and a main controller block [17]. The following flow diagram shows the operation of a complete and functioning ECT Data Acquisition System.



Data Acquisition Model for ECT [17]

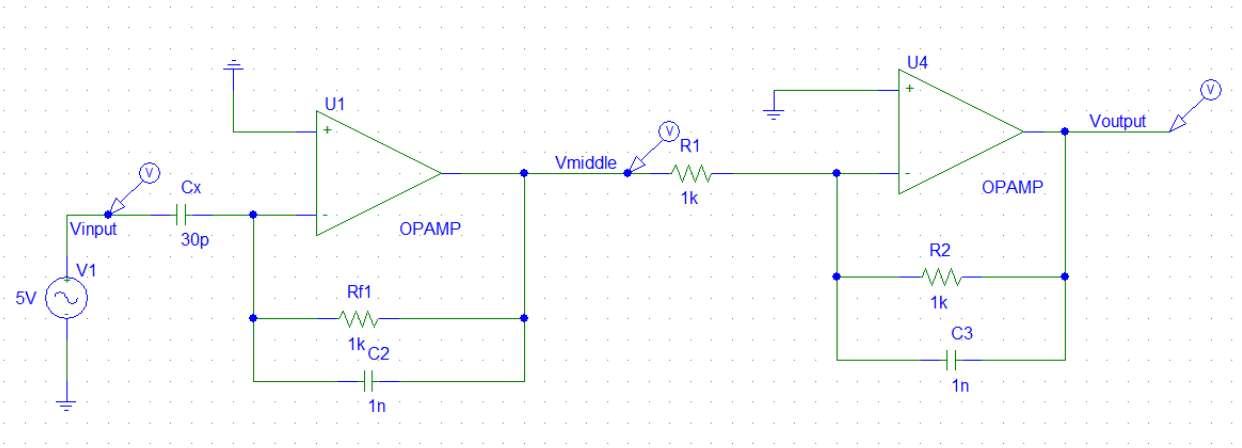
Another reason for the choice is that the system centralizes the entire Data Acquisition System using a Microcontroller [17]. This is in contradictory with another model of Data Acquisition System Model which utilizes the front compensation technique. In this technique, the data in the Signal Processing Unit will go be converted back to analogue signals and the reverse processing are implemented to obtain the minus nature of the input in measurement circuits [18]. Though the technique is working well in performing multiphase flow analysis, the complex design and algorithm implementation requires advance technology and expensive devices.

The Signal Generator block in the Signal Conditioning Circuit functions as to supply the system with the appropriate type and level of excitation signal to the system. The design of the signal generator block must contain the appropriate treatment of the signal generated and also noise treatment in order to sustain a stable input to the system. The first design is a very compact design with just a capacitance C1 as the filtering mechanism [31]. The measurement circuit is fairly simple without the use of many capacitors and resistors. It utilizes the properties of the operational amplifiers such as the infinitely large resistance value between the positive terminal and negative terminal to create isolation.



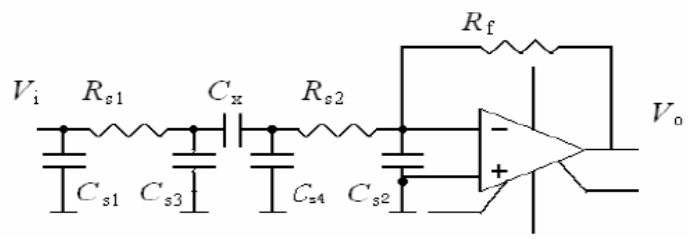
First Design of DAS [31]

The second design to be reviewed are called the Low Capacitance Measurement Circuit and it is considered a good design as most of the capacitance values obtained in utilization of ECT are of low magnitudes. The design is as follows:



Second Design of DAS [18]

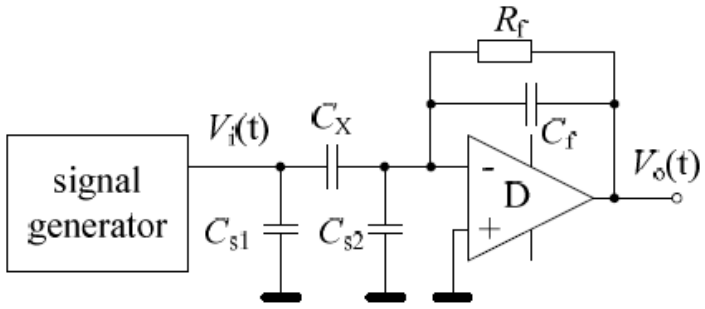
In this DAQ system, the unit is divided into two parts which are the signal generation part and the amplifier part. The design is good in term of the application of capacitance to filter out noise and to obtain a stable input operation to the system. The system also has an amplifier part that can be tuned to meet the specification of the users. However, the systems have a major drawback which is the existence of stray capacitance. The full stray capacitance profile is as follows:



Stray Capacitance Profile of Design 2

As seen from the above diagram, the design poses a big issue in its stray capacitance problem. Several tunings of the values of the elements can be made and an additional compensation circuit is suggested [18]. These major drawbacks have made this design impractical and another set of design is reviewed.

The third design of the system poses many advantages. The design developed has a very high speed response, unaffected by stray capacitance effects and it has a very low drifting level. This Ac-based capacitance circuit is shown below:



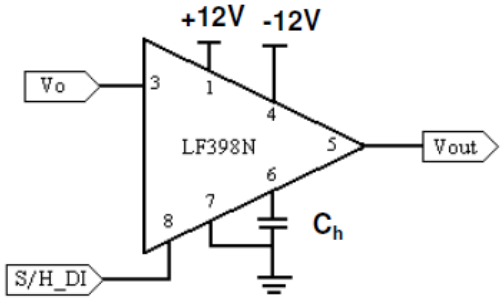
Third Design of DAS [19]

The utilization of the system must be done carefully as certain considerations must be made in order to produce a high speed and accurate signal generating circuit [19].

1) The value of $R_f\omega C_f$ must be significantly higher than 1 in order to make the system's sensitivity not dependent to the excitation frequency and to make it only controlled by the voltage at the excitation side and the feedback capacitance.
2) The value of $R_f\omega C_f$ must be significantly lower than 1 as otherwise, the system will acquire more acquisition time and this will limits the speed of the system. There is also the problem of the phase shift of the output signal but it can be overcome with the use of oscillators.
3) The value of $R_f\omega C_f$ must be carefully chosen as to create a system that does not directly relates the sensitivity of its performance with the excitation frequency but it is fast enough to be used real-time.

The design can be utilized as proper tuning would make the design immune to stray capacitance effects and it is not require additional circuitry that makes it more complicated.

Sample and hold circuit is used in the system as it will keep the information in place while waiting for the measurement to finish. Proper Sample and Hold (S&H) Circuit is needed to ensure the correct arrangements of the measurement data are done and for signal synchronization purposes. This type of circuitry also is usually used before an Analogue to Digital (A/D) Converters to ensure proper sampling and synchronization [19]. The design for an efficient S&H circuit is as follows:



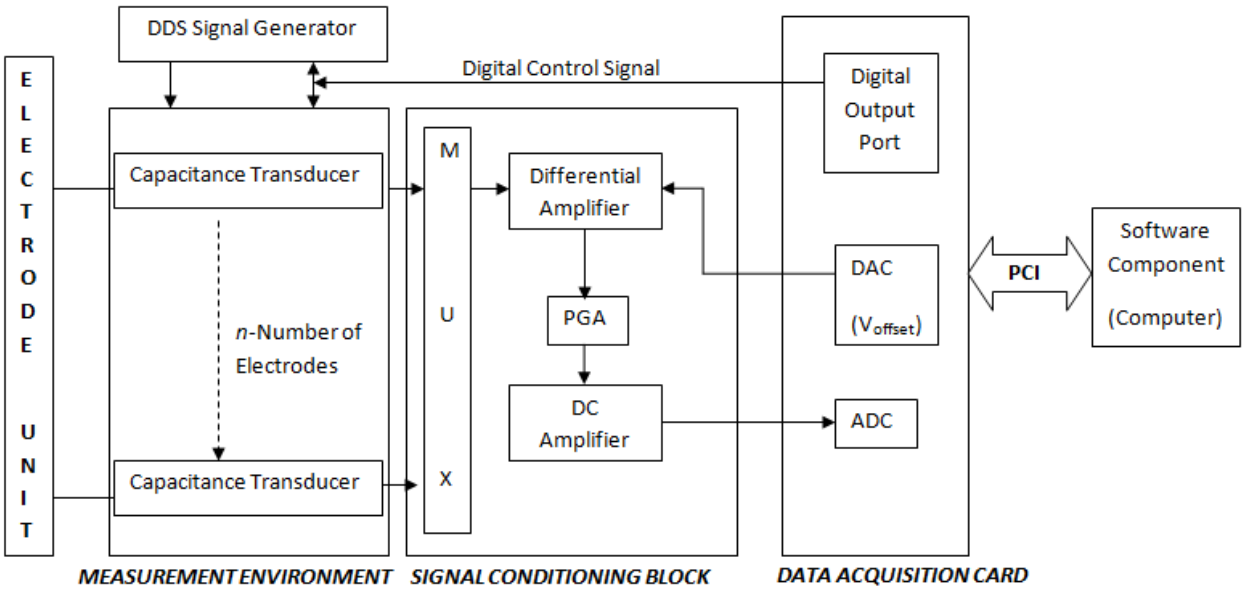
Design of the Sample and Hold Circuit

The circuitry have a very good droop rate that represents the discharge rate of the system, a very fast acquisition time and have a very high input resistance and low output resistance [21]. These characteristics are essential in the development of a good sample and hold circuit.

Another very essential component in the Data Acquisition System is the switching Circuits. In the ECT system, switching is needed in order to manage the activation and deactivation of all of the electrodes. A typical eight electrode ECT system measurement will starts the acquisition process by activating Electrode 1 and measuring the potential between Electrode 1 and 2 (C_{12}). The next round of measurement will involves Electrode 1 to be reactivated again and the potential is measured between Electrode 1 and Electrode 3 (C_{13}). The process repeats itself until the value of C_{18} is obtained. Then, Electrode 2 will be activated and the value of C_{23} is determined followed by C_{24} until C_{28}. The cycle continues until it reaches expected number of measurement which is given by:

$$Measurement\ No = \frac{(Electrode\ Number)(Electrode\ Number - 1)}{2} = \frac{8 * (8-1)}{2} = 28$$

After much reconsideration and reviews, a newer method that takes into accounts all advantages and disadvantages of the previous reviewed methods have been devised. The reason for the change is that the microcontroller-based system is so centralized to the microcontroller itself and if any faults or problems were to happen to the microcontroller, it will annihilate the whole measurement protocol. The following diagram illustrates the new approach that had been considered for the project.



Layout of the new Data Acquisition System Architecture [7]

As stated before, an AC-based ECT system owns an advantageous curve compared to the other methods as it results in accurate, precise results without having to design complex systems. DC-based ECT system has also been reviewed but due to the unreliable results and complex circuitry, AC-based ECT system is used.

A microcontroller-based system is a good system to be used but it poses its own drawbacks. With ample programming, a microcontroller is flexible and fast but it does not have enough speed to become a high-speed ECT system. It is also hard to interface the microcontrollers with the computer as well as the sensor setup. The compatibility issue is the main reason as to why the microcontroller based system is deemed insufficient for the project. Apart from that, if any changes were to be made with the microcontroller itself, the device needs

to be extracted out of its circuitry and onto the microcontroller platform to be reprogrammed before reinstallation. This is very troublesome and could leads to a very inefficient system.

In conjunction to the objective of the project which is to develop a better ECT DAS system, a newer method that centralizes around the National Instrument Data Acquisition System is chosen. The method is an improvement of the previous methods as the National Instrument Data Acquisition System is very compatible with the sensor setup being build. It is also readily compatible with any PC configurations such as PCI and USB configurations.

The method also offers better architecture as the system would be centralized to a Data Acquisition Card and changes can be made straight to the card. There is no need for extraction or reinstallations of microcontrollers to the modules as the card itself is build equipped with other modules such as filtering modules, multiplexing modules and counter modules. The system is also very flexible in term of speed as the system can be applied to a high-speed system and also to a low-speed system. This is very useful for demonstration and industrial purposes as several applications do not require such high speed but they require more clarity of the readings.

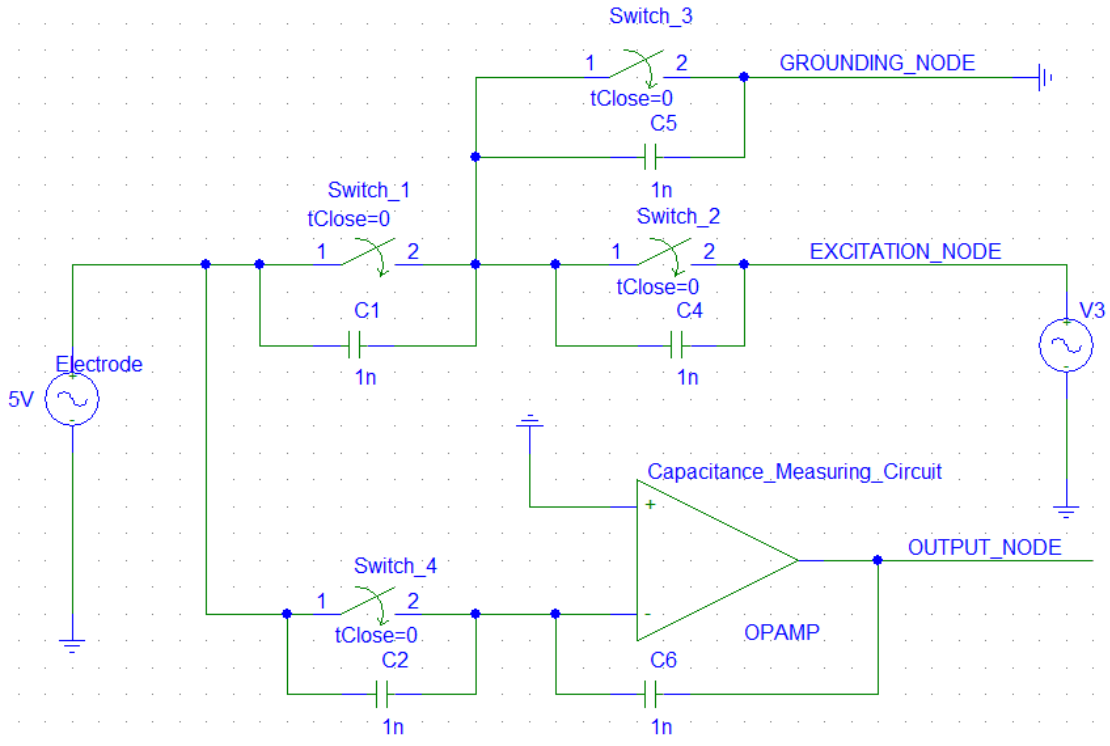
Another major reason for the change is that the system is readily compatible with any National Instrument Software such as National Instruments Laboratory Virtual Instrumetation Engineering Workbench or more commonly known as NI LabVIEW. All programming and synchronizations can be made via the software and its flexibility and familiar interface environment provides better options for the programmers. Ultimately, the system offers better results than the microcontroller-based system as it is more accurate, precise and faster which leads to a better end representation of the imaging area.

As illustrated before, switching component is very important to ECT system. There are many switching devices that are readily available and a comparative study is done to choose the most optimal switching device to be used in the ECT system.

Device	Advantage(s)	Disadvantage(s)
Manual Switch	• Easy to troubleshoot • Cheap	• Slow • Requires manual control
Bipolar Junction Transistor (BJT)	• Fast speed up to milliseconds • Easy to implement	• Requires external circuitry elements for appropriate biasing
Metal Oxide Semiconductor Field Effect Transistor (MOSFET)	• Very fast response up to nanoseconds	• Very sensitive to static
Relay Unit	• Able to handle large current and voltages • Fast switching speed up to milliseconds	• Bulky in size compared to others • Risk of synchronization drift
Monolithic CMOS device (ADG 201A)[32]	• Very fast switching time • Stable • Large signal handling capability (±15V)	• Static sensitive

In the project, the Monolithic CMOS device ADG 201A is used. The device is a quad-switch module that operates independently. As it is developed using the LC2MOS process, it has a very high range of analogue signal tolerance of ±15V and it also has a high breakdown. It operates on the inverted logic control mechanism and it has a very high switching speed of 33MHz.

As stated before, a newer method would be used in the system. An utmost vital aspect in ECT Data Acquisition System is the capacitance measuring circuit. Without a proper capacitance measuring circuit, the system would not be able to produce results for a good end representation of the imaging area. An approach is taken where a separation of the signal generator block and the capacitance measurement circuit is no longer needed. The new method would combine the two blocks in coming up with a new circuit that could control the excitation of the electrodes and the capacitance measurement of the electrodes. The circuit is as follows:



Circuit Diagram of ECT Signal Conditioning Circuit [33]

The above diagram illustrates the chosen Signal Conditioning Circuit that is used in the project. In this mechanism, the electrode acts as both a voltage source and a voltage detector. The electrode could only be in one state in a particular time and not both states simultaneously. The electrode is connected directly to the excitation signal source through switch 1 and switch 2. The switches are placed in parallel to a capacitor as this is to suppress the effect of stray capacitance. Consequently, switches 3 grounds the excitation signal when required to and switch 4 connects the electrode to the capacitance measuring unit which consists of an operational amplifier, capacitors and resistors. The operational amplifier is used to completely isolate the measurement environment with the other blocks.

There are two modes of the electrode namely the excitation mode and the measuring mode. In excitation mode, Switch 1 and Switch 2 would be activated and Switch 3 and 4 would be deactivated. This is to allow the signal from the sine wave generator would be connected to the electrode as to excite the imaging area appropriately. Switch 3 is deactivated as to prevent the excitation signals to be earthen. Switch 4 is also deactivated as no measurements are to be done in this mode.

In the measuring mode, Switch 1 and 2 would be deactivated and Switch 3 and 4 would be activated. Switch 1 and 2 are closed as to prevent the signals from the electrode to coincide with the excitation signal. Switch 4 is activated as to allow the measured signal to be connected to the Capacitance Measuring Circuit (LM6264). Switch 3 is close as it connects the coupling capacitance to earth and help to remove the effect of inter-electrode capacitance. A main concern in using a CMOS analog switches are the effect of switch coupling capacitances which indirectly connects the sine wave signal generator to the electrodes. This partial connection between the two could interfere with the measuring signals that lead to incorrect data. Thus, by activating switch 3, the sine wave signal would not get connected as so and it will get grounded providing the electrode with the isolation it needs.

The main advantage of the circuit is that it integrates both crucial part which is the excitation and measuring modes of the system making the system more compact and efficient. In order to achieve this, it is very vital that the switches are controlled systematically as to prevent possible errors such as synchronization errors and leakage currents. Furthermore, it applies the

concept of an AC-Based ECT system that have been proved to be very efficient in coming up with accurate representation of the imaging area [34].

2.6 External Computer Element

The last ECT block is the External Computer block or the tomographic image reconstruction block. This block deals with the interpretation of the measured data and translates it into meaningful representation with a user-friendly environment. The image reconstruction implementation in ECT system poses its own challenges as there are many irregularities and uncertainties in these multi-component and multi-phase systems [23]. As for these reasons, there is no one general solution to the reconstruction of the images. Often, a numerical-based approach is taken to tackle the irregular nature of the system. The two commonly-used algorithms for ECT systems are Linear Back Projection (LBP) method and Linear Forward Projection (LFP) method [13]. The main difference of the two methods is that LBP is a non-iterative method while LFP is an iterative method. Another notable solution to the problem is the development of Radial Basis Function method developed recently [23]. The following table shows the distinctive properties of the current leading image reconstructive methods.

Image Reconstructive Method	Advantage(s)	Disadvantage(s)
Linear Back Projection (LBP) Method (Non-iterative Method) [24, 25]	• Fast speed • Less complicated algorithm • Very useful for on-line imaging purposes	• Less Accurate • Threshold filters are needed to reduce blurring effects • Not useful in most advanced applications where higher accuracy and speed is needed.
Linear Forward Projection (LFP) Method (Iterative Method) [26]	• Produces better and more accurate images compared to LBP • Does not rely on sensitivity matrix for the forward problem modeling of measurement area	• Iterative in nature that makes it slower than LBF • More complicated than LBP Method
Radial Basis Function (RBF) Method [23]	• Produces more reliable representation of the measurement area	• Slower in response • More complicated as it involves nonlinear functional mapping of the inputs and the outputs

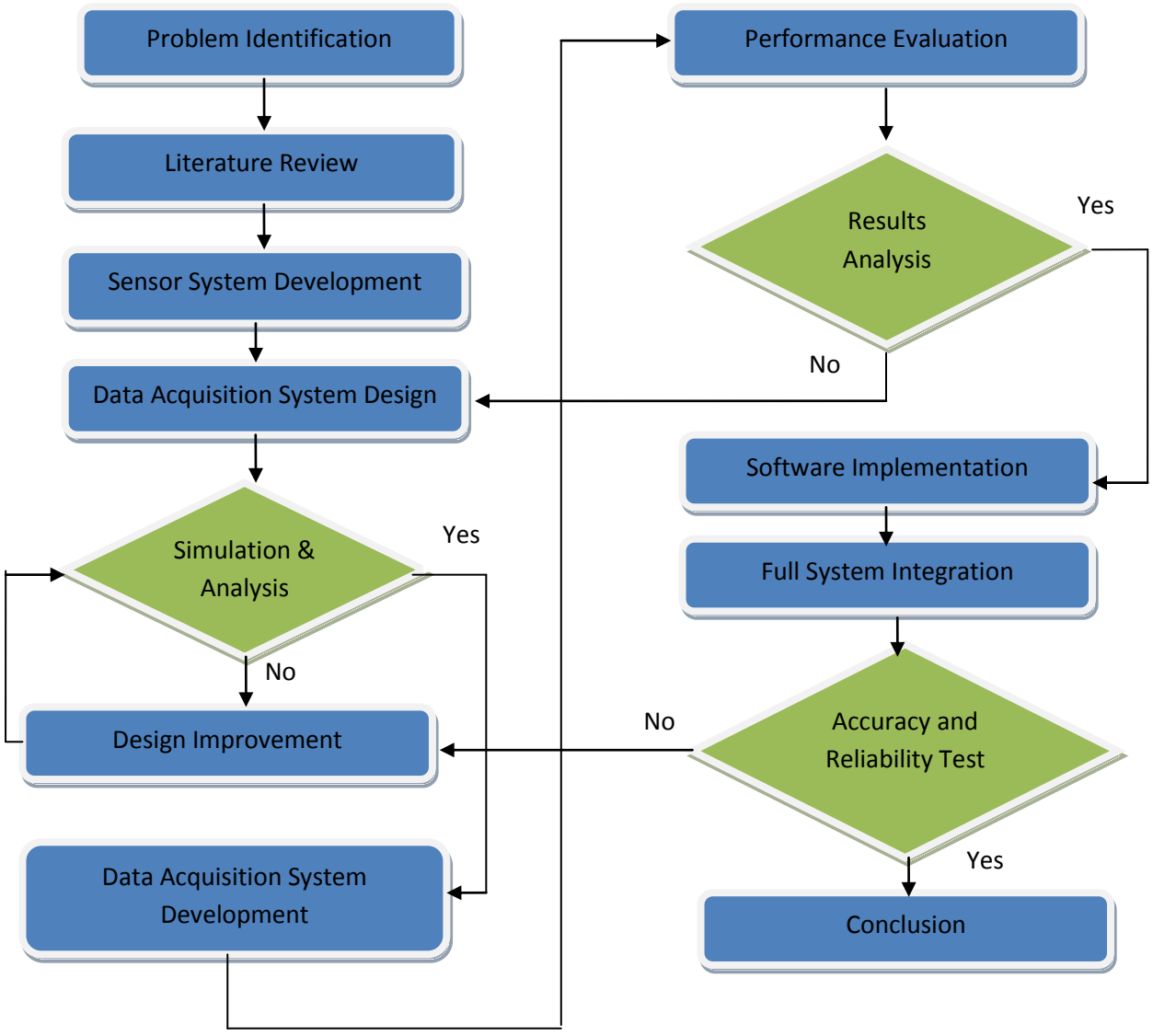
Even with the development of these image reconstruction algorithms, there is still room for improvements as there is no certain unifying modeling technique to be used in developing the images of the measurement area. Other factors such as Mixture Model Correlation used also affects the end image of the system. The usual models used are Series Mixture Models, Parallel Mixture Model, Maxwell Mixture Model and the combination of the four [30] The modeling approach of the measurement area in term of dielectric dispersion mapping is also of interest. Different modeling approach will yield a different representation of the results. Thus, test implementations must be done in order to identify the most optimal model to represents the measurement area of the project. In the interest of the project, a Linear Back Projection (LBP) method is chosen to be implemented as it shows sufficient accuracy and reliability for the case at hand [4, 17 & 27]. The abundant publications and the simplicity of the method are also the reasons for the choice of the method.

CHAPTER 3

METHODOLOGY

3.1 Research Methodology

The research is based on the following flowchart:



The flow chart is devised to guide the author into completing the project. All steps in the flow chart must be followed to ensure the project could be executed successfully.

3.2 Project Block Description

Methodology	Definition / Description
Problem Identification	• Defining the problems and criteria for the proposed solution to the problem.
Literature Review	• Performing reviews of previous scientific publications in arriving to the solution to the problem. • Set objectives and milestones of the project.
Sensor System Development	• Designing a suitable ECT Sensor Unit for the project. • Coming up with a working model of Sensor Unit
Data Acquisition System Design	• Designing measurement circuits, switching mechanisms, filter blocks and integrate them all to work together.
Simulation & Analysis	• Simulates the Data Acquisition System Design by using PSPICE and MULTISIM. • The outputs are analyzed to study the system's reliability.
Data Acquisition System Development	• Building the Data Acquisition System block which covers the programming of microcontrollers, realizing all ICs and other implementations.
Performance Evaluation	• Tests the Data Acquisition System with Sensor Unit
Results Analysis	• Analyze results to ensure optimal accuracy and precision. • Determines whether system needs to be revised again.
Full System Integration	• Combines all the ECT blocks developed for them to work collaboratively.
Accuracy and Reliability Test	• Performs several test measurements to build an accuracy and reliability profile of the system. • Determines whether the system is accurate enough or needs to be revised.

3.4 Tools and Equipment Used

The project combines the building of the physical unit of ECT and the algorithm development for the system. Thus in achieving this, several hardware and software are used in the project.

The project uses the National Instruments Data Acquisition System which comprises of a Data Acquisition Card, cables and its connector block. The function of the Data Acquisition card is to:

1) To assist the interface of the hardware with the computer Peripheral Component Interconnect (PCI) port.

2) To produce the appropriate control signals for auxiliary functions such as multiplexing, signal generators and Programmable Gain Array (PGA) functions.

3) To convert the analogue signals containing crucial indicator of the capacitance level obtained from the measurement environment to digital signals using the Analog-to-Digital Converter (ADC) unit.

4) To convert the digital controlling signals from the PC to analog signals to fix a constant offset for the Digital-to-Analog Converter (DAC) unit.

In choosing a NI Data Acquisition Card, many considerations must be made in term of its speed, number of bits used in the system, analogue and digital I/O available, number of counters and sensitivity. Two cards that stands out the most are the PCI 6062 E-Series and the PCI 6251 M-Series. Both cards are available and after serious consideration, PCI 6251 M-Series is chosen to be used in the project for a number of reasons. The card is much faster and more accurate than the other. The most interesting feature of the card is that it has 16 Analogue Inputs which is a lot for a DAQ Card. It has an Update Rate of 2.8M Samples/sec and it is also equipped with 24 Digital I/O. The card itself also is multifunctional and operates with PCI which offers adequate speed for a high-speed ECT system. These features allow the research to be flexible in designing an optimal and efficient Data Acquisition System for Electrical Capacitance Tomography.

Auxiliary devices such as SCB-68A Connector Block and SHC68-68-EPM Shielded Cable are also needed in this project. By using these devices, there are minimal chances of noise interruptions and these increases the overall efficiency of the system.

Apart from that, sixteen ADG 201A switches are needed for the synchronization and the mode-control of all the electrodes. Several high speed operational amplifiers (LM6264) are also needed as to quantify the capacitance of the circuit. The project would also require several Printed Circuit Boards (PCB) in order to systematically build the signal-conditioning circuits on the boards to further control the signal flow in the Data Acquisition System. PCB is chosen as it is very compact, saves up space and very reliable for acquisition purposes.

In this project, the main software that is used is the NI LabVIEW software. The software is specially made by National Instrument and usually used to configure NI products. In the project, the software would be used in two parts; to configure the Data Acquisition Card, interfaces the measuring environment with the computer processing environment and to process the data obtained from the measurements.

MULTISIM is simulation software that is compatible with National Instrument Utiliboard. It is useful in testing the compatibility of NI products with systems. It is also very helpful and powerful simulation software. MATLAB or Matrix Laboratory is a programming environment that uses fourth-generation programming language. It is mainly used for mathematical modeling and graphing purposes. In this project, MATLAB is used mainly for Tomographic Image Reconstruction purposes where it will translate the effective potential readings using some specialized algorithm. It will then transpose the values on a sensitivity map for a clearer representation of the area of interest. MATLAB is also chosen to be the used as it offers an extensive processing tools such as Digital Signal Processing tools and Simulink extensions for simpler and faster programming environment.

3.5 Gantt Chart

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Selection of Topic	■	■												
Initial Research			■	■										
Submission of Extended Proposal					■	■								
Proposal Defense							■							
Initial Design								■	■					
Hardware Survey										■				
Simulation and Analysis											■	■		
Draft for Interim Report													■	
Interim Report Submission														■

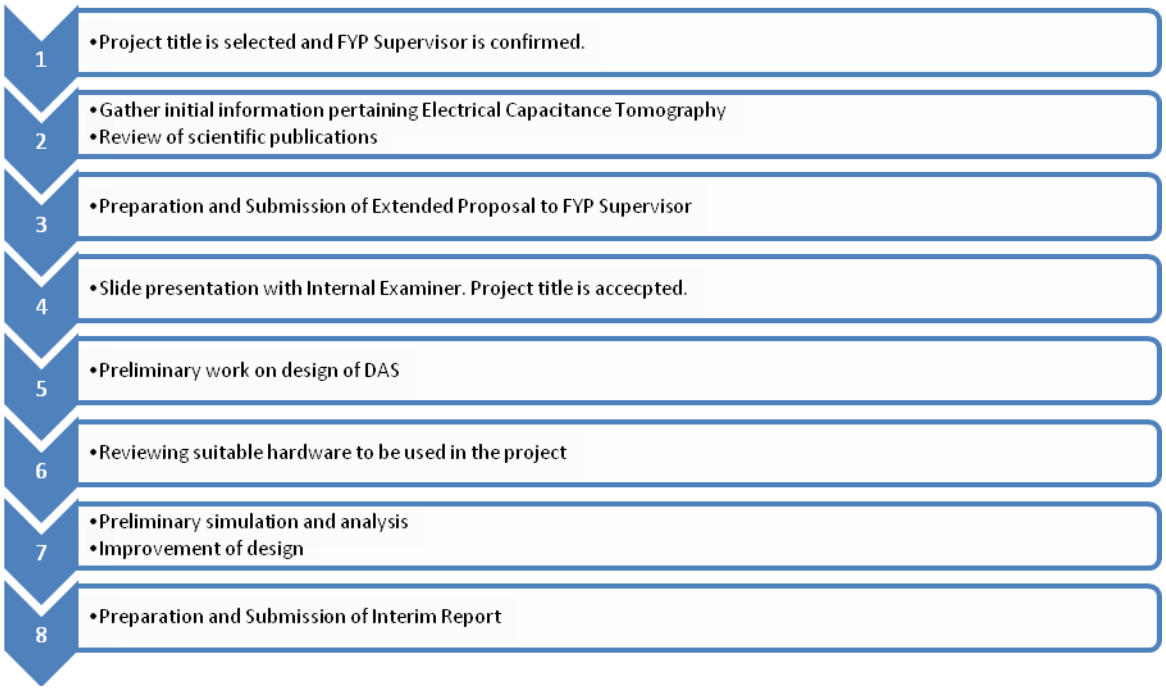
Gantt chart For FYP 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Improvement of Design	■	■												
Integration with Sensor Unit			■											
Software Implementation				■	■	■								
Overall System Integration							■							
Test Measurement								■						
Pre-EDX Preparation									■	■				
Submission of Final Report										■				
Submission of Dissertation											■			
Submission of Technical Paper												■		
Oral Presentation													■	
Hardbound Project Dissertation														■

Gantt chart for FYP 2

3.6 Key Milestone

Several important events have been tagged as the key milestone for the project. These events are also based on the Gantt chart devised before. If all milestones are completed and achieved, the project has been executed properly. The key milestone for FYP 1 is as follows:



The key milestones for FYP 2 are as follows:

Until now, the project have surpasses much milestones that have been targeted for the project. Firstly, a monumental change from a microcontroller based to a more efficient system that uses NI Data Acquisition System. The shift is essential for the project as it increases the speed and precision of the system while reducing the workload of heavy PIC programming. In order to choose the appropriate Data Acquisition Card, the author have reviewed multiple electronics catalogs and revised tens of datasheets in coming up with the most efficient Data Acquisition Card; the PCI 6251 M-Series. It is more advanced compared to E-Series and less superior to its adjacent S-Series but the card has its own cost advantage.

Secondly, a better signal conditioning circuit has been chosen for the project. Much efforts have been put to search for a suitable switch to be used in the project as there are many criteria to be satisfied ranging from the operating voltage level, switching time to leakage current tolerance.

A series of Printed Circuit Boards (PCB) have been designed and fabricated in order to provide the system with its capacitance measuring system. The board consists of a combination of three individual boards combined next to each other and a central control unit is placed along with the other boards.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Overview of the Measurement System

In the initial part of the project, a comprehensive design of the Data Acquisition System for the Electrical Capacitance Tomography is targeted. The basis of the design is the use of AC Measurement Circuit using the mechanism devised before.

In this system, a standard Malaysia household power voltage source is chosen as the input to the system. Reason being is to make it standardize to be used in the country. The voltage source would be of 220 V, 50 Hz and is AC in nature. Using a high-end power module, the voltage level would be changed to lower levels of +5V and +15 V. This is done to give the circuit its flexibility in case a higher level voltage ECT testing is desired. By using voltage switch units, the current levels and voltage levels of the input signal could be manipulated to have the suitable stability and to ensure its reliability.

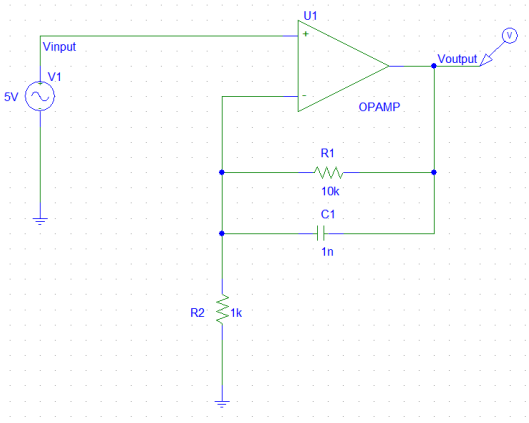
Then, the input signal would be treated with another sequential circuit to deduce an AC signal input excitation, which is the basis of the measurement system. The excitation signals are then stimulate the copper electrodes surrounding the area of interest through a complex digital/analog switching mechanism.

The potential difference between electrodes would then be measured via a control mechanism by the same switching mechanism. This is to ensure only the potential difference of a pair of effective electrodes be measured at a time. These readings would then be treated with a filtering block in order to suppress any noise disturbances in the system.

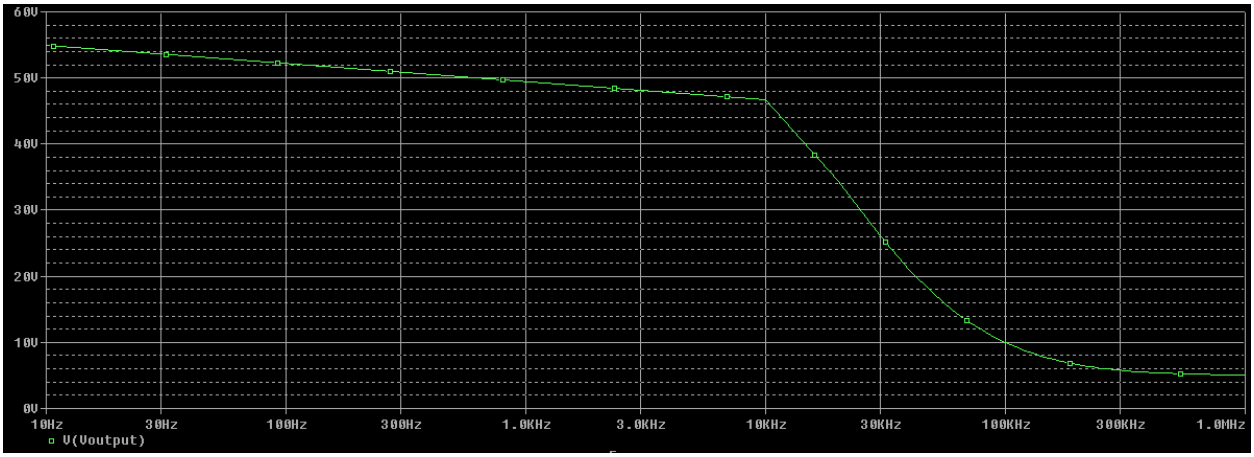
Next, the readings would then be transmitted to the Data Acquisition Card to be treated accordingly with proper PGA conditioning. The process normalizes the potential reading and reduces the error present in the system. The charge/discharge nature of the circuit is perfect for the measurement of the electrode-to-electrode capacitance and afterwards, the results would be processed by the Tomographic Image Reconstruction Algorithm Block with the help of the interfaces of PCI port and NI Data Acquisition System.

4.1 Simulation of Low Pass Filter

In the measurement system, the readings are prone to unwanted noise from the surroundings. To prevent such discrepancies, a low-pass filter is installed to suppress the noise as to increase the reliability of the system. A low-pass filter is simulated using PSPICE to justify its functionality and use in the system.



Schematics of the Low-Pass Filter



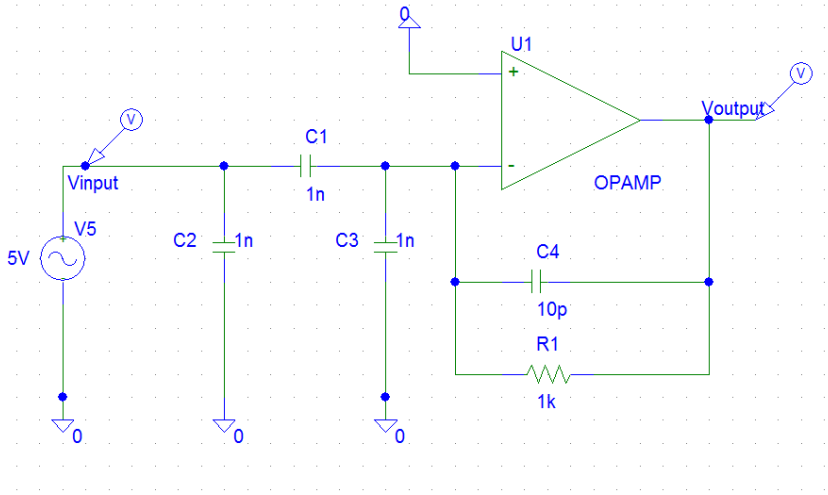
Low-Pass Filter Implementation

The result shows the end result after a signal is being filtered by the filter implementation. The critical frequency of the result above is around 10 kHz. The critical or cutoff frequency can be changed by changing the values of R1 and C1. The result shows that the filter is good in allowing any signals that have a frequency lower than the cutoff frequency and it suppresses the signals that are not.

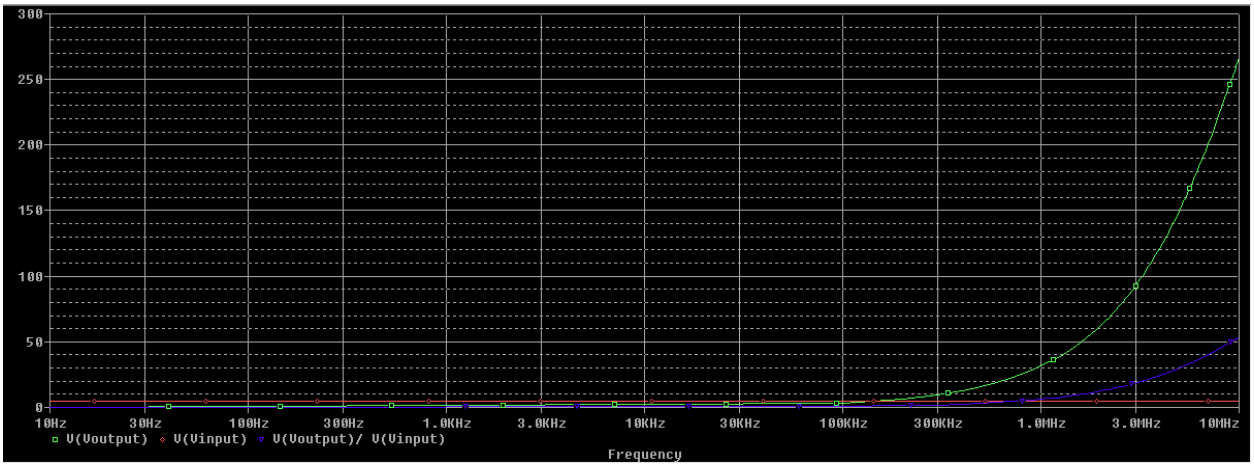
It is also noteworthy to point out that filter system implementation would not completely blocks all noise present in the system but it reduces the average noise distribution thus making the system more reliable and accurate.

The low-pass filter will be implemented throughout the circuitry in order to reduce the chances of noise appearing in the end output spectrum. This will also makes the circuitry more stable and more reliable.

4.2 Simulation of Measurement Circuit



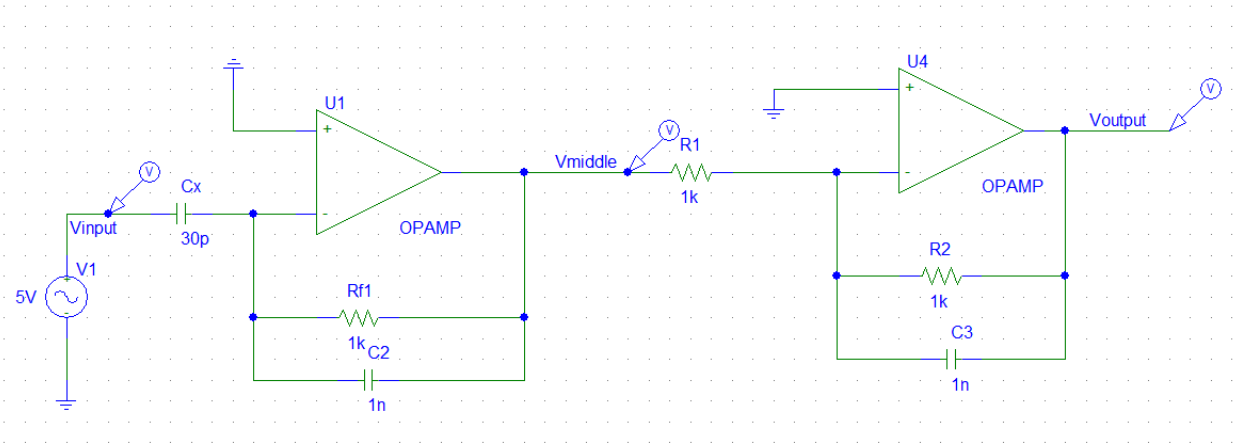
First Measurement Circuit



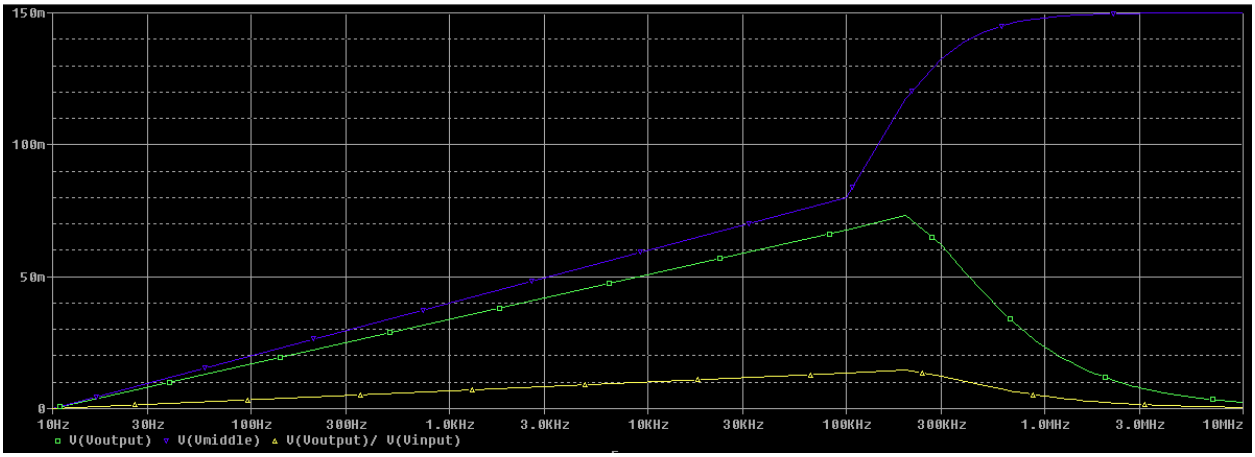
First Measurement Circuit Results

As seen from the results of the first measurement circuit, the system have a low gain at low frequency. In this ECT system, low-frequency is of interest as higher frequencies tend to be noisy in nature. Thus, in achieving this, the system shows promising potentials as it does not have any inconsistency or breakage in any point throughout the spectrum. The blue line also indicates that the gain change is almost constant for all frequencies lower than 300 kHz. Since the potential readings would only be of lower frequency, this is a good option. The only drawback of the system is that the gain value is too low and sometimes the value of the potential differences needs to be amplified to a certain level. The drawback can be curbed with the use of an external amplifying circuit.

Next, another form of measurement circuit is been analyzed.



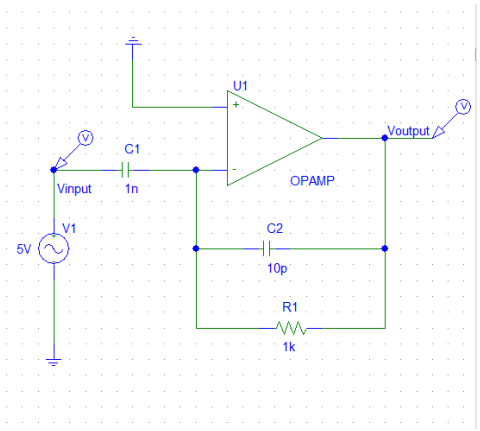
Second Measurement Circuit



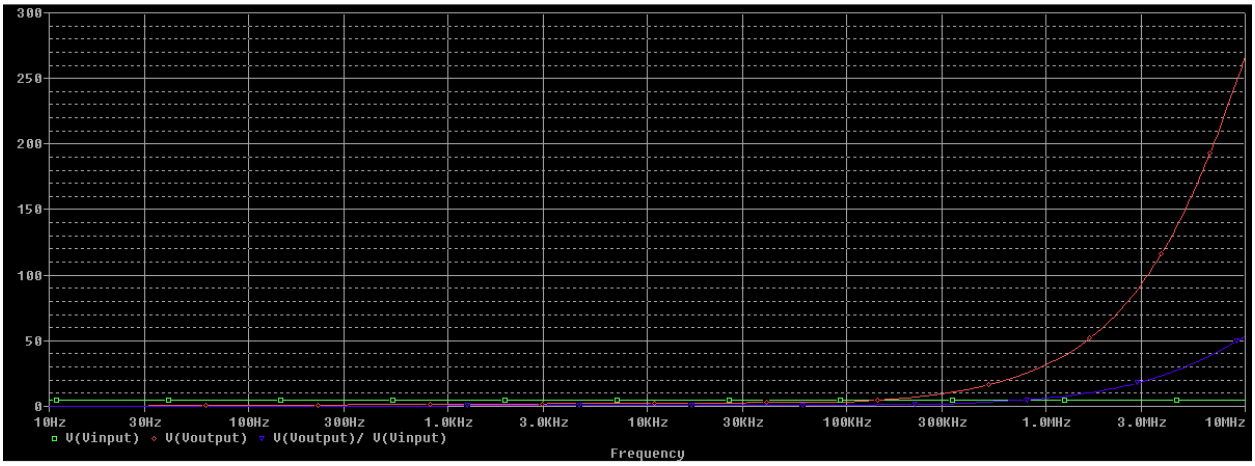
Results of the Second Measurement Circuit

In this measurement circuit, the left part of the circuit is responsible for the conditioning of the input signal and the right part is the amplifying circuit. Based on the response of measurement circuit, the system does not have any inconsistency or breakage throughout the spectrum. The gain value of the system is higher than that of the measurement circuit. The system has an advantage of being connected to the amplifying circuit and the circuit can be tuned to the desired level by the user. As signals of low frequency is used in the system, the system shows promising potential to be used.

Then, another measurement circuit is simulated using PSPICE to verify its output response.



Third Measurement Circuit

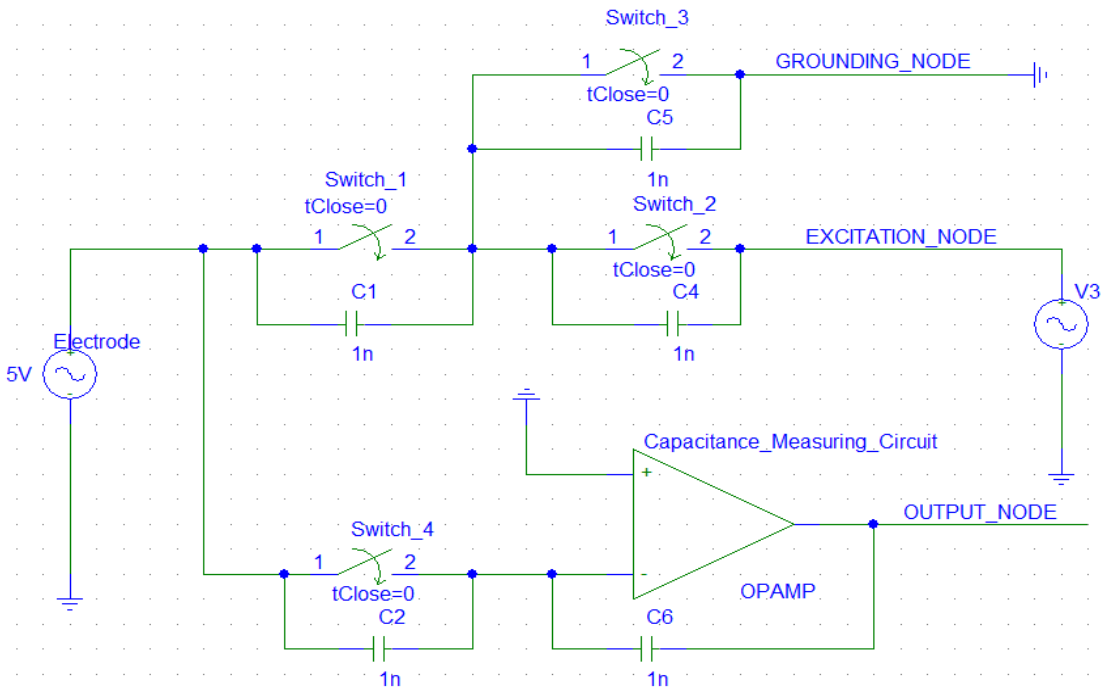


Results of Third Measurement Circuit

The third measurement circuit shows a simple measurement circuit that is a candidate to be used in the project. As seen in the layout of the circuit, C1 is responsible for the noise reduction mechanism and the rest of the circuit is to condition the input signal. It also acts as an amplifier circuit. Based on the simulation result, the output response shows an almost constant gain value indicating a stable circuit. The output response also does not have any breakage in its spectrum and the gain value escalates at frequencies of higher than 100 kHz. As the output from the sensor is treated with a low-pass filter before transmitted to the measurement circuit, the gain escalation would not affect the output of the system. Bear in mind that the system could be tuned with simple mathematical derivation and change in the value of capacitances and resistance to the system.

4.3 Signal Conditioning Circuit

With the recent change in the Data Acquisition System architecture, a new signal-conditioning circuit is chosen to be used in the project. The circuit is illustrated as follows:



Circuit diagram of the Ac-Based ECT Data Acquisition System Architecture

The circuit is more suitable to be used in the system for a number of reasons:

1) It utilizes the concept of AC-Based system which has been proved to optimize the performance of an ECT system.

2) The architecture integrates both excitation circuit of the electrode with the measuring circuit of the electrode.

3) The utilization of switch 3 eradicates the effect of switch coupling capacitance and improves the performance of measurement of the inter-electrode capacitance.

4) The mechanism also makes the system to be free from stray capacitances.

5) The system is very stable and does not have a high drift factor.

6) The system is also accurate, stable and precise as compared to others.

The output voltage of the system could be described using the following equation:

$$V_o = -\frac{j\omega C_{eff} R_f}{j\omega C_f R_f + 1} V_{in}$$

Where ω is the frequency in rad, C_{eff} is the effective capacitance between the electrodes of interest, R_f is the feedback resistance, C_f is the feedback capacitance and V_{in} is the input voltage.

As to improve the circuit's performance, the following condition must be met.

$$\frac{1}{\omega C_f} \ll R_f$$

And this results in:

$$V_o = -\frac{C_{eff}}{C_f} V_{in}$$

As proved by the equation, the effective capacitance between the electrodes could be obtained by determining the input voltage and measuring the output voltage. The linear relationship also shows that if the condition is fulfilled, the resulting effective capacitance measurement is not dependent to the input frequency of the system thus increasing the efficiency of the system.

It is also noteworthy to state that the negative sign does not mean that the voltages are reversed to one another; it just denotes the utilization of an inverting operational amplifier.

4.4. Data Acquisition Card Implementation

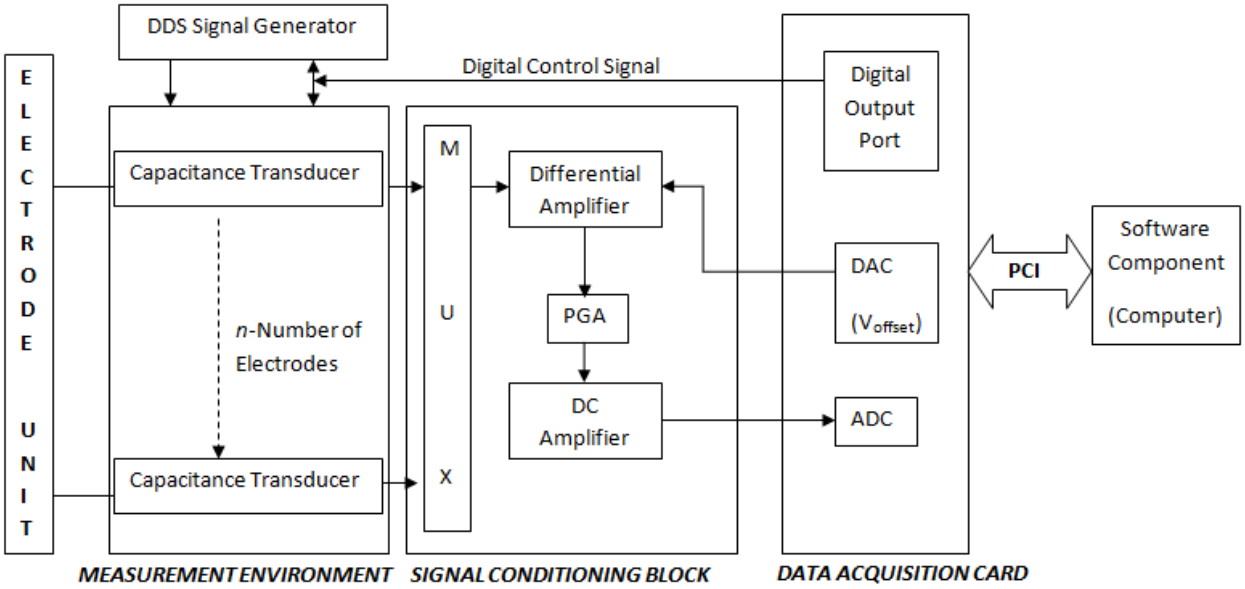


Diagram of the AC-Based ECT Data Acquisition System Architecture

Based on the new architecture, the DAQ Card would also centralize all measuring mechanisms. The system starts with the integration of all system blocks. The software through the DAQ Card would initialize a measurement by applying a starting signal to the Digital Output Port. The Digital Output Port would signals the DDS Signal Generator to jumpstarts a measurement by exciting the appropriate electrodes. The electrodes could only take in the role of one mode at a time; either excitation mode or measuring mode. The role designation would be controlled by the Multiplexer (MUX) unit with the help from the DAQ Card.

The signal measurements would then pass through the Differential Amplifier that compares the incoming signal with the offset voltage supplied by the DAC unit. Appropriate scaling would then be performed by the Programmable Gain Array (PGA) that would then passes it to DC Amplifier to be then converted to digital signal by the ADC block. The digital representation of the measurements would be transferred to the computer via the PCI protocol and it would then be processed by the computer via the running software (LabVIEW).

The architecture is very integrative and collaborative. All components must be carefully-configured in order to ensure an efficient measurement. An essential advantage of the architecture is that any changes can be made through the DAQ Card that would then configure

all the blocks accordingly. The extensive use of counter unit in the system also provides excellent synchronization for the switching control mechanism. As PCI 6251 M-Series is equipped with these appropriate mechanisms, it will be the best device to be applied to the system.

Another interesting aspect of the PCI 6251 M-Series utilization is that the system could be configured by the user themselves. This allows the users to change the systems accordingly. Such feature is very useful in the event of sensor units testing and correctional protocols. The overall system speed, gain multiplier and even filter implementation could be configured straight through the PCI 6251 M-Series. It is then noteworthy that it is within the job scope of the author to develop such a system as delicate and as flexible as this system as it will eases the process of tomographic image reconstruction and future development of the system.

PCI 6251 M-Series Data Acquisition Card

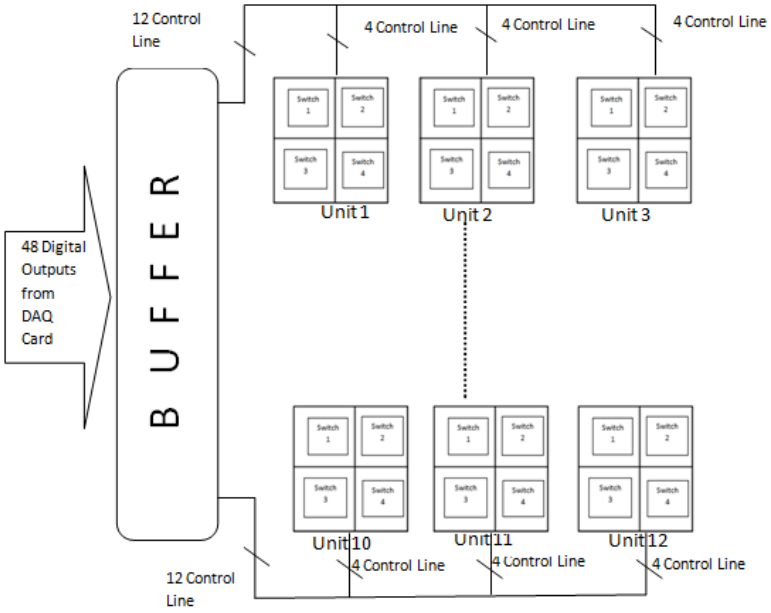
SHC-68A Connector Block

SHC68-68-EPM Cable

4.5 Measurement Circuit

In the initial stage of the measurement system development, a microcontroller-based system is first developed. After significant review of its end results, the system is deemed not sufficient enough to be used on the Electrical Capacitance Tomography system.

After that, the focus have shifted to the development of Data Acquisition System that revolves around PCI 6251 M-Series. The device is needed in controlling the switching of all signal conditioning circuits and interfaces the measurement environment and the software environment. The layout of the device control mechanism is illustrated as follows:

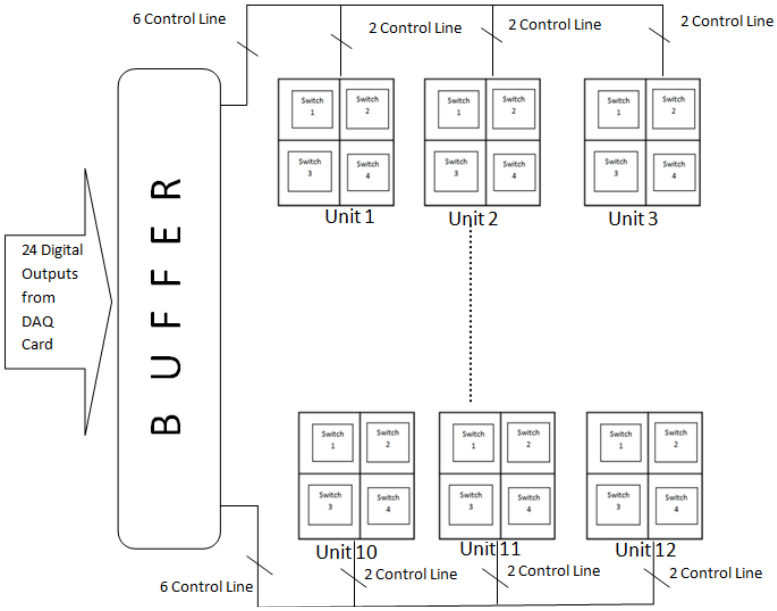


Layout of the Measurement Circuit

The above diagram illustrated the control mechanism of all switches present in the system. There are twelve individual units of the measurement circuits as the system implements a twelve electrode system. As seen in the diagram, the system utilizes forty-eight Digital Outputs from the card. This is highly-inefficient and a waste of the DOs. Even though each switch will be controlled individually, there are significant redundancies present in the system. Moreover, the card could only offer up to twenty four DOs per usage.

4.5.1 Control Unit Optimization

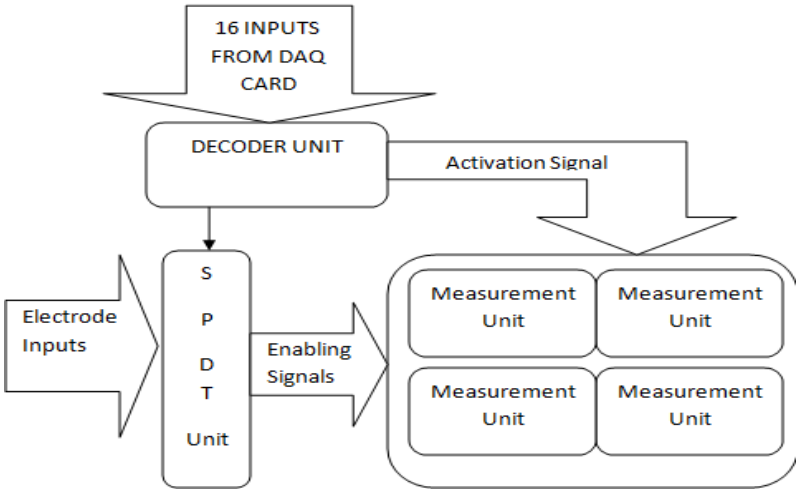
With the knowledge of number of Dos available with the PCI card, some optimization work must be done to increase the efficiency of the system. The first optimization work done on the system is as follows:



Measurement Circuit Layout 2

In this system, both control of Switch 1 and Switch 2, and Switch 3 and Switch 4, is shorted. In this way, the DO number could be cut by half. Each switch will be activated and deactivated simultaneously with its neighboring switch. The mechanism will provide flexible switching sequences to the system but it is still risky implementing such control mechanism. The risk lies in the card itself as some of the Dos might not be in proper status. They might be out of order and subsequent optimization must be designed to further improve the system.

In the next stage of the optimization, some multiplexing is applied where Single Pull Double Throw (SPDT) switches are used as there are no two switches next to each other need to be turned on at the same time. The SPDT unit used in this stage consists of a series of SPDT switches that is able to multiplex the electrode units and the mechanism is accompanied by eight control lines from the PCI Card.



Measurement Circuit Layout 3

The design is very useful as it cuts the amount of switching units needed to be used in the system from twelve individual units to only four individual units. It uses less power and it applies multiplexing mechanism on the control units. It also only uses sixteen DOs, eight for the SPDT synchronization and another eight to control the switching modes. The drawback of the system is that the system involves an SPDT network that could actually introduce more bottlenecks to the system. The speed of the measurement circuit is limited by the speed of the SPDT switches used in the system. This scheme then reduces the speed of the system. Another system must be designed to further improve the system.

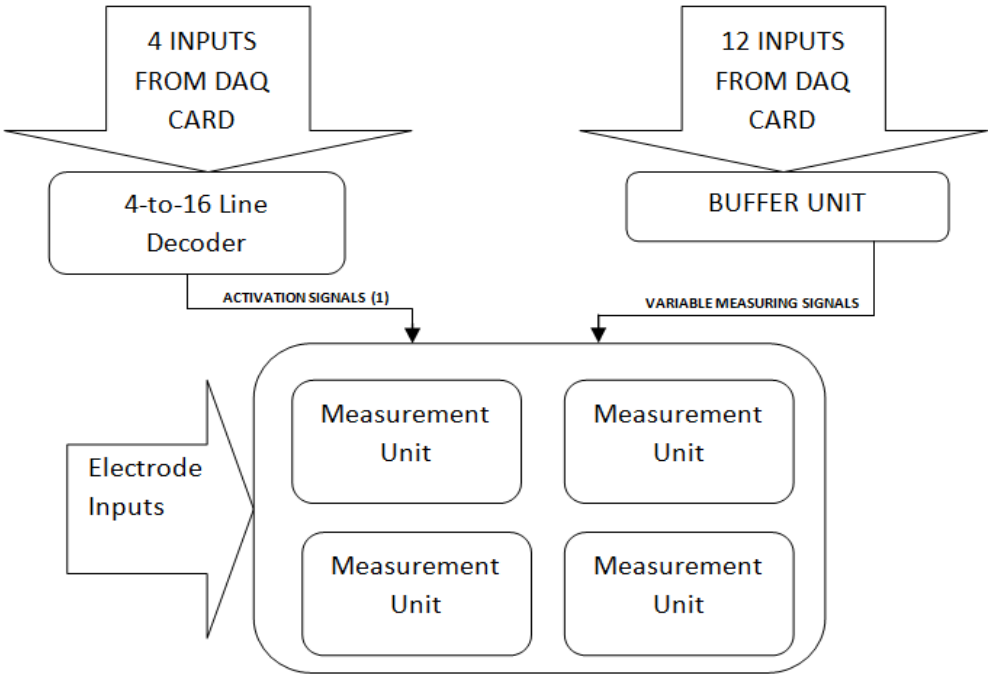
After profound analysis and reviews, another aspect of the measurement circuit must be considered. In this stage, the flexibility of the measurement circuit must be included in the system design. The issue that concerns the research is that the Electrical Capacitance Tomography sequencing is usually restricted to only one excitation electrode and one measurement electrode per frame. The author is now concern to the product flow inside the

vessels in between the frames where product distribution differs from the previous reading. To reiterate, the sequencing starts with V11, V12, V13 and after that, V_{23}, V_{24} until $V_{n-1,n}$.

With respect to the measurements, the reading of V_{21} will not be taken as it is assumed to be similar to V_{12} though some changes might be present during the time difference and these inaccuracies in data acquisition also affects the end representation of the system.

Another concerning issue is the fact that a better image representation could be yielded based from a wider measurement coverage. The system could actually achieve a higher efficiency by exciting one electrode and take measurements from the electrode that is suppose to provide the readings and the readings from the other two neighboring electrodes. Take as an example, when electrode 1 is excited and measurement should be taken from Electrode 2, readings could also be taken from Electrode 3 and Electrode 4, per say. The more reading provided by the system and the wider area of coverage per frame, the more data would be produced. Subsequently, this will yield a much better image representation of the area of interest at that specific time. A lot of research could be based on these fallacies and it is of the interest of the research to develop an effective Data Acquisition System for that specific fallacies.

With these fallacies in mind, another measurement circuit layout is build.



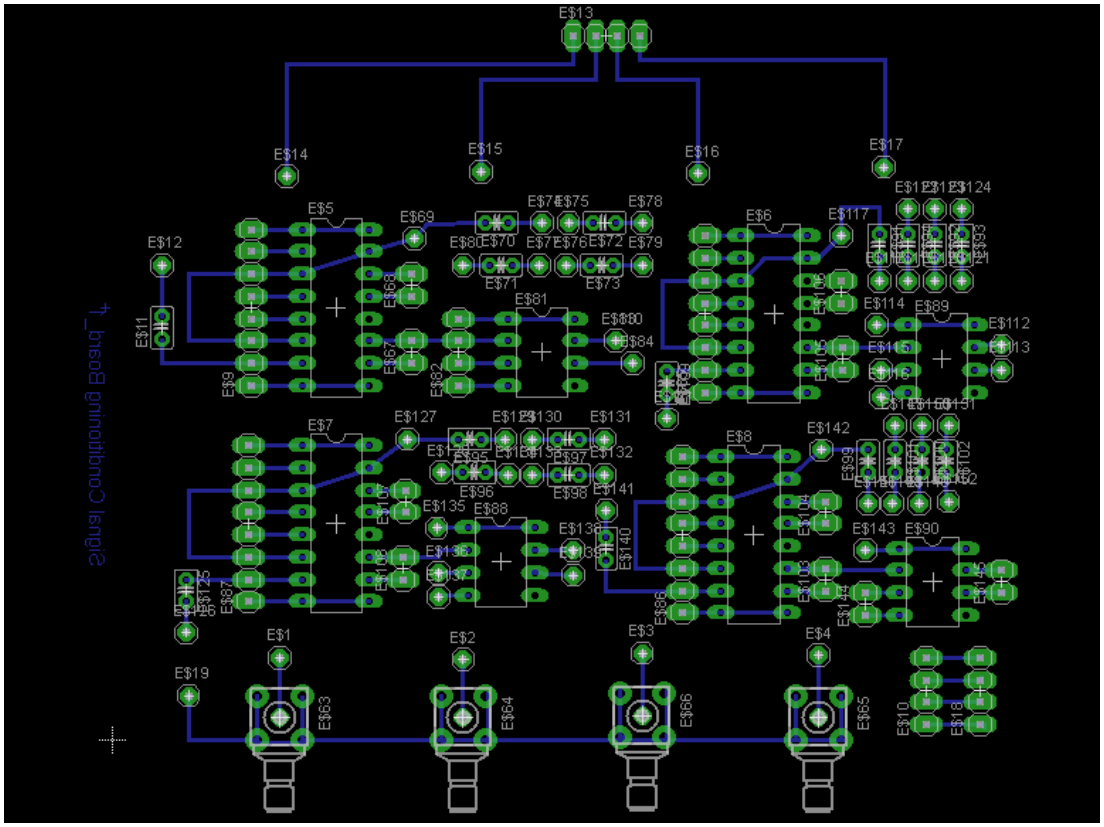
Measurement Circuit Layout 4

The new layout is based on the reasoning that the two modes should be controlled by two separate units. The 4-to-16 decoder unit functions as the controlling unit for the excitation signal and it only uses up to 4 inputs from the PCI Card. The decoder only activates one of its lines at a time and this will enables only one electrode to be excited at a time.

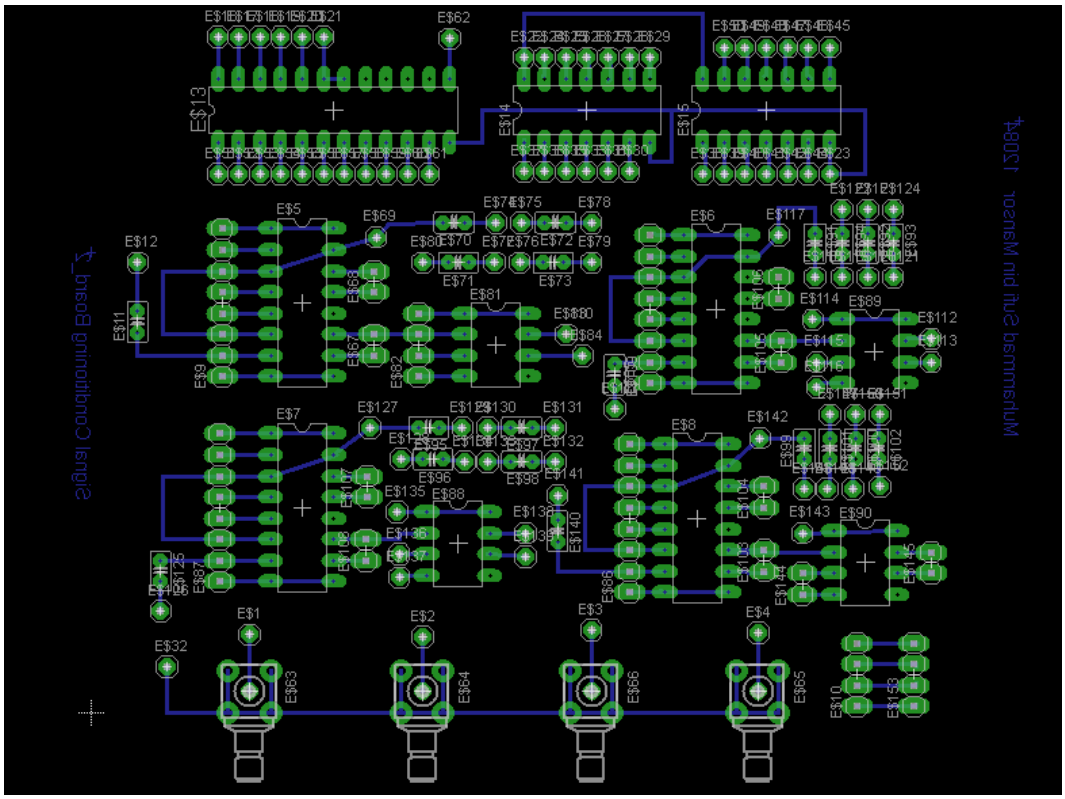
Another twelve DOs is needed for the input to the buffer unit as all twelve measurement electrodes should be controlled at all time. The buffer unit is just a series of inverters as the switches all operate on the basis of ACTIVE-LOW that only conducts electricity when a Low signal is introduced at its Enable pin. The twelve DOs will directly control all twelve measurement electrodes and this gives the circuit its most advantageous edge. This mechanism allows the system to take readings from several electrodes at a time thus allowing a wider coverage of inter-electrode measurements. The optimization also allows the system to operate like the conventional Electrical Capacitance Tomography system where only one-excitation-one-measurement scheme is used. The development of the new measurement layout not only utilizes minimal DOs from the PCI DAQ Card but also allows multiple electrode readings per excitation. The new layout is very suitable to be used especially in the education field where a lot of research could be invested in the area.

4.5.2 Fabrication of Printed Circuit Board (PCB)

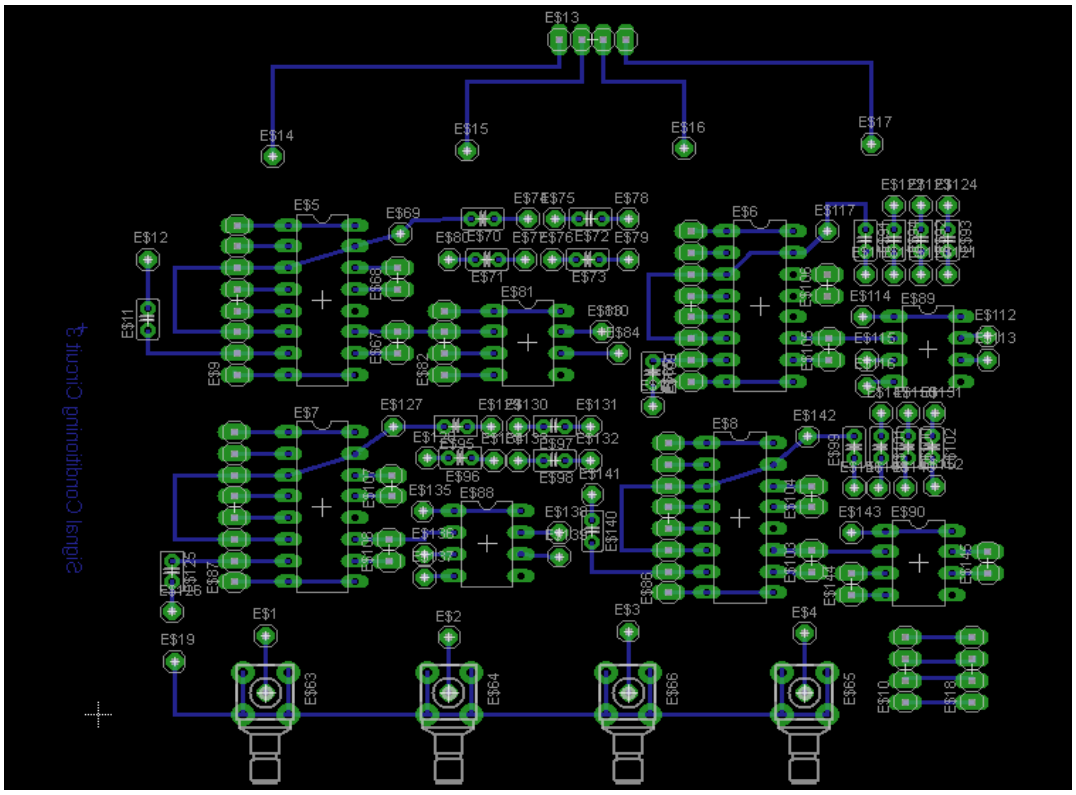
After having to revise the final version of the measurement circuit layout, the design of the PCB commences. The circuit board is designed using the Easily Applicable Graphical Layout Editor (Eagle) software. The following diagrams illustrate the Eagle designs:



Board 1



Board 2



Board 3

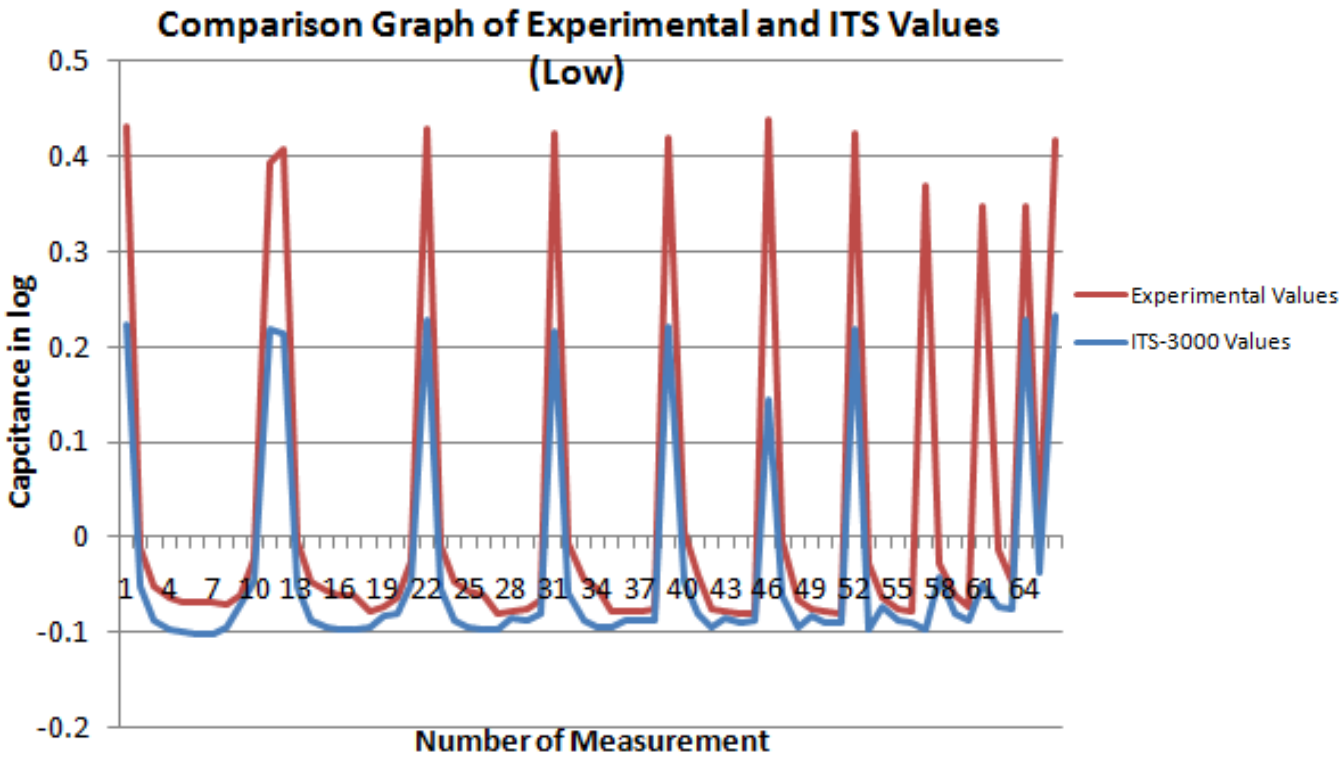
All three boards are aligned in such order: Board 1, Board 2 and Board 3. Board 2 contains the placement of the two controlling units for the Measurement Circuit Layout 4. The other two boards are connected to the middle board with the use of jumpers. In designing the Eagle software, many challenges have been faced such as incorrect placements of the devices and unavailability of two-sided PCB facilities that forces the author to make several PCB boards and uses a special Copper Pen as a tracer on top of the PCBs.

As illustrated in the PCB drawings, the system uses the Sub-Miniature Version B (SMB) plugs as it is a common practice in almost all Electrical Capacitance Tomography Systems. The advantages of using the plugs are that the outer layer of the plug are to be grounded at all times and only the middle plug is responsible to conduct electrical signals. This provides an extra layer of shielding from noise to the system. The only drawback of the plugs is that they are sometimes fragile and easily loose when reinstalled repeatedly.

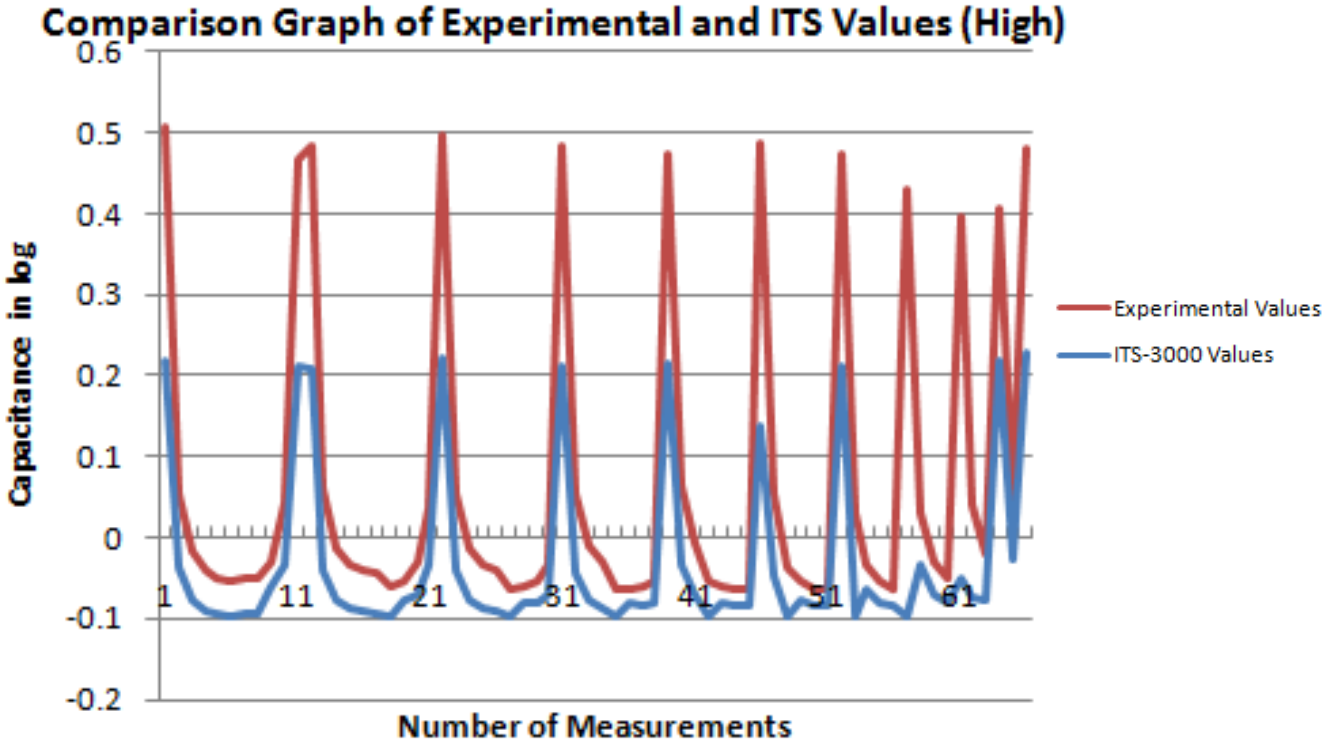
4.6 Results of Test Measurements

After the system have been devised, several test run have been made using the system that had been developed using the conventional measurement protocol of one excitation per one measurement electrodes system. In order to build a comparison study, the results from the utilization of the current measurement circuit is compared with data from the current Electrical Capacitance Tomography system used in UTP which is the ITS-3000 system.

The comparison starts with the comparison of the capacitance values in Low Calibration and in high calibration. Low Calibration is defined by conditions where the permittivity value is at its lowest with regards to the measurement of interest. In this round of measurement, the low calibration measurement is done with air ($\varepsilon \approx 1$) occupying in the imaging area



Next, de-ionized water ($\varepsilon \approx 80$) is used to perform measurements for the High Calibration part.



The graphs in red shows the results obtained using the new Data Acquisition System and the graph in blue indicates the results obtained from ITS-3000 system. The peaks represent the highest capacitance value which directly represents that the electrodes associated to the results are nearer to each other. As an example, the first peak is due to the high capacitance of electrode number 1 and 2 and the second peak is then due to electrode number 2 and electrode number 3.

Based on the graph of the Low Calibration, it is clear that both graphs follow the same trends and having similar shapes. The consistency is very important to demonstrate that the newly developed Data Acquisition System is very accurate and reliable.

The same goes for the graph of High Calibration where both graphs have almost the same shape. Not only that, on both graphs of Low Calibration and the High Calibration, the peaks are located at almost the same location showing a very significant similarity in data trend which in turn, correlates to an accurate and reliable Data Acquisition System.

There are some inconsistencies for the middle two peaks are these are the readings from ITS-3000's electrode number 8 and 9. It might be due to the constant attachments and extraction of the SMB plugs that causes the electrodes to not be properly connected. These drawbacks could be suppressed by proper handling of the sensitive connectors and its utilizations.

Another important aspect to the analysis is that the measurement levels of both graphs of the new DAQ and the ITS-3000 system are very different, though they shown high similarity in term of their shapes. This is most probably because of the difference in the measuring circuit implementation. All measuring circuits have their own ranges and values that they uniquely exhibit and this is not an erroneous result as they poses the same trends and they are both in agreement with each other signifying a very accurate and reliable system. The differences shall be entertained by the developer of the Tomographic Image Reconstruction as the individual values and the value differences are the important aspects in coming up with the end representation of the imaging area.

CHAPTER 5

CONCLUSION

The objective of the project is to come up with an efficient and reliable Data Acquisition System to be used for UTP's own Electrical Capacitance Tomography System. After careful analysis and scientific review, it is concluded that the Electrical Capacitance Tomography is a suitable solution to the problem posed in the initial part of the project which is the problem of multiphase flow analysis.

After reviewing the scientific publications, several circuitries are proposed in order to come up with the suitable architecture for the Electrical Capacitance Tomography. Then, several common measurement circuits are simulated and their results are compared and analyzed. Based on the careful analysis, the advantages and disadvantages of each measurement circuit are outlined and an improved and optimized measurement circuit is designed to be used in the system. The circuitry designed poses several advantages such as immune to stray capacitances., stable, reliable and also flexible.

Along the process, several hardware and software are reviewed and their profiles are compared to come up with the best hardware to be implemented to the system. Then, a PCB circuitry is then created to accommodate the hardware and to improvise on the current hardware utilization. Apart from that, a PCI 6251 M-Series is used to further increase the efficiency of the system by having a more centralized and reliable platform for all measurement activities.

Next, several test measurements are performed in order to come up with a comparative study of the new Data Acquisition System and the current Data Acquisition System, ITS-3000. After the comparison is made, it is concluded that the new Data Acquisition System is very reliable, accurate and precise. It also offers features such as multiple electrode readings per excitation that proves to be able to further alleviate the overall ECT efficiency.

For future development, the author hope that a new Tomographic Image Reconstruction Algorithm could be developed by future students to further improves the performance of the Electrical Capacitance Tomography System. The author also suggests that better hardware and software are to be used in the future development to further enhance the system in producing online measurement. In order to test the system developed, the author also suggests the ECT system to be tested with several other multiphase flow measurements such as different concentration of oil and water and also other liquids to build up more results to come up with the efficiency profile of the Electrical Capacitance Tomography system. It is also the authors hope that a complete study on the effect of multiple electrode readings per frame to the end image representation is done as to further alleviate the overall system efficiency.

CHAPTER 6

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APPENDIX

Technical Sales
United States
(866) 531-6285
info@ni.com

Last Revised: 2011-10-21 10:32:43.0

High-Speed M Series Multifunction Data Acquisition - 16-Bit, up to 1.25 MS/s, up to 80 Analog Inputs

- 16, 32, or 80 analog inputs at 16 bits, 1.25 MS/s (1 MS/s scanning, NI 6255 specified at 750 kS/s scanning)
- Up to 4 analog outputs at 16 bits, 2.8 MS/s (2 µs full-scale settling)
- 7 programmable input ranges (±100 mV to ±10 V) per channel
- Up to 48 TTL/CMOS digital I/O lines (up to 32 hardware-timed at 10 MHz)
- Two 32-bit, 80 MHz counter/timers
- Analog and digital triggering
- X1, X2, or X4 quadrature encoder inputs
- 2-year calibration interval

Overview

NI M Series high-speed multifunction data acquisition (DAQ) devices are optimized for superior accuracy at fast sampling rates. These devices have NI-MCal calibration technology for improved measurement accuracy and six DMA channels for high-speed data throughput. They have an onboard NI-PGIA 2 amplifier designed for fast settling times at high scanning rates, ensuring 16-bit accuracy even when measuring all channels at maximum speeds. All high-speed devices have a minimum of 16 analog inputs, 24 digital I/O lines, seven programmable input ranges, analog and digital triggering, two counter/timers, and an extended two-year calibration interval.

NI recommends high-accuracy M Series devices (NI 628x) for 5X more measurement sensitivity or industrial M Series devices (NI 623x) for 60 VDC isolation and superior noise rejection.

See the NI USB-625x data sheet for information specific to USB M Series devices.

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Requirements and Compatibility

OS Information

- Windows 2000/XP
- Windows Vista x64/x86
- Linux®
- Mac OS X
- Windows 7

Driver Information

- NI-DAQmx
- NI-DAQmx Base

Software Compatibility

- ANSI C/C++
- LabVIEW
- LabVIEW SignalExpress
- LabWindows/CVI
- Visual Studio .NET

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Comparison Tables

Family	Bus	Analog Inputs	AI Resolution (bits)	Analog Outputs	AO Resolution	Max Update Rate (MS/s)	AO Range (V)	Digital I/O	Correlated (clocked) DIO

Family	Bus	Analog Inputs	AI Resolution (bits)	Analog Outputs	AO Resolution	Max Update Rate (MS/s)	AO Range (V)	Digital I/O	Correlated (clocked) DIO
NI 6250	PCI, PXI	16	16	0	-	-	-	24	8, up to 10 MHz
NI 6251	PCI, PCI Express, PXI, PXI Express, USB	16	16	2	16	2.8	±10, ±5, ±ext ref	24	8, up to 10 MHz
NI 6254	PCI, PXI	32	16	0	-	-	-	48	32, up to 10 MHz
NI 6255	PCI, PXI, USB	80	16	2	16	2.8	±10, ±5, ±ext ref	24	8, up to 10 MHz
NI 6259	PCI, PCI Express, PXI, PXI Express, USB	32	16	4	16	2.8	±10, ±5, ±ext ref	48	32, up to 10 MHz

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Application and Technology

M Series for Test

For test, you can use M Series high-speed analog inputs and 10 MHz digital lines with NI signal conditioning for applications including electronics test, component characterization, and sensor measurements. High-speed M Series devices are compatible with NI SCC and SCXI signal conditioning platforms, which provide amplification, filtering, and power for virtually every type of sensor. These platforms also are compliant with IEEE 1451.4 smart transducer electronic data sheet (TEDS) sensors, which provide digital storage for sensor data sheet information.

M Series for Control

M Series digital lines can drive 24 mA for relay and actuator control. By clocking the digital lines as fast as 10 MHz, you can use these lines for pulse-width modulation (PWM) to control valves, motors, fans, lamps, and pumps. With four waveform analog outputs, two 80 MHz counter/timers, and six DMA channels, M Series devices can execute multiple control loops simultaneously. High-speed M Series devices also have direct support for quadrature encoder measurements, protected digital lines, and digital debounce filters for control applications. With up to 80 analog inputs, 32 clocked digital lines, and four analog outputs, you can execute multiple control loops with a single device. For higher-count control loops, you can use M Series devices in conjunction and tightly synchronized with National Instruments analog output devices for 64 or more loops. With the NI SoftMotion Development Module for LabVIEW, you can create a complete custom motion controller with M Series devices.

M Series for Design

You can use the wide range of I/O – from 80 analog inputs to 48 digital lines – to measure and verify prototype designs. M Series devices and NI LabVIEW SignalExpress interactive measurement software deliver benchtop measurements to the PC. With LabVIEW SignalExpress interactive configuration-based steps, you can quickly create design verification tests. The fast acquisition and generation rates of high-speed M Series devices along with LabVIEW SignalExpress provide on-the-fly design analysis. You can convert your tested and verified LabVIEW SignalExpress projects to LabVIEW applications for immediate M Series DAQ use, thus bridging the gap between test, control, and design applications.

M Series Performance on PCI Express

National Instruments was the first company to empower engineers and scientists to use the PCI Express and PXI Express buses for data acquisition. PCI Express M Series boards contain six DMA channels to maximize data throughput without using PC processing time. The PCI Express bus delivers the highest bandwidth compared to any other PC bus, and it eliminates throughput bottlenecks by providing 250 MB/s per-direction bandwidth across the x1 (“by one”) lane for increased data transfer. Each slot allocates dedicated bandwidth, meaning that multiple PCI Express boards do not share bandwidth for data transfer. With this improvement over the shared-bandwidth PCI architecture, all onboard I/O runs simultaneously while data is transferred to and from PC memory across the bus. The PXI Express specifications integrate PCI Express signaling into the PXI Standard, which increases backplane bandwidth from 132 MB/s to 6 GB/s, a 45 times improvement. Both PCI Express and PXI Express facilitate a smooth transition to new hardware by providing complete backward compatibility to software written for applications that use PCI or PXI, respectively.

Hybrid-Slot-Compatible PXI Modules

PXI M Series modules are hybrid-slot-compatible so that you can use them in both PXI slots and the hybrid slots found in new PXI Express chassis. The PXI Systems Alliance specifies that hybrid-slot-compatible PXI modules use modified slot connectors to mechanically fit in both PXI slots and hybrid slots. This mechanical change:

- Provides compatibility with past, current, and future PXI chassis
- Maintains existing product specifications
- Requires no software changes (application or driver)
- Maintains speed and capability of all PXI communication (PXI Express signaling is not provided)

However, hybrid-slot-compatible PXI modules do not include the pins used to implement PXI local bus communication, which is used for backplane SCXI control from the right-most PXI slot in PXI/SCXI combination chassis (PXI-1010, PXI-1011, PXI-1050, and PXI-1052). For these applications, NI provides unmodified PXI M Series modules that maintain the required local bus capabilities. Refer to the SCXI Control of PXI/SCXI Combination Chassis section in the Ordering Information section for part numbers.

Industrial Data Acquisition

When you need performance and accuracy from a data acquisition device in an electrically noisy or harsh environment, consider National Instruments industrial M Series devices (NI 623x). NI industrial DAQ devices offer a set of high-reliability features, including isolation, ±20 mA current I/O, 24 V digital logic levels, and digital debounce filters. Isolation prevents ground loops, rejects high common-mode voltages, and protects users and equipment from high-voltage transients. Four to 20 mA current loops are immune to most sources of electrical noise and voltage (IR) drops along extensive cable lengths. Sourcing or sinking 24 V digital I/O interfaces directly with pumps, valves, relays, and other industry-standard sensors and actuators, and programmable debounce filters remove glitches and spikes from switches and relays connected to digital input lines.

Simultaneous and Intelligent Data Acquisition

When you need to obtain performance from a data acquisition device beyond the capabilities of a multifunction data acquisition device, National Instruments provides simultaneous sampling with NI S Series and intelligent data acquisition with NI R Series. The S Series architecture dedicates an analog-to-digital converter (ADC) per channel to provide higher aggregate sampling rates compared to multiplexed devices. S Series devices are ideal for applications including IF digitization, transient recording, ultrasound and sonar testing, and high-energy physics. R Series multifunction DAQ devices contain a field-programmable gate array (FPGA) that is reconfigurable using the LabVIEW FPGA Module.

They combine analog input, analog output, and digital I/O on a single device. You can customize these devices to develop capabilities such as complete control over the synchronization and timing of all signals and operations; user-defined onboard decision-making logic; and digital lines individually configurable as input, output, counter/timers, PWM, flexible encoder inputs, or user-defined communication protocols.

Recommended Accessories

Signal conditioning is required for sensor measurements or voltage inputs greater than 10 V. NI SCXI is a versatile, high-performance signal conditioning platform optimized for high-channel-count applications. NI SCC provides portable, flexible signal conditioning options on a per-channel basis. Visit **ni.com/sigcon** for resources on available NI signal conditioning.

Recommended Driver Software

National Instruments measurement services software, built around NI-DAQmx driver software, includes intuitive application programming interfaces, configuration tools, I/O assistants, and other tools designed to reduce system setup, configuration, and development time. National Instruments recommends using the latest version of NI-DAQmx driver software for application development in NI LabVIEW, LabVIEW SignalExpress, LabWindows™/CVI, and Measurement Studio software. To obtain the latest version of NI-DAQmx, visit **ni.com/support/daq/versions**. NI measurement services software speeds up your development with features including the following:

- A guide to create fast and accurate measurements with no programming using the DAQ Assistant
- Automatic code generation to create your application in LabVIEW; LabWindows/CVI; LabVIEW SignalExpress; and C#, Visual Studio .NET, ANSI C/C++, or Visual Basic using Measurement Studio
- Multithreaded streaming technology for 1,000 times performance improvements
- Automatic timing, triggering, and synchronization routing to make advanced applications easy
- Thousands of free software downloads available at **ni.com/zone** to jump-start your project
- Software configuration of all digital I/O features without hardware switches/jumpers
- Single programming interface for analog input, analog output, digital I/O, and counters on hundreds of multifunction data acquisition hardware devices

M Series devices are compatible with the following versions (or later) of NI application software – LabVIEW, LabWindows/CVI, or Measurement Studio versions 7.x; and LabVIEW SignalExpress 2.x.

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Ordering Information

For a complete list of accessories, visit the product page on ni.com.

Products	Part Number	Recommended Accessories	Part Number
NI PCI-6250			
NI PCI-6250 Requires: 1 Cables , 1 Connector Blocks	779069-01	**Cables:** Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PXI-6250			
NI PXI-6250 Requires: 1 Cable , 1 Connector Block	779116-01	**Cable:** Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PCI-6251			
NI PCI-6251 Requires: 1 Cables , 1 Connector Blocks	779070-01	**Cables:** Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PCIe-6251			
NI PCIe-6251 Requires: 1 Cables , 1 Connector Blocks	779512-01	**Cables:** Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PXI-6251			
NI PXI-6251 Requires: 1 Cables , 1 Connector Block	779631-01	**Cables:** Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PXIe-6251			
NI PXIe-6251 Requires: 1 Cables , 1 Connector Block	779777-01	**Cables:** Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PCI-6254			
NI PCI-6254	779071-01		

Requires: 2 Cables , 2 Connector Blocks		**Connector 0:**	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
		Connector 1:	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
NI PXI-6254			
NI PXI-6254 Requires: 2 Cables , 2 Connector Block	779118-01	**Connector 0:**	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
		Connector 1:	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
NI PCI-6255			
NI PCI-6255 Requires: 2 Cables , 2 Connector Block	779546-01	**Connector 0:**	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
		Connector 1:	
		Cables: Shielded - SHC68-68 Cable (2m) ***Also Available: Unshielded*	191945-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
NI PXI-6255			
NI PXI-6255 Requires: 2 Cables , 2 Connector Block	779547-01	**Connector 0:**	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
		Connector 1:	
		Cables: Shielded - SHC68-68 Cable (2m) ***Also Available: Unshielded*	191945-02
		Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals, Custom*	776844-01
NI PCI-6259			
NI PCI-6259 Requires: 2 Cables , 2 Connector Blocks	779072-01	**Connector 0:**	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
		Connector 1:	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
		Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
NI PCIe-6259			
NI PCIe-6259 Requires: 2 Cables , 2 Connector Blocks	779513-01	**Connector 0:**	
		Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02

	Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
	Connector 1:	
	Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
	Connector Blocks: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
NI PXI-6259		
NI PXI-6259 Requires: 2 Cables , 2 Connector Block	779632-01	**Connector 0:**
	Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
	Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
	Connector 1:	
	Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
	Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
NI PXIe-6259		
NI PXIe-6259 Requires: 2 Cables , 2 Connector Block	779778-01	**Connector 0:**
	Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
	Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01
	Connector 1:	
	Cables: Shielded - SHC68-68-EPM Cable (2m) ***Also Available: Unshielded*	192061-02
	Connector Block: Spring-Screw_Terminals - SCB-68 ***Also Available: BNC_Terminals*	776844-01

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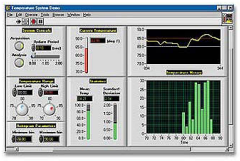
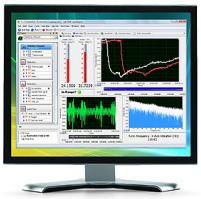
Software Recommendations

LabVIEW Professional Development System for Windows



- Advanced software tools for large project development
- Automatic code generation using DAQ Assistant and Instrument I/O Assistant
- Tight integration with a wide range of hardware
- Advanced measurement analysis and digital signal processing
- Open connectivity with DLLs, ActiveX, and .NET objects
- Capability to build DLLs, executables, and MSI installers

NI LabVIEW SignalExpress for Windows

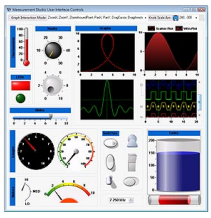


- Quickly configure projects without programming
- Control over 400 PC-based and stand-alone instruments
- Log data from more than 250 data acquisition devices
- Perform basic signal processing, analysis, and file I/O
- Scale your application with automatic LabVIEW code generation
- Create custom reports or easily export data to LabVIEW, DIAdem or Microsoft Excel

NI LabWindows™/CVI for Windows

- Real-time advanced 2D graphs and charts
- Complete hardware compatibility with IVI, VISA, DAQ, GPIB, and serial
- Analysis tools for array manipulation, signal processing statistics, and curve fitting
- Simplified cross-platform communication with network variables
- Measurement Studio .NET tools (included in LabWindows/CVI Full only)
- The mark LabWindows is used under a license from Microsoft Corporation.

NI Measurement Studio Professional Edition



- Support for Microsoft Visual Studio .NET 2010/2008/2005
- Customizable Windows Forms and Web Forms controls for test and measurement user interface design
- Hardware integration support with data acquisition and instrument control libraries
- Automatic code generation with data acquisition, instrument control, and parameter assistants
- Cross-platform communication with network variables
- Analysis libraries for array operations, signal generation, windowing, filters, signal processing

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Calibration

NI measurement hardware is calibrated to ensure measurement accuracy and verify that the device meets its published specifications. To ensure the ongoing accuracy of your measurement hardware, NI offers basic or detailed recalibration service that provides ongoing ISO 9001 audit compliance and confidence in your measurements. To learn more about NI calibration services or to locate a qualified service center near you, contact your local sales office or visit ni.com/calibration.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

Specifications listed below are typical at 25 °C unless otherwise noted. Refer to the *M Series User Manual* for more information about NI 625*x* devices.

Analog Input	
Number of channels	
NI 6250/6251	8 differential or 16 single ended
NI 6254/6259	16 differential or 32 single ended
NI 6255	40 differential or 80 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed

INL	Refer to the *AI Absolute Accuracy Table*
Sampling rate	
Maximum	
NI 6250/6251/6254/6259	1.25 MS/s single channel, 1.00 MS/s multi-channel (aggregate)
NI 6255	1.25 MS/s single channel 750 kS/s multi-channel (aggregate)
Minimum	No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Input coupling	DC
Input range	±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V, ±0.1 V
Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	100 dB
Input impedance	
Device on	
AI+ to AI GND	>10 GΩ in parallel with 100 pF
AI- to AI GND	>10 GΩ in parallel with 100 pF
Device off	
AI+ to AI GND	820 Ω
AI- to AI GND	820 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz)	
Adjacent channels	-75 dB
Non-adjacent channels	-90 dB[1]
Small signal bandwidth (-3 dB)	1.7 MHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	
PCI/PCIe/PXI/PXIe devices	DMA (scatter-gather), interrupts, programmed I/O
USB devices	USB Signal Stream, programmed I/O
Overvoltage protection (AI <0..79>, AI SENSE, AI SENSE 2)	
Device on	±25 V for up to four AI pins
Device off	±15 V for up to four AI pins
Input current during overvoltage condition	±20 mA max/AI pin

[1] For USB-6255 devices, channel AI <0..15> crosstalk to channel AI <64..79> is -67 dB; applies to channels with 64-channel separation, for example, AI (*x*) and AI (*x* + 64).

Settling Time for Multichannel Measurements

NI 6250/6251/6254/6259

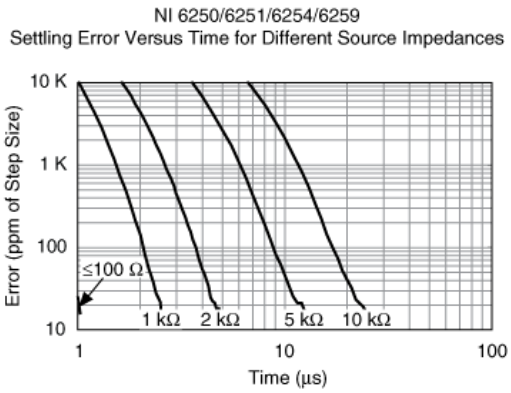
Range	±60 ppm of Step (±4 LSB for Full Scale Step)	±15 ppm of Step (±1 LSB for Full Scale Step)
±10 V, ±5 V, ±2 V, ±1 V	1 µs	1.5 µs
	1.5	

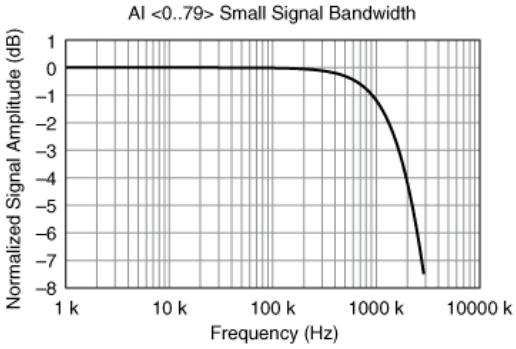
±0.5 V	µs	2 µs
±0.2 V, ±0.1 V	2 µs	8 µs

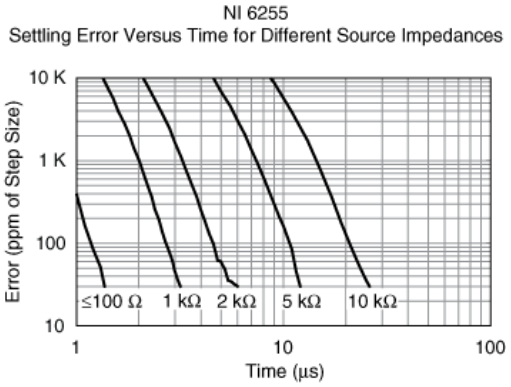
NI 6255

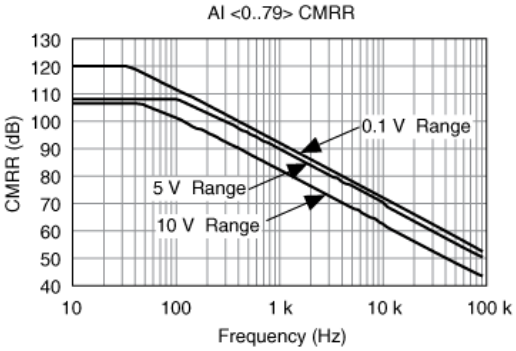
Range	±60 ppm of Step (±4 LSB for Full Scale Step)	±15 ppm of Step (±1 LSB for Full Scale Step)
±10 V, ±5 V, ±2 V, ±1 V	1.3 µs	1.6 µs
±0.5 V	1.8 µs	2.5 µs
±0.2 V, ±0.1 V	3 µs	8 µs

Typical Performance Graphs









Analog Triggers

Number of triggers	1
Source	
NI 6250/6251	AI <0..15>, APFI 0
NI 6254/6259	AI <0..31>, APFI <0..1>
NI 6255	AI <0..79>, APFI 0
Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Source level	
AI <0..79>	±full scale
APFI <0..1>	±10 V
Resolution	10 bits, 1 in 1,024
Modes	Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering
Bandwidth (-3 dB)	
AI <0..79>	3.4 MHz
APFI <0..1>	3.9 MHz
Accuracy	±1%

APFI <0..1> characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection	
Power on	±30 V
Power off	±15 V

Analog Output

Number of channels	
NI 6250/6254	0
NI 6251/6255	2
NI 6259	4
DAC resolution	16 bits
DNL	±1 LSB
Monotonicity	16 bit guaranteed
Accuracy	Refer to the *AO Absolute Accuracy Table*
Maximum update rate	
1 channel	2.86 MS/s
2 channels	2.00 MS/s
3 channels	1.54 MS/s
4 channels	1.25 MS/s
Timing accuracy	50 ppm of sample rate
Timing resolution	50 ns
Output range	±10 V, ±5 V, ±external reference on APFI <0..1>
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA
Overdrive protection	±25 V
Overdrive current	20 mA
Power-on state	±5 mV[2]
Power-on glitch	1.5 V peak for 1.5 s
Output FIFO size	8,191 samples shared among channels used
Data transfers	
PCI/PCIe/PXI/PXIe devices	DMA (scatter-gather), interrupts, programmed I/O
USB devices	USB Signal Stream, programmed I/O

AO waveform modes:

- Non-periodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

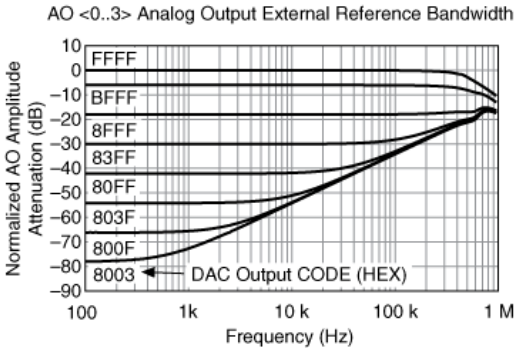
Settling time, full scale step 15 ppm (1 LSB)	2 µs
Slew rate	20 V/µs
Glitch energy at midscale transition, ±10 V range	
Magnitude	10 mV
Duration	1 µs

[2] For all USB-6251/6259 Screw Terminal devices, when powered on, the analog output signal is not defined until after USB configuration is complete.

External Reference

APFI <0..1> characteristics	

Input impedance	10 kΩ
Coupling	DC
Protection	
Power on	±30 V
Power off	±15 V
Range	±11 V
Slew rate	20 V/µs



Calibration (AI and AO)

Recommended warm-up time	15 minutes
Calibration interval	2 years

AI Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale[1] (µV)	Sensitivity[2] (µV)
Positive Full Scale	Negative Full Scale									
10	-10	60	13	1	20	21	60	280	1,920	112.0
5	-5	70	13	1	20	21	60	140	1,010	56.0
2	-2	70	13	1	20	24	60	57	410	22.8
1	-1	80	13	1	20	27	60	32	220	12.8
0.5	- 0.5	90	13	1	40	34	60	21	130	8.4
0.2	- 0.2	130	13	1	80	55	60	16	74	6.4
0.1	- 0.1	150	13	1	150	90	60	15	52	6.0

Accuracies listed are valid for up to two years from the device external calibration.

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

GainError = ResidualAIGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualAIOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

$$\text{NoiseUncertainty} = \frac{\text{RandomNoise} \cdot 3}{\sqrt{100}}$$ For a coverage factor of 3 σ and averaging 100 points.

[1] Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C

TempChangeFromLastInternalCal = 1 °C

number_of_readings = 100

CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

GainError = 60 ppm + 13 ppm · 1 + 1 ppm · 10 GainError = 83 ppm

OffsetError = 20 ppm + 21 ppm · 1 + 60 ppm OffsetError = 101 ppm

$$\text{NoiseUncertainty} = \frac{275\ \mu\text{V} \cdot 3}{\sqrt{100}}$$ NoiseUncertainty = 83 µV

AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty AbsoluteAccuracy = 1920 µV

[2] Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

AO Absolute Accuracy Table

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale[1] (µV)
Positive Full Scale	Negative Full Scale							
10	-10	75	17	1	40	2	64	2,080
5	-5	85	8	1	40	2	64	1,045

[1] Absolute Accuracy at full scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration.
Accuracies listed are valid for up to two years from the device external calibration.

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)

GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualOffsetError + AOOffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

Digital I/O/PFI

Static Characteristics	
Number of channels	
NI 6250/6251/6255	24 total, 8 (P0.<0..7>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
NI 6254/6259	48 total, 32 (P0.<0..31>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typ, 20 kΩ min
Input voltage protection[3]	±20 V on up to two pins

[3] Stresses beyond those listed under Input voltage protection may cause permanent damage to the device.

Waveform Characteristics (Port 0 Only)	
Terminals used	
NI 6250/6251/6255	Port 0 (P0.<0..7>)
NI 6254/6259	Port 0 (P0.<0..31>)
Port/sample size	
NI 6250/6251/6255	Up to 8 bits
NI 6254/6259	Up to 32 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	2,047 samples
DI Sample Clock frequency	
PCI/PCIe/PXI/PXIe devices	0 to 10 MHz[4]
USB devices	0 to 1 MHz system dependent[4]
DO Sample Clock frequency	
PCI/PCIe/PXI/PXIe devices	
Regenerate from FIFO	0 to 10 MHz
Streaming from memory	0 to 1 MHz system dependent[4]
USB devices	
Regenerate from FIFO	0 to 10 MHz
Streaming from memory	0 to 1 MHz system dependent[4]
Data transfers	
PCI/PCIe/PXI/PXIe devices	DMA (scatter-gather), interrupts, programmed I/O

USB devices	USB Signal Stream, programmed I/O
DO or DI Sample Clock source[5]	Any PFI, RTSI, AI Sample or Convert Clock, AO Sample Clock, Ctr *n* Internal Output, and many other signals

[4] Performance can be dependent on bus latency and volume of bus activity.

[5] The digital subsystem does not have its own dedicated internal timing engine. Therefore, a sample clock must be provided from another subsystem on the device or an external source.

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Recommended Operation Conditions[6]

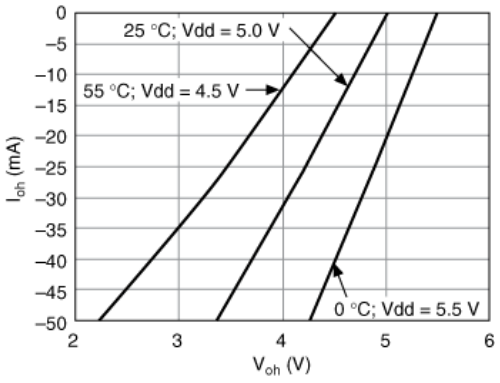
Level	Min	Max
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH})		
P0.<0..31>	—	-24 mA
PFI <0..15>/P1/P2	—	-16 mA
Output low current (I_{OL})		
P0.<0..31>	—	24 mA
PFI <0..15>/P1/P2	—	16 mA

Electrical Characteristics

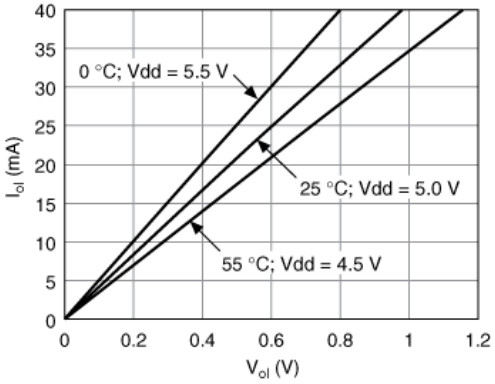
Level	Min	Max
Positive-going threshold (VT+)	—	2.2 V
Negative-going threshold (VT-)	0.8 V	—
Delta VT hysteresis (VT+ - VT-)	0.2 V	—
I_{IL} input low current (V_{in} = 0 V)	—	-10 µA
I_{IH} input high current (V_{in} = 5 V)	—	250 µA

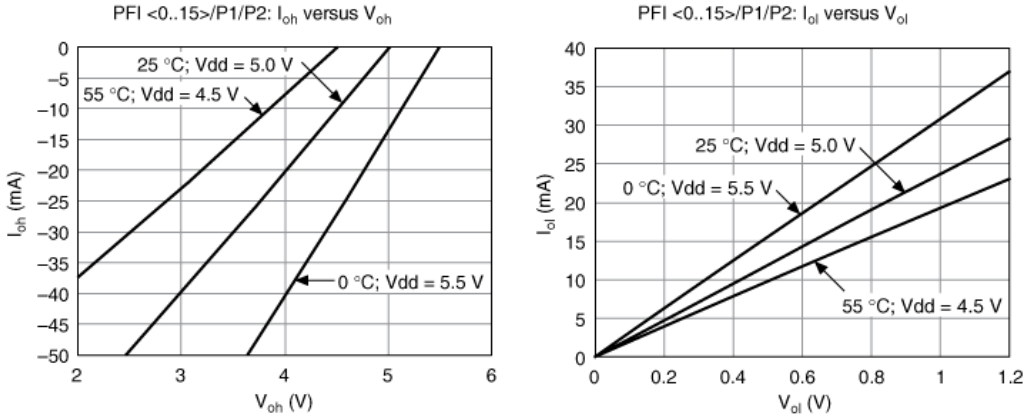
Digital I/O Characteristics[6]

P0.<0..31>: I_{oh} versus V_{oh}



P0.<0..31>: I_{ol} versus V_{ol}





[6] On earlier versions of the USB-6251 Screw Terminal (part numbers 194929A/B/C-0*x*) and the USB-6259 Screw Terminal (part numbers 194021B/C-0*x*), the digital I/O characteristics of P0.<16..31> match the characteristics of PFI <0..15>. Refer to the November 2006 version of the *NI 625x Specifications* (part number 371291G-01) for more details.

General-Purpose Counter/Timers	
Number of counter/timers	2
Resolution	32 bits
Counter measurements	Edge counting, pulse, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	80 MHz, 20 MHz, 0.1 MHz
External base clock frequency	0 MHz to 20 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Routing options for inputs	Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
FIFO	2 samples
Data transfers	
PCI/PCIe/PXI/PXIe devices	Dedicated scatter-gather DMA controller for each counter/timer; interrupts, programmed I/O
USB devices	USB Signal Stream, programmed I/O
Frequency Generator	
Number of channels	1
Base clocks	10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm
Output can be available on any PFI or RTSI terminal.	
Phase-Locked Loop (PLL)	
Number of PLLs	1
Reference signal	PXI_STAR, PXI_CLK10, RTSI <0..7>
Output of PLL	80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases
External Digital Triggers	
Source	Any PFI, RTSI, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase

Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Digital waveform generation (DO) function	Sample Clock
Digital waveform acquisition (DI) function	Sample Clock
Device-To-Device Trigger Bus	
PCI/PCIe devices	RTSI <0..7>[7]
PXI/PXIe devices	PXI_TRIG <0..7>, PXI_STAR
USB devices	None
Output selections	10 MHz Clock; frequency generator output; many internal signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

[7] In other sections of this document, *RTSI* refers to RTSI <0..7> for PCI/PCIe devices or PXI_TRIG <0..7> for PXI/PXIe devices.

Bus Interface

PCI/PXI devices	3.3 V or 5 V signal environment
PCIe devices	
Form factor	x1 PCI Express, specification v1.0a compliant
Slot compatibility	x1, x4, x8, and x16 PCI Express slots[8]
PXIe devices	
Form factor	x1 PXI Express peripheral module, specification rev 1.0 compliant
Slot compatibility	x1 and x4 PXI Express or PXI Express hybrid slots
USB devices	USB 2.0 Hi-Speed or full-speed[9,10]
DMA channels (PCI/PCIe/PXI/PXIe devices)	6, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1
USB Signal Stream (USB devices)	4, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

All PXI-625x devices support one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

Table 1. PXI/SCXI Combo and PXI Express Chassis Compatibility

M Series Device	M Series Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
PXI-6250	191325D-04/191325E-04L	No	Yes
PXI-6251	191325D-03/191325E-03L	No	Yes
	191325D-13/191325E-13L	Yes	No
PXI-6254	191325D-02/191325E-03L	No	Yes
PXI-6255	193618A-01	No	Yes
PXI-6259	191325D-01/191325E-01L	No	Yes
	191325D-11/191325E-11L	Yes	No
Earlier versions of PXI-6251/ 6254/6259	191325C-0*x* 191325B-0*x*	Yes	No

All NI PXIe-625*x* devices may be installed in PXI Express slots or PXI Express hybrid slots.

[8] Some motherboards reserve the x16 slot for graphics use. For PCI Express guidelines, refer to ni.com/pciexpress.

[9] If you are using a USB M Series device in full-speed mode, device performance will be lower and you will not be able to achieve maximum sampling/update rates.

[10] Operating on a full-speed bus may result in lower high-speed full-speed performance.

Power Requirements

Current draw from bus during no-load condition[11]

PCI/PXI devices	
+5 V	0.03 A
+3.3 V	0.725 A
+12 V	0.35 A
PCIe devices	
+3.3 V	0.925 A

+12 V	0.35 A
PXIe devices	
+3.3 V	0.45 A
+12 V	0.5 A
Current draw from bus during AI and AO overvoltage condition[11]	
PCI/PXI devices	
+5 V	0.03 A
+3.3 V	1.2 A
+12 V	0.38 A
PCIe devices	
+3.3 V	1.4 A
+12 V	0.38 A
PXIe devices	
+3.3 V	0.48 A
+12 V	0.71 A

Caution USB-625*x* devices must be powered with NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

USB power supply requirements	11 to 30 VDC, 20 W, locking or non-locking power jack with 0.080" diameter center pin, 5/16-32 thread for locking collars

[11] Does not include P0/PFI/P1/P2 and +5 V terminals.

Power Limits

Caution Exceeding the power limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI devices	
+5 V terminal (connector 0)	1 A max[12]
+5 V terminal (connector 1)	1 A max[12]
PCIe devices	
Without disk drive power connector installed	
+5 V terminals combined	0.35 A max[12]
P0/PFI/P1/P2 and +5 V terminals combined	0.39 A max
With disk drive power connector installed	
+5 V terminal (connector 0)	1 A max[12]
+5 V terminal (connector 1)	1 A max[12]
P0/PFI/P1/P2 combined	0.39 A max
PXI/PXIe devices	
+5 V terminal (connector 0)	1 A max[12]
+5 V terminal (connector 1)	1 A max[12]
P0/PFI/P1/P2 and +5 V terminals combined	2 A max
USB devices	
+5 V terminal	1 A max[12]
P0/PFI/P1/P2 and +5 V terminals combined	2 A max
Power supply fuse	2 A, 250 V

[12] Has a self-resetting fuse that opens when current exceeds this specification.

Physical Requirements

Printed circuit board dimensions	
NI PCI-6250/6251/6254/6255/6259	9.7 × 15.5 cm (3.8 × 6.1 in.)
NI PCIe-6251/6259	9.9 × 16.8 cm (3.9 × 6.6 in.) (half-length)

NI PXI/PXIe-6250/6251/6254/6255/6259	Standard 3U PXI
Enclosure dimensions (includes connectors)	
NI USB-6251/6255/6259 Screw Terminal	26.67 × 17.09 × 4.45 cm (10.5 × 6.73 × 1.75 in.)
NI USB-6251/6259 BNC	28.6 × 17 × 6.9 cm (11.25 × 6.7 × 2.7 in.)
NI USB-6251/6255/6259 Mass Termination	18.8 × 17.09 × 4.45 cm (7.4 × 6.73 × 1.75 in.)
NI USB-6251/6255/6259 OEM	Refer to the *NI USB-622x/625x OEM User Guide*
Weight	
NI PCI-6250	142 g (5 oz)
NI PCI-6251	149 g (5.2 oz)
NI PCI-6254	152 g (5.3 oz)
NI PCI-6255	164 g (5.8 oz)
NI PCI-6259	162 g (5.6 oz)
NI PCIe-6251	161 g (5.7 oz)
NI PCIe-6259	175 g (6.1 oz)
NI PXI-6250	212 g (7.5 oz)
NI PXI-6251/6254	222 g (7.8 oz)
NI PXI-6255	236 g (8.3 oz)
NI PXI-6259	233 g (8.2 oz)
NI PXIe-6251	208 g (7.3 oz)
NI PXIe-6259	221 g (7.8 oz)
NI USB-6251 Screw Terminal	1.2 kg (2 lb 10 oz)
NI USB-6255/6259 Screw Terminal	1.24 kg (2 lb 11 oz)
NI USB-6251/6255/6259 Mass Termination	816 g (1 lb 12.8 oz)
NI USB-6251 OEM	140 g (4.9 oz)
NI USB-6255/6259 OEM	172 g (6.1 oz)
I/O connector	
NI PCI/PCIe/PXI/PXIe-6250/6251	1 68-pin VHDCI
NI PCI/PCIe/PXI/PXIe-6254/6255/6259	2 68-pin VHDCI
NI USB-6251 Screw Terminal	64 screw terminals
NI USB-6255/6259 Screw Terminal	128 screw terminals
NI USB-6251 BNC	21 BNCs and 30 screw terminals
NI USB-6259 BNC	32 BNCs and 60 screw terminals
NI USB-6251 Mass Termination	1 68-pin SCSI
NI USB-6255/6259 Mass Termination	2 68-pin SCSI
Disk drive power connector (PCIe devices)	Standard ATX peripheral connector (not serial ATA)
USB-6251/6255/6259 Screw Terminal/USB-6251/6259 BNC screw terminal wiring	16-28 AWG

Maximum Working Voltage[13]

NI 6250/6251/6254/6255/6259 channel-to-earth	11 V, Measurement Category I

⚠ **Caution** Do *not* use for measurements within Categories II, III, or IV.

[13] Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Environmental

Operating temperature	
PCI/PXI/PXIe devices	0 to 55 °C
PCIe devices	0 to 50 °C
USB devices	0 to 45 °C

Storage temperature	-20 to 70 °C
Humidity	10 to 90% RH, noncondensing
Maximum altitude	2,000 m
Pollution Degree (indoor use only)	2
Shock and Vibration (PXI/PXIe Devices Only)	
Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random vibration	
Operating	5 to 500 Hz, 0.3 g_{rms}
Nonoperating	5 to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A

Note For EMC compliance, operate this device with shielded cables.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the NI and the Environment Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

At the end of their life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。
关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。
(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

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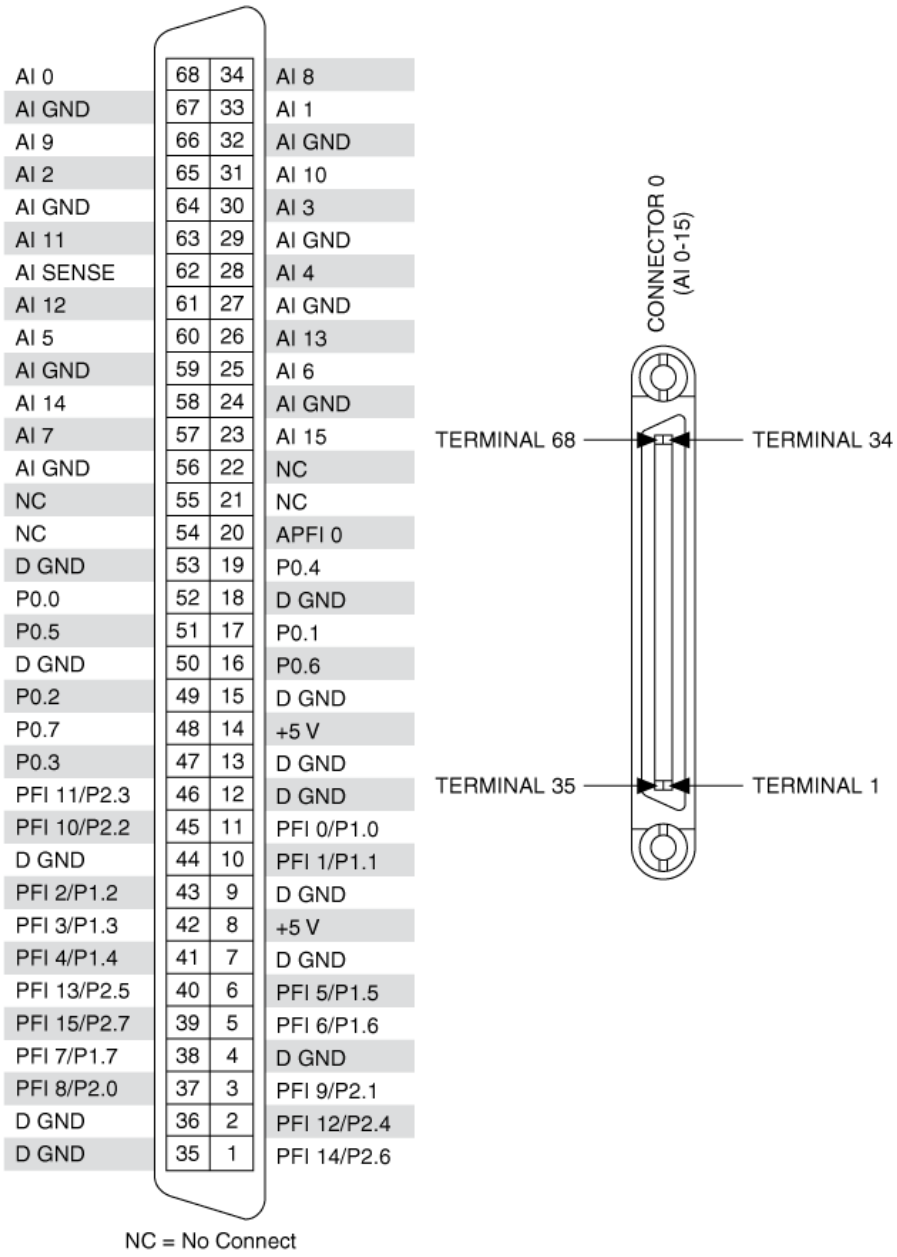
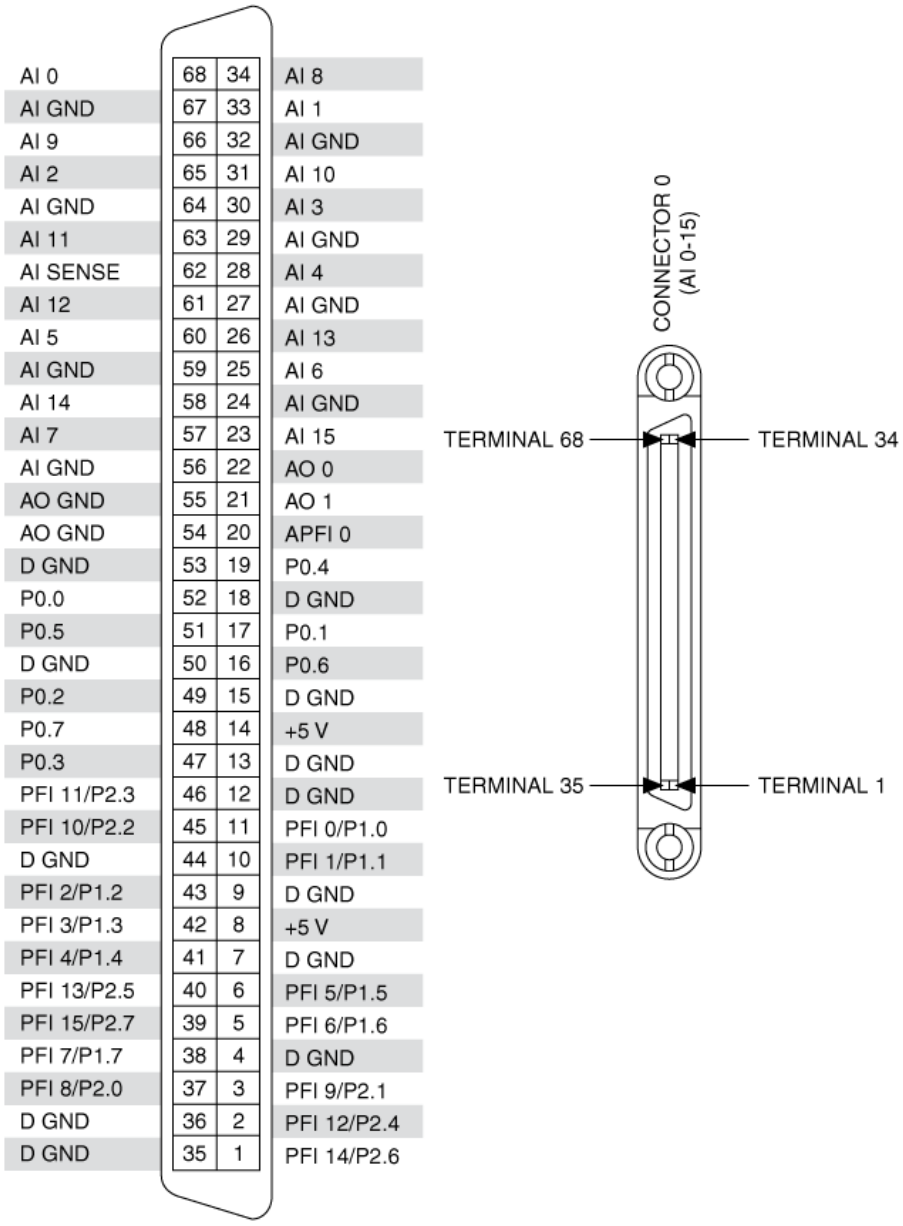
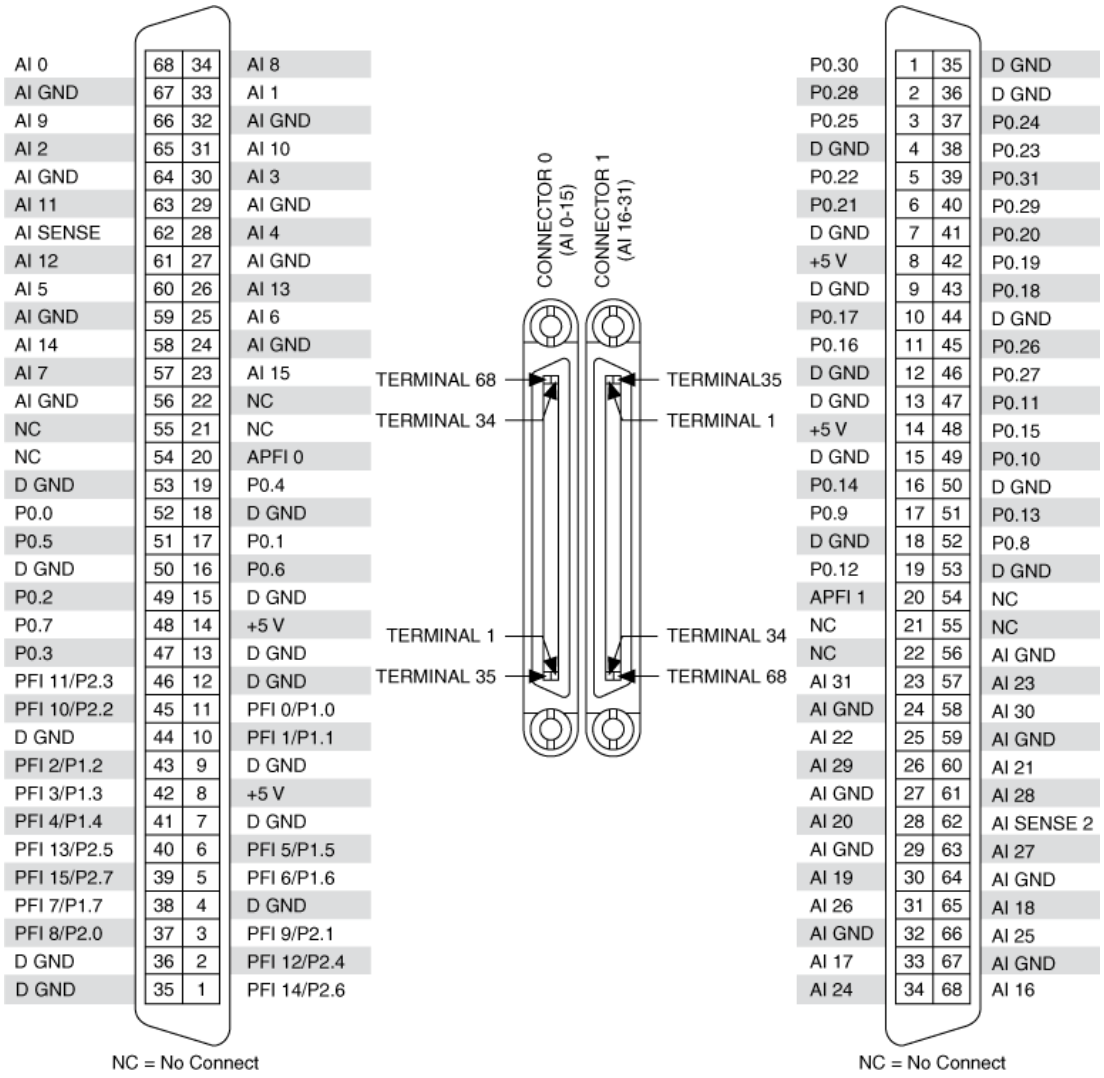
Pinouts/Front Panel Connections



NI PCI/PXI-6250 Pinout



NI PCI/PCIe/PXI/PXIe-6251 Pinout



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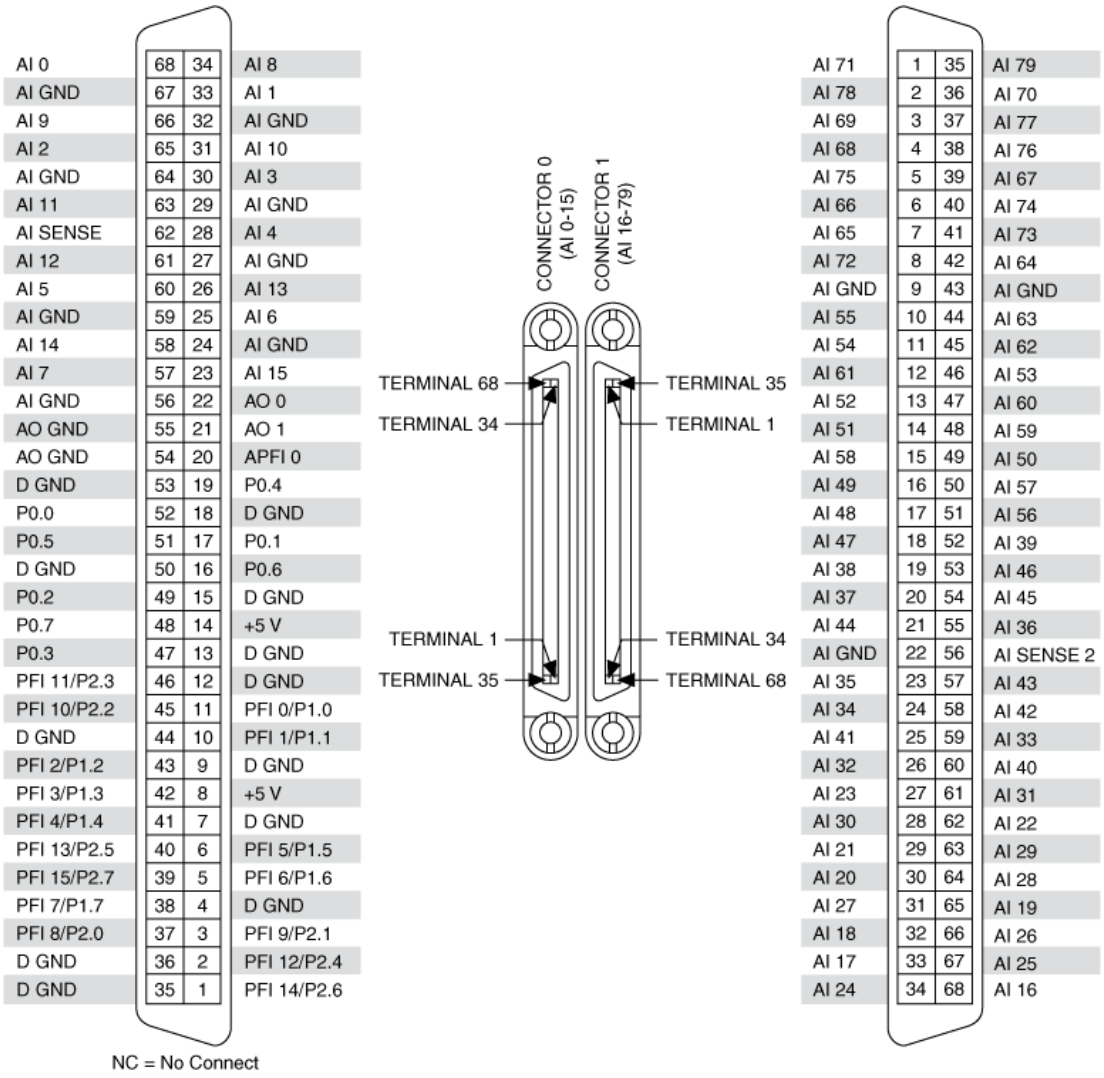
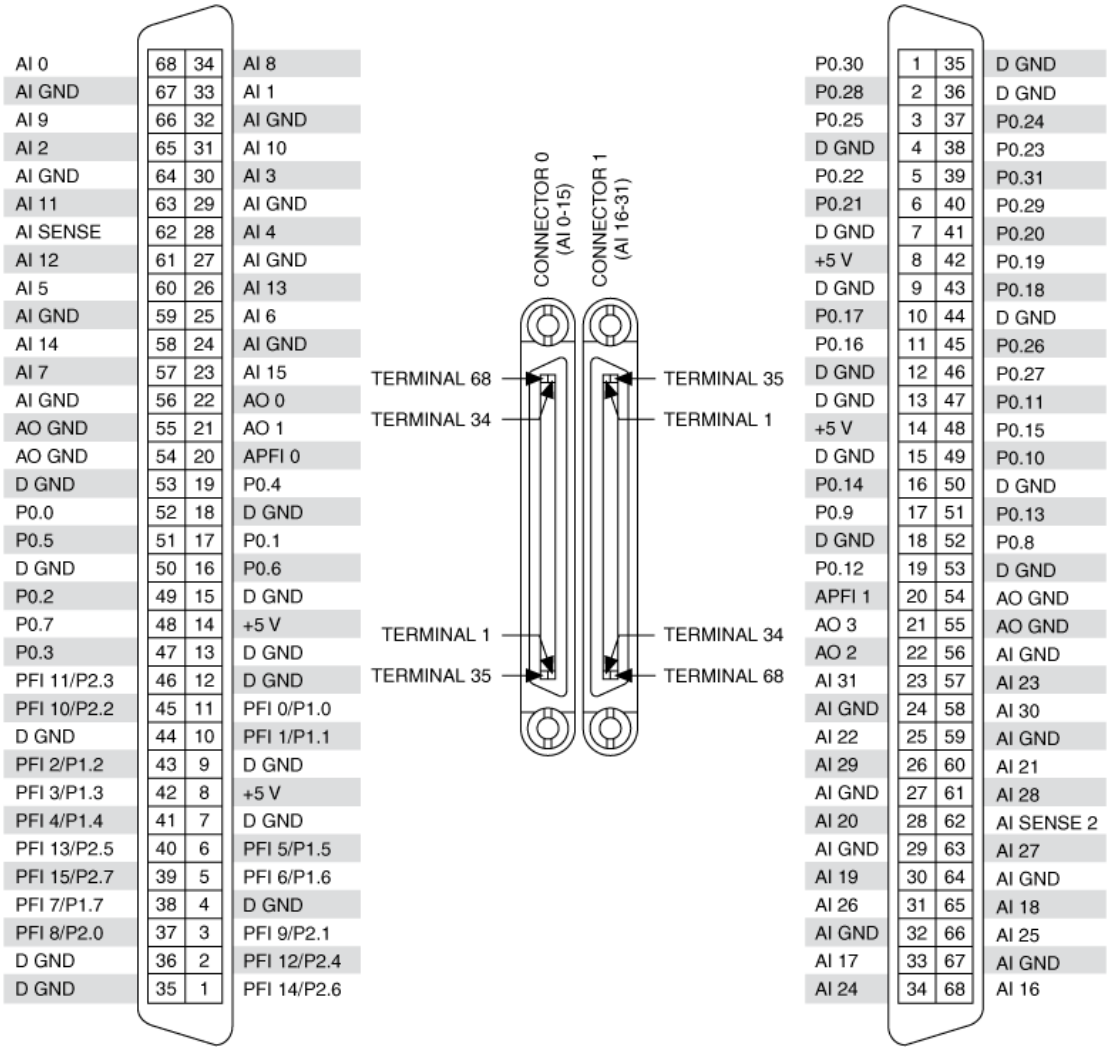


NI PCI/PXI-6255 Pinout



NI PCI/PCIe/PXI/PXIe-6259 Pinout

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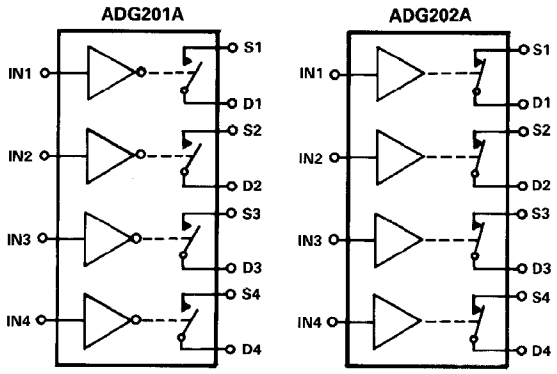
LC²MOS
Quad SPST Switches

ADG201A/ADG202A

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω)
Low Leakage (0.5nA)
Break Before Make Switching
Extended Plastic Temperature Range (−40°C to +85°C)
Low Power Dissipation (33mW)
Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
Superior Second Source:
ADG201A Replaces DG201A, HI-201
ADG202A Replaces DG202

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG201A IN	ADG202A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

ADG201A/ADG202A—SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise specified)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	$-10V \leq V_S \leq +10V$
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$; $V_S \mp 14V$; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
OFF Isolation	80		80		80		dB typ	V_S = 10V(p-p); f = 100kHz
								R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D 30mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
Voltage at IN . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

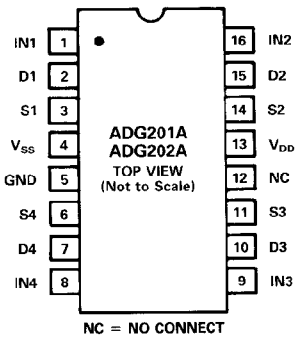
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201AKN	−40°C to +85°C	N-16
ADG201AKR	−40°C to +85°C	R-16A
ADG201AKP	−40°C to +85°C	P-20A
ADG201ABQ	−40°C to +85°C	Q-16
ADG201ATQ	−55°C to +125°C	Q-16
ADG201ATE	−55°C to +125°C	E-20A
ADG202AKN	−40°C to +85°C	N-16
ADG202AKR	−40°C to +85°C	R-16A
ADG202AKP	−40°C to +85°C	P-20A
ADG202ABQ	−40°C to +85°C	Q-16
ADG202ATQ	−55°C to +125°C	Q-16
ADG202ATE	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

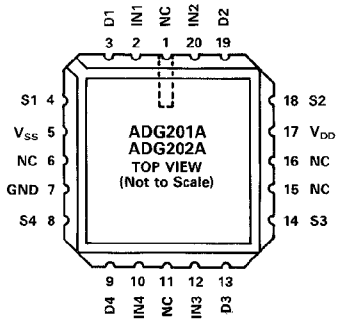
PIN CONFIGURATIONS

DIP, SOIC



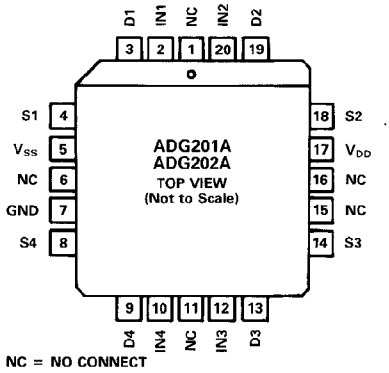
NC = NO CONNECT

LCCC



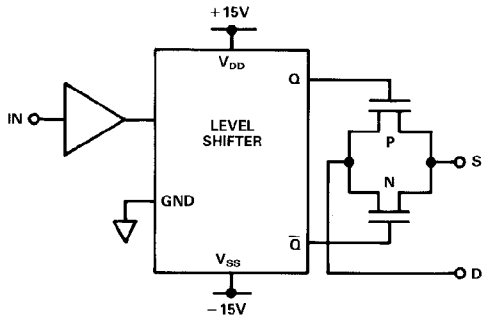
NC = NO CONNECT

PLCC



NC = NO CONNECT

ADG201A/ADG202A FUNCTIONAL DIAGRAM



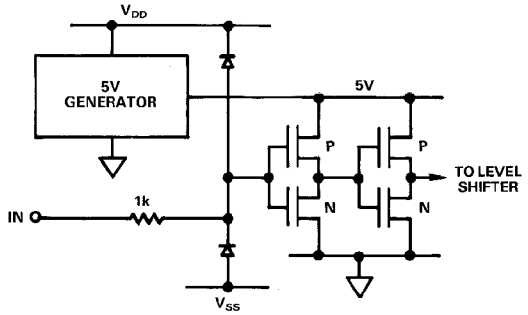
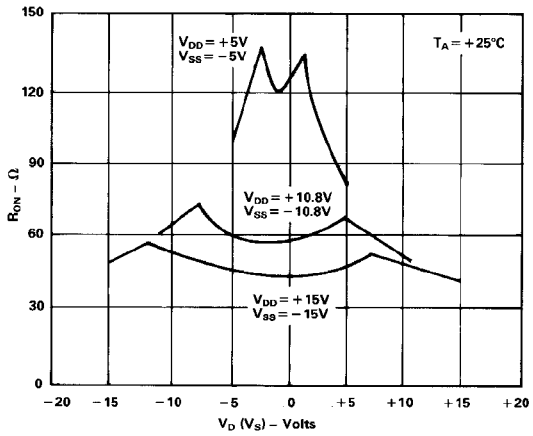


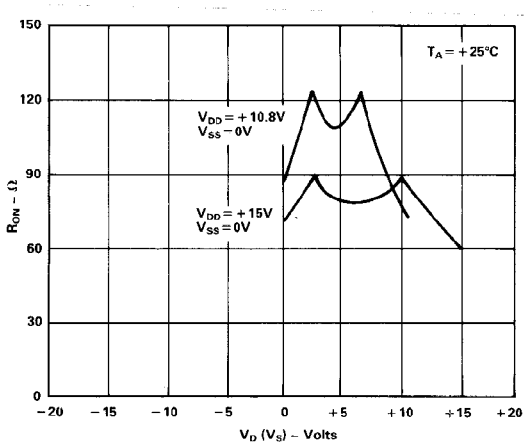
Figure 1. Typical Digital Input Cell

ADG201A/ADG202A—Typical Performance Characteristics

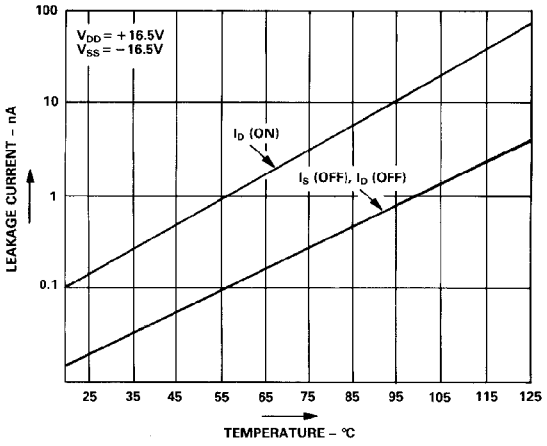
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



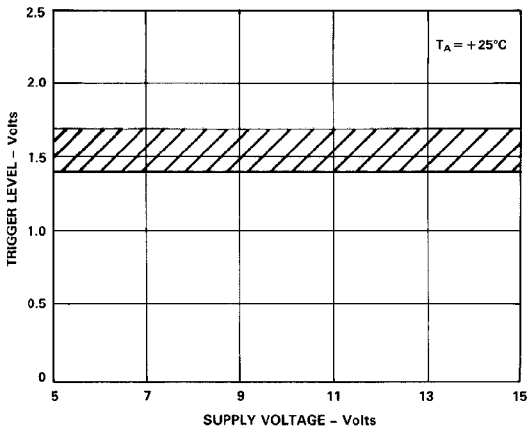
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



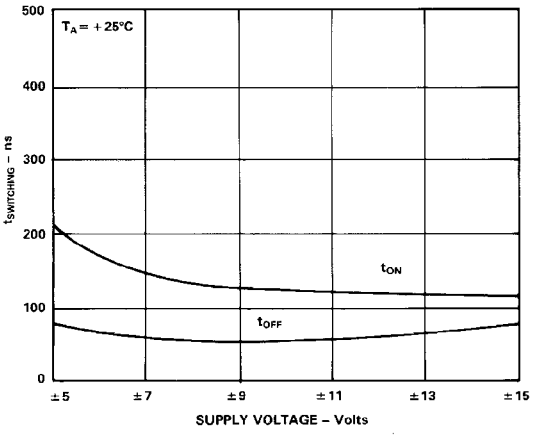
R_{ON} as a Function of V_D (V_S): Single Supply Voltage



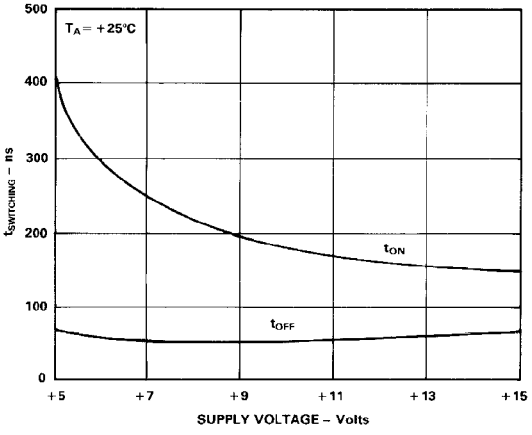
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



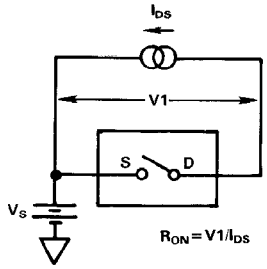
Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage



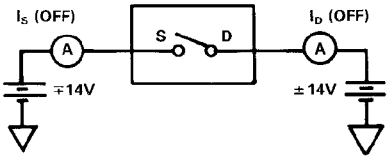
Switching Time vs. Supply Voltage (Dual Supply)



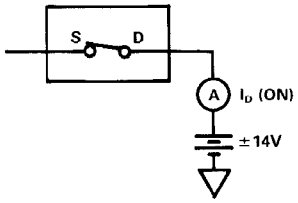
Switching Time vs. Supply Voltage (Single Supply)



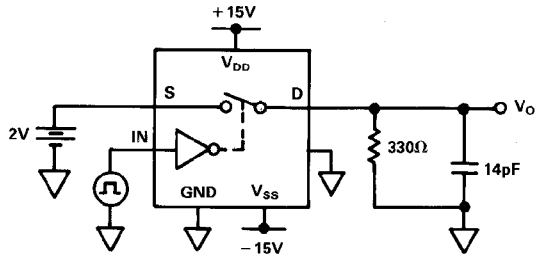
Test Circuit 1

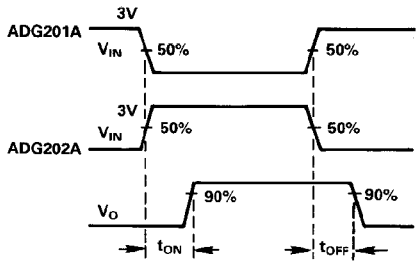


Test Circuit 2

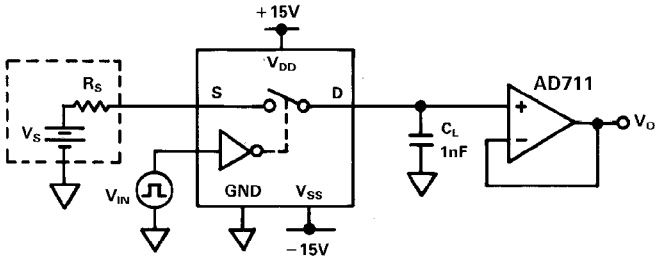


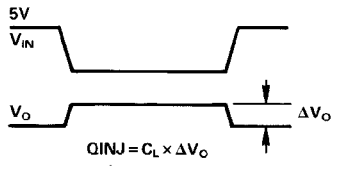
Test Circuit 3



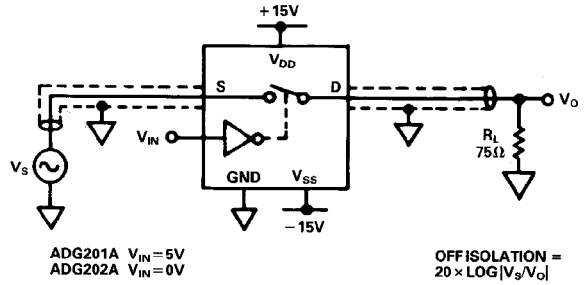


Test Circuit 4

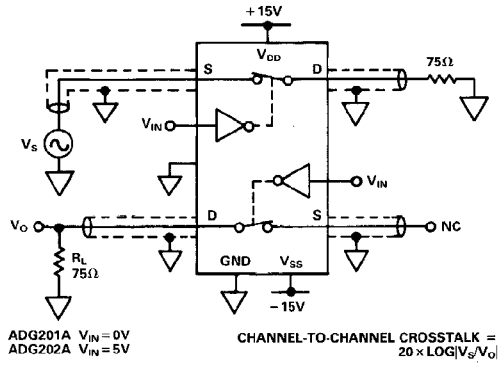




Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk

TERMINOLOGY

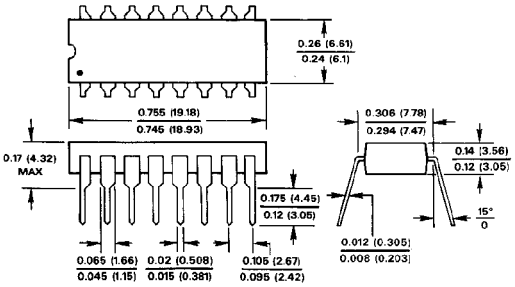
R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_D, C_S (ON)	Input or output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another
V_{INL}	Maximum Input Voltage for a Logic Low
V_{INH}	Minimum Input Voltage for a Logic High
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

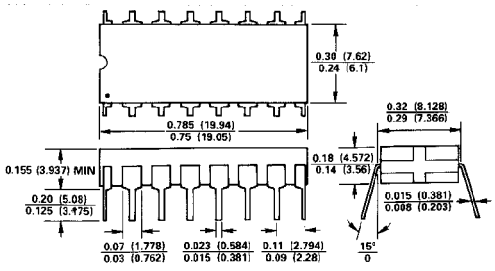
Dimensions shown in inches and (mm).

16-Pin Plastic (N-16)

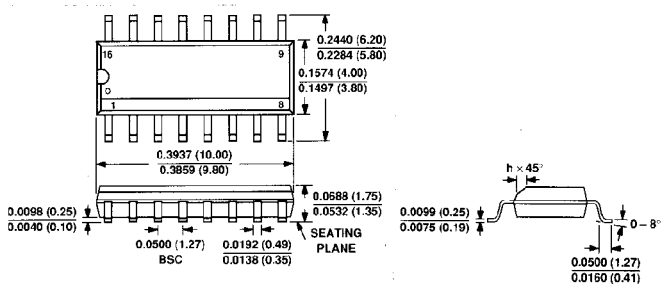


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

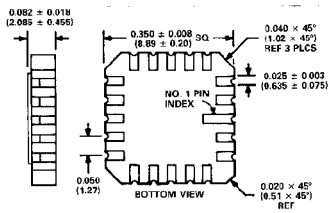
16-Pin Cerdip (Q-16)



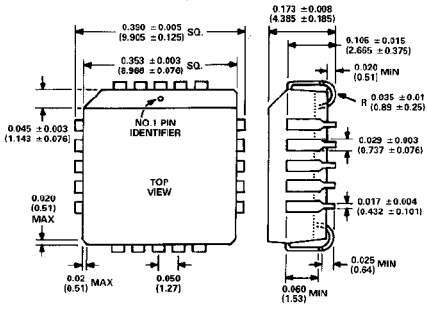
SOIC Package (R-16A)



20-Terminal Leadless Ceramic Chip Carrier (E-20A)



20-Terminal Plastic Leaded Chip Carrier (P-20A)



National Semiconductor

May 1999

LM6164/LM6264/LM6364
High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per µs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

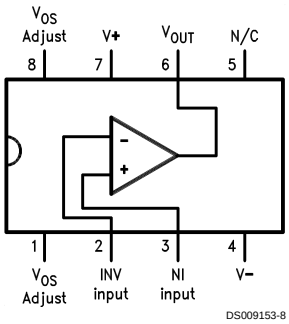
Features

- High slew rate: 300 V/µs
- High GBW product: 175 MHz
- Low supply current: 5 mA
- Fast settling: 100 ns to 0.1%
- Low differential gain: <0.1%
- Low differential phase: <0.1°
- Wide supply range: 4.75V to 32V
- Stable with unlimited capacitive load

Applications

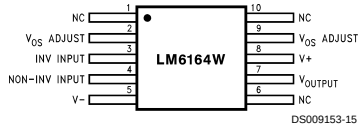
- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams



NS Package Number J08A, M08A or N08E

10-Lead Flatpak



Top View
NS Package Number W10A

VIP™ is a trademark of National Semiconductor Corporation.

Connection Diagrams (Continued)

Temperature Range			Package	NSC Drawing
Military $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	Industrial $-25^{\circ}C \leq T_A \leq +85^{\circ}C$	Commercial $0^{\circ}C \leq T_A \leq +70^{\circ}C$		
	LM6264N	LM6364N	8-Pin Molded DIP	N08E
LM6164J/883 5962-8962401PA			8-Pin Ceramic DIP	J08A
		LM6364M	8-Pin Molded Surface Mt.	M08A
LM6164WG/883 5962-8962401XA			10-Lead Ceramic SOIC	WG10A
LM6164W/883 5962-8962401HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage	
(Note 7)	±8V
Common-Mode Input Voltage	
(Note 11)	(V^+ − 0.7V) to (V^- + 0.7V)
Output Short Circuit to Gnd	
(Note 2)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260˚C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	−65˚C to +150˚C
Max Junction Temperature	
(Note 3)	150˚C
ESD Tolerance (Notes 7, 8)	±700V

Operating Ratings

Temperature Range (Note 3)	
LM6164	$-55^\circ C \le T_J \le +125^\circ C$
LM6264	$-25^\circ C \le T_J \le +85^\circ C$
LM6364	$0^\circ C \le T_J \le +70^\circ C$
Supply Voltage Range	4.75V to 32V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \ge 100$ kΩ and R_S = 50Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 4, 12)	LM6264 Limit (Note 4)	LM6364 Limit (Note 4)	Units
V_{OS}	Input Offset Voltage		2	4	4	9	mV
				6	**6**	**11**	max
V_{OS} Drift	Input Offset Voltage Average Drift		6				µV/˚C
I_b	Input Bias Current		2.5	3	3	5	µA
				6	**5**	**6**	max
I_{OS}	Input Offset Current		150	350	350	1500	nA
				800	**600**	**1900**	max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/˚C
R_{IN}	Input Resistance	Differential	100				kΩ
C_{IN}	Input Capacitance		3.0				pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 10)	2.5	1.8	1.8	1.3	V/mV
				0.9	**1.2**	**1.1**	min
		R_L = 10 kΩ	9				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9	+13.9	+13.8	V
				+13.8	**+13.8**	**+13.7**	min
			−13.5	−13.3	−13.3	−13.2	V
				−13.1	**−13.1**	**−13.1**	min
		Supply = +5V (Note 5)	4.0	3.9	3.9	3.8	V
				3.8	**3.8**	**3.7**	min
			1.5	1.7	1.7	1.8	V
				1.9	**1.9**	**1.9**	max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	105	86	86	80	dB
				80	**82**	**78**	min
PSRR	Power Supply Rejection Ratio	±10V ≤ V± ≤ ±16V	96	86	86	80	dB
				80	**82**	**78**	min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 4, 12)	LM6264 Limit (Note 4)	LM6364 Limit (Note 4)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ	+14.2	+13.5	+13.5	+13.4	V
				+13.3	**+13.3**	**+13.3**	min
			−13.4	−13.0	−13.0	−12.9	V
				−12.7	**−12.8**	**−12.8**	min
		Supply = +5V and R_L = 2 kΩ (Note 10)	4.2	3.5	3.5	3.4	V
				3.3	**3.3**	**3.3**	min
			1.3	1.7	1.7	1.8	V
				2.0	**1.9**	**1.9**	max
	Output Short Circuit Current	Source	65	30	30	30	mA
				20	**25**	**25**	min
		Sink	65	30	30	30	mA
				20	**25**	**25**	min
I_S	Supply Current		5.0	6.5	6.5	6.8	mA
				6.8	**6.7**	**6.9**	min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 4, 12)	LM6264 Limit (Note 4)	LM6364 Limit (Note 4)	Units
GBW	Gain-Bandwidth Product	F = 20 MHz	175	140	140	120	MHz
				100	**120**	**100**	min
		Supply = ±5V	120				
SR	Slew Rate	A_V = +5 (Note 9)	300	200	200	200	V/µs
				180	**180**	**180**	min
		Supply = ±5V	200				
PBW	Power Bandwidth	$V_{OUT} = 20\ V_{PP}$	4.5				MHz
T_S	Settling Time	10V Step to 0.1% A_V = −4, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +5	45				Deg
A_D	Differential Gain	NTSC, A_V = +10	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +10	<0.1				Deg
e_{np-p}	Input Noise Voltage	F = 10 kHz	8				$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	F = 10 kHz	1.5				$pA/\sqrt{Hz}$

Note 2: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105˚C/Watt, the molded plastic SO (M) package is 155˚C/Watt, and the cerdip (J) package is 125˚C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}.

Note 6: $C_L \leq 5$ pF.

Note 7: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 8: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

AC Electrical Characteristics (Continued)

Note 9: V_{IN} = 4V step. For supply = ±5V, V_{IN} = 1V step.

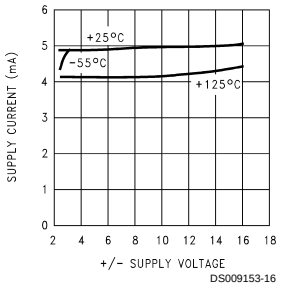
Note 10: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 11: The voltage between V^+ and either input pin must not exceed 36V.

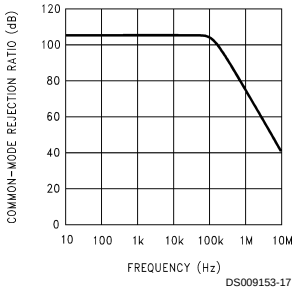
Note 12: A military RETS electrical test specification is available on request. At the time of printing, the LM6164J/883 RETS spec complied with the **Boldface** limits in this column. The LM6164J/883 may also be procured as Standard Military Drawing #5962-8962401PA.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25˚C unless otherwise specified)

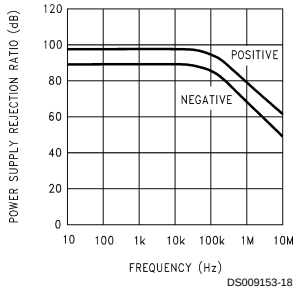
Supply Current vs Supply Voltage



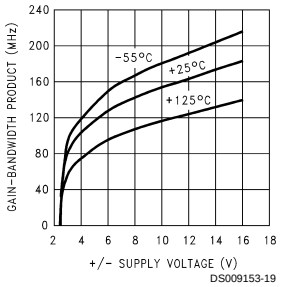
Common-Mode Rejection Ratio



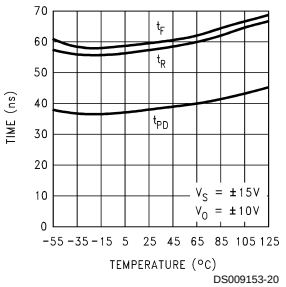
Power Supply Rejection Ratio



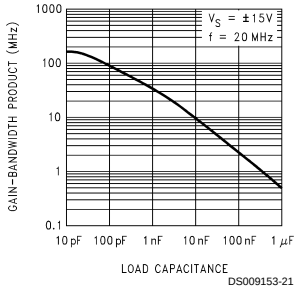
Gain-Bandwidth Product



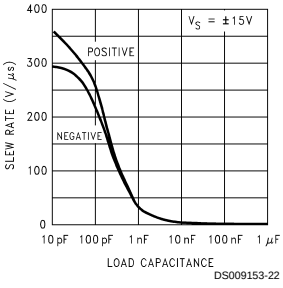
Propagation Delay Rise and Fall Time



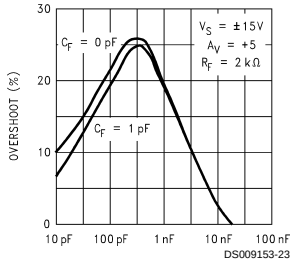
Gain-Bandwidth Product vs Load Capacitance



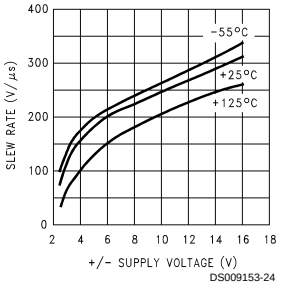
Slew Rate vs Load Capacitance



Overshoot vs Load Capacitance

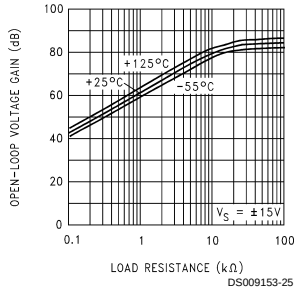


Slew Rate



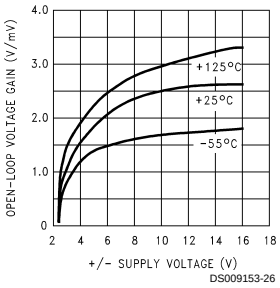
Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25˚C unless otherwise specified) (Continued)

Voltage Gain vs Load Resistance



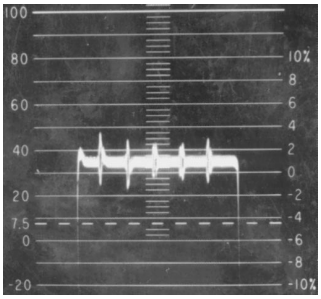
DS009153-25

Gain vs Supply Voltage



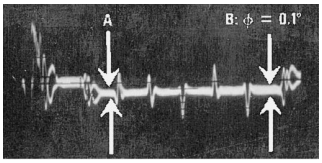
DS009153-26

Differential Gain
(Note 13)



DS009153-6

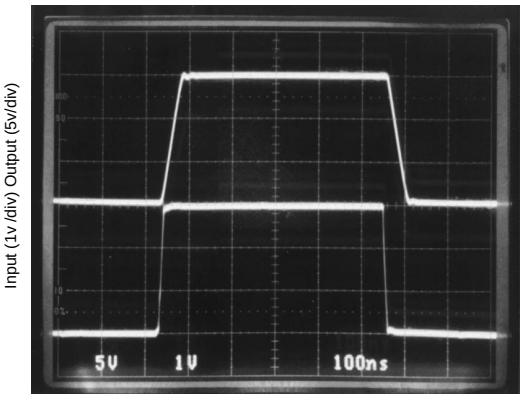
Differential Phase
(Note 13)



DS009153-7

Note 13: Differential gain and differential phase measured for four series LM6364 op amps in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system. Configured with a gain of +5 (each output attenuated by 80%)

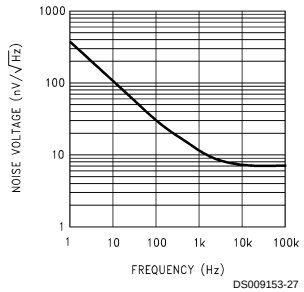
Step Response; Av = +5



DS009153-1

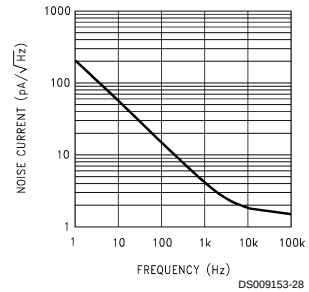
Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25˚C unless otherwise specified) (Continued)

Input Noise Voltage



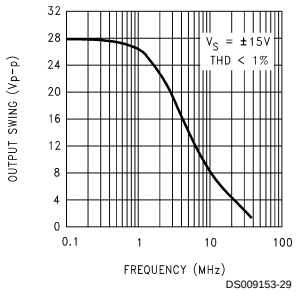
DS009153-27

Input Noise Current



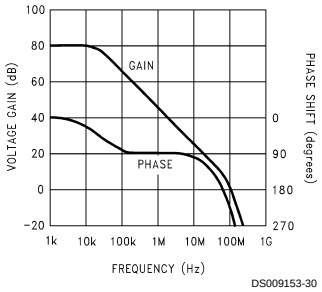
DS009153-28

Power Bandwidth



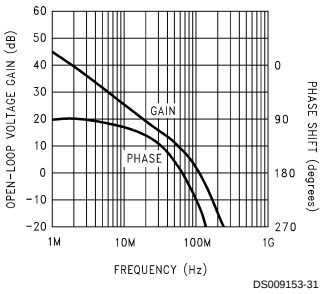
DS009153-29

Open-Loop Frequency Response



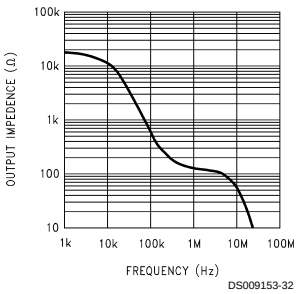
DS009153-30

Open-Loop Frequency Response



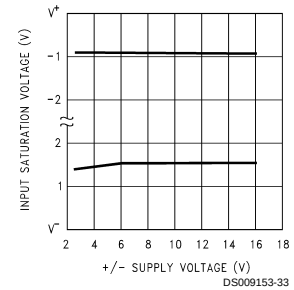
DS009153-31

Output Resistance Open-Loop



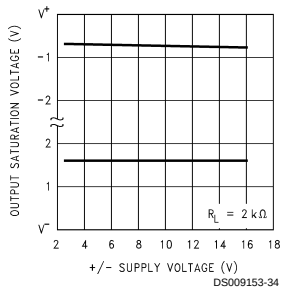
DS009153-32

Common-Mode Input Saturation Voltage



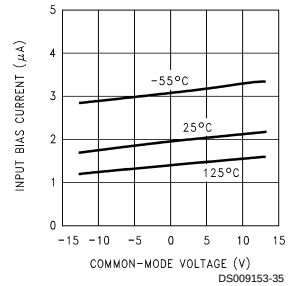
DS009153-33

Output Saturation Voltage



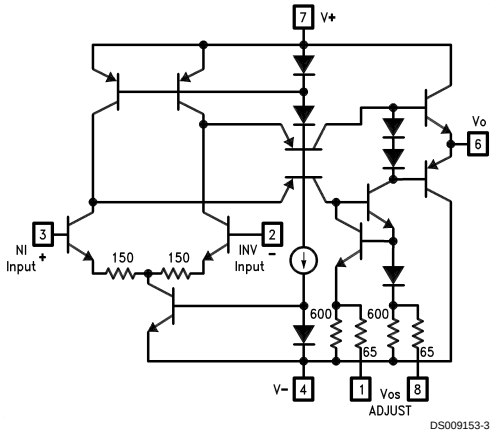
DS009153-34

Bias Current vs Common-Mode Voltage



DS009153-35

Simplified Schematic



DS009153-3

Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/µs), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

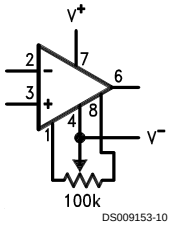
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 µF to 0.1 µF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 µF to 10 µF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

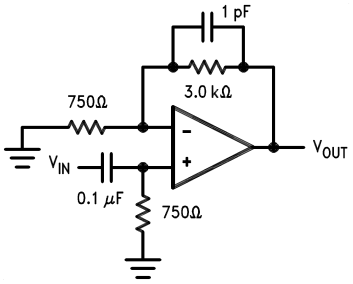
Typical Applications

Offset Voltage Adjustment



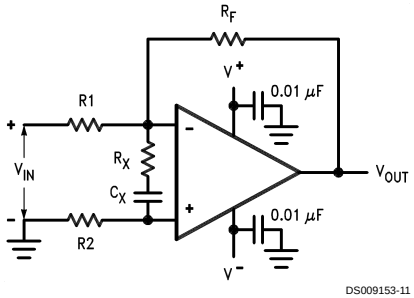
DS009153-10

Video-Bandwidth Amplifier



DS009153-12

Noise-Gain Compensation for Gains ≤5

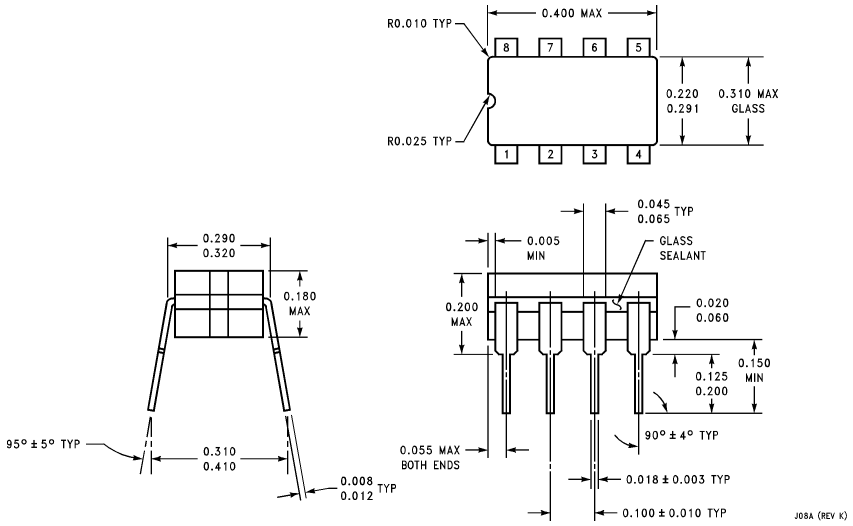


DS009153-11

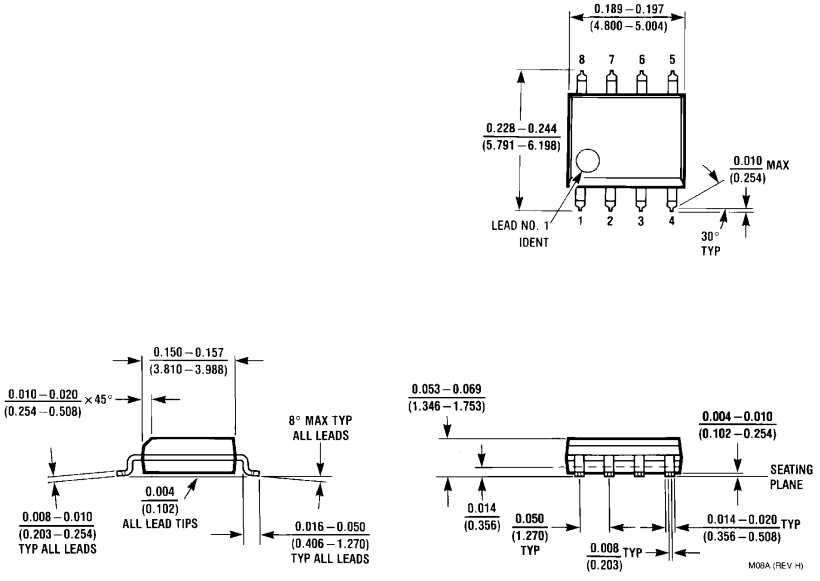
$R_X C_X \geq (2\pi \cdot 25\ MHz)^{-1}$

$5\ R_X = R_1 + R_F(1 + R_1/R_2)$

Physical Dimensions inches (millimeters) unless otherwise noted

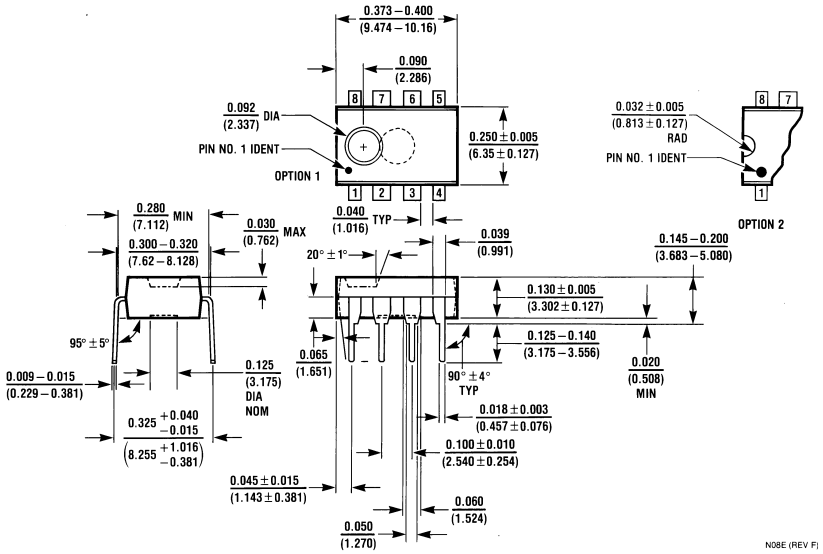


Ceramic Dual-In-Line Package (J)
Order Number LM6164J/883
NS Package Number J08A

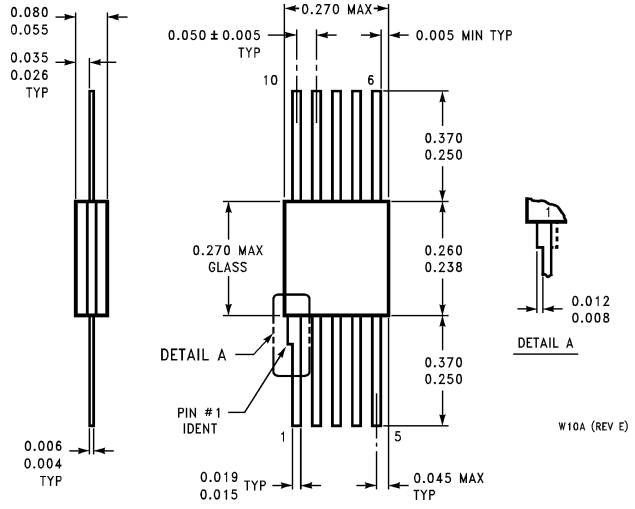


Molded Package SO (M)
Order Number LM6364M
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LM6264N or LM6364N
NS Package Number N08E



10-Pin Ceramic Flatpak
Order Number LM6164W/883
NS Package Number W10A

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS154
4-Line to 16-Line Decoder/Demultiplexer

General Description

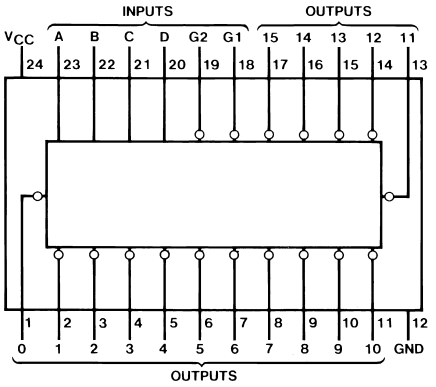
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 23 ns
  Strobe 19 ns
- Typical power dissipation 45 mW

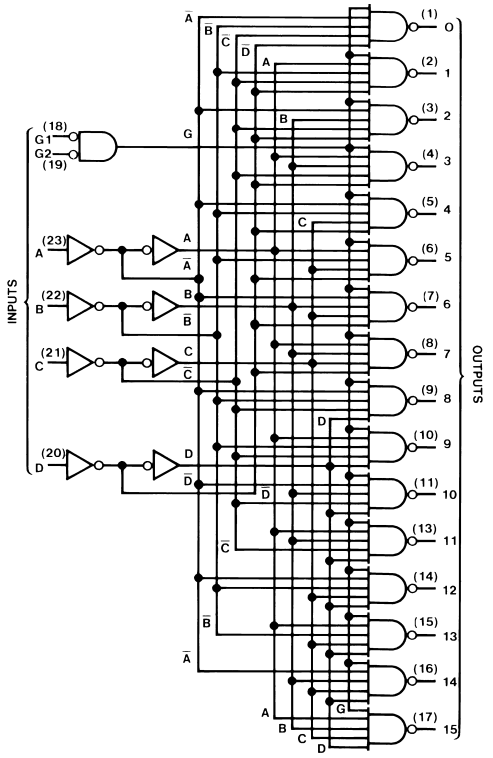
Connection and Logic Diagrams

Dual-In-Line Package



DS006394-1

Order Number DM54LS154J,
DM74LS154WM or DM74LS154N
See Package Number J24A, M24B or N24A



DS006394-2

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM74		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min			0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9	14	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20		25	ns

Switching Characteristics (Continued)

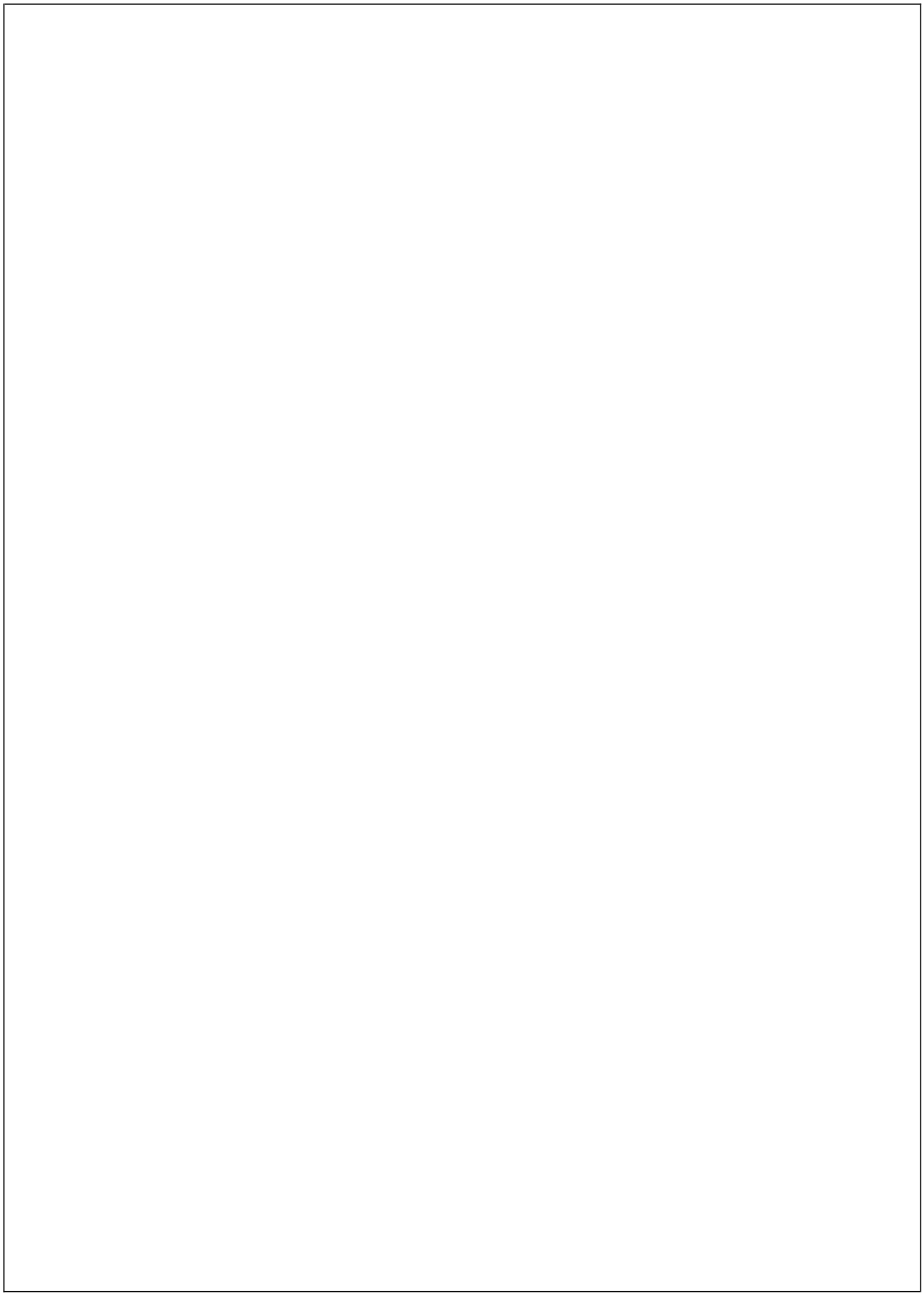
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		25		35	ns

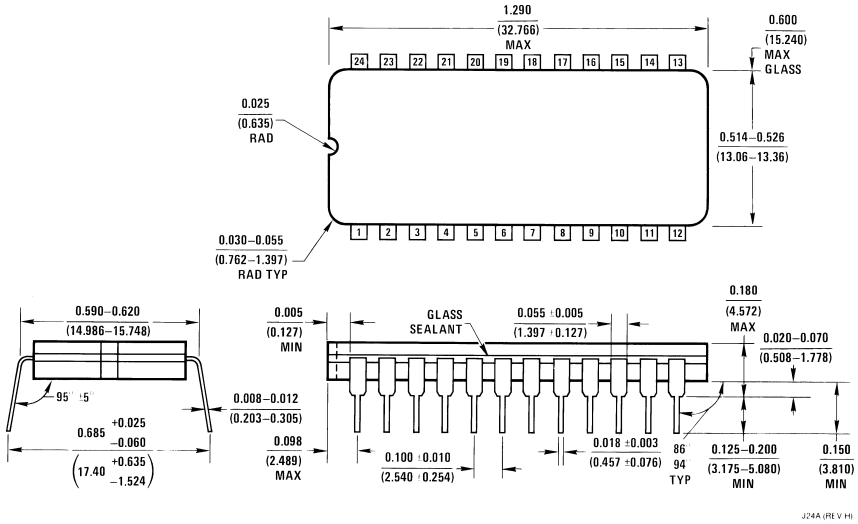
Function Table

Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

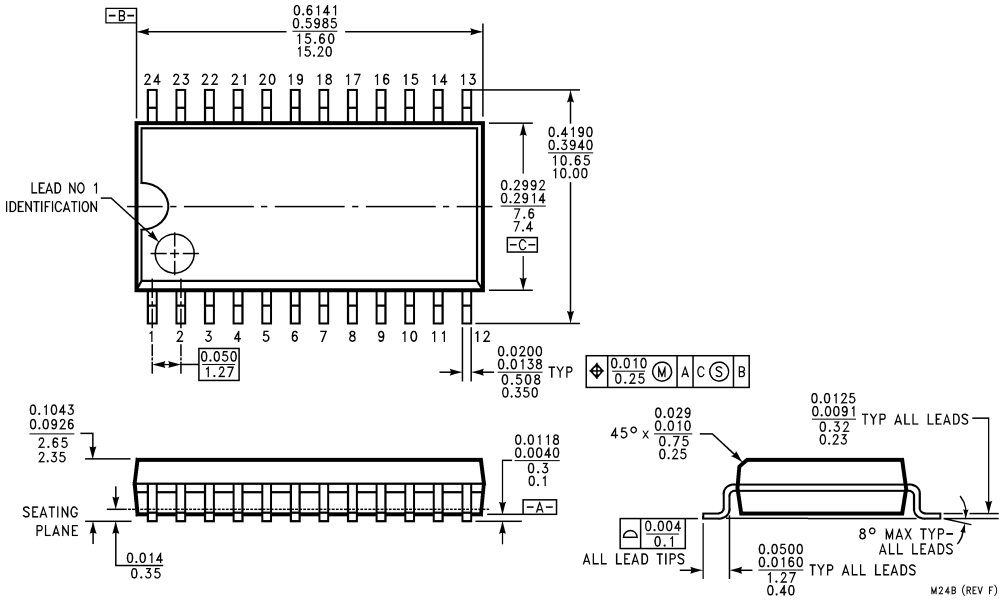
H = High Level, L = Low Level, X = Don't Care



Physical Dimensions inches (millimeters) unless otherwise noted

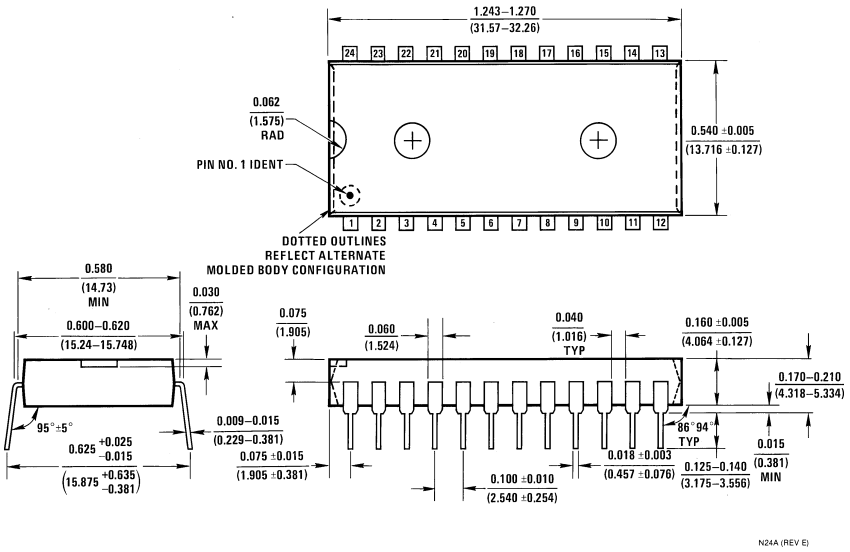


24-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS154J
Package Number J24A



24-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS154WM
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS154N
Package Number N24A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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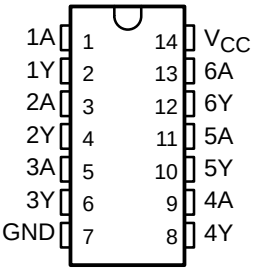
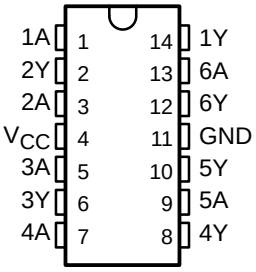
description

These devices contain six independent inverters.

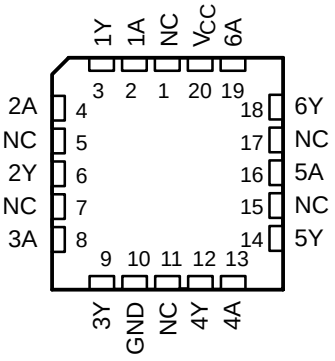
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
SN74S04 . . . D OR N PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

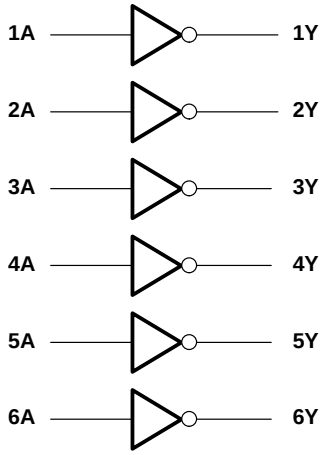
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC – D	Tube	SN7404D	7404
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP – NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
	SSOP – DB	Tape and reel	SN74LS04DBR	LS04
–55°C to 125°C	CDIP – J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP – W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC – FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

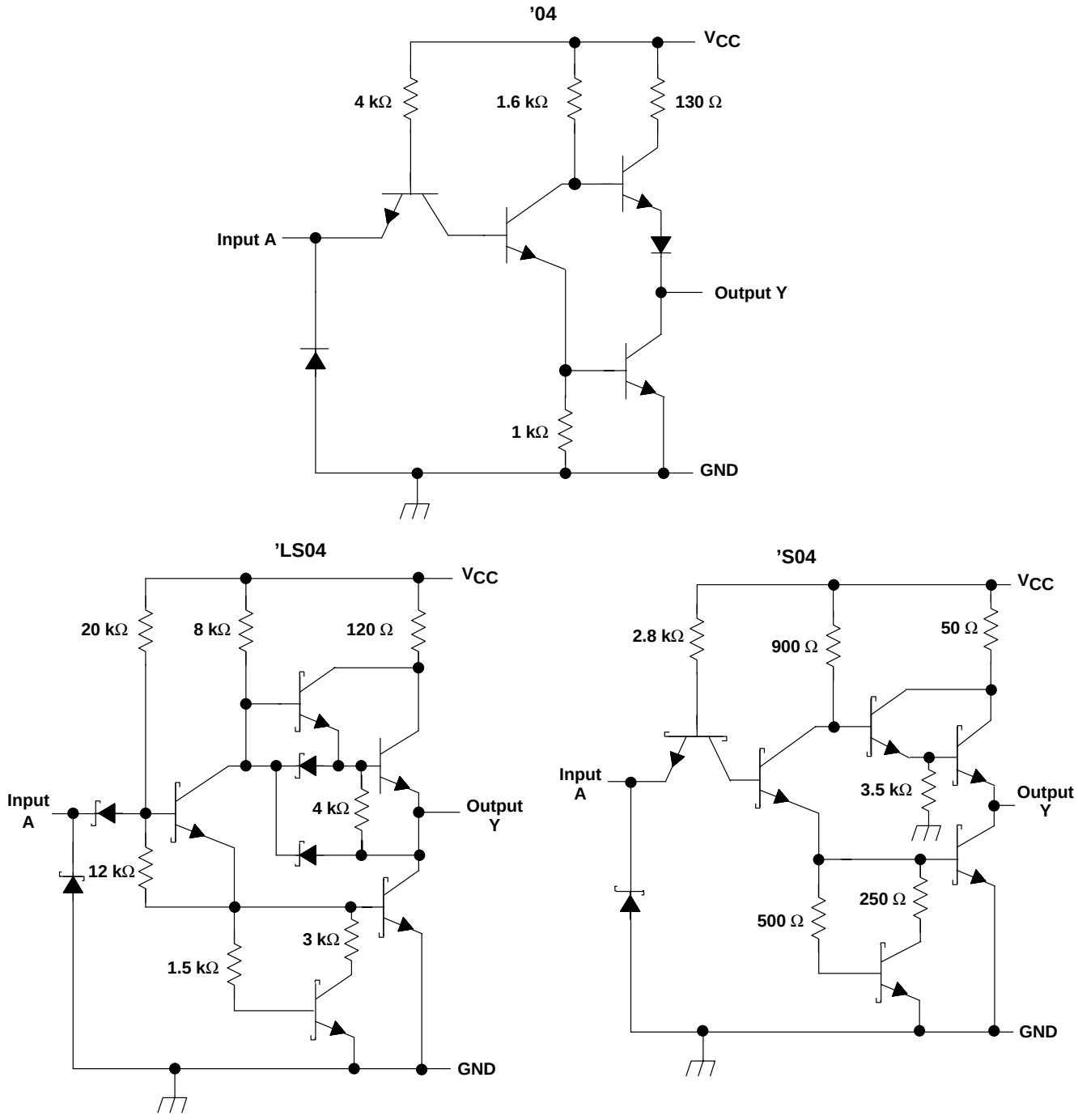
INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



$Y = \overline{A}$

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: '04, 'S04 . . . . . 5.5 V
'LS04 . . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5404			SN7404			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –12 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = –0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				–1.6			–1.6	mA
I_{OS}¶	V_{CC} = MAX			–20		–55	–18		–55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			18	33		18	33	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN5404 SN7404			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω,	C_L = 15 pF		12	22	ns
t_{PHL}						8	15	

recommended operating conditions

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04			SN74LS04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –18 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = –0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				–0.4			–0.4	mA
I_{OS}§	V_{CC} = MAX			–20		–100	–20		–100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54LS04 SN74LS04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 2 kΩ,	C_L = 15 pF		9	15	ns
t_{PHL}						10	15	

recommended operating conditions

		SN54S04			SN74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–1			–1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

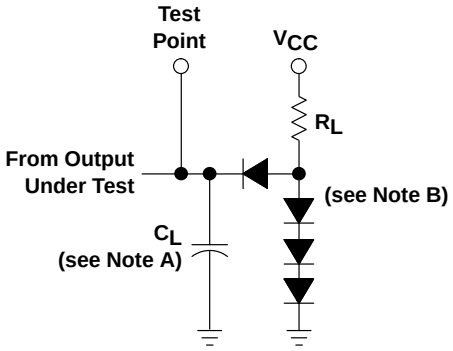
PARAMETER	TEST CONDITIONS†			SN54S04			SN74S04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = –1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V				–2			–2	mA
I_{OS}§	V_{CC} = MAX			–40		–100	–40		–100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			15	24		15	24	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

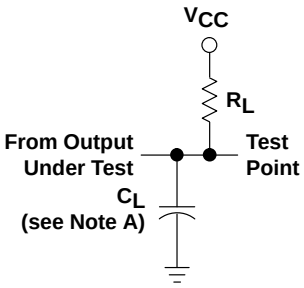
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54S04 SN74S04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		

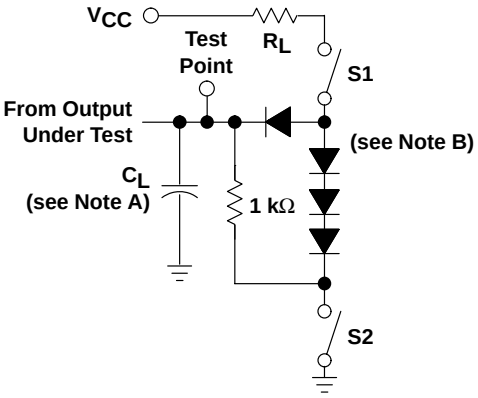
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



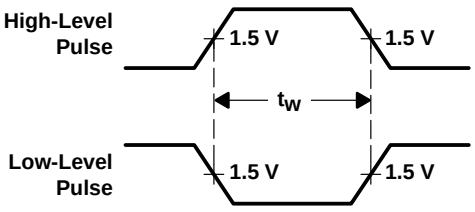
**LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS**



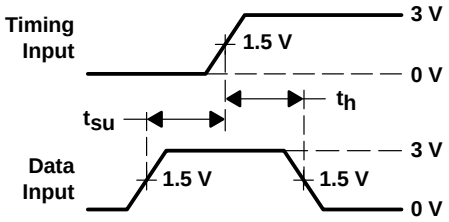
**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**



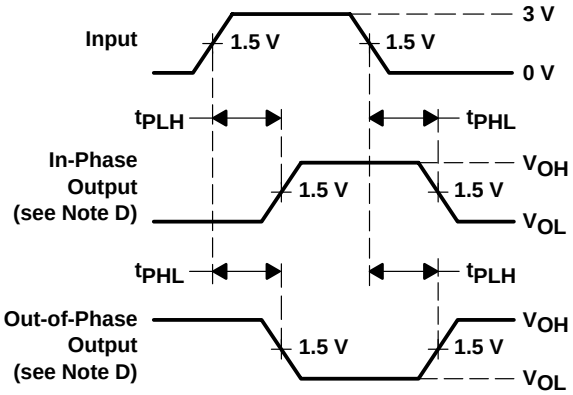
**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**



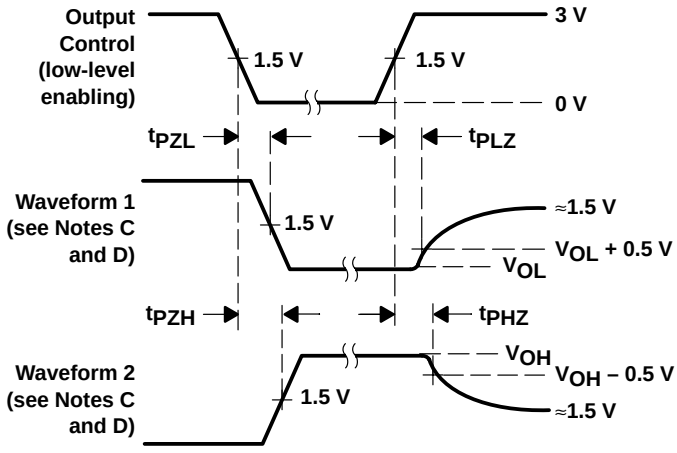
**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

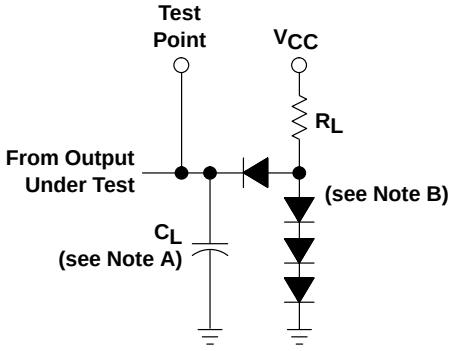


**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

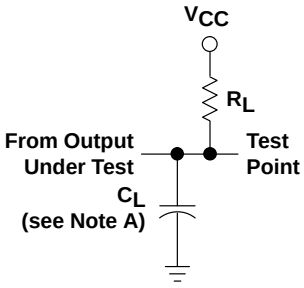
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

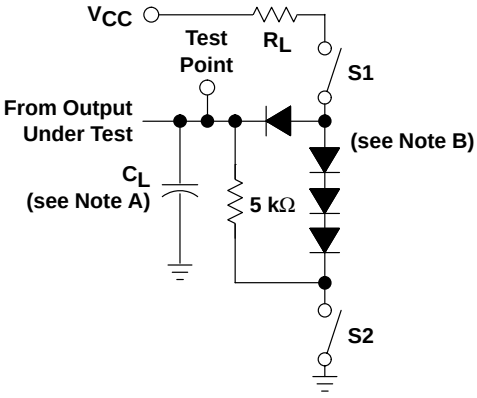
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



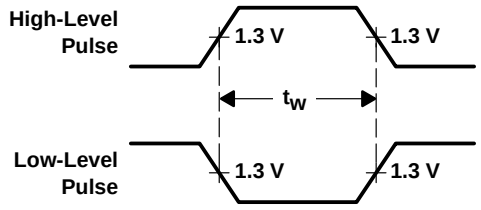
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



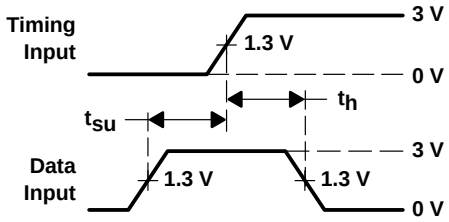
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



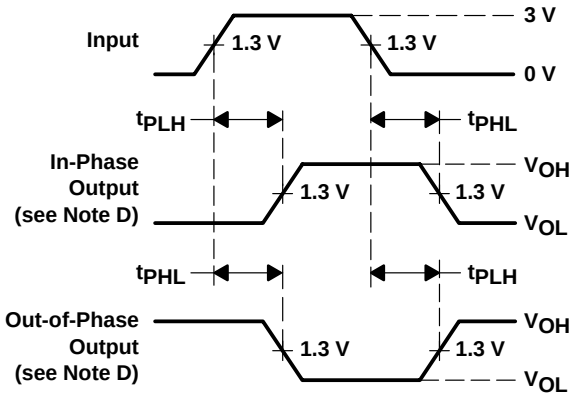
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



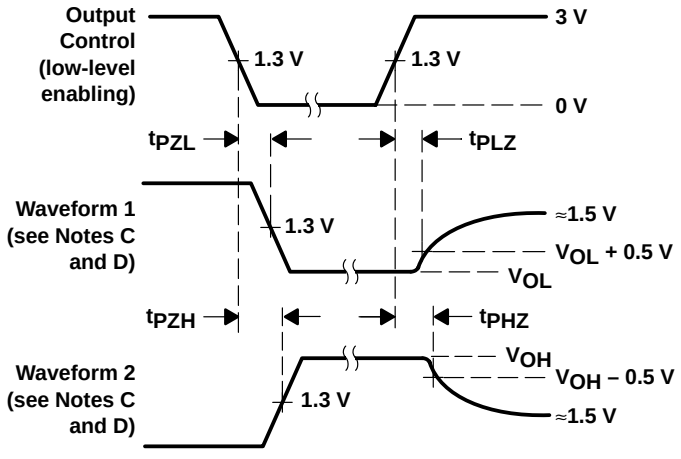
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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