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by

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by

NOR ZAIHAR YAHAYA

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hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

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DEDICATION

Above all I want to dedicate this work

To my PARENTS for their loving care

To my wife, NOR ADELA DINYATI for her caring love

To my children:

NAIM ZAFRAN

NAZRIN AQASHAH

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ABSTRACT

In this work, a new Synchronous Rectifier Buck Converter (SRBC) circuit is proposed that reduces low switching and conduction losses. Moreover, the Miller effect has also been reduced. The limitations of existing single-channel resonant gate driver (S-CRGD) is studied to determine the optimized parameter values in terms of duty cycle, dead time and resonant inductance. The findings result in designing the new SRBC circuit's symmetrical dual-channel resonant gate drive (D-CRGD). The aim is to generate low switching and gate drive losses by operating in Zero Voltage Switching (ZVS) and lower on-state drain voltage conditions. It is found that the SRBC can operate effectively at 1 MHz compared to the conventional SRBC in solving the issues of dead time and effect of switching frequency. Experimental results are presented to validate the analysis of the proposed design procedure and to demonstrate the performance of the proposed approach. In addition, several gate drive control schemes such as Fixed Dead Time (FDT), Adaptive Gate Drive (AGD) and Predictive Gate Drive (PGD) have been simulated and the results show that FDT can operate SRBC correctly with shorter dead time and eventually reduce body diode conduction loss. Even though FDT is prone to cross-conduction effect, the design stage is simple. Apart from this, AGD and PGD control schemes have also shown high level of efficiency. However, AGD generates more losses which makes PGD preferable in achieving a highly efficient converter although there are advantages in FDT scheme.

Keywords: Gate Drive, High Frequency, Resonant Snubber Network, Synchronous Rectifier Buck Converter.

ABSTRAK

Di dalam hasil kerja ini, litar peronta segerak penerus (SRBC) yang baru telah dicadangkan bagi mengurangkan kehilangan pengaliran. Selain itu, kesan Miller juga telah berkurangan. Tujuan utama hasil kerja ini adalah untuk memahami keterbatasan reka bentuk litar get pemacu yang boleh menjejaskan prestasi litar. Penyelaku Pspice digunakan untuk menentukan nilai optimum pemacu galah tiang elu yang meliputi kitaran suis hidup, waktu mati dan kearuhan salunan. Litar saluran tunggal pemacu get resonans (S-CRGD) dinilai yang memberikan hasil dalam reka bentuk get pemacu salunan saluran simetri (D-CRGD) untuk litar SRBC. Tujuannya adalah untuk menghasilkan pensuisan rendah dan pengurangan get pemacu beroperasi di penguisan voltan sifar (ZVS). Ini menunjukkan bahawa SRBC boleh beroperasi secara efektif pada julat 1 MHz berbanding dengan litar lazim. Keputusan kajian berdasarkan prototaip 15-W diusulkan untuk mengesahkan analisis tatacara rekabentuk yang dicadangkan dan untuk menunjukkan prestasi dari pendekatan yang dicadangkan. Selain itu, beberapa skim kawalan get pemacu telah diselakukan dan hasilnya menunjukkan bahawa waktu mati tetap (FDT) dapat membantu mendorong SRBC mengurangkan kerugian pengaliran tubuh diod. Walaupun FDT terdedah terhadap kesan lintas pengaliran, tahap reka bentuknya adalah mudah. Selain itu, pemacu get suai (AGD) dan pemacu get ramalan (PGD) skim kawalan juga menunjukkan tahap kecekapan yang tinggi. Namun, AGD terdapat beberapa kekurangan. Hal ini menjadikan PGD lebih baik walaupun terdapat kelebihan dalam skim FDT.

Kata kunci: Skim Litar Get Pemacu, Frekuensi Tinggi, Rangkaian Resonan, Litar Peronta Segerak Penerus

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LIST OF ABBREVIATIONS

AGD	Adaptive Gate Drive
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
D-CRGD	Dual-channel Resonant Gate Drive
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FDT	Fixed Dead Time
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PGD	Predictive Gate Drive
PWM	Pulse Width Modulation
RGD	Resonant Gate Drive
SRBC	Synchronous Rectifier Buck Converter
S-CRGD	Single-channel Resonant Gate Drive
TTL	Transistor Transistor Logic
ZCS	Zero Current Switching

ZVS	Zero Voltage Switching

LIST OF SYMBOLS

C_{iss}	Input Capacitance	(F)
D	Duty Ratio	(between 0 and 1)
f_r	Resonant Frequency	(Hz)
f_s	Switching Frequency	(Hz)
P_{diss}	Power Dissipation	(W)
$R_{ds(on)}$	On-state Resistance	(Ω)
T_D	Dead Time	(s)
T_s	Switching Period	(s)
V_{ds}	Drain-source Voltage	(V)
V_{gs}	Gate-source Voltage	(V)
V_N	Node Voltage	(V)
V_{ref}	Reference Voltage	(V)
V_{th}	Threshold Voltage	(V)
Z_0	Impedance	(Ω)

CHAPTER 1

INTRODUCTION

1.1 Chapter Overview

This chapter introduces the importance of the research in high frequency operation. The synchronous rectifier buck converter (SRBC) is adopted as the test circuit. The work is divided into simulation and experimentation. The aim is to investigate the performance of several gate drive and control techniques on the new SRBC.

1.2 Research Rationale

With switching frequency increased more than 1 MHz mark, the new state of the art converters have to be developed. For example, switching mode converters are required to provide power processing for applications ranging from computing and communications to medical electronics, powering microprocessors, cost effective, meet EMC (Electromagnetic Compliance) and the same time

i) reduce size and weight,

ii) improve load transient response,

iii) increase efficiency.

In recent years, there have been many studies focused on how to find better ways in regulating output current and voltage at variable loads, specifically in megahertz switching frequency. To achieve this, different types of resonant topologies have been proposed with an aim to achiev ter power schemes such as phase-shifted full-bridge, flyback, forward converters and many more. Nevertheless, the study only looks at the fixed load condition.

For instance, the synchronous rectifier buck converter (SRBC) can be adopted with the advancement of soft-switched topology. Switching aid networks such as ZVS and zero-current switching (ZCS) may be used to help improve converter's performance and hence further reduce switching loss. Moreover, low switching losses in the driving switches are required to design a high frequency gate drive circuit for SRBC.

1.3 Research Objectives

The primary objective of the research was to evaluate a "new" "Zero Voltage Switching Synchronous Rectifier Buck Converter (ZVS SRBC)" by comparing PSpice simulations with experimental measurements.

The secondary objective of the research was to demonstrate by PSpice simulations and experimental measurements the improved performance of the proposed system in terms of reduced gate drive loss and two SRBC MOSFET's power loss when compared to the Dual-Channel Resonant Gate Drive SRBC (D-CRGD SRBC)" and the conventional hard switched Synchronous Rectifier Buck Converter (SRBC).

1.4 Research Scope

The research will concentrate on the simulation of conventional and new dual-channel resonant gate driver (D-CRGD) for the new low-loss ZVS SRBC circuit. The PSpice circuit simulator is adopted in this work to observe the switching and circuit operating waveforms where the switching related losses will be determined for both circuits. The experimentation work is also carried out to verify the simulation. In addition, the simulation study on different gate drivers, effects on switching frequency, dead time and loads are the extension of the work which will be the preliminary results for further validation.

1.5 Chapter Summary

In the design of high frequency converter, the issue in getting the gate drive to operate accurately is important for the development of new low power SRBC. To do this, a comprehensive literature review is required to gather important data and evidences. The details are discussed in Chapter 2.

CHAPTER 2

LITERATURE REVIEW

2.1 Chapter Overview

This chapter looks into the history in the development of high frequency converter. It starts with techniques in gate drive design and its application in the converter. The importance, advantages and issues in resonant topologies are reviewed along with the implication on the performance of the converter, for example in terms of switching loss, body diode conduction loss and etc. There are also design constraints which include the role of limiting parameters in the gate driver as well as its control schemes and the switching MOSFET consideration. In addition, the effects of dead time, switching frequency, soft-switching technique on the converter are also explored in detail.

2.2 Gate Drive Circuit

The selection of gate drive circuit is crucial in high frequency converter design since it requires fast switching response and precise timing sequence that corresponds to power delivery capability. Fundamentally, a good gate driver must have high energy savings properties. Even though conventional gate driver is easy to implement, it generates high power dissipation.

On the other hand, resonant gate drive (RGD) circuit is preferred due to its low power loss. However, it normally involves complex circuit topologies which may eventually add to additional power loss in the circuit. With the attention in reducing the losses, the state-of-the-art RGD circuit is significant for the application of SRBC circuit. At high frequency, the effect of gate drive on overall performance and efficiency of converter becomes more critical since this can degrade power density of the converter [1].

Most of high frequency applications use silicon based devices such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In discrete and surface mount device implementation, MOSFET is commonly chosen because of its superior operation in high switching frequency. Nevertheless, there exists constraint and issues pertaining circuit development where comprehensive design and analyses have to be carried out.

2.3 Review of Gate Drive Techniques

Most of the time, the design of gate drive circuit has trade-offs between the level of voltage applied to the gate and level of switching frequency required for the switch. The other parameters include determination of dead time delay T_D, in the switching transition, duty ratio, D, resonant inductor, L_r, size of the transistor and isolation technique used to control the signal between input source and power MOSFET.

There are three basic types of driving sources in gate drive circuits. They are voltage driven and resonant topologies as shown in Figure 2.1(a, b) respectively [2]. First, in voltage driven topology, large energy will be dissipated and since there is no energy recovery, this topology is not suitable for high frequency operation. Power dissipation, P_v is given by Eq. (1).

$$P_v = f_s \times C_{iss} \times V_s^2 \tag{1}$$

where C_{iss} is the gate capacitance of power MOSFET and V_s is the input voltage source. From Figure 2.1(a), the maximum value of R_v given by Eq. (2) [2].

$$R_v = \frac{\Delta t}{1.6 \times f_s \times C_{iss}} \qquad (2)$$

where it is determined by required f_s whereas the minimum value, by C_{iss}. Δt is the time taken for C_{iss} to charge to maximum. Hence, there exists a maximum operating frequency which limits the charging capability of the gate [3]. Thus the voltage driven has limited capability in operating at high switching frequency.

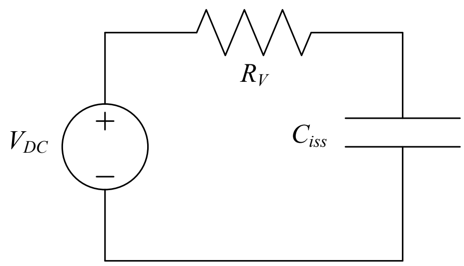

Figure 2.1(a) Voltage Driven

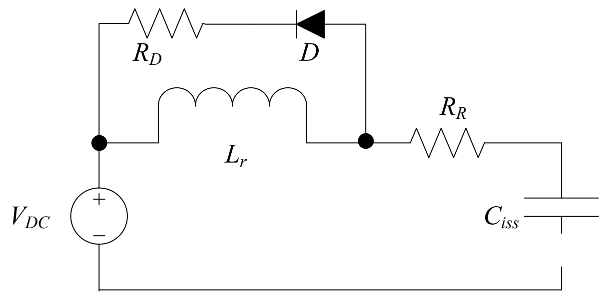

Figure 2.1(b) Resonant Driven

The resonant circuit shown in Figure 2.1(b) implies that all energy from resonant inductor L_r will be transferred to gate capacitance. As series resistance increases, only half of energy will be dissipated when the gate voltage reaches supply voltage. At this time, the resonant drive circuit operates in full resonance mode and this is comparable to voltage driven topology. Even though careful measures are taken to determine the suitability of topology, obviously there are tradeoffs between component counts, input voltage supply range, switching related losses and switching frequency.

2.3.1 Hard Switching Conventional Gate Drive Circuit

The conventional gate drive circuit was developed in 1970s. The issues related to the power dissipation loss and efficiency degradation had been discussed intensively by scholars especially in high frequency region. The circuit has limitations due to high switching frequency. As frequency increases, the driving loss is high causing high power dissipation in the external resistor R_G as indicated in Figure 2.2 (a). In hard switching, the dissipation of power loss in the switch is caused by rapid change in drain voltage and drain current which produce high stress in the switch. Even though switching loss can be reduced by minimizing these rapid changes in voltage and current, the effects of stray parameters such as inductance and capacitance in the circuit become obvious compared to low switching operation. Therefore, some energy is lost every time switches commutate [4].

The charging and discharging activities of input gate capacitance, C_{iss} of S_1 becomes very fast indicating longer turn-off transient. In addition, the discharging current in R_G becomes smaller which results in slower switching speed [5]. The conventional gate driver which consists of a resistor in the DC link has proven to have significant power losses [6]. Using PSpice circuit simulator, Figure 2.2(a) shows the conventional gate drive circuit driven by a totem-poled MOSFET configuration and its operating waveforms as indicated in Figure 2.2(b).

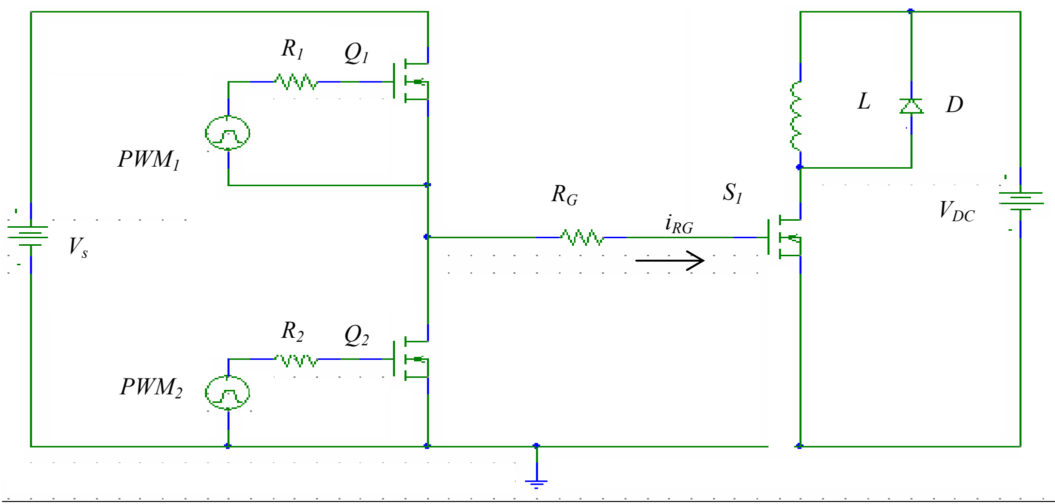

Figure 2.2(a) Hard Switching Conventional Gate Drive

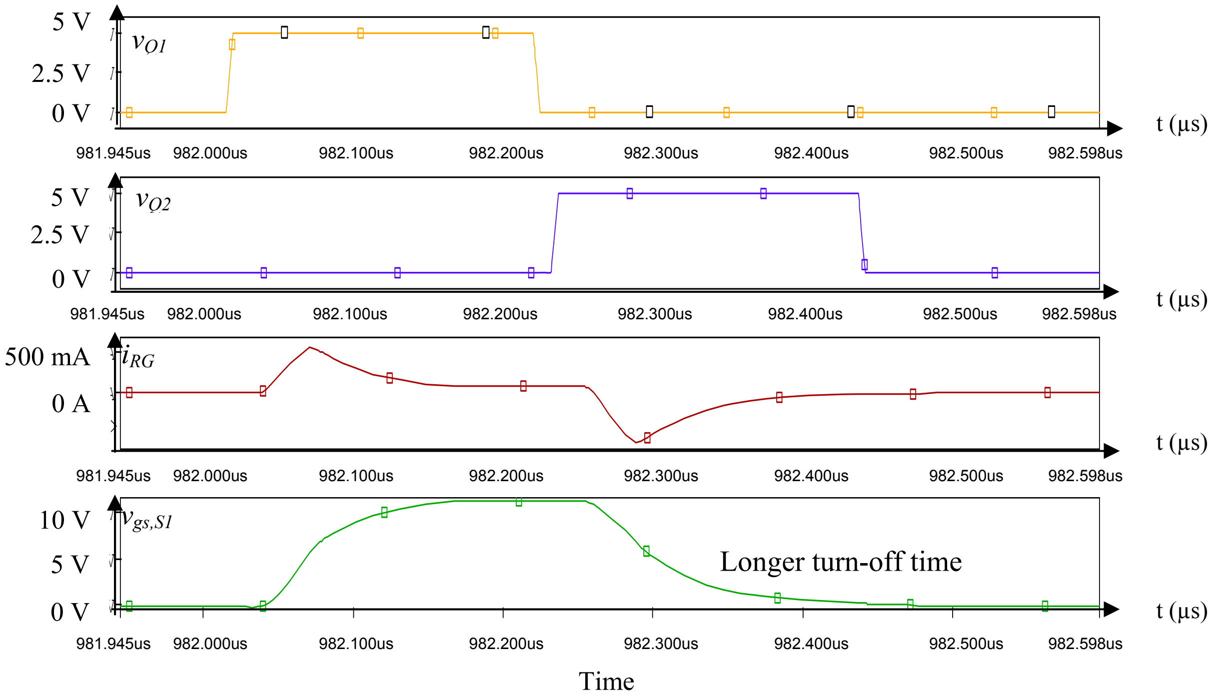

Figure 2.2(b) Conventional Gate Drive Waveforms

The two totem-poled driving MOSFETs Q_1 and Q_2 are used to drive signal to the power MOSFET, S_1 supplied by input V_s. Resistor, R_G is used as the RC-link for the pulses to flow. When PWM is applied, gate will draw current for a very short time to fully charge the gate of MOSFET. This draws the peak current to turn on gate with maximum voltage across it. During charging, the current will flow through R_G and $R_{ds(on),Q1}$ to charge C_{iss} of S_1 until gate level reaches V_s. During discharging of C_{iss}, the current is then drawn out from the gate through the reverse path until gate voltage reaches zero. Thus, double resistive power loss appears in the gate driver. The loss is much greater at a higher switching frequency.

Normally, the gate voltage takes a longer time to turn off as shown in Figure 2.2(b) than turn-on because it relies on resistive charging through gate and driver's resistance. This results in lower switching power loss during turn-on. The reason is that, the parasitic inductances provide a current snubbing effect which decreases the switching loss [7]. On the other hand, these inductances increase turn-off time by prolonging the recovery time. This can be observed when the load current is increased as the turn-off loss is proportional to i^2R [8]. In summary, some of the issues in conventional hard switching gate driver are listed below:

a) A longer turn-off time is not desirable to reduce switching loss as it is based on RC charge and discharge.

b) Higher / faster driving speed requires higher driving current that may increase loss.

c) Discharged current during switching transition becomes smaller than its peak. This will influence the charging and discharging of C_{iss} and hence the gate drive loss.

d) Charging and discharging of gate capacitance of the switch becomes fast causing malfunction of driver.

e) Induced turn-on dv/dt of the switch is dominant where it will not reduce with a shorter gate charging time.

f) Gate driving loss is high comparable to conduction loss at frequency higher than 200 kHz.

g) Cannot meet requirement of switching speed in high frequency application.

2.3.2 Switching Requirement and Losses in SRBC

In SRBC circuit operation, MOSFETs have to fulfill the system requirement in reducing loss and cost. The selection of MOSFET is based upon the following criteria:

a) Low power dissipation of switching device in megahertz range.

b) Figure of Merit of $R_{ds(on)}$ and gate charge.

c) Turn-on delay time ($t_{d(on)}$), rise time (t_{rise}), turn-off delay time ($t_{d(off)}$) and fall time (t_f) which have to be small for possible good switching performance.

On the other hand, the ideal switch in circle cannot satisfy the above criteria. When looking with the switching intervals during turn-on and off, it is obvious that significant differences compared to the MOSFET. Figure 2.3(a) shows the chopper circuit using ideal switch and its switching waveforms are indicated in Figure 2.3(b).

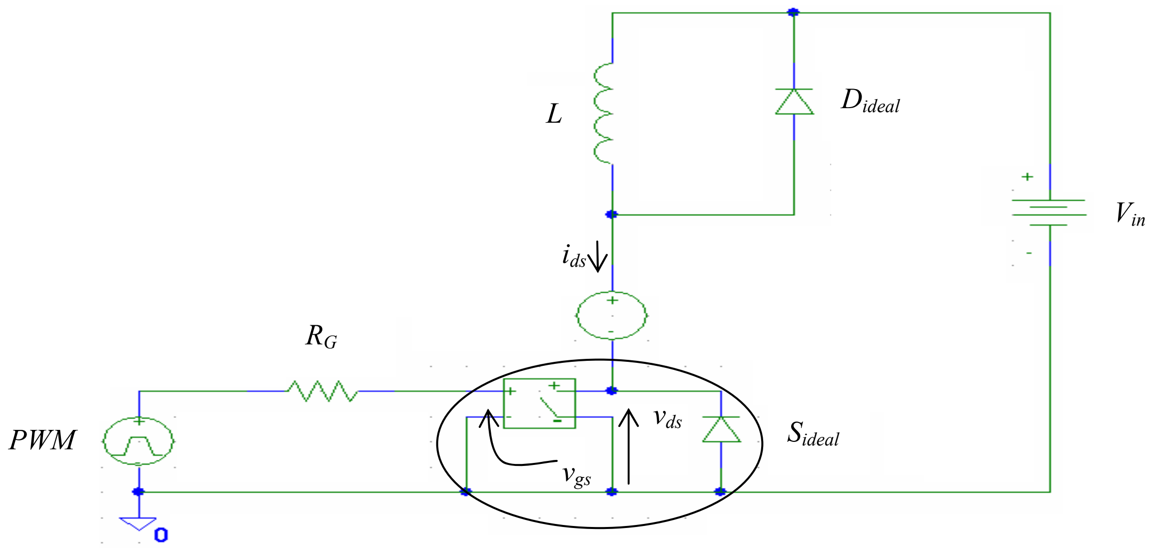

Figure 2.3(a) Ideal Switch in Chopper Circuit

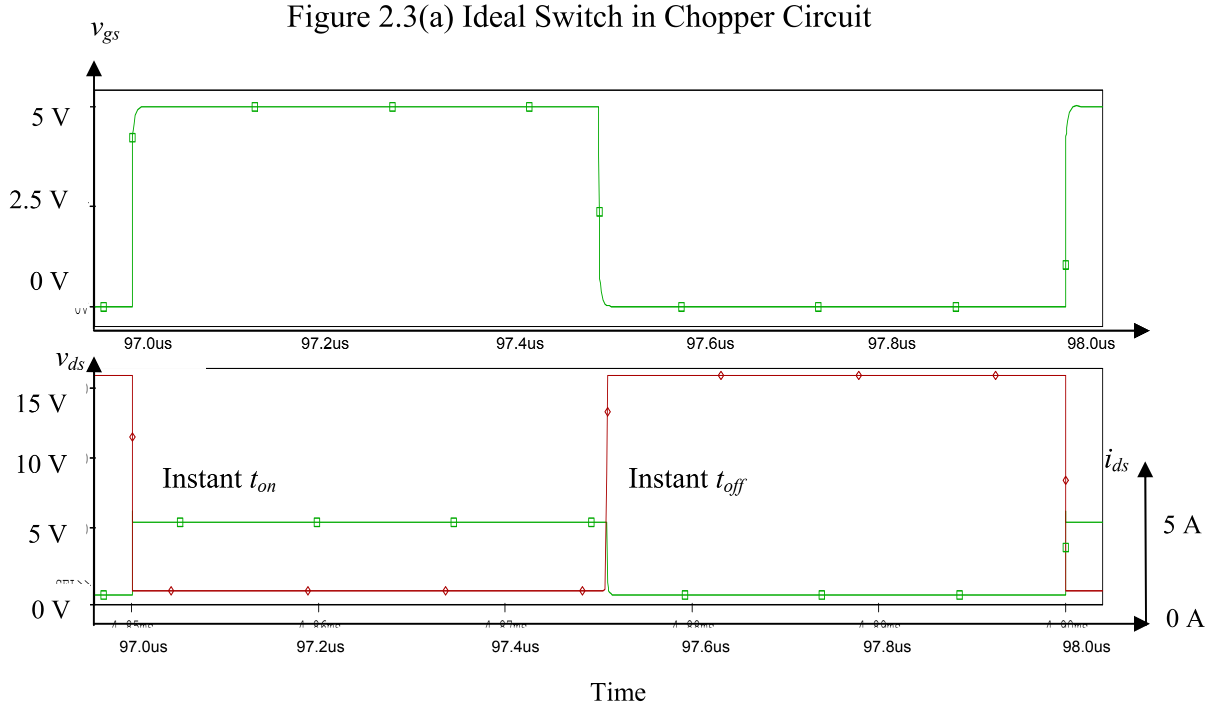

Figure 2.3(b) Turn-On and Off Characteristics of an Ideal Switch

Figure 2.3(b) clearly shows that there is no power loss (instant turn-on and off) during both switching transitions. This can be seen from the zero product of drain current and voltage of the ideal switch. Due to this, there are no turn-on and turn-off losses which are not realistic for real application. Even though the simulation result of Figure 2.3(a) successfully represents the suitability in high current and frequency, the actual operation will yet to require better switching device: the MOSFET.

2.3.2.1 Switching Characteristics of MOSFET

In MOSFET switching, the most important operational conditions are gate-source voltage (v_{gs}), drain-source voltage (v_{ds}) and drain current (i_{ds}). Figure 2.4(a) shows the inductive load test circuit for MOSFET and Figure 2.4(b) shows general switching characteristics of the MOSFET which explains the operation of turn-on and turn-off. The waveforms are generated using PSpice circuit simulator. The circuit is chosen because it is normally used for switching characterization and measurement.

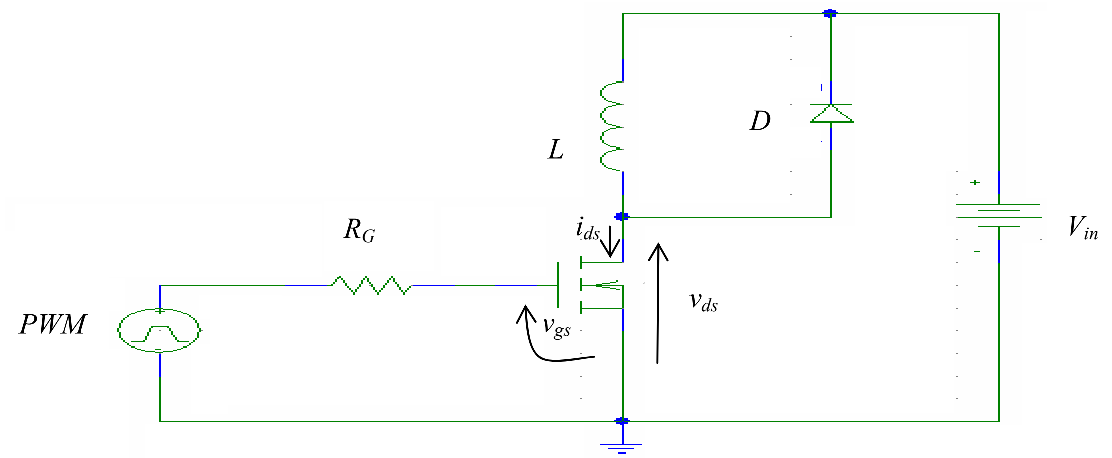

Figure 2.4(a) MOSFET in Chopper Circuit

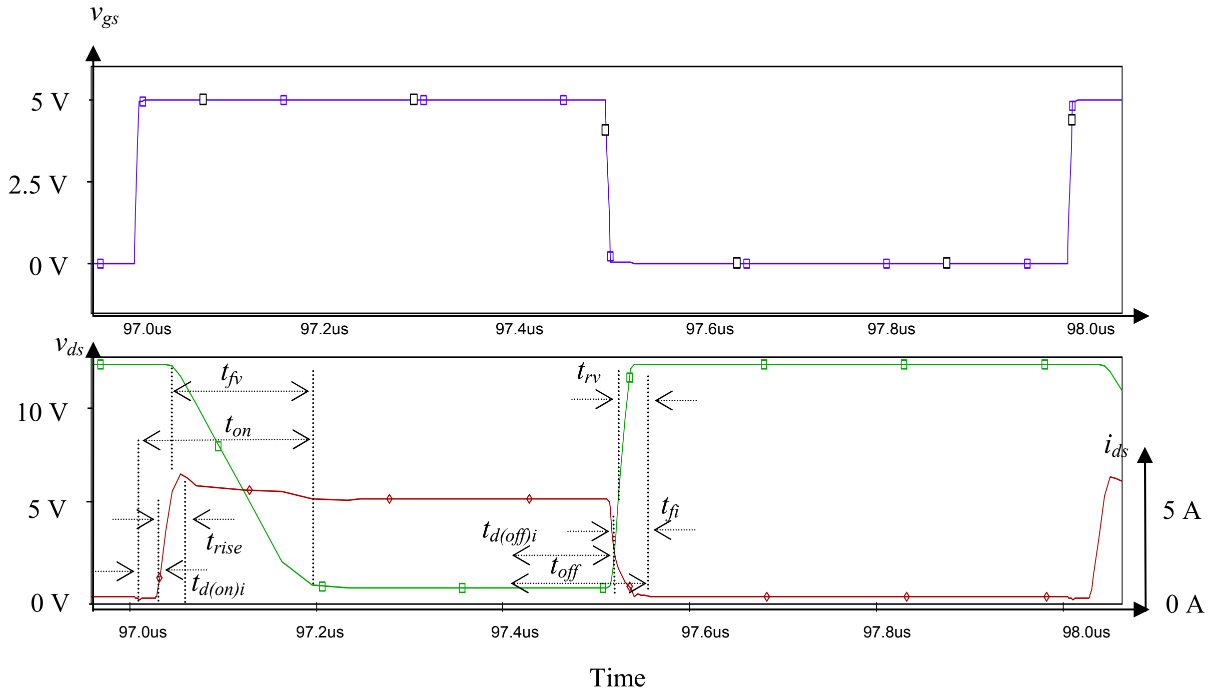

Figure 2.4(b) Turn-On and Off Characteristics of MOSFET

2.3.2.2 Turn-On and Off Characteristics

Turn-on time (t_{on}) and current turn-on delay time ($t_{d(on)i}$) indicate how fast MOSFET reacts during turn-on switching transient which gives total turn-on time. Increased delay time will eventually limit the maximum switching frequency. A longer turn-on delay can prolong the PWM signal received at the gate terminal of the MOSFET. In addition, the Miller effect [9] may affect the signal. It is a capacitive feedback where C_{gd} appears to be larger capacitance as seen from gate within small variation in V_{gs} value. Current rise time (t_{rise}) on the other hand contributes to how fast drain current reaches the load indicating the speed of the circuit. Other parameters such as voltage fall time (t_{fv}), di/dt of turn-on current, dv/dt turn-off voltage, current overshoot and turn-on energy loss (E_{on}) are included in the total turn-on duration.

The turn-off characteristics exhibit the same characteristics as the turn-on except for the behavior of voltage, current and their related switching times and losses which depend on turn-off duration. Among the parameters are turn-off time (t_{off}), current turn-off delay time ($t_{f(off)}$), current fall time (t_{fi}), voltage rise time (t_{rv}), di/dt of turn-off current, dv/dt of turn-on voltage, voltage overshoot and its respective turn-off energy loss as indicated in Figure 2.4(b). Since the switching loss in MOSFET is critical in high frequency operation, these turn-on and turn-off characteristics must be understood as they contribute to considerable switching losses in the MOSFET.

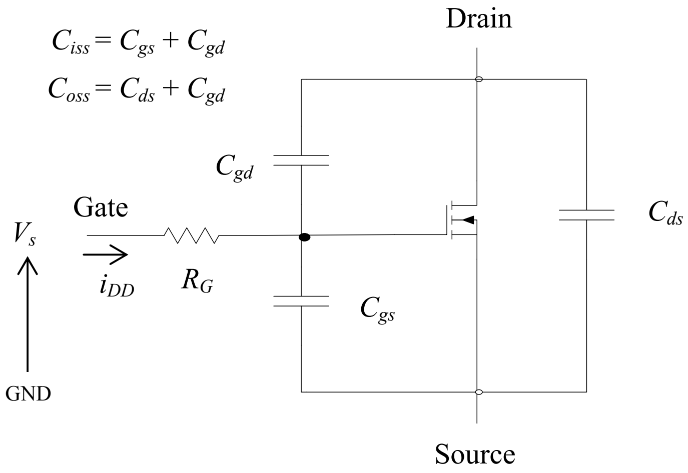

Figure 2.5 MOSFET Parasitic Capacitances

Figure 2.5 shows the parasitic capacitances of the power MOSFET. During switching cycle of the driving MOSFETs, the C_{iss} of S_1 will be charged by the energy from V_s and discharged to the ground leading to generation of pulses [10]. The total power supplied by the V_s is derived as

Cgd

$$P = \frac{1}{T_s} \times \int_0^{T_s} \left(V_s \times i_{DD}\right) dt = f_s \times V_S \times \int_0^{T_s} i_{DD}\, dt \tag{3}$$

where T_s is the switching period, f_s is he switching frequency of the circuit and i_{DD} is the instantaneous current flowing out from V_s into the circuit. The power MOSFET's v_{gs} of S_1 is charged by the same current i_{DD} from 0 to V_S and gate charge of S_1 from 0 to Q_G following the typical Q_G versus v_{gs} characteristic in the datasheet.

Gate
Vcc supply via 2
Rg
series auxiliary
switches at gate
Cgs

The equation is given by

$$Q_G(t) = \int_0^{T_s} i_{DD}\, dt \tag{4}$$

When combining Eq. (3) and Eq. (4), this gives the well known MOSFET gate driver loss equation given in Eq. (1).

In order to reduce this loss, RGD techniques have been introduced. For example, the techniques utilize LC resonance to charge and discharge the gate capacitance of main power MOSFET, S_1. The idea is to recover the energy stored in the gate capacitance, C_{iss} of main power MOSFET. From Figure 2.2(b), the switching power loss can be calculated using Eq. (1) and gate drive loss by replacing C_{iss} with C_{oss}. Since there are two driving MOSFETs of same type in the driver, the losses are approximately doubled.

From Figure 2.4(a), R_G limits the maximum gate current flow and allows root mean square (RMS) losses between R_G and internal drain-source on-resistance of power MOSFET, $R_{ds(on)}$. Reducing R_G brings no reduction in gate drive loss since it just shortens the charging and discharging times [11]. However, increasing effective gate resistance will reduce the switching speed.

On contrary, the impact of parasitic inductance is also important in the driver. For example, the parasitic common-source inductance creates a serious propagation effect during switching transitions and therefore increases switching loss, especially turn-off loss [12]. Consequently, the actual charged and discharged currents are much smaller resulting in higher switching loss [13, 14]. Thus, several methods have been introduced to solve the issues related to power dissipation and switching speed. Hence, the development of RGD circuit is pursued to help further improve the capability, reliability and performance of the driver.

2.4 Resonant Gate Drive Circuit

Generally, RGD circuit has evolved to overcome the issues when operating at high switching frequency. It is practically suitable to recover part or all of the energy stored in C_{iss} of S_1. The RGD circuit is designed only for specific applications and sometimes may not be suitable for others. If the application circuit uses only one switch, single-channel RGD can be applied. On the other hand, if the circuit has two switching devices, the applicable RGD circuits have to be designed to tailor the need for that circuit.

Until now, many studies have been conducted for the improvement of RGD circuits however they still require further development. The MOSFET's C_{iss} charges and discharges during the switching stage and thus significant energy losses are dissipated. Due to this, some of the dissipated energy must be recovered. Moreover, any RGD circuit which is incapable of fast cycle dynamics will not be suitable for high frequency applications. Below are the main requirements in designing a good RGD circuit:

a) Ability to have fast duty cycle dynamics.

b) Gate impedance of the switching device should be low after turning on and off to prevent false triggering.

c) Gate voltage must be well controlled after turning on and off.

d) Ability to have fast gate drive speed and at the same time produce low driving power losses.

In addition, there are also several other considerations to accommodate for high performance RGD, such as:

a) Propagation delay of input signal through switches' gate terminals.

b) Pulse width distortion of input gate signal.

c) PCB layout parasitic of power converter.

d) Device switching voltage swings and related EMI.

e) Determination of minimum pulse width for power MOSFET.

f) Protection features such as trip out and trip trigger input.

g) Drain voltage overdrive control to optimize efficiency.

h) Selection of gate capacitance value and Miller effect and start-up consideration

There are many RGD techniques have been introduced to solve technical issues in the design [1, 15, 16-20]. Unlike the conventional gate driver, only portion of energy in RGD circuit becomes thermal loss with the rest is stored in inductor [16]. Besides reducing the gate driving loss, some of the topologies suffer from at least one of the problems:

a) Suitable only for low-side (single-channel) and ground-referenced drives [1, 21-28].

b) Has bulky transformer or coupled inductance [1, 19, 22, 29-31].

c) Slower turn-on and/or off transition times leading to high conduction and switching losses [1, 21-23, 28-29].

d) Can only recover gate drive energy but limits total power savings.

e) Difficult to achieve high side driver [32].

f) Unable to effectively clamp the gate voltage of power MOSFET to driving voltage level during on-time and to ground during off-time which gives result in false triggering of gate conduction [1, 19, 21-23, 27-28].

Therefore, some designs such as ZCS-ZVS mixed-mode snubber, automatic energy recovery system, power efficient gate control, universal gate drive, hybrid gate drive, self-powered RGD, using leakage inductance of transformer and many more have been introduced. There are three important characteristics of RGD [10]:

a) Zero circulating current in order to minimize conduction loss in driver during turn-on of MOSFET.

b) Fast turn-on and off transition times to minimize conduction and switching losses in MOSFET.

c) Ability to clamp MOSFET gate to input voltage during turn-on and to ground during turn off in order to avoid false triggering and reduce induced dv/dt.

2.4.1 S-CRGD Circuit

As switching frequency increases, the S-CRGD circuit should be fast but also requires precise timing that corresponds to power delivery periods. In addition, good driver should have excellent loss saving properties. However, fast turn-on after C_{iss} is charged to V_s may block peak inductor current, $i_{Lr,peak}$ from flowing through reverse body diode of MOSFETs, which may result in higher power loss [33]. Any over voltage or under voltage of $v_{gs,Q1}$ and $v_{gs,Q2}$ is caused by voltage drop across parasitic reverse body diodes of the transistors. Figure 2.6(a) shows the conventional S-CRGD circuit. Unlike in Figure 2.2(a), the inductor, L_r is used as the link instead of resistor, R_G. The operating waveforms are shown in Figure 2.6(b).

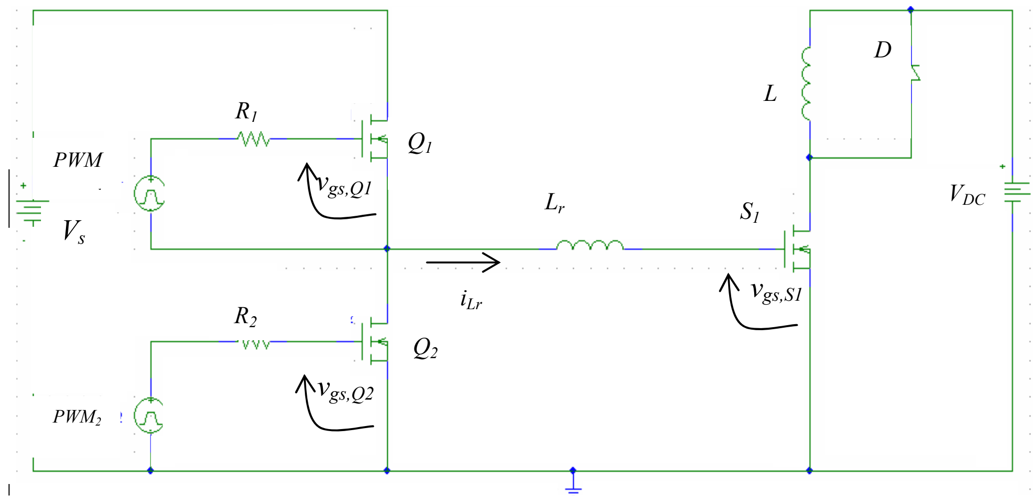

Figure 2.6(a) Conventional S-CRGD

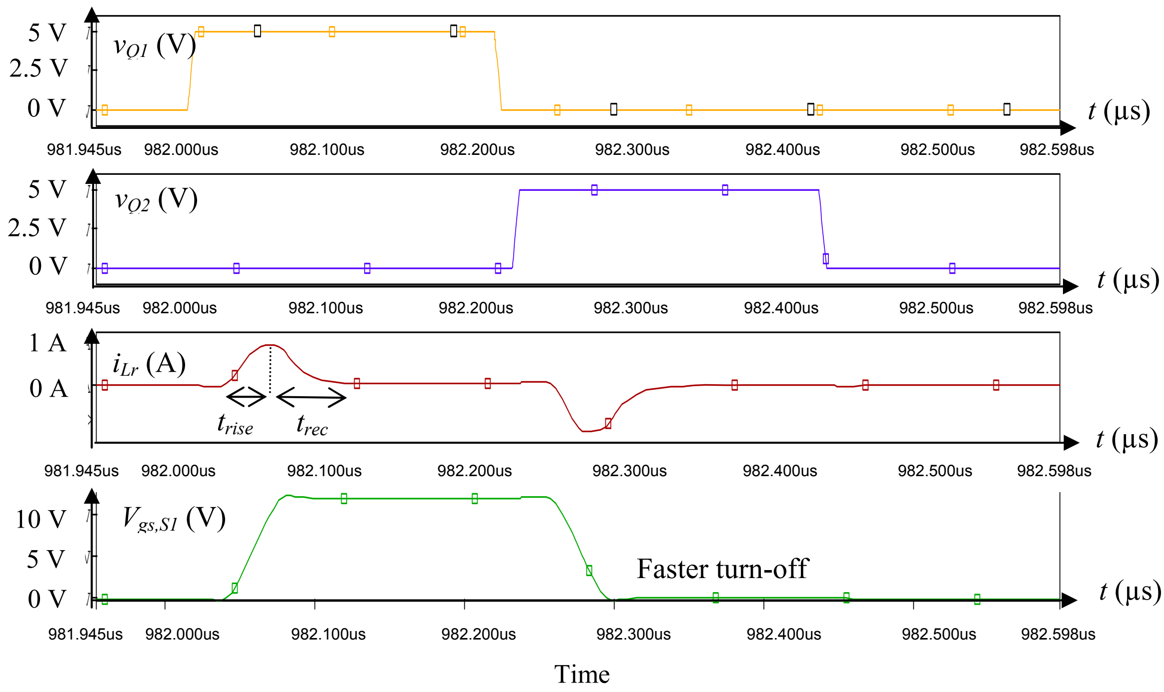

Figure 2.6(b) S-CRGD Waveforms

The operating condition of this circuit is similar to the conventional R_G gate driver, except the charging and discharging of gate capacitance of MOSFET is through inductor, L_r. One important remark is that Q_2 pulse width plays an important role in power energy savings in addition to the controlled Q_1 pulse. The turn-on speed depends on reverse recovery of body diode of the switch and for turn-off, it depends on gate drive circuit. A higher turn-off current may discharge C_{iss} of S_1 faster, providing shorter switching times and hence lower switching loss. On the other hand, oscillation during turn-off may reduce the turn-off speed due to higher di/dt and dv/dt of S_1.

2.4.2 Alternatives on S-CRGD Circuit Topologies

The S-CRGD circuit introduced in [34] is claimed to have full capability in recovering full energy with low dissipation. It has managed to recover some energy during both charging and discharging transitions. In addition, the circuit is independent on duty cycle of switch and hence driving frequency. Nevertheless, this S-CRGD circuit experiences an additional stress due to the additional switches used as auxiliary. Therefore, there are limitations in the parameter values which require optimization of duty cycle, D, dead time, T_D and L_r which are essential in achieving high frequency gate drive operation.

Another type of S-CRGD circuit uses the role of continuous inductor current in complete cycle to charge and discharge the gate of power MOSFET [16]. The resonant inductor is connected in series with an external capacitor. Here, the capacitor is used as a DC component of voltage across inductor. With the requirement of large capacitance value, this leads to the disadvantage on overall space limitation in circuit board despite of the advantages in operating independently with varying D and frequency. However, a constant circulating current during switching transitions results in higher power dissipation.

In designing a good S-CRGD circuit, the f_s and D have become the primary parameters. The switching speed of power device has to be as high as possible in order to reduce switching loss in power stage. However, the increase in switching speed will increase the power losses in RGD system. As a result, there must be an optimized switching speed that minimizes overall power losses especially in ZVS resonant network.

2.5 Resonant Switching

ZVS and ZCS are generated based on turn-on or turn-off, overvoltage snubber or even any combination of them. In high frequency operation, ZVS is preferred in high frequency power converter circuits because it can reduce the switching loss by maintaining low or zero voltage across the switch during switching transitions [35-36]. Fundamentally, it shapes the switch voltage waveform during the off time to create a zero-voltage condition for the switch to turn on [37]. This eventually leads to the benefits of reduction in EMI. Nevertheless, ZVS normally incurs losses that do not scale back with the output load, leading to difficulty in achieving light-load operation effectively. Having an improved ZVS design may solve this issue.

On the other hand, operating in ZCS can also minimize the switching loss. However, there is a greater concern in choosing this mode as it inhibits greater limitations in designing high frequency circuits. The upper limit of 2 MHz switching frequency is one of the limitations in ZCS mode [38] when operating off-line where slower transient response is reported especially in half-mode condition [39]. Even though full-mode operation can solve this limitation, it is difficult to implement at high frequency due to high body diode conduction loss experienced by the switch [40]. Thus, this leads to ZVS preference in high frequency converter design. In order to realize megahertz switching operation, the converter requires the following:

a) To have zero-voltage or zero-current in the switches at the instant of turn-on and turn-off, respectively.

b) To have diode's stored charge removed in the event of turn-off condition before next subsequent turn-on executes.

c) To ensure that the switching surge due to drain-source capacitance of the switch removed.

More importantly, the condition of ZVS is a function of duty ratio, *D*. In general, soft-switched DC-DC converters can have an advantage in lowering most of the related losses. However, drawbacks such as load dependent soft-switching range [41], complex control scheme [42] and high component stress make the design practically require accurate consideration.

Generally, there are two switching sub interval circuits of resonant transitions: one is during turn-on and the other during turn-off. The circuits are shown in Figure 2.7(a) and Figure 2.7(b) respectively. R_{eq} is the sum of all resistance in the path that includes resistance in wire and ESR of L_r and V_s is the voltage source. The initial inductor current and gate capacitor voltage are denoted as I_{Lr0} and V_{gs0}. In Figure 2.7(a), i_{Lr} (turn-on stage) can be expressed as Eq. (5) [19]:

$$i_{L_r}(t) = (I_{L_{r0}} - \frac{V_s}{R_{eq}})e^{-\frac{R_{eq}}{L_r}t} + \frac{V_s}{R_{eq}} \tag{5}$$

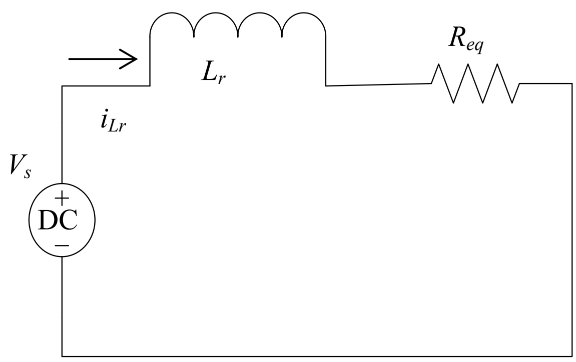

Figure 2.7(a) Resonant Switching Turn-On

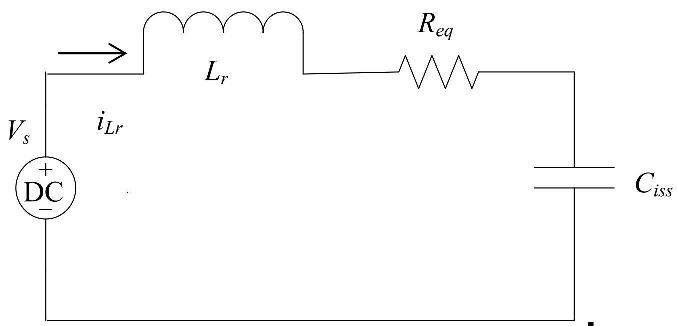

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Figure 2.7(b) Resonant Switching Turn-Off

Lr

DC Vs

By solving turn-off system in Figure 2.7(b), i_{Lr} and V_{gs} can be expressed as:

$$i_{L_r}(t) = \frac{V_s - V_{gs0} - 0.5R_{eq}I_{L_{r0}}}{\omega L_r} e^{-\alpha t}\sin(\omega t) + I_{L_{ro}} e^{-\alpha t}\cos(\omega t) \tag{6}$$

where $\alpha = \dfrac{R_{eq}}{2L_r}$, $\omega = \dfrac{\sqrt{4L_rC_{iss} - R_{eq}{}^2}}{2L_rC_{iss}}$

$$V_{gs}(t) = \frac{1}{C_{iss}}\int_0^t i_{Lr}(t)dt + V_{gs0} \tag{7}$$

Then the resistive power, $P_r(t)$ can be given as:

$$P_r(t) = \frac{R_{eq}}{T_s}\int_0^{T_s} i_{Lr}{}^2(t)dt \tag{8}$$

2.6 Q-Factor, Inductance and Performance of S-CRGD Circuit

Q-factor is a quality indicator which characterizes the rate of energy dissipation in resonant system. A high Q does not always represent better performance and high quality converter because it depends on the type of circuit topology used [43]. Generally, a high performance S-CRGD circuit should have a high value of Q so that more energy will be stored in the resonant components rather than being dissipated as power loss.

It can be determined from the resonant inductor value directly where size of inductor is important in high frequency operation. Here, the inductor value is proportional to Q-factor. In S-CRGD circuit [1], increasing inductance too high will increase switching loss. Therefore, the optimization between Q-factor and resonant inductance is required to ensure high performance of the gate driver.

The switching time in S-CRGD is determined from the value of L_r, t_{rise} and t_{fall} during the charging and discharging phases. This eventually determines the switching capability of the driver. From Figure 2.6(b), theoretically, the t_{rise} and t_{rec} will increase when L_r increases. For high switching application, t_{rise} should be small enough so that the power MOSFET can turn on faster.

The t_{rec} of the inductor current should not exceed the on-time of switching MOSFETs' Q_1 and Q_2. This is because, if t_{rec} is too long, the inductor current, i_{Lr} and $v_{gs,S1}$ will start to oscillate heavily and this is not favorable for the S-CRGD circuit. Besides, the relationship between the Q-factor and the switching response can be seen in the Q-factor Eq. (9) where it is proportional to L_r. This indicates that a higher L_r will eventually increase the t_{rise} and t_{rec} and hence reduce the switching speed as shown in Figure 2.6(b).

$$Q = \frac{1}{R_{eq}} \times \sqrt{\frac{L_r}{C_{iss}}} \tag{9}$$

$$P_{diss} = \frac{\pi}{2} \times \frac{V_s^2 \times R_{eq} \times C_{iss}^{\frac{3}{2}}}{\sqrt{L_r}} \tag{10}$$

A high value of Q-factor is required to improve the performance of S-CRGD in terms of power losses. It can be derived from a higher L_r but it will add to the board layout size and consequently, reduce the ability of S-CRGD to operate in high frequency switching application. From Eq. (10), a lower L_r will increase the power dissipation. It indicates that there will be a tradeoff in selecting this value. The selections for maximum value of inductor and the driving time of MOSFET have to be determined [12]. Usually 1-5 % of overall switching period time is taken for driving and by taking 5 % as the maximum value of driving time, an inequality of maximum value of inductor is given by Eq. (11).

$$L_{r,\max} \leq \frac{1}{C_{iss}} \times \left(\frac{5\%}{\pi \times f_s} \right)^2 \tag{11}$$

2.7 Summary of S-CRGD Topology Characteristics

Most of S-CRGD designs are at best for a single MOSFET but for dual MOSFETs, circuit complexity and cost constraint [44-46] are becoming the issues. For example, in D-CRGD developed by K. Yao et al. [19], issues of floating gate remain open during off and on states leading to massive noise generation. Complete understanding of S-CRGD circuit is required prior to designing a D-CRGD. Some issues and advantages of S-CRGDs are presented in Table 2.1.

Table 2.1 Summary of S-CRGD

Description of Gate Driver (GD)	**Magnetic Used for Resonance**	**Issues**	**Advantages**
Conventional GD [Lopez et al., 2003]: Gate capacitance is charged through push-pull totem-poled circuit	None. It is a RC configuration	GD loss is independent on load current so efficiency is affected in light load conditions	Simple and can easily be embedded in IC, offering high power density
Voltage clamped S-CRGD [Jacobson, 1993]	Coupled inductors	- Using leakage inductance may result in manufacturing variation - Cannot use a standard push-pull driver configuration	Fast turn-on can be achieved
Linear turn-off current S-CRGD [Strydom, 2004]	Large inductor	- Poor transient response - High switching loss due to constant circulating current - Large capacitor required	- Simple with less component count - Using push-pull driver
S-CRGD using gate capacitance as main energy storage [De Vries, 2002]	Small inductor	- Increases turn-on time due to large bi-directional voltage swing at MOSFET gate - Switching loss is high in driving switches - $R_{ds(on)}$ dependent	- Simple in circuit construction - Energy in gate capacitance is effectively recycled
Complete energy recovery S-CRGD [Chen et al., 2004]	Small inductor	- Inductor current depends on switch's conduction time	- Fast turn-on to allow for low driver's conduction loss

One of the examples of D-CRGD circuit is shown in Figure 2.8. The center-tapped transformer is used to boost the switch gate voltage as high as input source value. By controlling the timing of both MOSFETs, each of them can be turned on right after the other is turned off. Here, the charging and discharging of C_{iss} is by constant current source which may speed up the switching transition especially during turn-off. Ultimately, both S_1 and S_2 switches can turn on and turn off in complementary mode [47].

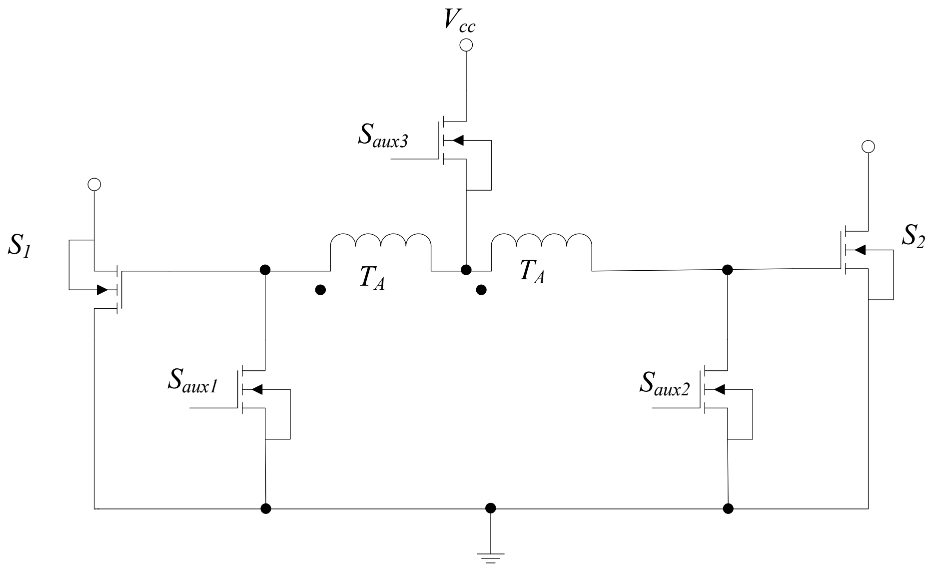

Figure 2.8 Center-Tapped D-CRGD [47]

Nevertheless, this D-CRGD does not have much of power saving property due to core loss of transformer. So, there are many other D-CRGD circuits proposed which have better driving capability to drive two MOSFETs in one switching cycle. However, there are lots of drawbacks in ensuring that S_1 and S_2 can properly conduct without incurring cross conduction. One of the solutions is by integrating the soft switching technique with gate drive control scheme for power loss reduction within low T_D.

2.8 Synchronous Rectifier Buck Converter (SRBC) Power Stage Circuit

In most low-voltage power module, switching power losses are dominant in the converter in addition to body diode conduction loss produced by two switches in SRBC, namely control switch and synchronous switch. Therefore, the switching waveforms for these switches must be operating in ZVS and the ideal finite on-state drain-voltage of S_2 has to be close to zero in ensuring minimum losses throughout the switching interval.

In SRBC circuit, a high current may be required to turn off control switch with low switching loss. Besides, incorrect choice of drain-source on-resistance ($R_{ds(on)}$) of the device will impose a constraint on the converter's performance. Even though resonant topology is employed, the turn-off issue remains unsolved. In contrast, synchronous switch needs a lower current in order to switch the device rapidly leading to difficulty in clamping the gate voltages. In addition, an independent bias supply can be allowed to optimally drive the switches using a simple voltage feed. This may help reduce the effect of stray capacitance in the converter which eventually lowers the switching loss. More importantly, issues related to dead time will greatly result in lower efficiency and affect the performance of the converter.

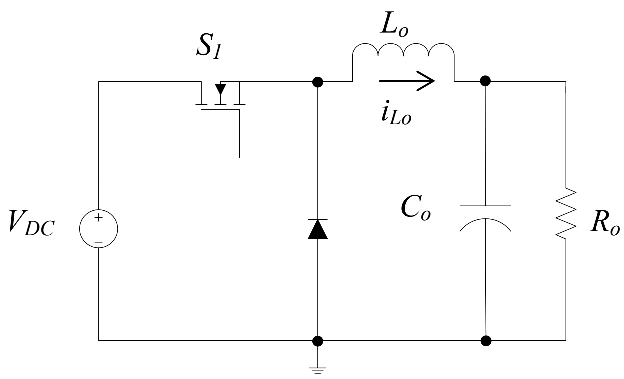

Figure 2.9 Buck Converter

A buck converter is shown in Figure 2.9. In this circuit, the freewheeling diode turns on shortly after the switch turns off which results in a voltage rise across the diode. Since the diode only conducts during S_1 turn-off, during continuous conduction mode (CCM), some energy will dissipate which gives power dissipation, P_d in diode given by Eq. (12). At this time, the diode will experience reverse recovery and it is related to voltage drop, V_d as defined by Eq. (13). D_{S1} is the duty ratio of S_1 switch and C_{diode} is capacitance of the diode during its reverse bias in CCM.

$$P_{d(on)} = \frac{1}{2} \times C_{diode} \times V_{DC}{}^2 \times f_s \tag{12}$$

$$P_{d(on)} = V_d \times (1 - D_{S1}) \times I_{Lo} \tag{13}$$

Figure 2.10 shows the SRBC as a modified version of the buck converter circuit topology where the diode is replaced with a second switch, S_2. This modification is a tradeoff between the increased cost and improved efficiency.

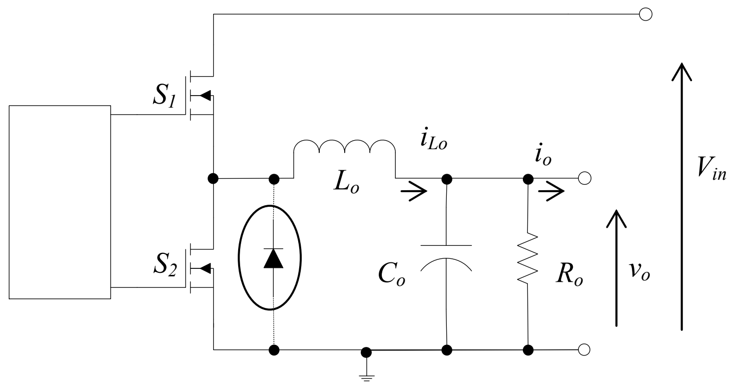

Figure 2.10 Conventional SRBC Circuit

In this circuit, a control switch, S_1 and synchronous switch, S_2 are conducting in complementary manner. Here, the charging and discharging of inductor current, i_{Lo} will produce output voltage based on duty cycle set by S_1. Replacing the diode (in circle) with switch S_2, may lower conduction loss, reduce the voltage spike of gate voltage of S_2 and improve the performance of converter.

Some of the advantages when utilizing S_2 are as follows [48]:

a) Allows bidirectional power flow.

b) Efficiency can be increased because on-state drain voltage drop of S_2 is less than forward voltage of the diode in buck converter.

However, using S_2 may also introduce some drawbacks such as:

a) Both S_1 and S_2 could accidently conduct if cross conduction occurs.

b) Higher losses are present in S_1 and S_2 and also in L_o.

c) May cause additional ripple overshoot in drain voltage of S_2.

d) Will introduce an induced dv/dt switching, which may degrade the performance of SRBC [49].

e) Feedback control circuit is complex

The power loss in S_2 is strongly dependent on the duty ratio, D and therefore proportional to its on-time. When power is transferred in the "reverse" direction, it acts much like a boost converter instead. Nevertheless, the advantage of this converter does not come without cost. Firstly, S_2 typically costs more than the freewheeling diode in buck converter circuit. Secondly, the complexity of the converter is vastly increased due to the need for a complementary-output switch driver. Other losses such as reverse recovery and body diode conduction losses during T_D also reduce the performance of the SRBC.

Moreover, when S_2 is used, it may degrade the efficiency of the converter at light load by disallowing i_{Lo} from entering the discontinuous conduction mode (DCM) and maintaining operation in CCM. This is due to the MOSFET bidirectional flow of i_{Lo}. In order to block any negative i_{Lo}, a good gate drive control scheme must be able to detect the current through the MOSFET and then switch it off when it is zero. Hence, this enables the SRBC to operate in DCM operation at light load and thus reduce the switching loss.

Generally, the faster S_1 turns on and off, the lower switching losses become.

However, as S_1 turns on faster, this will cause S_2 to experience high dv/dt induced turn-on. An induced dv/dt turn-on is the situation where S_2 can momentarily conduct even though gate drive signal instructs it to turn off. It is caused by a fast changing voltage of $v_{ds,S2}$. When S_1 conducts, full input voltage of V_{in} will not immediately appear at $v_{ds,S2}$. This is due to Miller's effect and turn-on delay at S_1. Then, $v_{ds,S2}$ induces a current to generate a voltage drop across internal gate resistance of S_2. If this induced gate voltage is bigger than $V_{th,S2}$, S_2 will be turned on while S_1 is still conducting. Thus, S_1 will have to carry load and shoot through current while S_2 conducts excessively with high power loss.

2.8.1 Switching of SRBC Circuit

There are two PWM pulses applied to the circuit as shown in Figure 2.11. The v_{gs1} pulse is used to drive S_1 whereas the complemented v_{gs2} pulse to drive S_2. It is crucial that both MOSFETs do not turn on at the same time [50]. A sufficient delay is added to avoid resultant peak rise of current significantly above $V_{th,S2}$, turning on both S_1 and S_2 switches accidentally [51]. Ideally, the pulses must be complementing each other without any T_D delay, but practically it has to be provided.

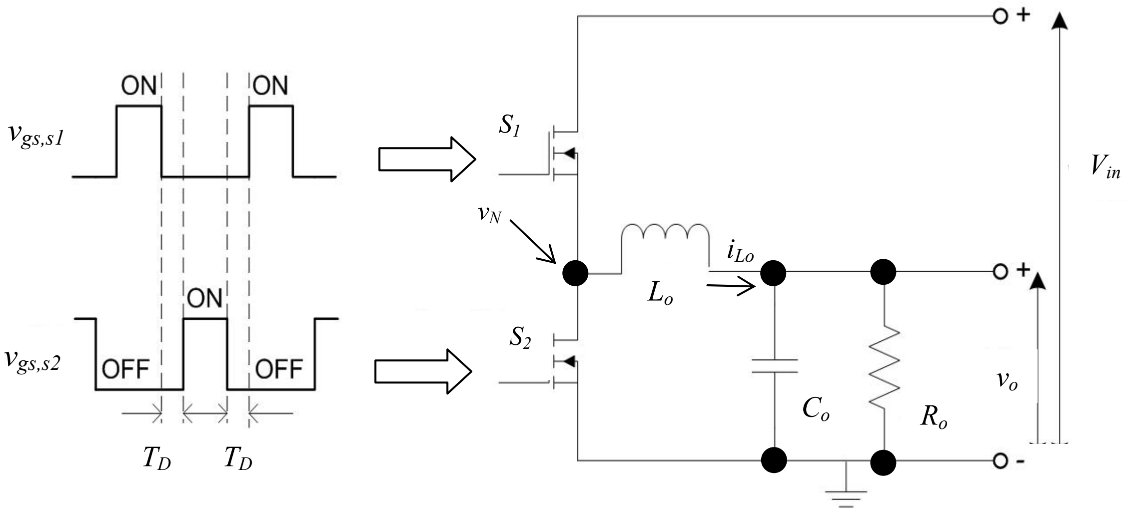

Figure 2.11 Switching in SRBC

When S_1 turns on, the drain voltage of S_2 increases, producing a fast change in voltage, dv within a very short time, dt. This dv/dt induced voltage results in an instantaneous current flow through C_{iss} of S_2. Consequently, possible shoot through is expected. So, higher V_{th} and low $R_{ds(on)}$ of MOSFET must be used to allow S_1 to carry high load current at low duty ratio.

The gate driver must also be able to slow down the rising edge of S_1 pulse and reduce the induced turn-on dv/dt. However, the switching power loss eventually will increase dramatically [52]. When S_1 is turned off, i_{Lo} continues to flow through either S_2 or its body diode. The details on S_1 and S_2 switching of SRBC are comprehensively explained in [53].

2.8.2 Dead Time and Cross Conduction

A T_D can be described as the duration where neither one of the switches is turned on as shown in Figure 2.12. The application of T_D has advantages and disadvantages depending on its applied duration. The T_D is one of the important parameters in designing gate driver since it relates to the total losses. Too long of T_D will introduce losses due to body diode conduction [54]. In fact, it may also add a subinterval of negative voltage to node switch which tends to reduce average of drain voltage of S_2 switch [55].

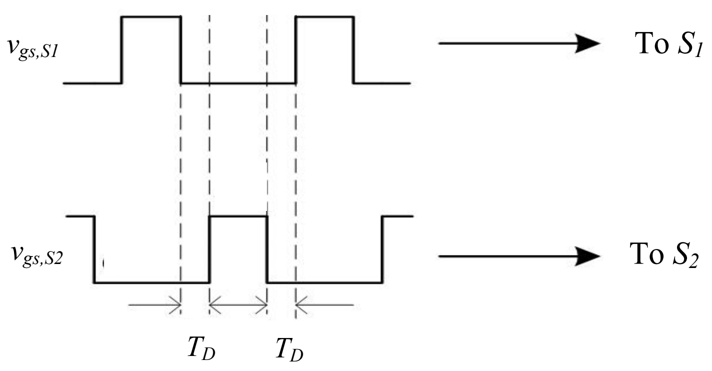

Figure 2.12 Application of T_D on Driving Pulses

Figure 2.13 shows the cross conduction waveform. It occurs when both MOSFETs are either fully or partially turned on where this provides a path for current to “shoot through” from supplied voltage to ground. An induced v_{gs} may occur resulting from this phenomenon. According to A. Elbanhawy [56], the cross conduction will lead to excessive power dissipation in both MOSFETs since the current will short the power supply to the ground through them and can damage one or both switches practically. In addition, having too short of T_D will cause a part of positive portion of node voltage, v_N is lost due to overlapping between two gate drive signals.

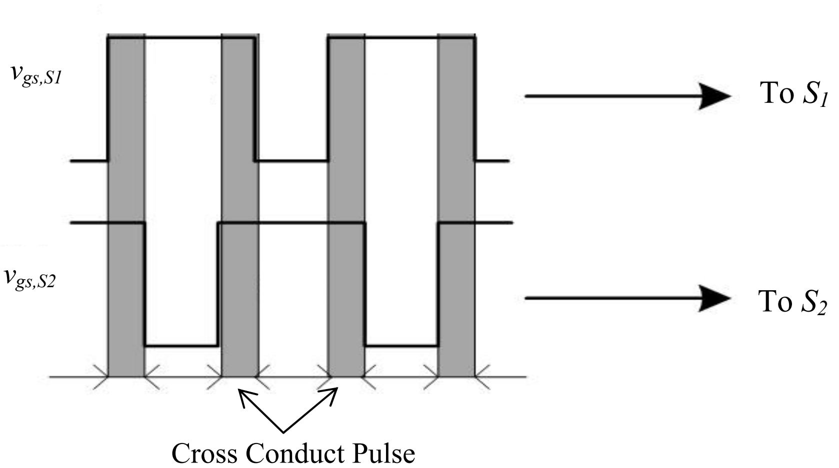

Figure 2.13 Cross Conduction Waveform

2.8.3 S_2 Body Diode Conduction

When S_1 and S_2 are off, parasitic body diode of S_2 is forward biased due to the continuity of i_{Lo}, and thus producing an undershoot of approximately - 0.7 V at v_N [51]. This whole negative duration indicates the duration of body diode conduction. Theoretically, S_2 body diode is turned on with ZVS by a circulating current that flows into L_o as soon as S_1 is turned off. However, S_2 can concurrently conduct with its body diode, creating stored charge that must be removed before S_2 can support voltage.

This leads to high switching loss in S_1 and an increase in reverse recovery loss in

S_2 body diode. So, S_2 needs to be turned off completely before S_1 starts to conduct during T_D. After T_D delay ends, S_2 will start to conduct. Since the forward voltage drop across S_2 is much lower than its body diode voltage drop, this will allow i_{Lo} to flow through S_2 instead [58]. Figure 2.14 shows the body diode conduction of S_2.

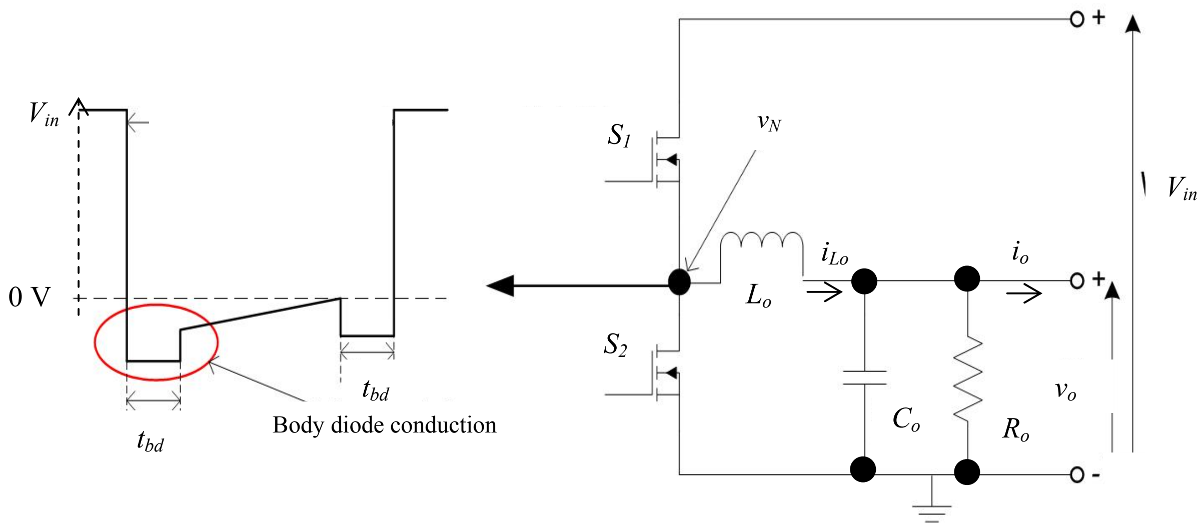

Figure 2.14 Body Diode Conduction of S_2

The body diode conduction time, t_{bd} is circled in Figure 2.14. The period of the body diode conduction is related to T_D. The longer T_D is, the longer t_{bd} will be. Allowing the i_{Lo} to flow through the body diode of S_2 switch has a degrading effect on the overall efficiency since it contributes to the losses. Note that the t_{bd} increases with T_D and so does the body diode conduction loss [59-60]. This shows that as T_D value increases, the power losses will increase thus affect the performance of the circuit. The body diode conduction loss is given by Eq. (14),

$$P_{bd} = 2 \times V_F \times I_o \times f_s \times t_{bd} \tag{14}$$

where V_F = body diode forward voltage drop and t_{bd} = body diode conduction time.

Thus, in order to have a low body diode loss, a shorter T_D delay is required. In high frequency low output voltage power stage, the additional loss due to body diode conduction can be as high as 6 % of the overall loss [51].

2.8.4 MOSFET's Switching and Conduction Losses

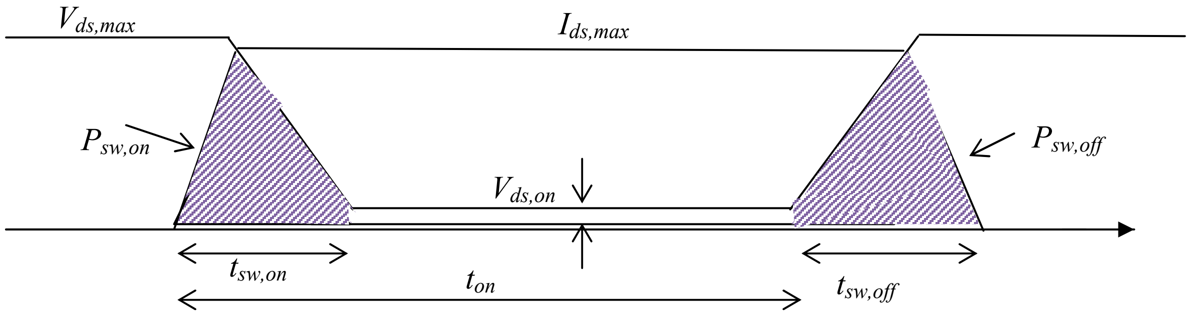

Figure 2.15 MOSFET Switching Power Dissipation

It is seen from Figure 2.15 that there is overlap between voltage across and current through the switch during the turn-on and off switching transitions. The product of these two waveforms gives the instantaneous power dissipation given by Eq. (15)

$$P(t) = V_{ds}(t) \times I_{ds}(t) \tag{15}$$

where V_{ds}= drain-to-source voltage and I_{ds} = drain-to-source current.

This instantaneous power dissipation occurs during switching transition and occurs twice per cycle. The switching loss can be calculated by using the fundamental formulas given in Eq. (16) and Eq. (17).

$$P_{sw,on} = \frac{1}{2} \times I_{ds,\max} \times V_{ds,\max} \times t_{sw,on} \times f_s \tag{16}$$

$$P_{sw,off} = \frac{1}{2} \times I_{ds,\max} \times V_{ds,\max} \times t_{sw,off} \times f_s \tag{17}$$

Therefore, the switching loss is proportional to the f_s, t_{on} and t_{off} times [61]. In addition, it is important to note that since there exists a non-zero $V_{ds,on}$ value, then the total switching loss is much more higher. Therefore, the total on-time switching loss can be modeled as Eq. (18).

$$P_{sw,on\_total} = [V_{ds,\max}(\frac{I_{ds} \times t_{sw,on}}{2}) + V_{ds,on}\{(t_{on} - t_{sw,on}) \times I_{ds}\}] \times f_s \tag{18}$$

In addition, equations Eq. (19) and Eq. (20) also show that during CCM, the conduction losses of S_1 and S_2 depend on their $R_{ds(on)}$ and duty ratio where the I_{RMS} is the current of MOSFET. Note that the equations assume rectangular waveforms for current and without dead time.

$$P_{COND,S_1} = (I_{ds1,\max})^2 \times R_{ds(on)S_1} \times D_{Sw1} \tag{19}$$

$$P_{COND,S_2} = (I_{ds2,\max})^2 \times R_{ds(on)S_2} \times D_{Sw2} \tag{20}$$

Looking at the equations, the conduction loss can be reduced by minimizing $R_{ds(on)}$ by selecting better MOSFET for both S_1 and S_2 [62].

2.8.5 Gate and Reverse Recovery Losses of Driving MOSFET in SRBC

Among other losses are gate drive losses, which contribute to dissipative driving losses of Q switch and its body diode loss, defined in Eq. (21) [63]. The gate drive losses are dissipated in the gate resistor and the driver.

$$P_{gate,Q_1} = Q_{oss,Q_1} \times V_{gs,Q_1} \times f_s \tag{21}$$

$$P_{RR} = \frac{1}{2} \times Q_{RR} \times V_{ds} \times f_s \tag{22}$$

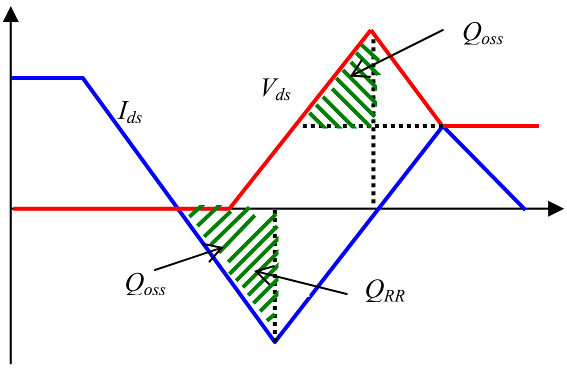

Figure 2.16 MOSFET Turn-off Model [64]

The output charge, Q_{oss} and reverse recovery charge Q_{RR} produce losses during turn-off. They are shown in Figure 2.16 as the shaded triangular areas [64]. In addition, during T_D, there also exists the reverse recovery current loss in diode which is given in Eq. (22) and this adds to total power loss in SRBC circuit as given in Eq. (23):

$$P_{total} = P_{sw} + P_{COND} + P_{gate} + P_{bd} + P_{RR..} \tag{23}$$

2.9 Ideal Operating Waveforms of SRBC

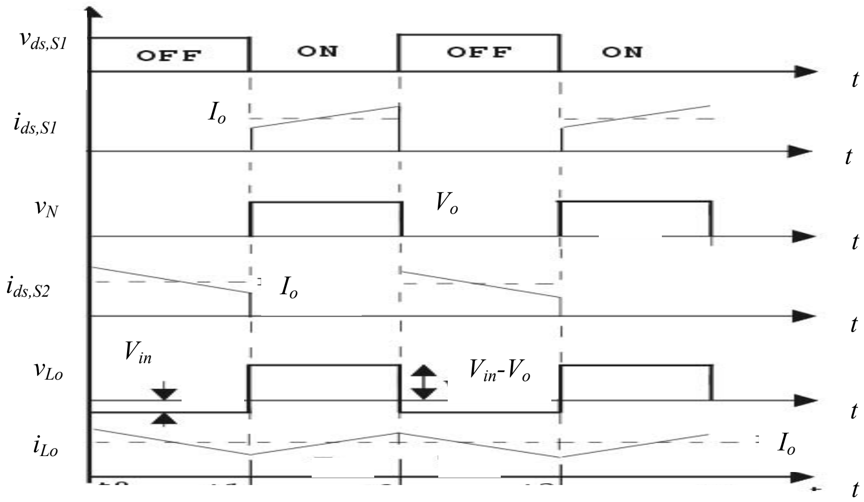

Figure 2.17 Zero Delay SRBC Waveforms [64]

Figure 2.17 shows the ideal operating waveforms for SRBC circuit. Depending on the applicable L_o value, the load current operates in CCM mode where heavy load current is expected to drive the output. Ideally, there will be no cross conduction. The drain current of S_1 and S_2 are conducting during turn-on of S_1 and S_2 respectively. Clearly by referring to the node switch, V_N waveform in Figure 2.17, there is no negative region indicating zero body diode conduction. Details in calculating the parameter values are described in details in [64]. By using the operation of CCM as reference, the design of SRBC in DCM (at boundary) can be formulated.

In order to design a converter, the switching frequency, f_s influences the efficiency of the system. At higher switching frequency, more power will be dissipated in the SRBC. Output capacitor, C_o is used to reduce the voltage ripple at the load. The charge of the capacitor used also depends on load current ripple and the switching frequency. The C_o must be large in order to sustain output voltage level. Using high level of equivalent series resistance (ESR) of electrolytic capacitor will result in large transient spike. On the other hand, ceramic capacitor has low ESR but limited capability to store energy for supplying energy to the load.

The function of the inductor is to limit the current through the load when the switch is conducting. One advantage in using inductor is that it can control the percentage of ripple. Smaller L_o can help increase faster transient response and high power density [65]. In addition, it can determine the circuit operation either in CCM or DCM. With a smaller L_o, the gate drive speed improves as this will increase transient time [21] but with the cost of high power loss.

Peak current will increase and this eventually adds to the RMS loss of the gate driver. The possible solution may suggest having shorter t_{rise} and t_{rec} of current and optimized L_o value given by Eq. (24) [1]. Nevertheless, this L_o is subject to manufacturing variation.

$$L_{o,opt} < \frac{1}{C_{iss}} \times \left(\frac{2 \times t_{rise,\max}}{\pi}\right)^2 \tag{24}$$

A higher L_o produces larger voltage swing at the load. In addition, this will lead to the reduction of switching time due to smaller gate voltage value, increase in t_{rise} and

t_{rec} and also switching loss. A low DCR value can be used to solve these issues. Even though, large L_o will reduce ripple, it limits the energy transfer speed. A small value can produce a faster slew rate. So, this is one of the reasons why L_o has to be selected properly.

2.9.1 Soft-Switching Technique in SRBC

The voltage mode soft-switching circuits have been widely used in recent years in DC-DC converter applications. This is due to the significant advantage in lowering conduction losses. Figure 2.18 shows an example of a ZVS auxiliary circuit block.

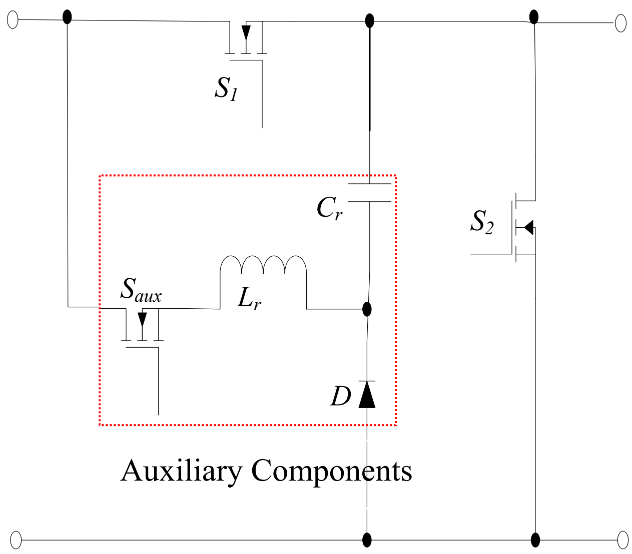

Figure 2.18 ZVS-SRBC Auxiliary Components

It is seen from Figure 2.18 that the switches S_1 and S_2 are supplied by independent PWM signals. As opposed to center-tapped D-CRGD shown in Figure 2.8, the additional components are not used to drive the gates. They are mainly the auxiliary parts which are used to achieve soft-switching operation. The circuit in Figure 2.18

employs a resonant network in parallel to S_1. The purpose is to generate ZVS for S_1 and ZCS for auxiliary switch, S_{aux} without increasing the switches' voltage and current stresses. A complete operation and advantages of this circuit is explained by A.K. Panda et al. [66].

The auxiliary components having lower rating values are commonly added to the existing circuit. Normally, they only operate partially within one complete cycle of switching frequency. This will add to the improvement in efficiency of the converter. However, modifications are still required in the circuit block to further solve issues in high switching related loss in ZVS-SRBC converters. Reducing switching losses in main switches in SRBC has not been given a great concern and being left unsolved in most literatures. Table 2.2 tabulates some of the issues.

Table 2.2 Issues of Auxiliary Circuits in SRBC

	Descriptions	**Issues / Drawbacks**
[Wang, 2006], [Chuang et al, 2008], [Lin et al, 2008]	Auxiliary switch is turned off while current stays on.	Produces switching losses and harmonics.
[Yang et al., 1993], [Filho et al., 1994], [Moschopoulos et al., 1995], [Tseng et al., 1998]	Auxiliary circuit causes high peak current stress in main circuit.	Requires higher current rated switch Increases conduction loss
[Huang et al., 2006]	Auxiliary circuit is able to reduce current stress	Circuit is complex

2.9.2 Selection of Operating Resonance Condition

When considering the soft-switching technique, the choice for LC combination in the SRBC gives significant impact to the performance of the converter. The difference in resonant and switching frequency results in variation of operating conditions, which include below resonance, at resonance and above resonance.

When varying the switching frequency to be greater, smaller or equal to the resonant frequency, the switching current waveform and resonant inductor current change due to the changes in impedance of the resonant tank [76-77].

Resonant frequency (f_r) exists in the resonant converter whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period [78]. Resonance occurs when the inductive reactance (X_L) and capacitive reactance (X_C) are equal in absolute values and the two impedances cancel each other out having the total impedance drops to zero. Resonant frequency formula can be represented as in Eq. (25).

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{25}$$

where L_r is the resonant inductive value and C_r is the resonant capacitive value.

By changing the resonant tank impedance, the output is therefore changed. For $f_s > f_r$, the resonant tank impedance is large thus small I_{Lr} value is produced causing the converter to work in ZVS mode. For $f_s < f_r$, the resonant tank impedance value is small causing the I_{Lr} to be large. While for $f_s = f_r$, the resonant is unity where the resonant tank impedance is zero and I_{Lr} at its maximum value [79]. This eventually may affect the performance of the converter. The resonant tank impedance formula can be represented by Eq. (26).

$$Z = \sqrt{(X_L - X_C)^2} \tag{26}$$

where $X_L = 2\pi f_s L$ and $X_C = \frac{1}{2\pi f_s C}$. The summary of each condition, its requirement and implication for series resonant LC configuration in SRBC is listed in Table 2.3 [79].

Table 2.3 Summary of Resonant Operation in DC/DC Converter

Below resonance	At resonance	Above resonance
• Requires lossy RC snubber, fast recovery diodes, di/dt limiting inductors • Power control is based on correct transformer and filtering circuit design • Converter operates in ZCS • High FET turn-on and off switching losses	• Not easy to achieve ZVS. • Suitable mostly for LLC converter.	• When drive current lags its voltage, S_1 and S_2 can transition with no voltage across them • ZVS is easily achieved • Ability to regulate against input voltage variation • Allows operation at high frequency without significant loss of converter efficiency • Ability to regulate output voltage down to zero load without turning off the resonance

2.10 Gate Drive Control Scheme for SRBC

Many gate driver control schemes for DC-DC converters have been introduced since 1990s. They include digital and also analog controls. In 1997, pulse based T_D compensator (PBDTC) was introduced [80] where the switching times were modified to compensate T_D so that v_o can be properly controlled in magnitude. In addition, it can adjust symmetric PWM pulses to correct voltage distortion. This replicates the fixed delay implementation. Some other literatures have discussed different methods in details and can be referred to [81-82].

Several analog techniques have been introduced to ensure "break before make" operation. They are the Fixed Dead Time (FDT), Adaptive Gate Drive (AGD) and Predictive Gate Drive (PGD). Each of them has its own characteristics, advantages and drawbacks which provide information for the suitability and cost effective gate driver design.

In order to obtain a higher efficiency with minimum switching loss, a gate drive control method needs to be implemented in new SRBC circuit. The control scheme provides the T_D between the state transitions of switches S_1 and S_2 to avoid cross conduction. A proper setting of T_D can decrease total power loss in switching converter without overloading and having instability issues. In order to avoid shoot through current, many drivers work with fixed T_D. Since this control scheme produces a lengthy T_D, it would easily generate high dissipation and hence reduce efficiency of the circuit. However, with accurate PWM settings, these results have shown otherwise.

The AGD control scheme is another way which can be applied where it holds a dynamic compensation of T_D and avoid short circuit of both MOSFETs. At the same time this will keep T_D value small enough to reduce body diode conduction losses [83]. A predictive control is claimed to be best in solving this problem where it uses predictive concept to predict and reduce T_D on the switching cycle of gate driver. Here, the problem related to T_D could be minimized.

2.10.1 Fixed Dead Time

FDT is the first operational mode used for synchronous rectifier converter circuit. The advantage of this technique is that it has a simple control circuit with lower voltage stress [84-85]. However, this scheme requires the T_D to be provided long enough to prevent cross conduction. A lengthy T_D would reduce the converter efficiency by allowing the body diode to conduct.

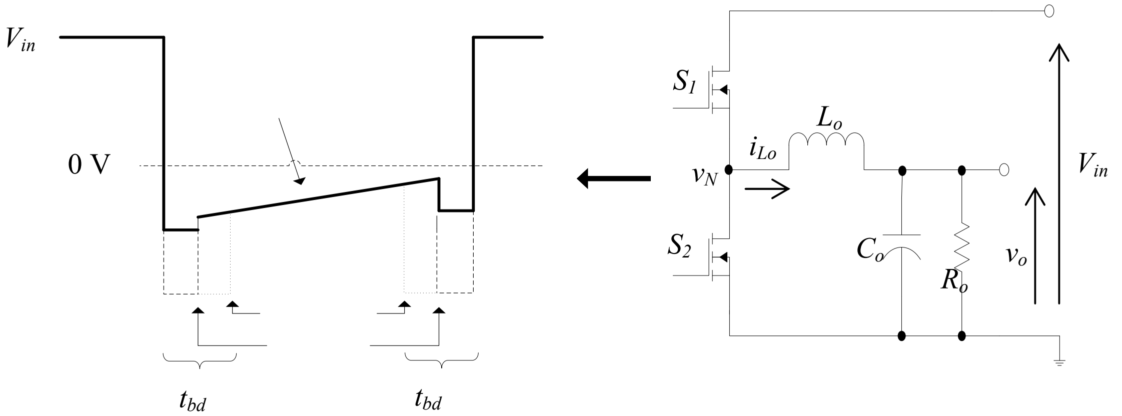

Figure 2.19 SRBC Switch Node Voltage

Channel Conduction

t (µs)

0 V

Figure 2.19 shows typical switch-node voltage waveform of SRBC. It shows the relative effects of FDT and AGD control schemes on t_{bd}. Theoretically, FDT scheme produces a longer t_{bd} and eventually reduces the channel conduction time. However, a precise timing control could solve this issue. During t_{bd}, the inductor current, i_{Lo} will flow from ground through the body diode of switch S_2 and L_o resulting the voltage drop across body diode which leads to the reduction in the efficiency of power conversion [83].

Switch

Vol

Fixed Delay

Adaptive Delay

t_{BD} t_{BD}

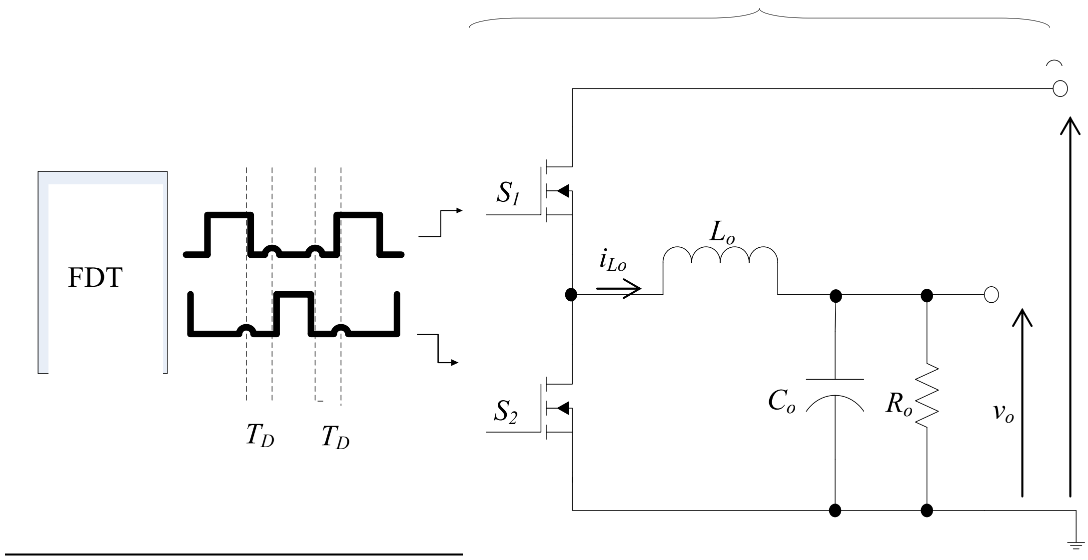

Figure 2.20 Fixed Dead Time SRBC Gate Drive

Figure 2.20 shows the block diagram of FDT control circuit integrated with SRBC circuit. The input signals produced by the drive circuit provide T_D to S_1 and S_2. In addition, the efficiency of FDT technique also varies with different type of MOSFETs' junction temperature and with lot-to-lot variation of the T_D delay during manufacturing [60].

2.10.2 Adaptive Gate Drive

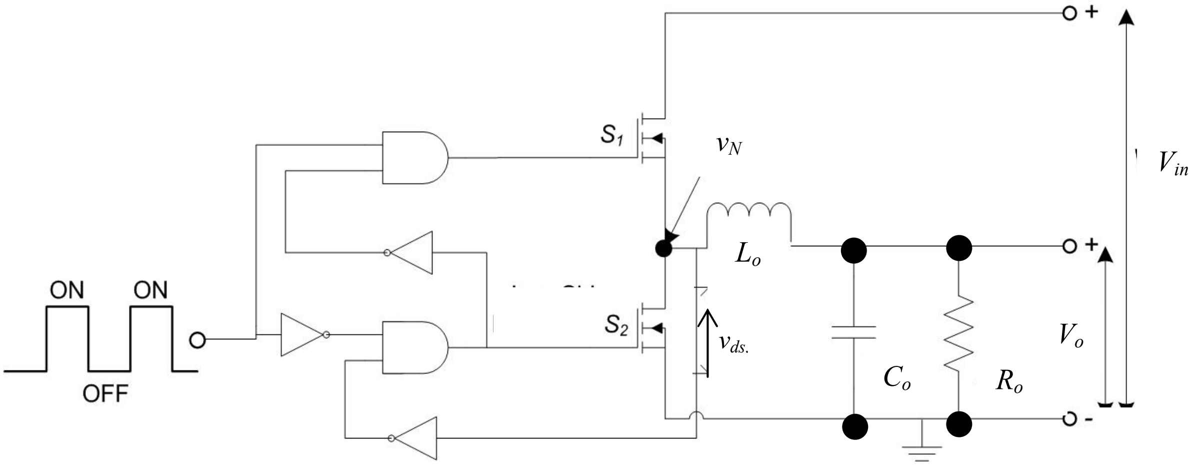

Figure 2.21 Adaptive Delay SRBC Gate Drive [93]

Figure 2.21 shows the Adaptive Gate Delay (AGD) control scheme. This second generation gate drive control scheme was introduced to overcome the limitation in the FDT. It uses a control loop that includes a digital delay line where it senses the drain to source voltage, v_{ds} of the S_2 and adjusts the digital delay line according to the amount of delay that should be applied to turn on S_2. Consequently, S_2 is turned on only when the v_N equals to zero [86].

The advantage of using this control scheme is that the adjustment of the delay can be made adaptively according to the type of MOSFET used. However, there is a disadvantage that comes from this control scheme. The variation of body diode conduction time interval is not easy to predict. This is due to the logic components used as the feedback circuit. Each of the components has its own propagation delay which may indirectly increase the T_D between the pulses.

2.10.3 Predictive Gate Delay

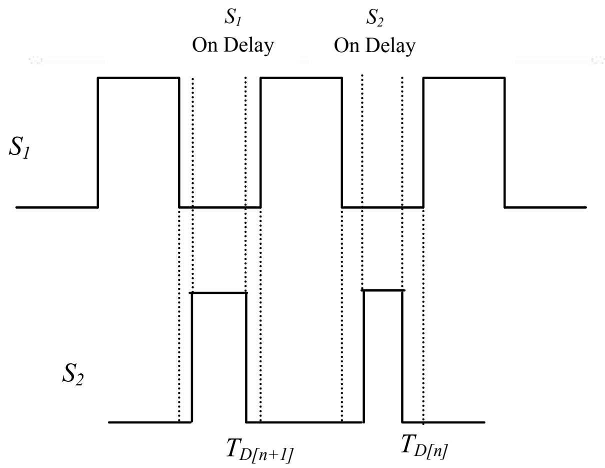

Figure 2.22 Predictive Control Timing

Since both FDT and AGD schemes have limitations, the PGD scheme was then introduced. It is a combination of a predictive circuit integrated with PWM where it has the ability to vary the T_D from time to time according to the feedback signal. The predictive time is shown in Figure 2.22. Here, the next T_D, $T_{D[n+1]}$ can be predicted and minimized based on the feedback.

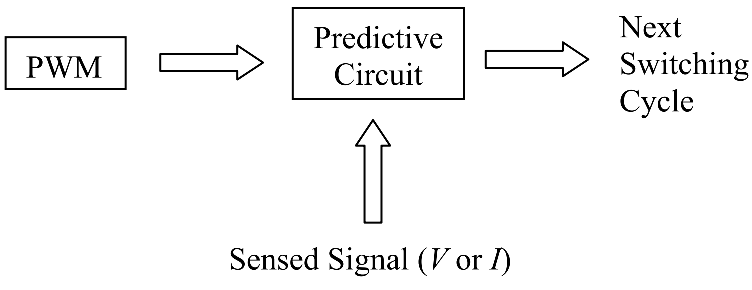

Figure 2.23 PGD Control Block Diagram

PGD uses feedback loop as shown in Figure 2.23 in order to reduce the T_D until it reaches near zero [87]. The predictive circuit will sense a signal from the node voltage of SRBC Circuit.

Table 2.4 Advantages and Disadvantages of Gate Drive Control Schemes

Fixed Dead Time	**Adaptive Gate Drive**	**Predictive Gate Drive**
- constant, pre-set delays for turn-off to turn-on intervals - simple in design - efficiency varies with MOSFET types and ambient temperature - Need to make delay long enough to cover entire application.	- variable delays based on volatage sensed on current switching cycle - uses state information from power stage to control turn-on of two gate drivers and set T_D - increases body diode conduction time caused by delay in cross coupling loops - unable to compensate for delay to charge MOSFET gate to threshold level - difficult to determine whether S_2 is off	- uses information from current switching cycle to adjust delays to be used in next cycle - can prevent body diode from being forward biased and hence cross conduction - increases power savings when MOSFET is turned on - minimizes reverse recovery loss in S_1 body diode. - tight layout regulation requirement

Table 2.4 shows the summary of all three gate drive control schemes for SRBC circuits. Even though FDT is not flexible, it has the simplest configuration and easy to drive the SRBC. The only issue is that a longer T_D has to be provided. However, this is not true since simulation results shown otherwise, the details of which are presented in Results and Discussion. The data in the table gives the advantages and disadvantages of different control schemes so that the choice of the design can easily be made based on cost, component count and simplicity.

2.11 Load Variation on SRBC

In any load conditions, switch S_1 will experience switching loss whereas reverse recovery loss is in S_2 body diode. However, these losses can be minimized by allowing i_{Lo} to operate in DCM. A high output inductance, L_o value can be used so that i_{Lo} flow will allow S_1 body diode to turn on prior to S_1 during T_D [88]. This ensures that the current is mostly DC. On the other hand, in CCM, switch S_1 will experience hard switching since i_{Lo} never touches zero. This is in contrast to the operation of S_2 where in CCM, current can easily reverse and reduce the body diode recovery loss. As the converter load current varies, contribution of power dissipation will vary as well. During T_D interval, different inductor currents give different operational waveforms [89] as shown in Figure 2.24.

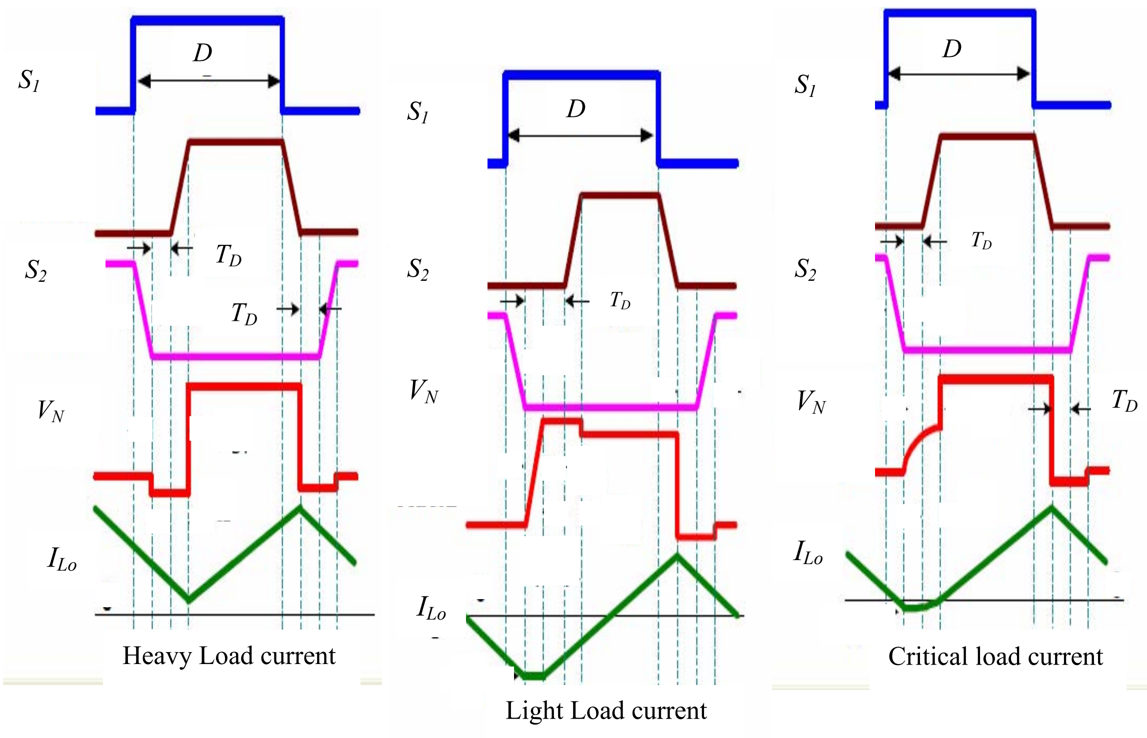

Figure 2.24 SRBC Load Effects [89]

2.11.1 Continuous Conduction Mode

From Figure 2.24, when switch S_2 is turned off, the i_{Lo} is positive indicating CCM operation. In SRBC circuit, the switch node, V_N is clamped to the ground by body diode of S_1. The S_1 switch starts to turn on after T_D. V_N level will rapidly increase from the ground to the input voltage. Here, switching loss of S_1 dominates power dissipation and it can cause considerable voltage drop in rectifying stage where current can reverse in S_2.

Due to constant turn-on time during PWM rising edge, the V_N for heavy load condition is given by Eq. (27) [89]:

$$V_{N,heavy} = \frac{(t_{D,S_1} - t_{on})}{t_{sw}} \times V_{in} \tag{27}$$

2.11.2 Discontinuous Conduction Mode

PWM converter can suffer from lower conversion efficiencies during light loads [90]. Here, the conduction loss is insignificant as the switching loss is very high [90, 91]. In order to reduce the switching loss, S_1 has to operate in ZVS. A high i_{Lo} ripple must be allowed so that it can have negative polarity.

In this condition, the negative i_{Lo} will start to charge C_{ds} of S_2 to the input voltage. In DCM, the negative polarity i_{Lo} can turn on the body diode of S_1 before the switch itself. The delay time of switch node is much shorter than the heavy load current condition. Consequently, switching power loss in S_1 can be reduced and moreover S_1 can effectively operate in ZVS condition [88]. However, gate drive loss is dominant under this load condition [92].

Assuming i_{Lo} is constant during T_D, the node voltage is given by Eq. (28) [89].

$$V_{N,light} = D \times V_{in} + \frac{C_{ds,s_2} 2V_{in}^{2}}{2 \times t_{on} \times (i_{Lo,avg} + \{\frac{(V_{in} - V_o) \times D \times t_{on}}{2 \times L_o}\})} \tag{28}$$

2.12 Improving SRBC Weaknesses

The SRBC may require improvement in the gate drive capability in driving both switches and the reduction in power dissipation in the converter. The gate drive circuit must be able to synchronize the switching without incurring too much of body diode conduction loss. In addition, the switches in SRBC should operate in ZVS mode with minimal turn-off drain voltage. This will in turn minimize the entire switching loss during each cycle. The detail of methodology is described in Chapter 3.

2.13 Chapter Summary

There are lots of reviews discussing about the advantages and issues in the design of gate driver for better SRBC circuit. In addition, from the requirement of high frequency application, the loss reduction aspects have been debated for the intention to increase the level of converter's performance. Several types of gate drive control schemes have contributed to various views in terms of choice, effectiveness and simplicity in the design. All information gathered will be used as guidelines in the development of chronological methodology for this project.

CHAPTER 3

METHODOLOGY

3.1 Chapter Overview

The simulation and experimental analyses are carried out for both S-CRGD and new SRBC circuits. However, the other investigations concentrating on the Q-factor of S-CRGD, switching frequency, effects on variation in load, effects on T_D and also comparison of gate drive control schemes of new SRBC are done through simulation only. Methodology is explained in details with all relevant reasoning. Figure 3.1 shows the summary of methodology involved in this work.

S-CRGD [1]

Parameter Limitations Study
→ Simulation
→ Experiment

Expectations:
a) Optimized L_r, T_D and D
b) Switching Loss in Q_1 and Q_2
c) Loss Analysis
d) Gate Drive Loss

Simulation Work Only (Chp. 5)

S-CRGD [1]

Q-Factor Analysis

Expectations:
Finding optimized Q-factor & L_r

⇒

D-CRGD

Using optimized parameters from S-CRGD + New SRBC Circuit

→ Simulation → Experiment

Expectations:
a) Floating turn-off v_{ds} of S_1 and S_2
b) Switching Loss
c) Efficiency
d) Steady-State Analysis
e) Modes of Operation

Simulation Work Only (Chp. 5)

New SRBC Circuit

Dead Time Effects
Frequency Variations
Loading Effects
Study on Gate Drive Control

Expectations:
Which one is the best solution for high frequency gate drive and suitable for SRBC? What are the limitations and drawbacks?

Figure 3.1 Summary of Methodology

3.2 Parameter Limitations on S-CRGD Circuit

The first step in this research work is to determine the optimized parameters in the S-CRGD circuit. The idea of better S-CRGD circuit for SRBC is to achieve precise timings of PWM signals for S_1 and S_2 MOSFETs. Based upon the S-CRGD circuit, the design must look into a tradeoff between switching and gate drive loss in order to produce better switching operation of S_1 and S_2.

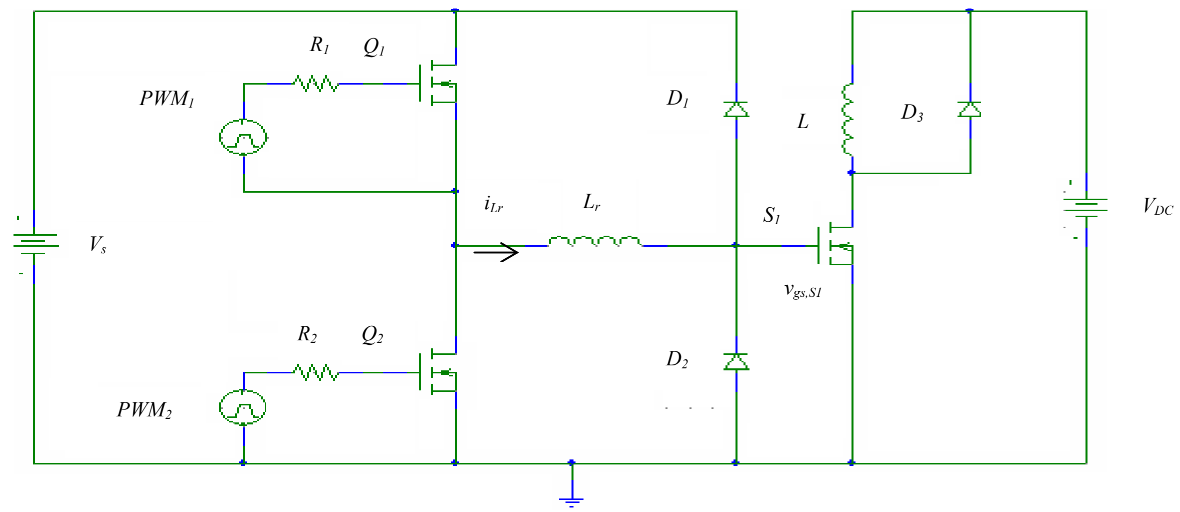

Figure 3.2 S-CRGD

In this work, a S-CRGD circuit is used as shown in Figure 3.2. Due to the fact that this S-CRGD uses a small inductor, produces faster turn-on speed and low body diode conduction loss, it has been chosen as the basis in the design methodology for the development of a dual-channel topology. Simplicity and full energy recovery are the main reasons why this type of S-CRGD circuit is referred to this work. By using push-pull type configuration and clamped diodes, the circuit is able to generate better switching response at the gate of S_1.

3.2.1 Power Stage Simulation Setup

PSpice simulator is used to study the behavior of voltage and current in the inductor and the power MOSFET's C_{iss}. There are three important parameters which will influence the operating waveforms of S-CRGD circuit: D, T_D and L_r. The significant impact of not using optimized parameter values have not been explained extensively. The S-CRGD circuit as shown in Figure 3.2 is utilized to investigate the effects of these parameters with respect to driver's switching losses using simulation. The details of each limitation are explained and the parameters used in the simulation are given in Table 3.1.

Table 3.1 Simulation Parameters of S-CRGD for f_s = 1 MHz

Components	**Parameter Settings in PSpice Simulator and Components' Ratings**
PWM_1	V_1 = 0 V, V_2 = 5 V, $t_r = t_f$ = 5 ns, PW = 200 ns, PER = 1000 ìs, t_d = 0 ns
PWM_2	V_1 = 0 V, V_2 = 5 V, $t_r = t_f$ = 5 ns, PW = 200 ns, PER = 1000 ìs, t_d = 232 ns
Q_1, Q_2	PSMN130-200D/PLP, 200 V / 20 A, $R_{ds(on)}$ = 0.130 Ω
D_1, D_2, D_3	1N6392, 45 V / 60 A
S_1	IRFP250, 200 V / 33 A, $R_{ds(on)}$ = 0.085 Ω
L_r	9 nH
V_s	12 V
V_{DC}	48 V

The D determines the length of conduction time of power MOSFET, S_1 and it must provide sufficient on-time for i_{Lr} to completely charge and discharge. Otherwise, this eventually results in oscillation during turn-off and hence generates power loss.

On the other hand, by varying T_D, the consequences may both add to further switching loss and speed reduction. This in turn necessitates optimizing D, T_D and L_r in the tradeoff between size of L_r, switching loss and speed of the driver circuit.

3.2.1.1 Effects of Duty Ratio

In 1 MHz switching frequency, pulse width duration of 200 ns is chosen as a benchmark in the design, resulting in a duty ratio of 0.20 because from this, the inductor value can be determined. The reason is to evaluate the impact of charging and discharging of inductor current during the conduction of Q_1 and Q_2. From here, the gate charging response of S_1 is observed so that the oscillation count and hence switching loss can be calculated. The significance impact of D in S-CRGD circuit is based on the following factors:

a) Relationship between the duration of charging / discharging time with respect to D.
b) Consequence of i_L for shorter and longer duration of applied D.
c) Power dissipation in S-CRGD.
d) The selection of diode for current recovery time.

3.2.1.2 Effects of Dead Time

Two separate PWM settings (PWM_1 and PWM_2) are given in PSpice simulator in accordance to Table 3.1. The generated signals will produce two sets of sequential pulses with different time delay. Consequently, in between them, there will be a delay time, indicating that both PWMs are off. It is important to include this interval to ensure low conduction loss of body diode in Q_1 and Q_2 in addition to avoid shoot through current.

Here, the FDT technique is employed due to its simplicity. The T_D is set fixed at 15 ns generated by the dual-channel PWM generator. For a constant L_r value of 9 nH and 0.20 of D, the i_{Lr} of different T_D values are observed via simulation during its turn-off phase. The oscillation count is measured and the implications on applied T_D duration are investigated. It is expected that there will be some variations in oscillation count leading to power dissipation. Therefore, in this case, an optimized T_D value can be obtained using iterative method.

3.2.1.3 Effects of Resonant Inductor

In the resonant network, i_{Lr} charges and discharges with respect to the applied pulse width of PWM_1 and PWM_2. Thus the gate terminals of Q_1 and Q_2 will draw current for a short time which is used to fully charge the capacitance of $v_{gs,S1}$. By changing the value of L_r, the flow of current can be observed through simulation within a specific duty ratio of 0.20.

The L_r value is varied from 1 nH to 50 nH and the investigation is focused on the ringing count during turn-off of Q_1 and Q_2 switch. For a fixed T_D of 15 ns being the predetermined value, the simulation to determine the optimized L_r is carried out. The expected result gives the best value of L_r indicating optimized turn-on speed hence low inductive oscillation effect.

3.2.2 Experimental Setup of S-CRGD Circuit

The experimentation took place in power electronics research lab. All of the PWM settings, D, T_D and L_r values follow the simulation setup. The experimental components used are shown in Table 3.2. The V_{DC} is reduced to 25 V for safety reason due to expected high overshoot current.

Table 3.2 Experimental Parameters of S-CRGD for f_s = 1 MHz

Components	**Parameter Settings & Ratings**
PWM_1 , PWM_2	A dual-channel Function Generator Tektronik AFG3102
Q_1, Q_2	STP22NF03L, 30 V / 22 A, $R_{ds(on)}$ = 0.038 Ω
D_1, D_2, D_3	SDP06S60, 600 V / 6 A
S_1	IRFI540NPBF, 100 V / 20 A, $R_{ds(on)}$ = 0.052 Ω
L_r	10 nH
V_s	12 V
V_{DC}	25 V

A 12-V input voltage, V_s is used and the PWM outputs are first fed into MOS driver EL7104 before connecting to the gate of MOSFET switches, Q_1 and Q_2. The driver is not used in the simulation because the PWM settings are sufficient to generate precise signals to the gate of MOSFETs. All of the parameter limitations are investigated using the optimized values as defined in the simulations: D = 0.20, L_r = 10 nH, T_D = 15 ns. The picture of the experimental S-CRGD circuit board is shown in Appendix A.

The experimental results are used in the design of the D-CRGD for driving SRBC circuit. The D-CRGD is simulated and measured through experiment. The methodology process is discussed in the next section. The components used in the simulation have different rating values such as for diodes and switches since the library files for the ones used in the experiment are not available. Therefore, the closest ratings available are selected in the simulation.

3.3 New D-CRGD Circuit

Using the optimized parameters as determined in the single-channel topology, the new D-CRGD circuit is shown in Figure 3.3. This is the second step in the work whereby simulation and experimental analyses are conducted. The D-CRGD circuit has the ability to drive S_1 and S_2 switches of SRBC circuit effectively due to its features in fast switching speed and low switching loss. The body diode conduction loss is also expected to be reduced to minimum value. The details on the circuit operation and its loss analysis are discussed in the next chapter.

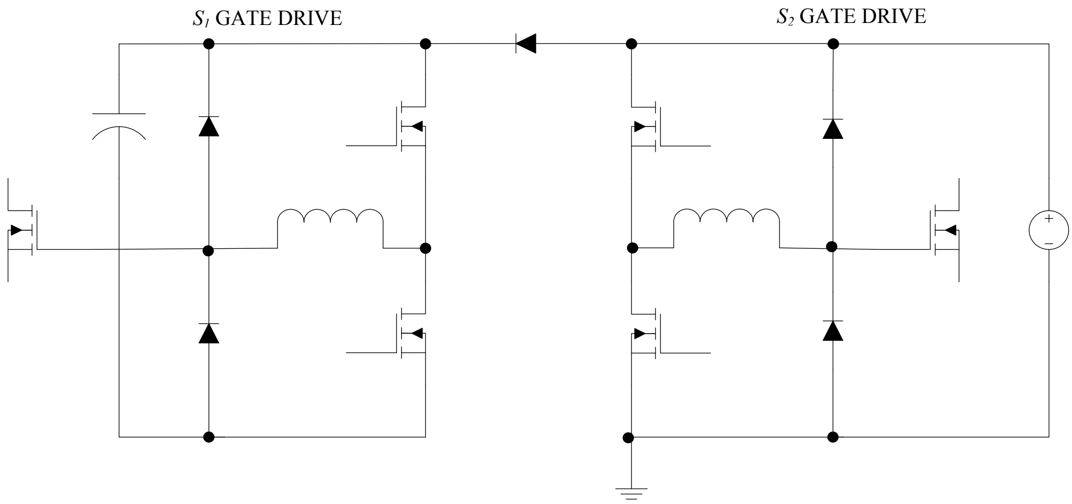

Figure 3.3 New D-CRGD

The circuit contains two symmetrical S-CRGDs as shown in Figure 3.2, having the advantage of the bootstrap components, D_a and C_a compared to work done in [12]. In the simulation, both left and right circuits generate two different pulse widths at the gate of S_1 and S_2. Using four driving FETs, Q_1 to Q_4, the simulation principle is similar to Figure 3.2. Here, there are some changes to the simulation setup especially at the right circuit where the PWM of S_2 operates in 1-D. The T_D separation maintains at 15 ns. Table 3.3 shows the parameters assigned in simulation setup.

Table 3.3 Simulation Parameters of D-CRGD for f_s = 1 MHz

Components	Parameter Settings & Ratings
V_{p1}	200 ns, delay t_{d1} = 15 ns
V_{p2}	765 ns, delay t_{d2} = 232 ns
V_{p3}	312 ns, delay t_{d3} = 284 ns
V_{p4}	670 ns, delay t_{d4} = 955 ns
D_1 to D_4, D_a	1N6392, 45 V / 60 A
L_1, L_2	9 nH
Q_1 to Q_4	PSMN130-200D/PLP, 200 V / 20 A, $R_{ds(on)}$ = 0.130 Ω
C_a	100 µF
S_1, S_2	IRFP250, 200 V / 33 A, $R_{ds(on)}$ = 0.085 Ω
V_s	12 V

3.3.1 Experimental Setup of D-CRGD Circuit

There are two function generators used to provide four different synchronized pulses and thus drive Q_1 to Q_4 switches. The parameters used are tabulated in Table 3.4. The gate voltages of S_1 and S_2 in Figure 3.3 are measured and verified with the simulation. It is noticed that the diodes and switches used in the simulation and experiment are different in ratings. The reason is that the unavailability of the library files of the experimental components. Nevertheless, the ratings are comparable.

Table 3.4 Experimental Parameters of D-CRGD for f_s = 1 MHz

Components	Parameter Settings & Ratings
V_{p1} to V_{p4}	2 dual-channel Function Generators Tektronik AFG3102
D_1 to D_4, D_a	SDP06S60, 600 V / 6 A
L_1, L_2	10 nH
Q_1 to Q_4	STP22NF03L, 30 V / 22 A, $R_{ds(on)} = 0.038\ \Omega$
S_1, S_2	IRFI540NPBF, 100 V / 20 A, $R_{ds(on)} = 0.052\ \Omega$

3.4 New SRBC Circuit

By having correct driving pulses in S_1 and S_2 generated by the new D-CRGD circuit in Figure 3.3, the new SRBC circuit can be operated effectively. Figure 3.4 shows the new SRBC circuit. In this subsequent step, the circuit is also simulated and measured experimentally. Table 3.5 shows the additional passive components for ZVS used in the circuit. The operation of new SRBC and analysis of circuit performance are presented in the results and discussion chapter.

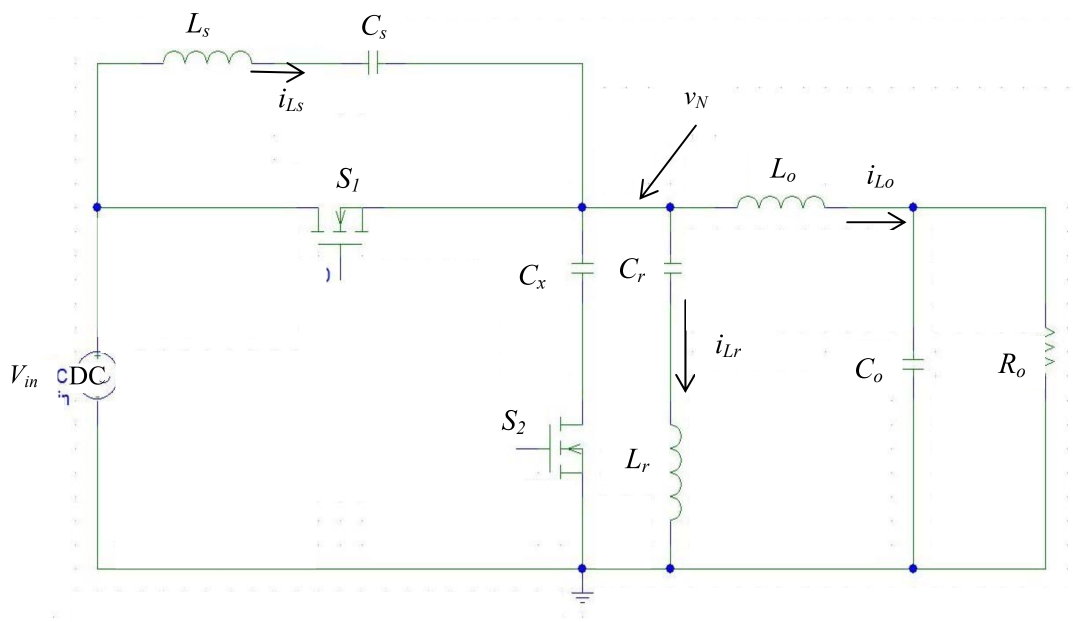

Figure 3.4 New SRBC

Table 3.5 Components Used in New SRBC Circuit

Components	Parameter Settings & Ratings
L_s, L_o, L_r	0.9 ìH, 18 ìH, 15 ìH
C_s, C_x, C_r, C_o	100 ìF, 1 mF, 95 ìF, 100 ìF
V_{in}	48 V
R_o	10 Ω

Since the new ZVS is operated in DCM, the critical value of L_o has been calculated using Eq. (29) where it is found to be 4 μH. Therefore, 18 μH is chosen. Hence C_o is determined using Eq. (30) and Eq. (31) respectively. By multiplying the calculated C_o value of 30 μF by a higher factor to guarantee good output regulation, this gives 100 μF.

$$L_{crit} = [1 - \frac{V_o}{V_{in}}].(\frac{R_o}{2f_s}) \qquad (29)$$

$$C_o = \frac{\Delta I_o}{8 f_s \Delta V_o} \qquad (30)$$

where $\Delta V_o = \frac{\pi^2 (1 - D_{S1}) V_o}{2} . (\frac{f_r}{f_s})^2$ (31)

To ensure ZVS operation for S_1 and S_2, the L_r, L_s, C_r and C_s values are carefully selected based on $X_L = 2\pi \times f_s \times L_{r,s}$ and $X_C = \frac{1}{2\pi \times f_s \times C_{r,s}}$ respectively. This may help establish ZVS drain-gate voltage behavior. Also C_x of 1 mH is used to minimize the drain voltage of the switch. Appendix B shows the experimental new ZVS-SRBC test circuit board.

In the simulation, the results are expected to indicate better performance of new

SRBC with lower losses. Among the results to be observed in the simulation are:

a) Gate voltages of S_1 ($v_{gs,S1}$) and S_2 ($v_{gs,S2}$).

b) Drain voltages of S_1 ($v_{ds,S1}$) and S_2 ($v_{ds,S2}$).

c) Drain currents of S_1 ($i_{d,S1}$) and S_2 ($i_{d,S2}$).

d) Currents in L_s, L_r and L_o.

e) Body diode conduction of S_2

3.5 Chapter Summary

The methodology starts with the simulation and experimentation of S-CRGD circuit to determine the best limiting parameters which are based on specific requirements. Then those values will be applied in the design of D-CRGD network. Using two-pulse generators, the new SRBC is simulated and verified experimentally. All of the results are compared, analyzed and discussed in Chapter 4. In addition, some additional simulation work are presented in Chapter 5 which include the analyses of Q-factor in S-CRGD, implication on switching, dead time and variation in loads of new SRBC.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Chapter Overview

The simulation and experimental results are discussed thoroughly in this chapter. The new D-CRGD and SRBC topologies are derived and evaluated in terms of switching, conduction and body diode conduction losses. When the simulation and experimental results are compared, they present similarities in operating waveforms within acceptable range of output values.

4.2 Simulation of S-CRGD Circuit

In Figure 3.2, two pulses which provide square-waved periodic signals fed into both switches Q_1 and Q_2 respectively. The pulsating waves oscillate at 1 MHz switching frequency. By getting the signals from PWM_1 and PWM_2, Q_1 and Q_2 produce waveforms as shown in Figure 4.1. It can be seen that the turn-off time of $v_{gs,S1}$ is faster than the conventional gate drive circuit as shown in Figure 2.2(b). Based on second-order RLC system, the i_{Lr} and $v_{gs,S1}$ are given by Eq. (32) and Eq. (33) respectively.

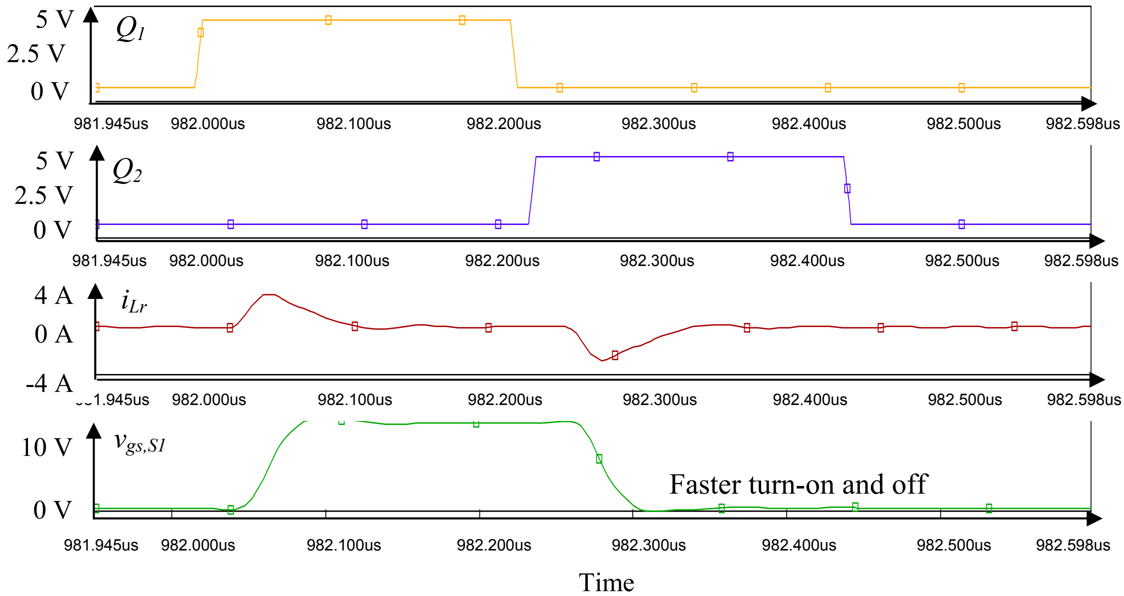

Figure 4.1 S-CRGD PSpice Simulated Waveforms

$$i_{L_r}(t) = I_{L_0} e^{-\frac{R_{eq}}{2L_r}t} \cos\left(\frac{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^{\ 2}}}{2L_r} t\right) + \frac{2V_{in} - 2V_{C_{iss}} - R_{eq} I_{L_r}}{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^{\ 2}}} e^{-\frac{R_{eq}}{2L_r}t} \sin\left(\frac{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^{\ 2}}}{2L_r} t\right) \qquad (32)$$

Given $V_{gs,S_1} = V_{C_{iss}}$

$$V_{gs,S_1}(t) = V_{g_0} + \frac{1}{C_{iss}} \int_0^t i_{L_r}(t) dt \qquad (33)$$

When Q_1 is turned on, the inductor current, i_{Lr} starts to develop. Switch Q_2 at this time is not conducting. Here, assuming that $i_{L0} = 0$, $V_s = V_g$ and $V_{Ciss} = 0$, i_{Lr} is given by Eq. (34), charged to maximum value and so is $v_{gs,S1}$.

This $v_{gs,S1}$ increases exponentially as given by Eq. (35) which is then clamped to input source, V_s of 12 V. R_{eq} is the total gate resistance in the RGD and this value is calculated in the range 1.3 - 1.7 Ω which includes resistance in the wire and the MOSFET from datasheet.

$$i_{L_r}(t) = \frac{2V_g}{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^2}} e^{-\frac{R_{eq}}{2L_r}t} \sin\left(\frac{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^2}}{2L_r}t\right) \tag{34}$$

$$v_{gs,S_1} = V_{C_{iss}} + \frac{1}{C_{iss}}\int_0^t i_{L_r}(t)dt \tag{35}$$

$$i_{L_r}(t) = -\frac{2V_g}{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^2}} e^{-\frac{R_{eq}}{2L_r}t} \sin\left(\frac{\sqrt{\frac{4L_r}{C_{iss}} - R_{eq}^2}}{2L_r}t\right) \tag{36}$$

The duration of the charging current depends on L_r and $Z_0 = \sqrt{\frac{L_r}{C_{iss}}}$ being the impedance of S-CRGD. Once it is fully charged, i_{Lr} in Eq. (34) starts to discharge to zero through body diode of Q_2, L_r, D_1 and back to V_s. For a specified time given after Q_1 is turned off, Q_2 takes its turn to conduct. Then the previously clamped 12-$V_{gs,S1}$ is discharged to zero and the discharging voltage equation is the same as given by Eq. (33). The i_{Lr} is charged again to maximum but now in the negative direction which gives Eq. (36). Once charged, it is charged back up to zero [93] and this process repeats for the subsequent cycles.

4.2.1 Optimization of Duty Ratio

The summation of charging and discharging time of i_{Lr} is used as a benchmark to determine the minimum operating range of D. As shown in Figure 4.2, the 200 ns pulse width of 1 MHz switching frequency indicates a portion of 20 % turn-on time from one cycle. Here, during the conduction of Q_1, i_{Lr} is charged to maximum. Then the discharging phase will commence only when i_{Lr} is fully discharged until it reaches zero.

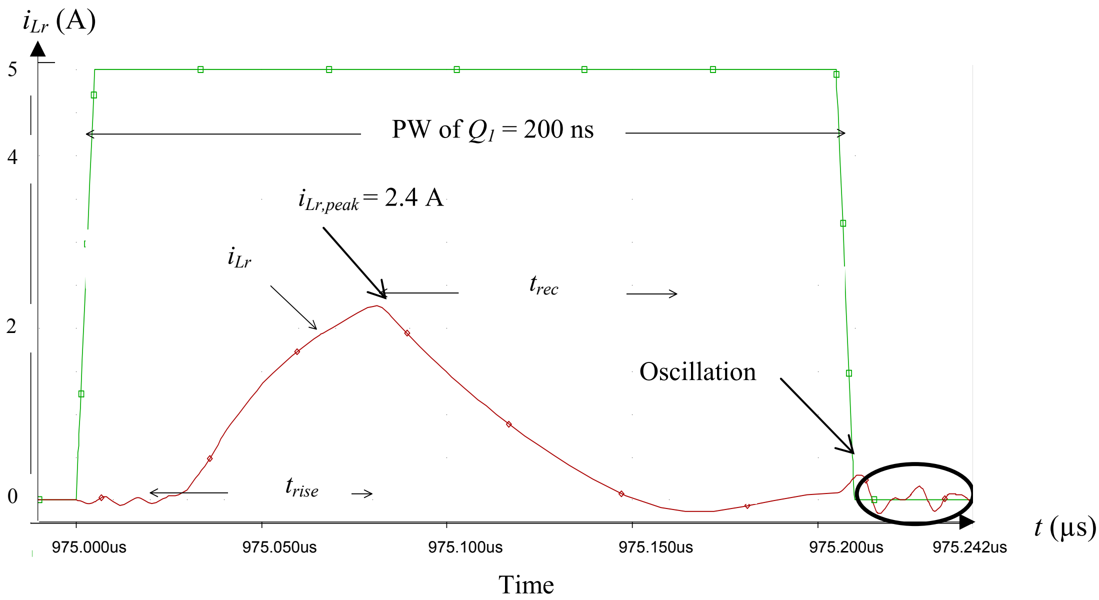

Figure 4.2 Charging & Discharging of i_{Lr} with Respect to Q_1 Turn-On

The discharged current, i_{Lr} requires a considerable amount of time before the turn-on sequence ends. This is known as the recovery time, t_{rec} which is given by Eq. (37).

$$t_{rec} = \pi\sqrt{L_r C_{iss}} \tag{37}$$

Here, the duration of charging is shorter due to on resistive charging effects through gate and driver resistance. Looking at Figure 4.2, the duration of charging and discharging of current must be within the given pulse width. To do this, PWM_1 has to provide sufficient on-time duration which will allow i_{Lr} to flow without disruption. Faster recovery free-wheeling diodes can be used to increase the charging time and hence speed of the converter. At the end of Q_1 turn-on time, there exist some oscillations which are clearly seen in the diagram.

The i_{Lr} charging and discharging behavior of Q_2 are identical to Q_1. When Q_2 conducts, Q_1 is off at this time. The negative peak i_{Lr} of both switches are found to be slightly reduced which are shown in Figure 4.3. It is due to higher parasitic resistance gained in C_{iss} of S_1 during the switching transition. Increasing pulse width in PWM_1 will eventually increase D of $v_{gs,S1}$ as well. On the other hand, reducing the width too short may force discharged i_{Lr} to oscillate at the end of $v_{gs,S1}$ turn-off sequence which will be discussed in the next section. This consequently increases dissipation and gives rise to stress in the S-CRGD circuit.

4.2.2 Optimization of Resonant Inductor

In the resonant network, i_{Lr} charges and discharges with respect to the applied pulse width of PWM_1 and PWM_2. Thus the gate terminals of Q_1 and Q_2 will draw current for a short duration of time which is used to fully charge the $v_{gs,S1}$. Here i_{Lr} is at maximum, I_{peak} given by Eq. (38) and the time taken for i_{Lr} to reach maximum from zero is given by Eq. (39). The shorter the time, the faster the turn-on speed will be. In addition, the rise time, t_{rise} Eq. (40) and recovery time, t_{rec} Eq. (37) of i_{Lr} also depend on the value of L_r.

$$i_{L_r(peak)} = \frac{V_{C_{iss}}}{Z_O} \tag{38}$$

$$t_{peak} = \frac{\tan^{-1}\left(\dfrac{2L_r\sqrt{\dfrac{4L_r}{C_{iss}} - R_{eq}{}^2}}{R_{eq}}\right)}{2\sqrt{\dfrac{4L_r}{C_{iss}} - R_{eq}{}^2}} \tag{39}$$

$$t_{rise} = \frac{\pi}{2}\sqrt{L_r C_{iss}} \tag{40}$$

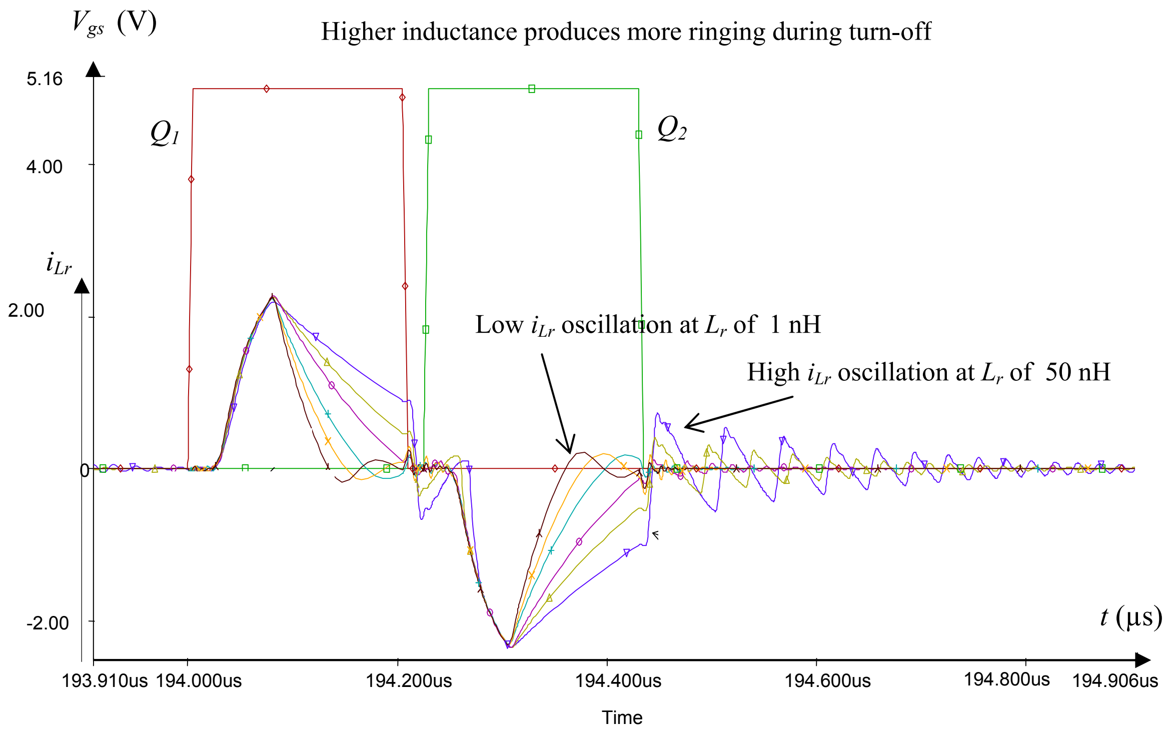

Figure 4.3 S-CRGD i_{Lr} versus L_r (200 ns pulse, 15 ns T_D) PSpice Simulation

As L_r value increases, the charging and discharging time of i_{Lr} also increase. As shown in Figure 4.3, it shows a limit in L_r value for the generation of $v_{gs,S1}$ before i_{Lr} starts to oscillate at turn-off. Using 200 ns pulse width, L_r of 40 nH or below are chosen for T_D of 15 ns. It is seen that when higher L_r is used, i_{Lr} will produce more ringing and thus increase diode conduction loss.

During turn-on, the charging time of i_{Lr} will represent the turn-on speed of the driver. Increasing L_r will result in increasing turn-on time and hence leading to a slower speed. However, introducing a very small L_r will reduce the transient response at the cost of limiting the operating current flow within the resonant tank. This eventually increases peak current, I_{peak} of i_{Lr} and consequently produces higher power loss.

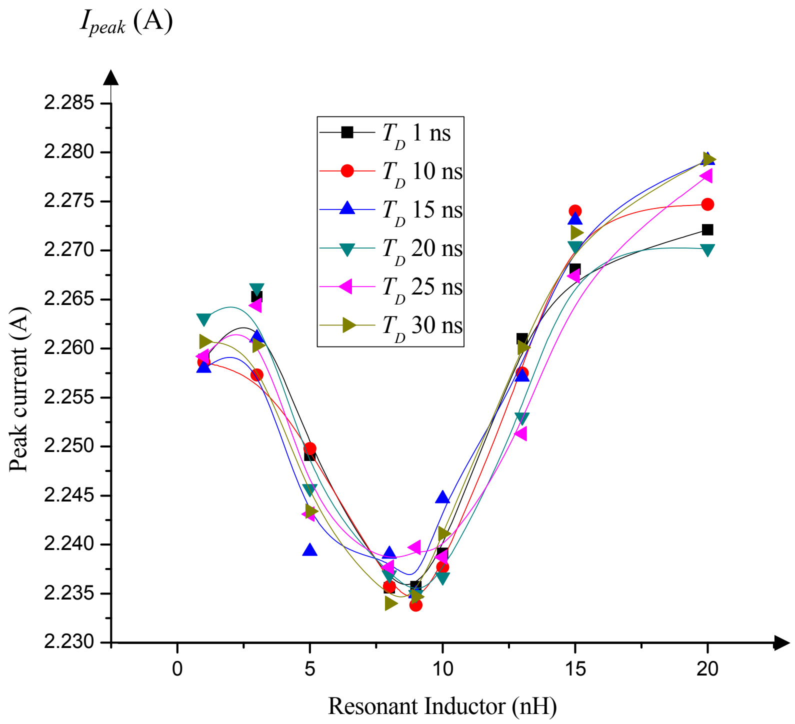

Figure 4.4 S-CRGD I_{peak} versus T_D (200 ns pulse, 9 nH inductor)

In another important aspect, switching loss is directly proportional to speed. In order to reduce this loss, one option is to reduce the speed. However, this is not desirable in high frequency application. T_D is also important in the optimization of switching losses. Fig 4.4 shows the relationship between L_r and peak current of i_{Lr} for different T_D values ranging from 1 ns - 30 ns. It is found that the optimized L_r value is around 9 nH - 10 nH.

4.2.3 Optimization of Dead Time

A FDT control scheme is chosen due to its simplicity whilst the PWMs are generated by the dual function generator. T_D can be easily set up to avoid shoot-through current between switches. Using the L_r of 9 nH, the i_{Lr} of different T_D values during turn-off phase of $v_{gs,S1}$ are studied via simulation.

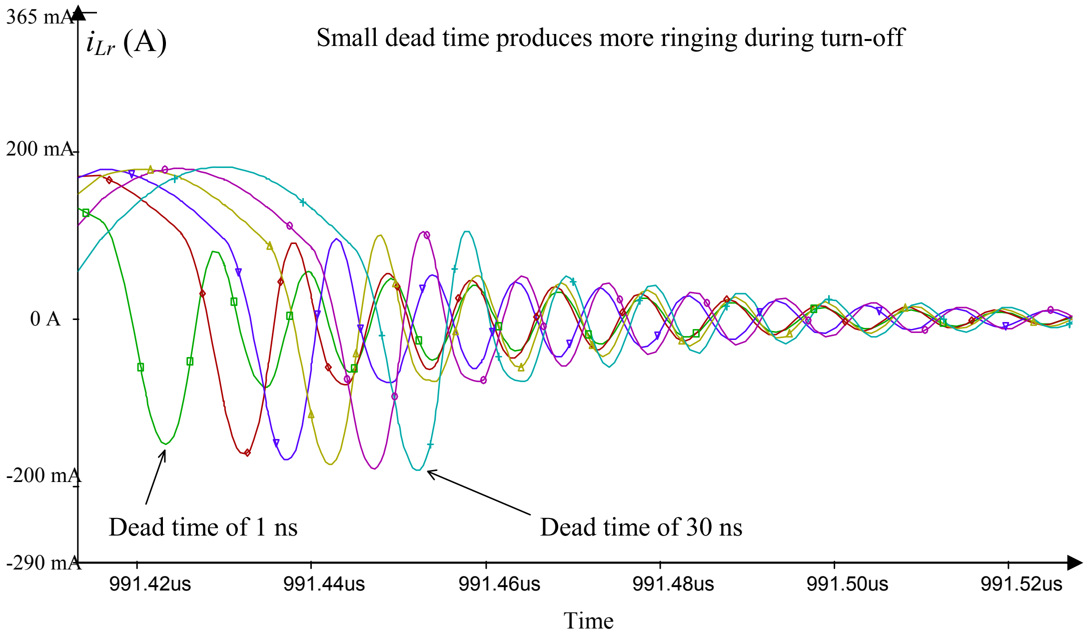

Figure 4.5 S-CRGD 9 nH i_{Lr} Ringing versus T_D PSpice Simulation

As shown in Figure 4.5, it is found that there are presence of ringing in i_{Lr} which can cause variation in power losses at $v_{gs,S1}$ during turn-off. It is also observed that when T_D is set to a smaller value, there are more ringing counts. One way to solve this is by increasing T_D. However, if T_D is applied too long, $v_{gs,S1}$ will appear to be floating and hence this may give rise to higher dissipation in the circuit.

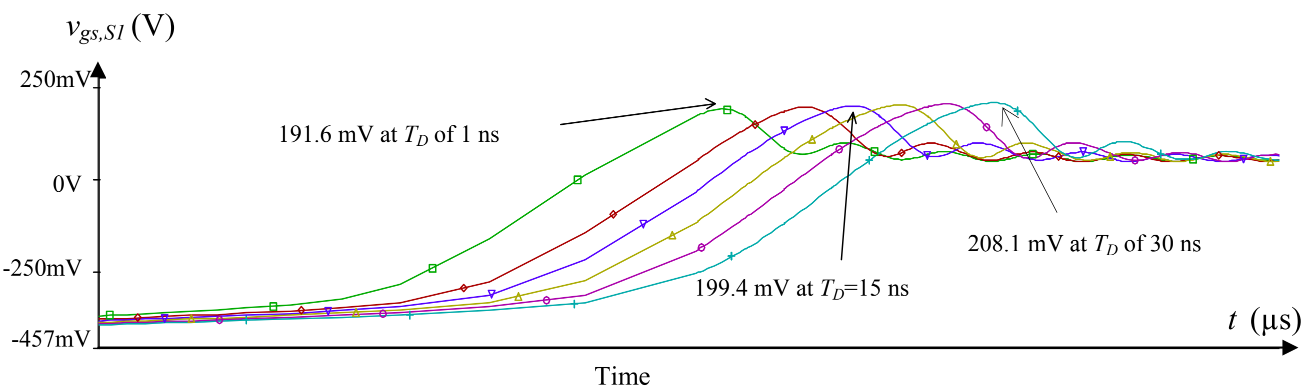

Figure 4.6 S-CRGD 9 nH $v_{gs,S1}$ Ringing versus T_D PSpice Simulation

In addition, the T_D can be determined from the tradeoffs between speed and power dissipation at turn-off. Referring to Figure 4.6, a longer duration of T_D introduces higher ringing overshoot voltage hence higher EMI. Even though the difference is small, the values are quite distinct and comparable. This pattern comes from the energy stored in the inductance when it is released across parasitic capacitance of S_1.

At lower T_D, this gives result in the lowest ringing peak of $v_{gs,S1}$. However, T_D of 1 ns does not guarantee protection against cross conduction. Therefore, based on the design parameters, Figure 4.7 shows that the optimized T_D value is found to be 15 ns with respect to peak current of i_{Lr}. The smaller peak current allows for lower power dissipation.

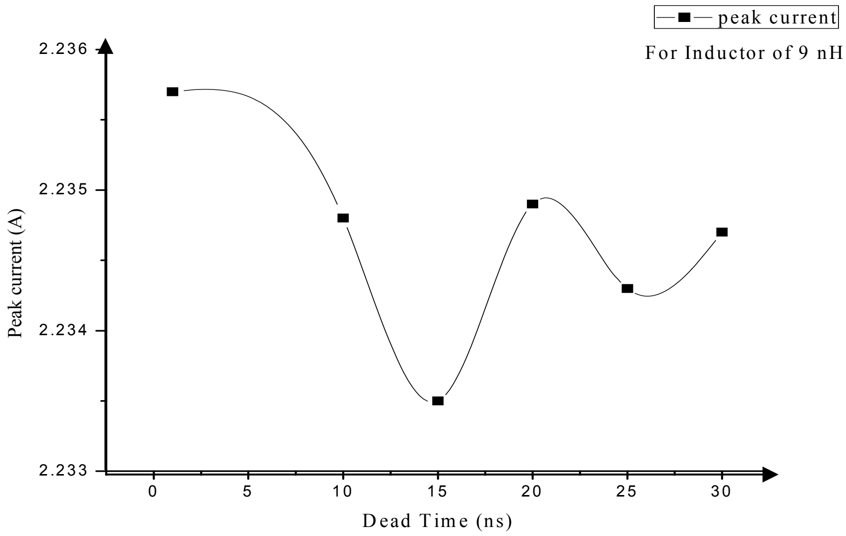

Figure 4.7 S-CRGD 9 nH i_{Lr} Peak Optimization versus T_D PSpice Simulation

4.2.4 Q-Factor Vs Inductor

In this part of work, a graph of Q-factor versus inductor value and gate resistance power losses is plotted as shown in Figure 4.8. Q is optimized for optimum gain in S-CRGD with respect to L_r. There are two curves plotted: one is the Q-factor and the other is the gate resistance power loss which is calculated using Eq. (41).

It is clearly shown that there is an intersection point between these two curves, indicating L_r of 12 nH, which results in the Q-factor of 0.68.

$$P_{R_{eq},loss} = \frac{R_{eq}}{(R_{eq} + Z_O)} \times Q_G \times V_s \times f_s \tag{41}$$

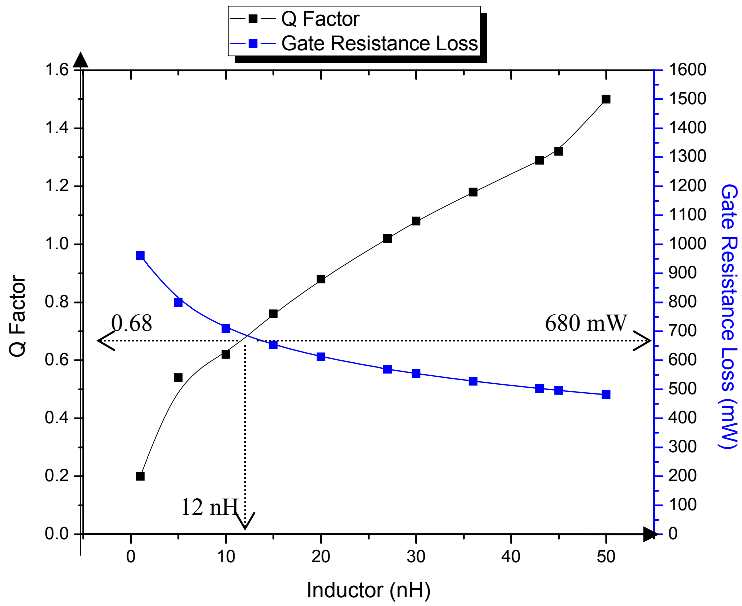

Figure 4.8 S-CRGD L_r Inductance and Q Factor PSpice Simulation

A higher Q-factor indicates more energy storage in the resonant system and reduction in gate power losses. Even though it is desired to get a higher Q for better performance of gate driver circuit, the Q is only for this S-CRGD circuit topology (Q = 0.5 as reported in [94]).

However, there is a limitation in selecting a higher L_r value. As previously shown in Figure 4.3, as inductor value increases, the time taken for the inductor current, i_{Lr} to completely discharge increases, which will cause oscillation during turn-off and increases gate voltage, $V_{gs,S1}$ power loss. This eventually adds up to total gate drive losses in S-CRGD circuit. It is observed that i_{Lr} takes a longer time to charge and discharge as L_r increases. In Figure 4.3, the maximum L_r value is within the range 20 ns - 30 nH. Thus, the $L_{r,max}$ is determined to be 22 nH, being the upper boundary limit using Eq. (12).

Due to the high oscillation in i_{Lr} at higher L_r value, total S-CRGD loss is expected to increase. However, from Eq. (39), the gate resistance power loss is reduced. More importantly, in order to operate the gate driver efficiently with high performance, there is a tradeoff between L_r value and switching loss. Table 4.1 summarizes the results.

Table 4.1 Q-Factor Comparison of S-CRGD Performance

Inductor value	**5 nH**	**12 nH**	**43 nH**
Q factor	0.54	0.68	1.29
Gate resistance power loss	798.98 mW	680.27 mW	502.38 mW
Level of Total RGD Loss	LOW but high gate loss	Best	HIGH due to oscillation

Table 4.1 clearly shows that 12 nH inductance value gives best indicator in terms of power losses and switching capability. The Q-factor does not only depend on L_r alone, but other parameter such as input capacitance of power MOSFET, C_{iss}.

4.2.5 Loss Analysis of S-CRGD Circuit

In S-CRGD circuit, the charging and discharging of i_{Lr} generates a resonant link between S_1 and V_s. Comparing to the conventional totem-poled gate drive circuit, more energy could be saved. The switching loss in S-CRGD circuit is normally high especially in the driving transistors, Q_1 and Q_2. This loss is usually caused by rapid turn-on and turn-off switching transitions. Where switching loss is a variable parameter that consistently changes with respect to variation in L_r, T_D and D, this can be reduced by adopting snubber network [95].

By lowering the peak current of i_{Lr} this will lead to a faster turn-on speed. In this case, when different L_r and fixed t_{rise} are applied, this will generate different peak current values. Here, the performance of the S-CRGD can be evaluated.

The average power loss equations for driving switches Q_1-Q_2, diodes D_1-D_2 and gate voltage of S_1 are given in Eq. (15), Eq. (42) and Eq. (43) respectively.

$$P_D = \frac{2V_F}{2V_F + V_{in}} \times \frac{\sqrt{\frac{L_r}{C_{iss}}}}{R_{eq} + \frac{L_r}{C_{iss}}} \times f_s \times V_{in} \times Q_G \tag{42}$$

$$P_{gate,S_1} = i_{L_r} \times V_{gs,S_1} \tag{43}$$

where V_F is forward voltage drop of D_1 and D_2, Q_G is the gate charge of S_1 and f_s is the switching frequency. From simulation, the switching loss of Q_1 and Q_2 are dominant as shown in Figure 4.9. By applying higher L_r value, this results in lower peak current and thus reduces switching loss but with the cost of reducing speed.

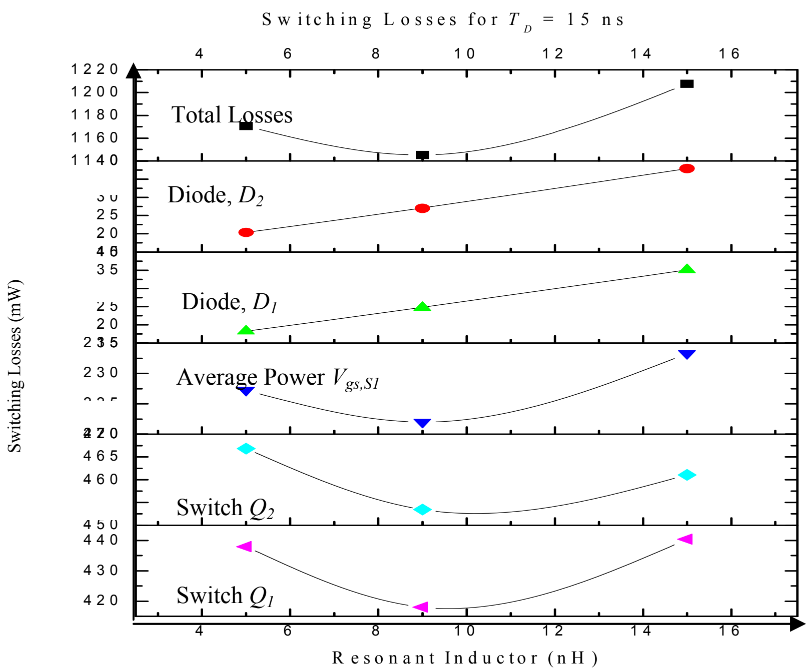

Figure 4.9 S-CRGD PSpice Simulation Switching Loss Distribution

Figure 4.9 shows the distribution of switching loss in the S-CRGD circuit. It is noticeable that the switching losses in transistors are high and dominant. Both switching losses in diodes behave linearly to L_r because more time is required for i_{Lr} to charge and discharge within the circuit and along the diode path. This adds to the oscillation of i_{Lr} which contributes to the loss.

Nevertheless, there will be an upper limit of L_r where too high, will force i_{Lr} to generate high oscillation in the circuit. The switching losses in D_1 and D_2 are found to be minimal. The $v_{gs,S1}$ power loss on the other hand is about one half (222 mW) of turn-off switching loss in Q_1 (418.02 mW) and Q_2 turn-on switching loss of 453.47 mW which makes up of 19.4 % out of total switching loss of 1.15 W at 9 nH with T_D = 15 ns, D = 0.20 and f_s = 1 MHz. If the switching losses of Q_1 and Q_2 can be further reduced, this will eventually increase power loss savings in S-CRGD.

4.3 Operation of S-CRGD: Experimental Results

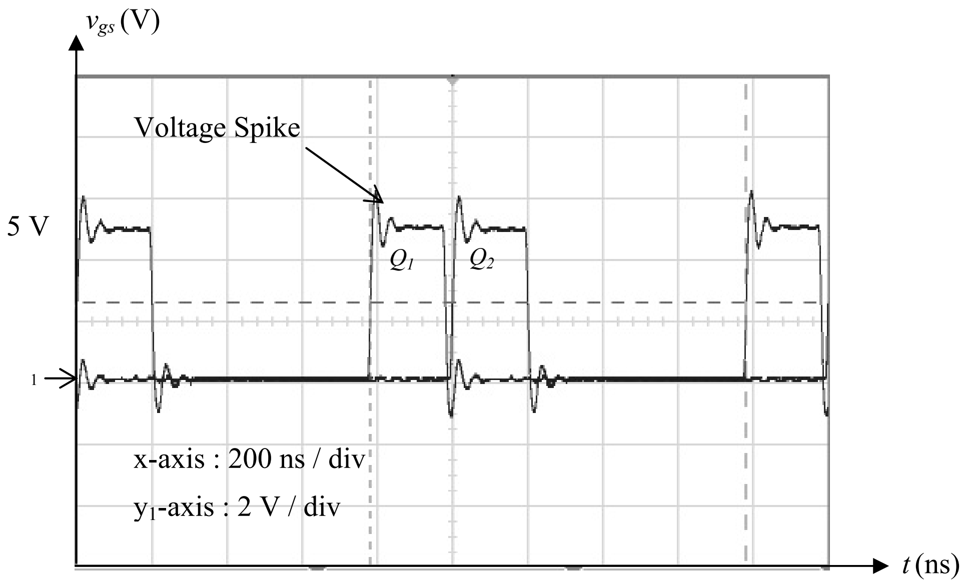

Figure 4.10 S-CRGD PWM Experimental Waveforms

Using function generator, two PWM signals of 200 ns each are generated with T_D of 15 ns. This is shown in Figure 4.10. The experimental work is based on the optimized values of L_r = 10 nH, T_D = 15 ns and D = 0.20 according to the setup values in Table 3.2. As seen in Figure 4.10, there is a voltage spike during the initial turn-on time. These pulses are then fed to the gates of N-channel MOSFETs Q_1 and Q_2 respectively.

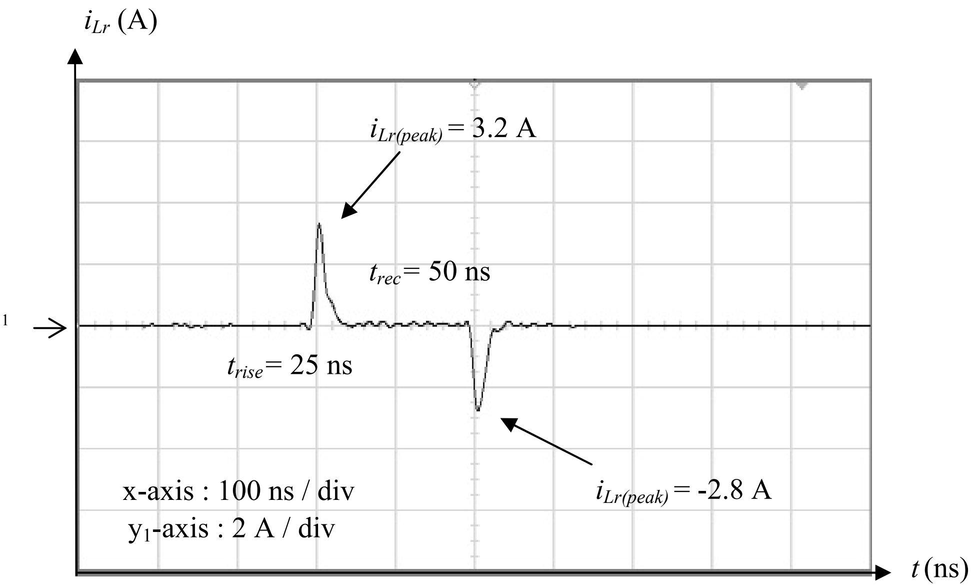

Figure 4.11 S-CRGD i_{Lr} Experimental Waveform

The experimental behavior of charging and discharging i_{Lr} is shown in Figure 4.11. The positive peak current is about 3.2 A and t_{rise} and t_{rec} taken by this current are about 25 ns and 50 ns respectively. These results show resemblance of i_{Lr} behavior found by the simulation as shown in Figure 4.3.

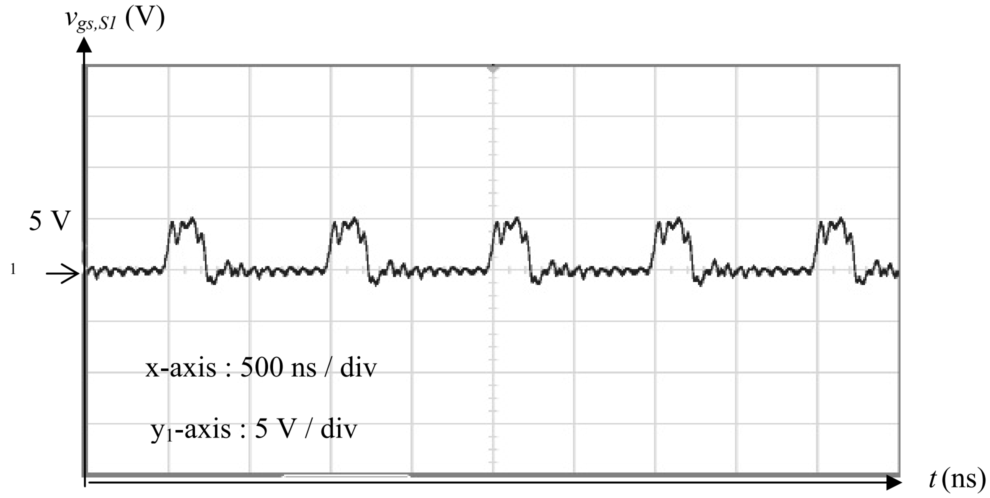

Figure 4.12 S-CRGD $v_{gs,S1}$ Experimental Waveform

The charging of i_{Lr} yields the charging of $v_{gs,S1}$ to maximum peak of 5 V as shown in Figure 4.12. This result is compared with the simulation illustrated in Figure 4.1. However, due to stray inductance experienced by the switch caused by the parasitic capacitance, some oscillations are seen in the experiment.

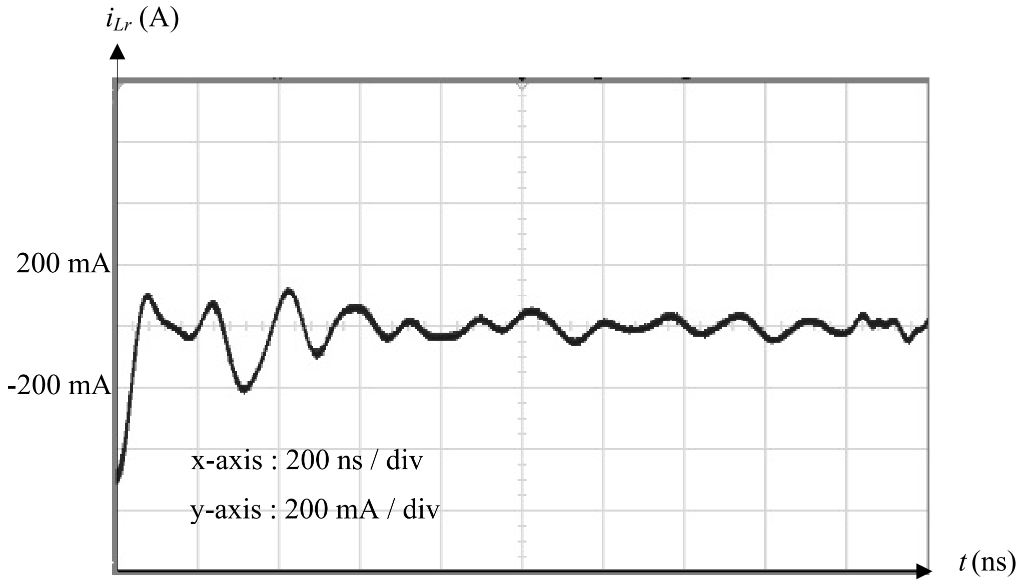

Figure 4.13 S-CRGD i_{Lr} Experimental Turn-Off Oscillation

The noise also leads to the oscillation of i_{Lr} during turn-off of $v_{gs,S1}$. From simulation result referred to Figure 4.5, the ringing current amplitude of 200 mA is observed. The experimental result shown in Figure 4.13 has proven this. In order to justify that switch, S_1 conducts correctly, the drain current and voltage at the load are measured as shown in Figure 4.14. Both of them correspond to the inductive load circuit where peak current and voltage measure 2.25 A and 22 V respectively based on given load parameters.

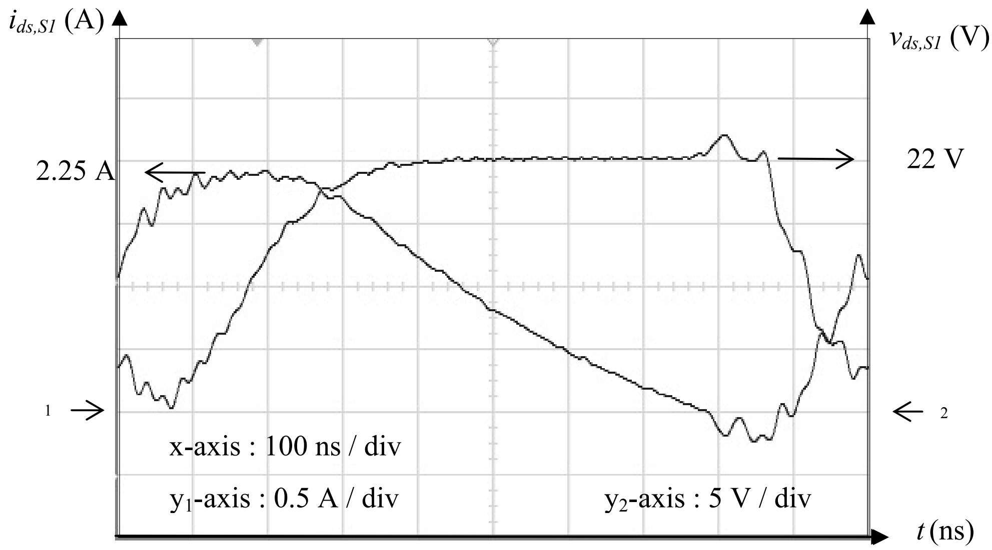

Figure 4.14 S-CRGD Experimental i_{ds} versus v_d

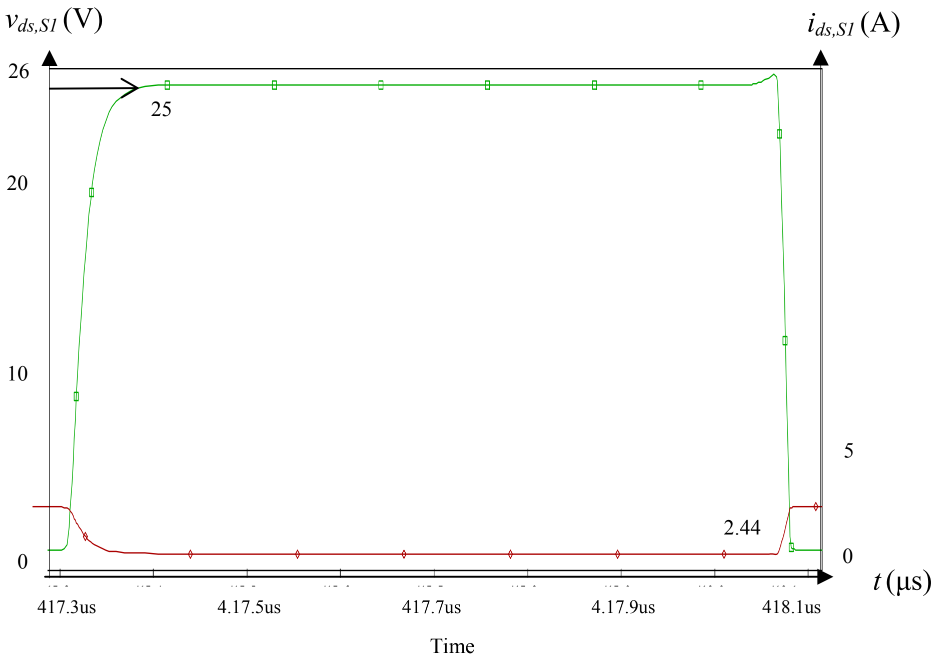

Figure 4.15 S-CRGD i_{ds} versus v_{ds} PSpice Simulation

The simulated waveforms obtained are also given in Figure 4.15 for comparison and they are in agreement with the experiment. Therefore, all of the experimental results validate the simulation. The outcomes show a promising proof of the work. The comparative data is tabulated in Table 4.2. All three sets of data are analyzed based on different results taken from experiment, simulation and MathCAD. The peak of i_{Lr}, t_{rise}, t_{rec}, switching loss in Q_1, $P_{sw,Q1}$ and $P_{sw,Q2}$ are compared to validate the simulation results.

Table 4.2 S-CRGD: Comparison of Simulated and Experimental Data

Parameters	Experiment	Simulation	% Diff	MathCAD	% Diff to Experiment
$i_{Lr(peak)}$ A Eq. (38)	3.20	2.40	25.00	3.60	11.11
t_{rise} (ns) (40)	25	30	16. 67	25.81	3.14
t_{rec} (ns) (37)	50	58	13.79	51.62	3.14
$P_{sw,Q1(off)}$ (mW) (17)	425.20	418.02	1.69	420.34	1.14
$P_{sw,Q2(on)}$ (mW) (16)	438.50	453.47	3.30	447.80	2.08

The numerical analysis using MathCAD is carried out to compare the experimental results with the simulation data. From Table 4.2, the experimental data validates the simulation. The MathCAD calculation has also proven that in most cases, the analysis is acceptable. However, the simulated peak i_{Lr} value is slightly lower compared to the experiment. This is due to the convergence settings done in the simulation setup.

4.4 Operation of D-CRGD: Simulation Results

The new D-CRGD circuit in Figure 3.3 is simulated using the parameter setup given in Table 3.3. The circuit is used to generate the fixed T_D for SRBC circuit and it consists of four switches Q_1 to Q_4. Both sets of switches Q_1–Q_2 and Q_3–Q_4 behave symmetrically. The inductor L_1 and L_2 connect the driving switches to the power MOSFETs, S_1 and S_2. The D-CRGD circuit provides two driving signals with duty cycle D and 1-D powered by a single input voltage source, V_s of 12 V. Duty ratio of 0.20 is produced to allow for inductor current requirement. The optimized L_1 and L_2 values used for the circuit are 9 nH with T_D of 15 ns.

The bootstrap diode, D_a and capacitor, C_a have the advantages in reducing the losses in D-CRGD circuit. When Q_2 is turned on, C_a will charge up V_s via D_a to generate an output voltage of $V_s - V_{Da}$. Consequently, this causes Q_1 to "float" at the gate of S_1. D_a will generate some forward voltage drop, $V_{F,Da}$ while charging C_a and reverse bias power loss during reverse recovery. More importantly, C_a can prevent voltage transient at $v_{ds,S1}$, avoid significant heat loss and support high peak current drawn from V_s during turn-on. In addition, C_a voltage will rise slightly above V_s to provide needed gate drive voltage for S_1.

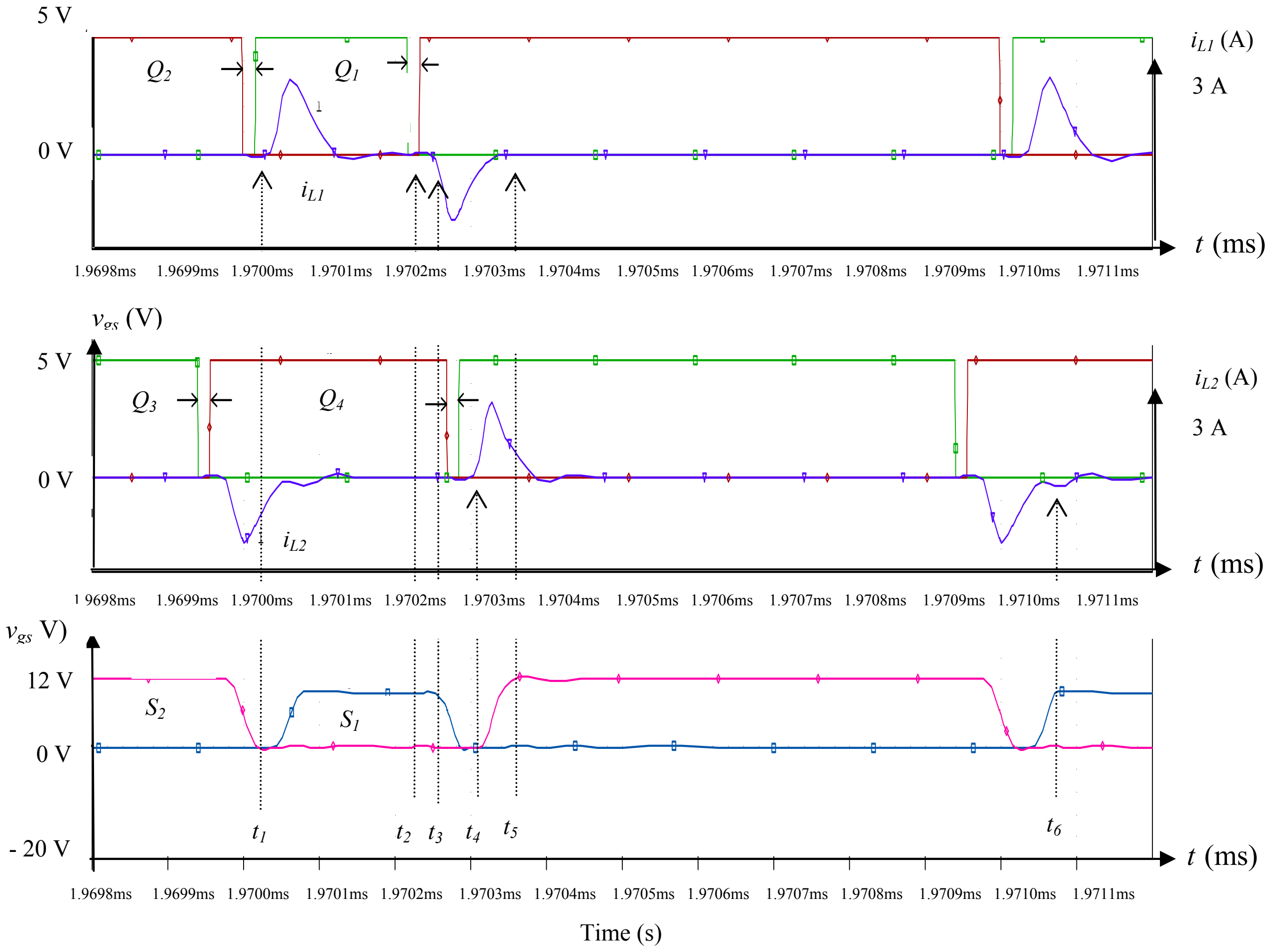

Figure 4.16 New D-CRGD PSpice Simulation Waveforms

Figure 4.16 shows the operating waveforms of D-CRGD circuit. This circuit generates two output gate voltages which complement each other. V_{p1} and V_{p2} generate pulses for Q_1 and Q_2. At t_1, when switch Q_1 turns on, inductor current, i_{L1} develops. Q_2 is off at this time. Then, i_{L1} is charged exponentially to maximum value and so is the gate voltage of S_1, $v_{gs,S1}$ which is clamped to input source, V_s of 12 V. The time taken for i_{Lr} to reach maximum and its peak value are calculated using Eq. (38) and Eq. (39) respectively where i_{Lr}(t) is given in Eq. (32). When $v_{gs,S1}$ reaches its maximum value, i_{L1} starts to discharge through free-wheeling low impedance path, $Q_{2,bodydiode}$-L_1-D_1-V_{ca}. This discharged current depends on the time given for Q_1 conduction. In this case D is 0.20 and this value must be at least the sum of t_{rise} and

t_{rec}. If the time is insufficient, oscillation of the current will occur at the end of Q_1 turn-off, as shown in Figure 4.3. This result is not desirable as it leads to higher switching loss.

At t_2, Q_1 stops to conduct. After T_D of 15 ns ends, the switch Q_2 is turned on. At t_3, i_{L1} charges to maximum with negative value and $v_{gs,\ S1}$ is discharged to zero. Due to symmetrical behavior of the left and right circuits, at t_4, Q_3 starts to conduct. At this time, Q_2 is still conducting while Q_4 is off. With similar fashion as in Q_1 conduction, i_{L2} charges to maximum positive value and same goes to the gate voltage of S_2, $v_{gs,S2}$. The previously negative i_{L1} increases back to zero value at t_5 through D_2-L_1-$Q_{1,bodydiode}$-V_{ca} and i_{L2} is then discharged through $Q_{4,bodydiode}$-L_2-D_3-V_s at t_6. The duration of $v_{gs,S2}$ conduction is complement to $v_{gs,S1}$ which is D_{S2} as illustrated in Figure 4.17.

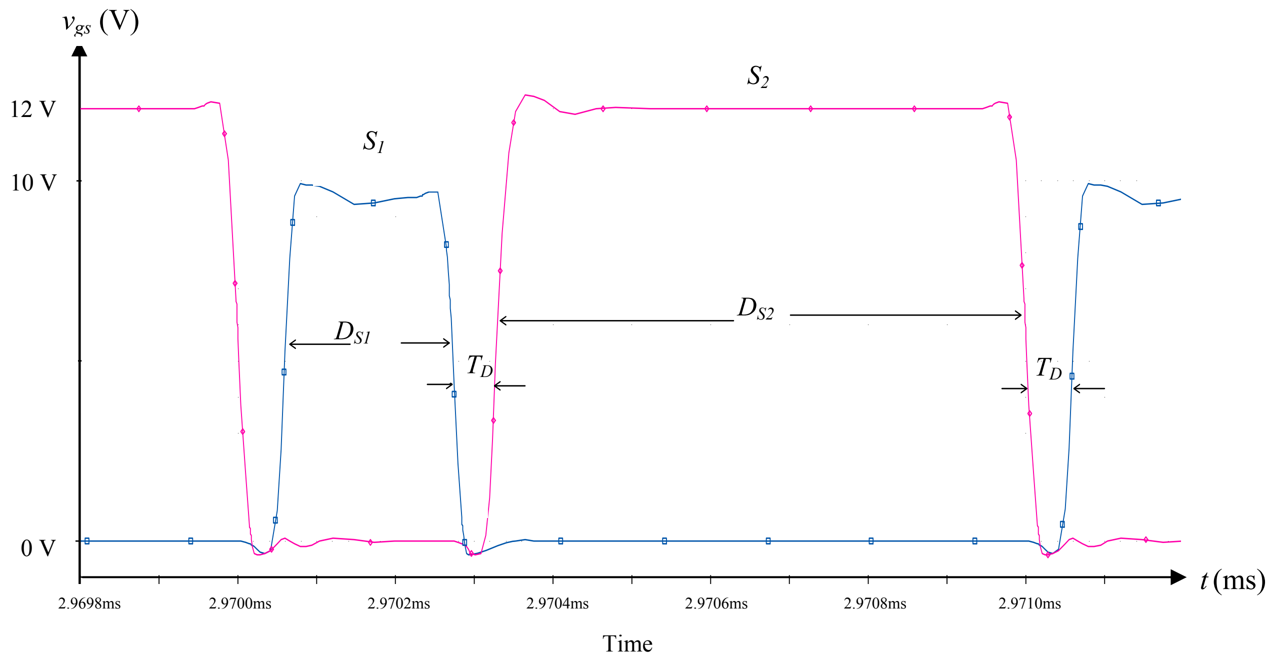

Figure 4.17 New SRBC 15ns Delay Switch Gate Pulse PSpice Simulation

The maximum of $v_{gs,S1}$ is clamped only about at 10 V with duty ratio, D_{S1}. On the other hand, $v_{gs,S2}$ goes to a maximum value of 12 V with D_{S2}. The value of $v_{gs,S1}$ should be equal to $v_{gs,S2}$ at 12 V in order to have balanced voltages. But because of the addition of C_x in the new SRBC circuit, there is a voltage drop of 1.7 V. Therefore, the simulation shows a result of $v_{gs,S1}$ = 12 – 1.7 = 10.3 V ≈ 10 V. The purpose of adding C_x to the circuit is to eliminate floating voltages at $v_{ds,S1}$ and $v_{ds,S2}$ during turn-off so that there will be less switching losses in the circuit. Since both $v_{gs,S1}$ and $v_{gs,S2}$ are not of the same amplitude, the internal capacitance, C_{iss} for both switches is not the same. C_{iss} can be obtained from the basic formula defined by the $Q = CV$. A lower gate voltage will draw less gate charge from the switch and vice versa.

The circuit operation can also be explained in terms of energy processing. When Q_1 is turned on, energy is transferred from the power source, V_s to the resonant inductor and the gate capacitor. When $v_{gs,Q1}$ reaches its peak, freewheeling of energy at inductor occurs. Then, the energy is returned back to V_s. Therefore, the D-CRGD demonstrates less power consumption compared to the conventional RG gate driver because of the energy recovery process.

The circuit operation during the discharging transition is as follows. When Q_2 is turned on, resonance takes place and the capacitive energy is transferred to the inductor. When i_{L1} starts to increase to the negative peak value, energy is merely freewheeling and finally, when the inductor current returns to zero, the inductor energy is also returned to the power source, V_s. The circuit shows resemblance of symmetry of a conventional gate driver. The Q_3-Q_4 operating conditions are identical to Q_1-Q_2 with the only difference in the switching intervals.

4.5 Operation of SRBC: Simulation Results

The new SRBC circuit shown in Figure 3.4 operates in ZVS condition. The S_2 switch has a longer conduction time compared to S_1. This is due to lower natural operation value of D_{S1} which results in high S_2 on-state loss hence the need to reduce the losses. Since the switches are conducting in complementarily manner configured by the D-CRGD circuit, they will not cross-conduct each other. During T_D, once S_1 is turned off, the circulating discharged inductor current, i_{Lo} at the load will flow into body diode of S_2 while it is yet in off condition. ZVS can be achieved here for this switch. However, S_2 has to be completely turned off before S_1 turns on. When S_2

conducts, it is expected that $S_{2,bodydiode}$ remains on. In the case of DCM operation, the negative load inductor current, i_{Lo} can be applied where it firstly turns on $S_{1,bodydiode}$ before the main body of the switch itself. Here, S_1 experiences ZVS condition leading to reduction of switching losses at S_1 [96].

In all conditions, S_1 has to turn on with a minimal stress. Here, S_1 must operate in ZVS due to the fact that the i_{Lo} variation in either DCM or CCM operation can alter the state of switching loss levels. In other words, S_1 is dominant in generating the most loss in the SRBC circuit. One way to solve this is by employing additional L_s and C_s components which are connected in parallel to S_1 [51]. The capacitor C_x is used to prevent floating drain voltage of S_1 while L_r and C_r are for ZVS operation of S_2 switch. Using this mode, both switches can now be operated in ZVS condition, leading to commutation of discharged i_{Lo} through $S_{2,bodydiode}$ and $S_{1,bodydiode}$ safely with an effectively lower switching loss. The operating gate and drain voltage as well as drain current waveforms of the new SRBC circuit are shown in Figure 4.18.

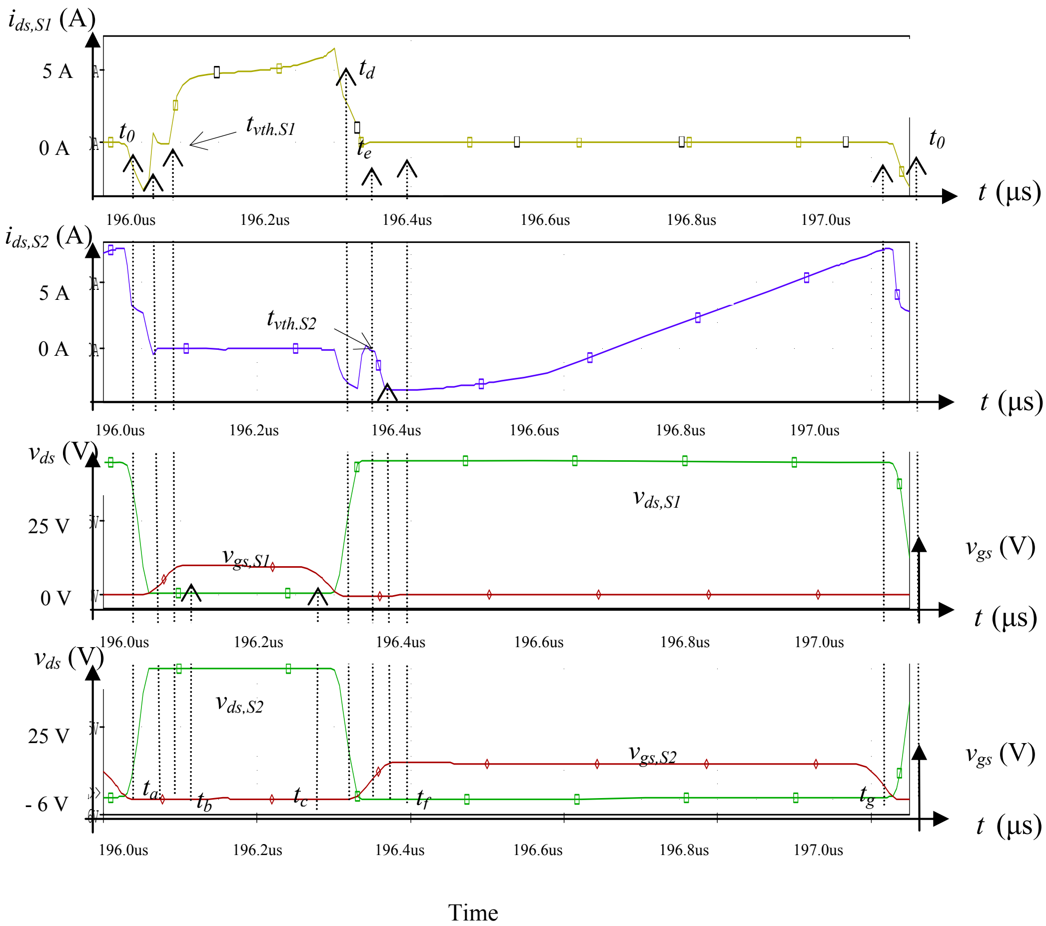

Figure 4.18 New SRBC Waveforms

There are seven modes of operation in the new SRBC circuit, shown in Figure 4.19. Mode 1 starts from the initial condition at $t < t_0$. The components used in the simulation are not ideal and they are based on actual specifications provided by the manufacturers. The figure shown is for steady-state condition. It is assumed that drain-source capacitances of S_1 and S_2 are the same. Initially, in Mode 1, S_1 is off and S_2 is conducting. All charging and discharging of capacitances and the flow of currents are shown in the figure. The diode seen in Figure 4.19 represents the body diode of the switch.

The mode of operation continues to Mode 2, $t_0 < t < t_a$ where S_1 and S_2 are off. Here, the T_D is set to be 15 ns. The output inductor current, i_{Lo} is operating in DCM, specifically in critical load condition. When S_2 in the previous mode is turned off during T_D, all i_{Lo}, i_{Lr} and i_{Ls} are constant. This can be clearly seen in Figure 4.20. However, the $i_{ds,S1}$ and $i_{ds,S2}$ are non-zero during this interval indicating the conduction of body diodes leading to a small portion of power loss. It is expected that in 1 MHz switching frequency, this loss is unavoidable but can be reduced with precise gate drive control scheme. The C_x continues to charge with the amount of $V_{in} - 2v_{ds,S1/S2}$. At the end of t_a, i_{Ls} starts to freewheel along the body diode of S_1 and the same time charges C_s. This leads to ZVS in S_1 where $v_{gs,S1}$ will only turn on once $v_{ds,S1}$ turns off. Thus, Miller's effect has been reduced significantly [97].

When S_1 starts to conduct, the negative current of $i_{ds,S2}$ which is at peak value will reduce to zero. During this Mode 3 ($t_a < t < t_b$), S_2 is still off. Here i_{Lr} and i_{Ls} increase in a linear fashion and hence charge C_r and C_s respectively. i_{Lo} is also charging up L_o. On the other hand, C_x is charged to its maximum value. In the complementarily operated mode of SRBC circuit, obviously $v_{ds,S2}$ must swing at maximum V_{in} value and $v_{ds,S1}$ at this interval should be zero. This is due to the freewheeling phase of $i_{ds,S1}$ which makes $v_{gs,S1}$ first reach zero before $\mathrm{v}_{ds,S1}$ becomes high.

When $v_{gs,S1}$ reaches its threshold value at $t_{vth,S1}$, $i_{ds,S1}$ starts to develop exponentially until maximum. This current will circulate through L_s and C_s which brings theoretically an additional forward voltage drop of 0.7 V in S_1 leading to $V_{gs,S1}$ of 12.7 V. However, this value is not seen in the simulation. $v_{gs,S1}$ continues to increase to 12 V and remains constant in Mode 4 ($t_b < t < t_c$).

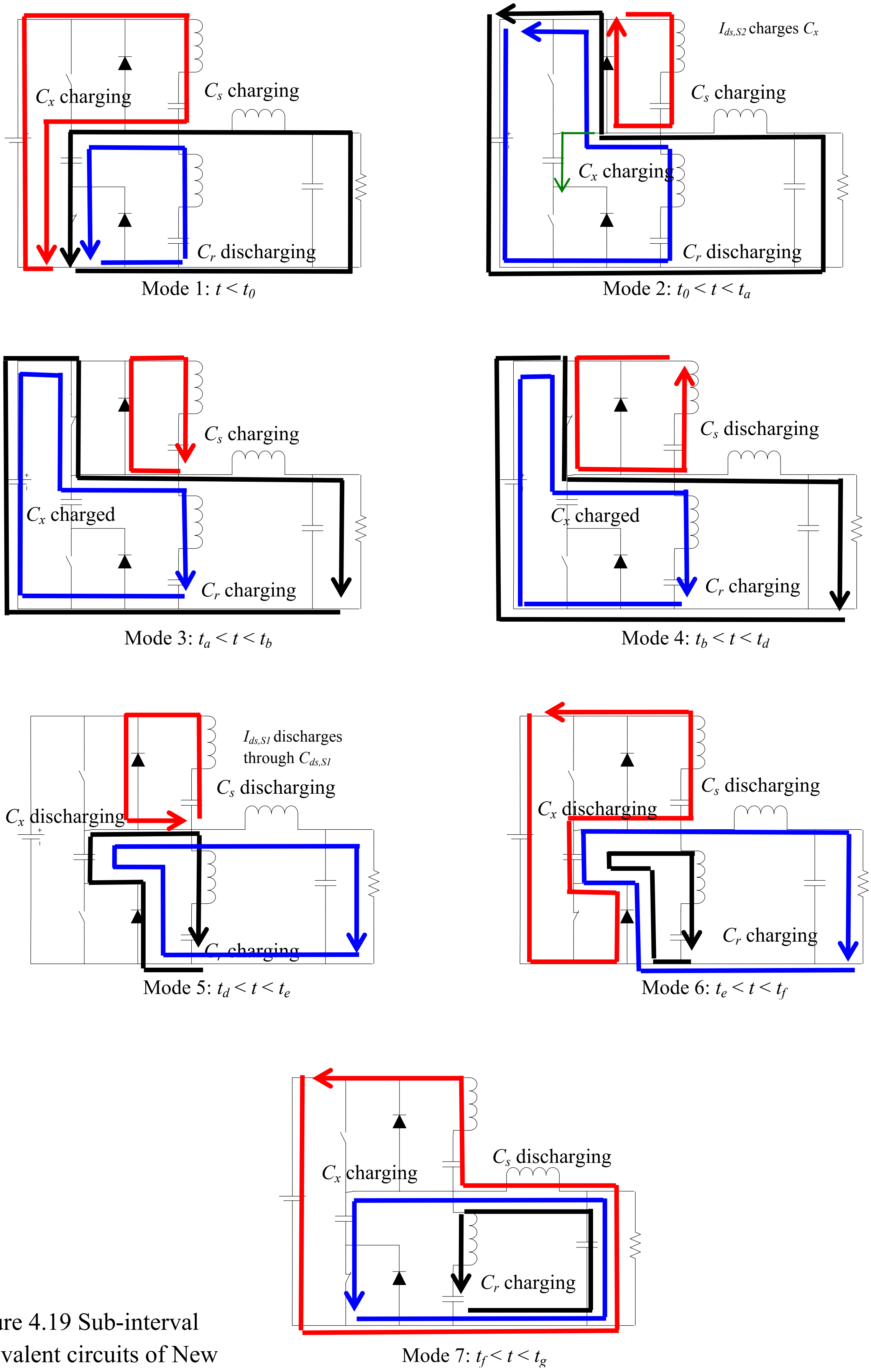

Figure 4.19 Sub-interval equivalent circuits of New SRBC

At t_d, $i_{ds,S1}$ will reach the peak value and this occurs when S_1 stops conducting. On the other hand, S_2 is not yet turned on which indicates the T_D interval. During Mode 5 ($t_d < t < t_e$), both drain voltages of S_1 and S_2 are conducting. Here, $v_{ds,S1}$ increases and $v_{ds,S2}$ decreases. This reflects the decreasing pattern of conducting $i_{ds,S1}$ and $i_{ds,S2}$. C_x is now discharged to zero giving the momentarily rise of $i_{ds,S2}$ before reducing back to zero. As a result, V_{Cx} will be withdrawn from the gate voltage of S_1 which gives result in lower peak $v_{gs,S1}$ value of only 10 V during turn-on.

In Mode 6 ($t_e < t < t_f$), $i_{ds,S1}$ is now turned zero. However, due to the decrease of $v_{ds,S2}$ and an increase of $v_{ds,S1}$ at the same time, this makes $i_{ds,S2}$ decrease to maximum negative value. This clearly shows the similar pattern for $i_{ds,S1}$ and $i_{ds,S2}$ for both T_D intervals. The next sequence shows switch S_2 where it starts to conduct causing $i_{ds,S2}$ back to zero at $t_{vth,S2}$. This current will again get back to its previous state before increasing to maximum when S_1 is off, leading to zero $i_{ds,S1}$.

In Mode 7 ($t_f < t < t_g$), S_2 is fully turned on and S_1 is off. $i_{ds,S2}$ increases linearly as C_x is charged again. However, C_s is discharged back through L_s-V_{in} path. Here, $v_{ds,S2}$ is kept constant at V_{in} until t_g where S_2 then starts reducing the value back to zero at t_0, signaling the decreasing $i_{ds,S2}$ and $v_{ds,S1}$ from the peak and V_{in}, respectively. Then the circuit continues the next switching cycle with the same operating condition.

Figure 4.20 shows the inductor currents of the new SRBC circuit. The L_sC_s and L_rC_r pairs are used to commutate i_{Lo} from $S_{2,bodydiode}$ to $S_{1,bodydiode}$ effectively during T_D. Basically the roles of both LC pairs are the same. It can be seen that during T_D, drain voltage signals for both switches operate in exact complementarily fashion. This will minimize the diode conduction losses. Furthermore, L_s and L_r help charged and discharged $i_{ds,S1}$ and $i_{ds,S2}$ to freewheel completely in each of the switch's conduction cycle, and hence reduce the switching losses.

There are four ZVS points as indicated at t_0, t_a, t_d and t_e which indicate a minimal or zero cross conduction seen at the intersection points between the drain and gate voltages. More importantly, the $v_{ds,S1}$ is not floating. A non-zero value makes the whole turn-on duration of S_1 experiencing a higher switching loss and eventually increasing the body diode conduction loss.

Using this new SRBC circuit, switching loss during entire S_1 turn-on interval can be fully diminished where $v_{ds,S1(on)}$ is reducing to zero.

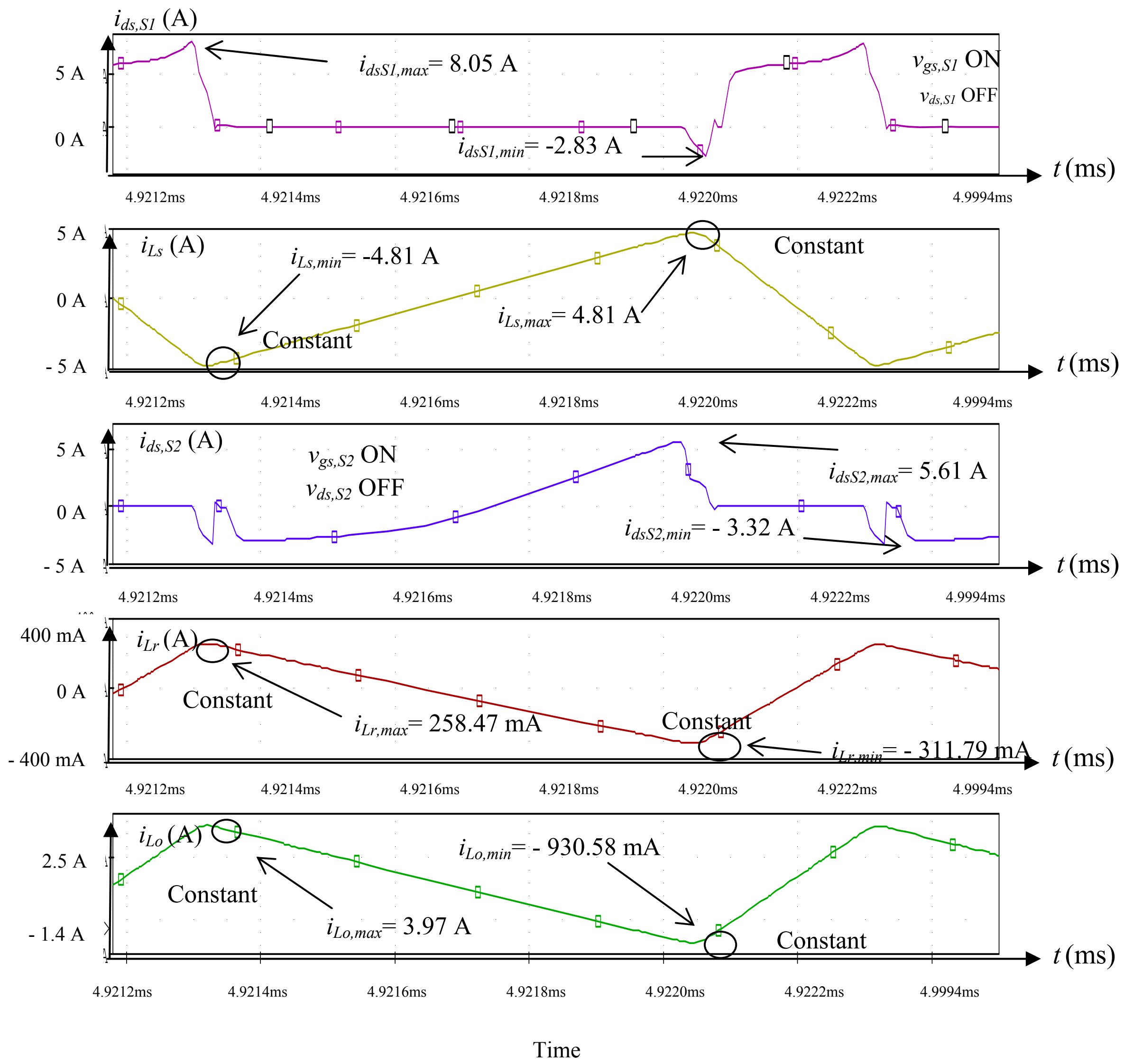

Figure 4.20 Currents of New SRBC Circuit

The output inductor peak current, $i_{Lo,max}$ is much larger than $i_{Ls,max}$ and $i_{Lr,max}$, indicating the criterion to achieve ZVS condition [95]. The drain voltage floating issue has been resolved by maintaining zero voltage during S_1 turn-on. A capacitor C_x is added in series with S_2 to lower S_1 gate voltage of new SRBC circuit. This does not affect the operation of new SRBC circuit where the only difference is the amount of gate charge used in the calculation of S_2 switching loss is higher. The output voltage at the load is only fluctuating with fewer ripples. Interestingly, even though extra components are added, the switching losses and body diode conduction losses are reduced. However, the peak i_{Lo} value is slightly reduced at the output of new SRBC circuit.

4.5.1 Resonant Configuration of New SRBC Circuit

The configuration of inductor and capacitor forms a resonant circuit which acts as a filter to decrease the switching losses in the circuit. From the new SRBC circuit, two LC resonant filters can be identified as shown in Figure 4.21.

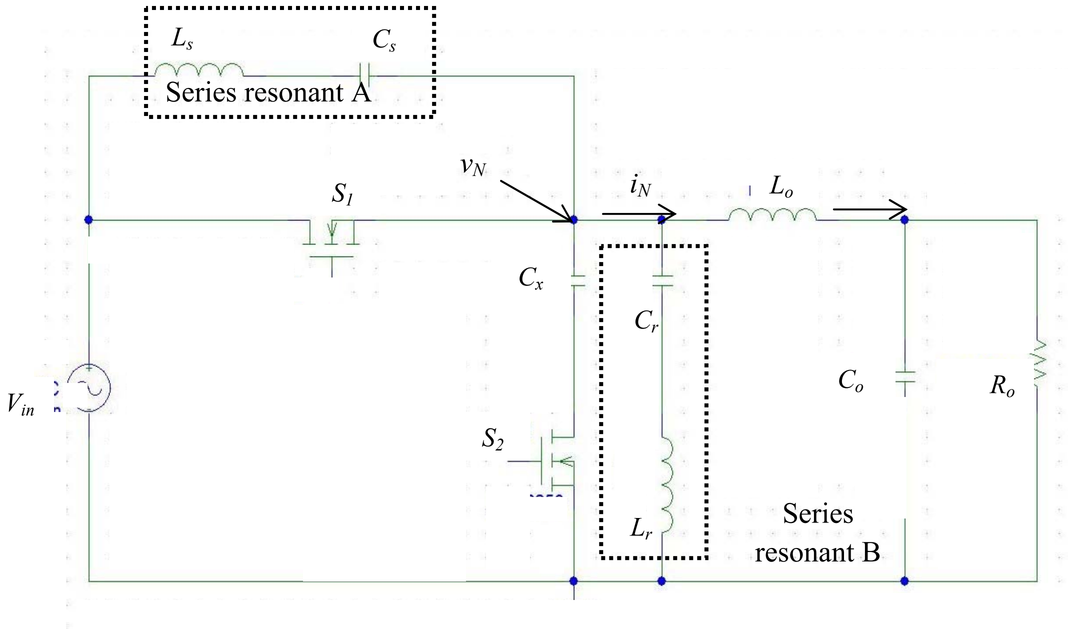

Figure 4.21 Series Resonant of New SRBC Circuit

There are two series connected resonant circuits: one is connected in parallel to S_1 and the other parallel to S_2. The study is only concentrated in the case of un-damped condition.

In summary, during turn-on of switches, the resonant current and voltage for the series and parallel network are given in Eq. (44) and Eq. (45) respectively.

LC series network:

$$i_L(t) = I_{L0}\cos\omega_0(t-t_0) + \frac{V-V_{c0}}{Z_o}\sin\omega_0(t-t_0) \tag{44}$$

$$v_c(t) = V - (V-V_{c0})\cos\omega_0(t-t_0) + Z_o I_{L0}\sin\omega_0(t-t_0) \tag{45}$$

For network A, $V = V_{in}$ and for B, $V = v_N$

In the resonant switching circuit, inductor smoothens the current passing through it while the capacitor reduces the voltage ripple content. The combined LC switching aid network therefore reduces the ripple in the output to a lower level. The chief advantage of the resonant converters is reduced switching loss. Because turn-on or turn-off transitions of the switches occur at zero crossing of the voltage waveform, it reduces or eliminates some of the switching loss [48]. Therefore, resonant converters can operate at higher switching frequencies. ZVS also reduces the switching stress and converter-generated EMI, consequently lowers the switching power losses.

4.6 New SRBC Circuit: Experimental Results

The circuit was constructed on PCB and the experiment was done in the lab following the component selection based on Table 3.5. The S_1 and S_2 switches are of the same type of high power MOSFETs as used in the RGD experimentation: IRFI540NPBF. Both gates of S_1 and S_2 are driven by the D-CRGD circuit as shown in Figure 3.3. With the load fixed at 10 Ω, the measurements were taken, compared with the simulation results and analyzed.

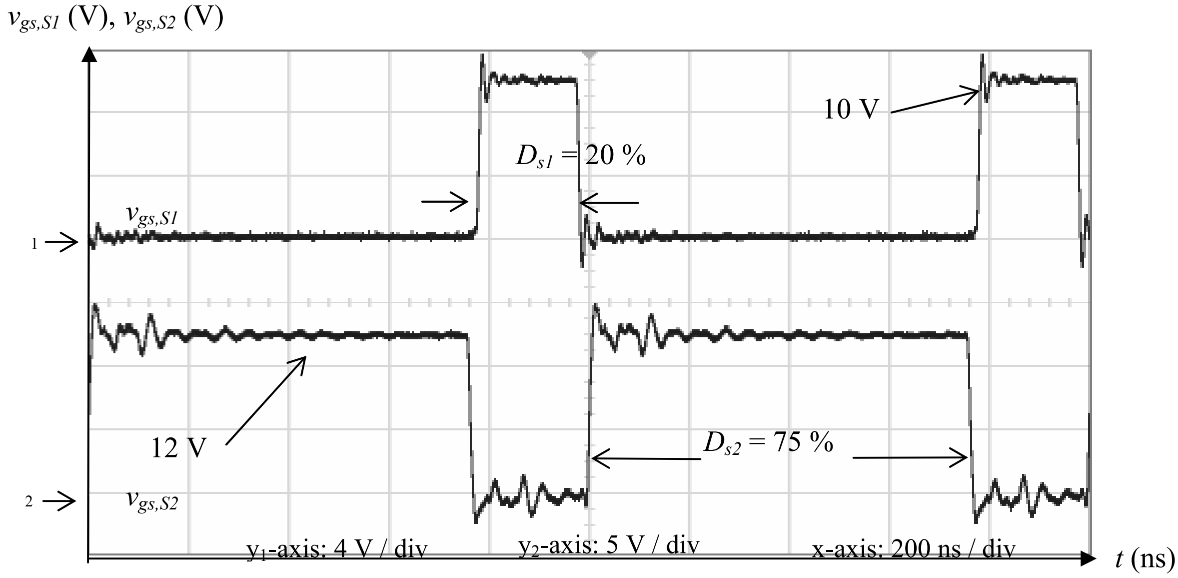

Figure 4.22 Gate Voltages of S_1 and S_2 Experimental Waveforms of New SRBC

The two complementary pulses for S_1 and S_2 are shown in Figure 4.22. It clearly shows that the duty ratio, D of S_1 is 0.20 and S_2 is supposed to be 0.80. However, due to the insertion of T_D of 15 ns, this makes up the squeeze in S_2 pulse width of only 0.75. There are some ripples seen during the forward turn-on voltage and during turn-off in S_1. In addition, S_2 gate voltage pulses contain more ringing due to the recovery transient process during T_D. Nevertheless, the results indicate low rippled voltage swings in both pulses.

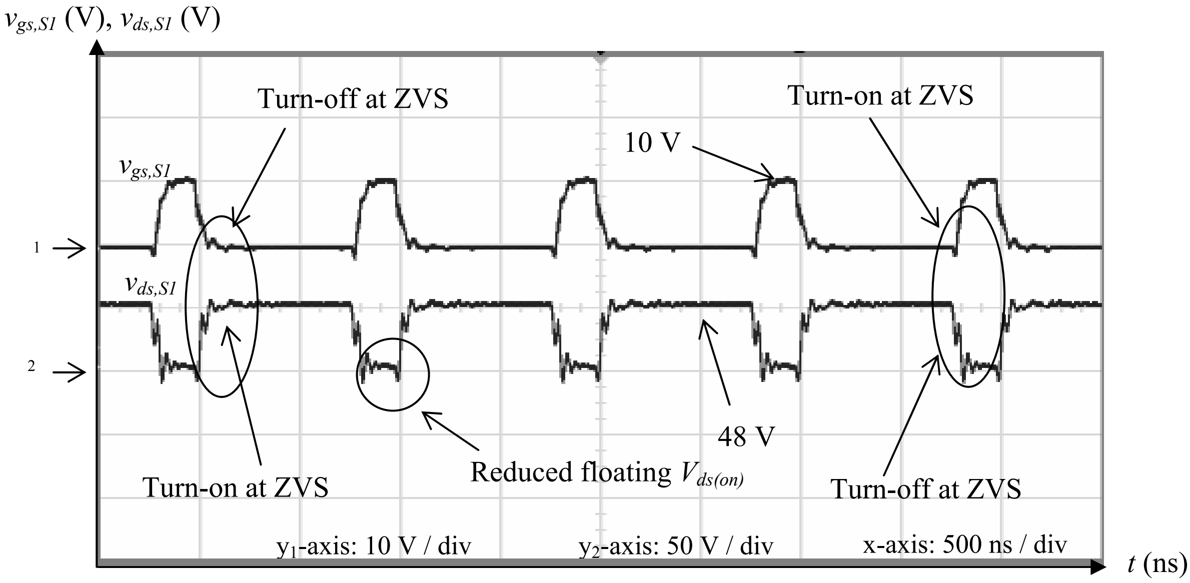

Figure 4.23 Gate and Drain Voltages of S_1 Experimental Waveforms of New SRBC

In the new SRBC circuit, the turn-off drain voltages of S_1 and S_2 are minimized to zero. This eventually leads to a significant reduction in switching loss. Equation (18) shows how the loss can be reduced. For example, if we look at the entire turn-on switching interval, there will exist non-zero power dissipation in between turn-on and turn-off intersection of i_{ds} and v_{ds} waveforms. Adding all these will definitely increase the total switching loss in the device. Clearly, if $V_{ds(on)}$ is further reduced, thus the switching loss will decrease.

The gate voltage peak value of S_1 is only approximately 10 V due to the difference in charged capacitance, C_x of 1.3 - 2 V to solve floating drain voltage issue. On the other hand, $V_{gs,S2}$ remains at 12 V-peak. It is also interesting to observe that the turn-on/turn-off transition and vice versa shown in Figure 4.23 are operating successfully in ZVS mode. This proves that the new SRBC circuit can reduce power losses in the switches.

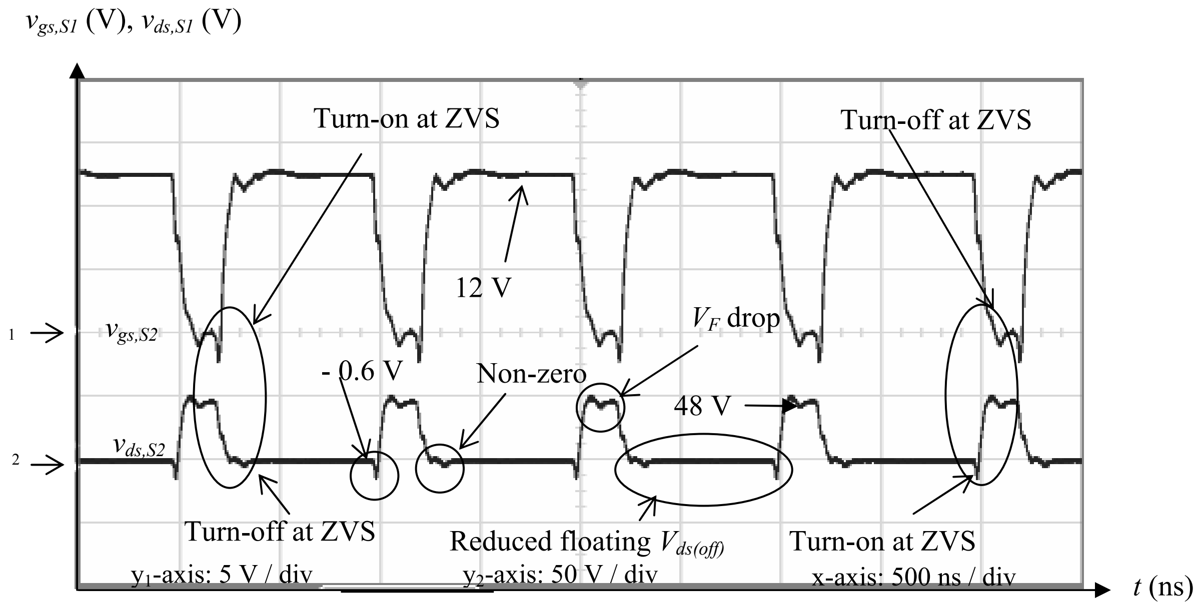

Figure 4.24 Gate and Drain Voltages of S_2 Experimental Waveforms of New SRBC

The same operating conditions of v_{ds} and v_{gs} of S_2 are seen in Figure 4.24. Remarkably, the $V_{ds(off)}$ has also been reduced close to zero. The ZVS mode shown does not perform as good as in S_1 since the free-wheeling load current during T_D takes a longer time to charge through C_x as indicated in Mode 5. Nevertheless, the ZVS operation is working properly in spite of a little forward voltage drop during turn-on of $v_{ds,S2}$. This is due to loop parasitic inductor to form a resonant circuit with C_{oss} of S_2. Apparently, before the turn-on of $v_{ds,S2}$, there is a small negative voltage drop of -0.6 V which is common in the operation of the switch. However, its turn-off is positive, indicating a reduction in body diode conduction loss in S_2.

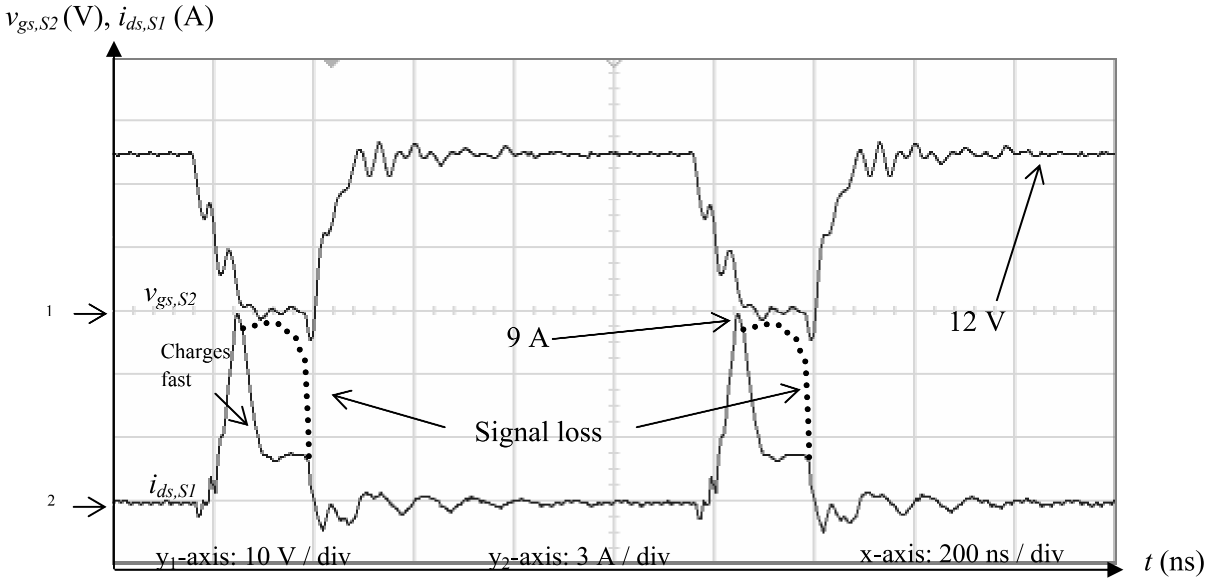

Figure 4.25 Gate Voltage of S_2 and Drain Current Experimental Waveforms of S_1 of SRBC

The drain current of S_1 in Figure 4.25 shows the charging operation during its turn-on. The i_{ds} charges rapidly to maximum as S_1 turn on. This increases the switching speed with the cost of slightly higher overshoot to 9 A from the simulated value of 8 A. Once it is at peak, the L_s increases the discharging of i_{Ls} and bringing $i_{ds,S1}$ to a new value of about one-third of its peak during resonant indicated as signal loss (dotted line). The loss portion of this current will flow to the body diode of both switches leading to a small loss in body diode conduction during T_D. This is an unsatisfactory result in which more work has to be done to rectify this issue.

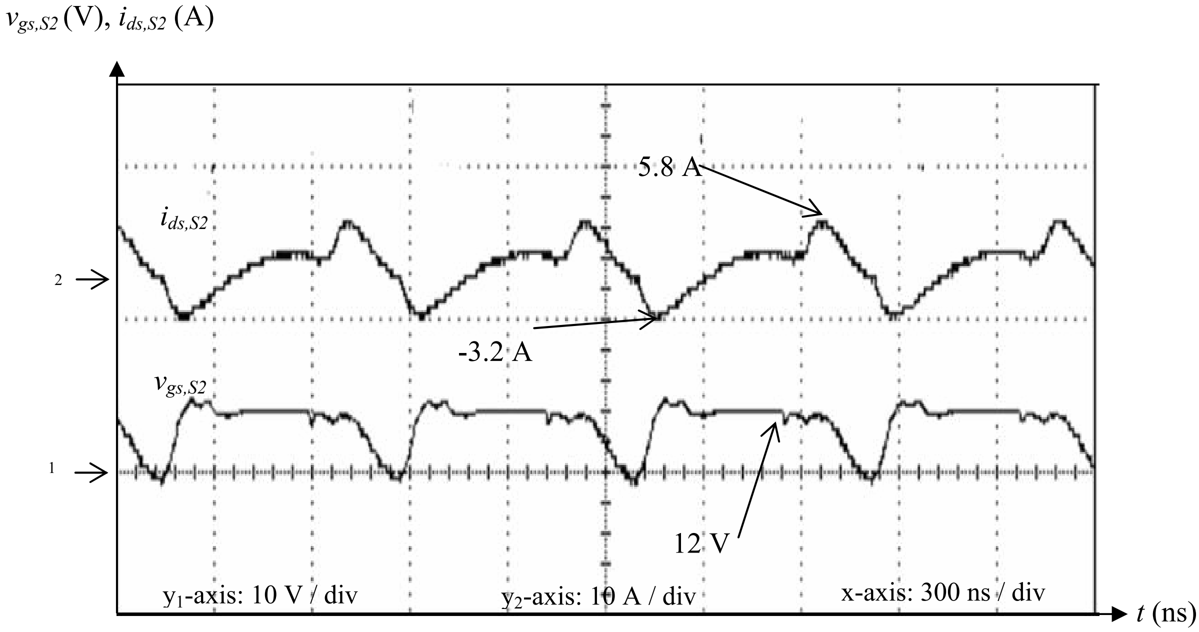

Figure 4.26 Gate Voltage and Drain Current Experimental Waveforms of S_2 of New SRBC

Figure 4.26 shows the $i_{ds,S2}$ waveform with respect to S_2 switch. Comparing with the simulated waveform in Figure 4.18, it is clearly proven that $i_{ds,S2}$ will continue to discharge even though S_2 is already turned off. Despite to the impact of loss portion in $i_{ds,S1}$ signal, the $i_{ds,S2}$ will continue flowing in S_2 body diode producing a small amount of body diode conduction loss. Apparently, this loss is inevitable in high frequency operation and not easy to reduce entirely.

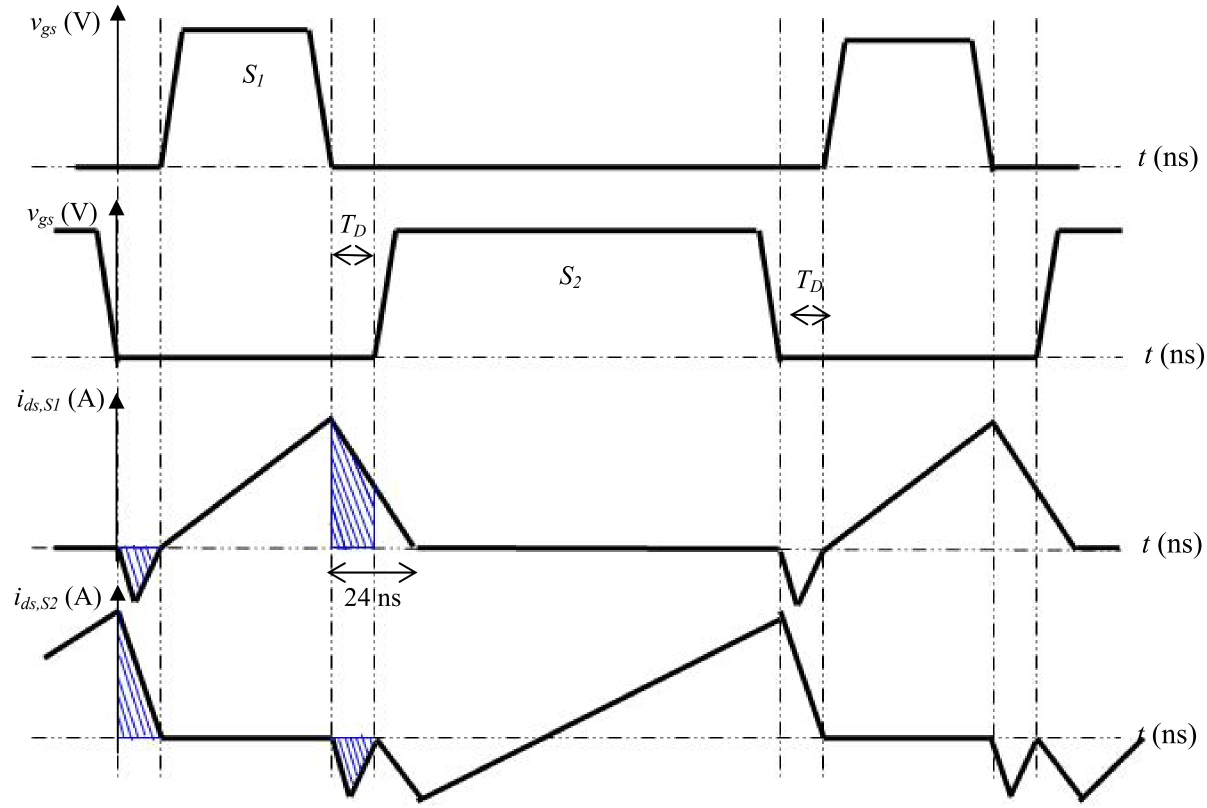

Figure 4.27 Body Diode Conduction of New SRBC

The waveform of body diode conduction loss is redrawn based on simulation work as shown in Figure 4.27. Interestingly, even though the body diode conducts, it only takes about 24 ns and the total shaded areas in Figure 4.27 indicate the amount of losses of approximately 25.7 mW. This result explains why $i_{ds,S1}$ and $i_{ds,S2}$ behave in such manner as shown in the waveforms obtained in the experimental setup.

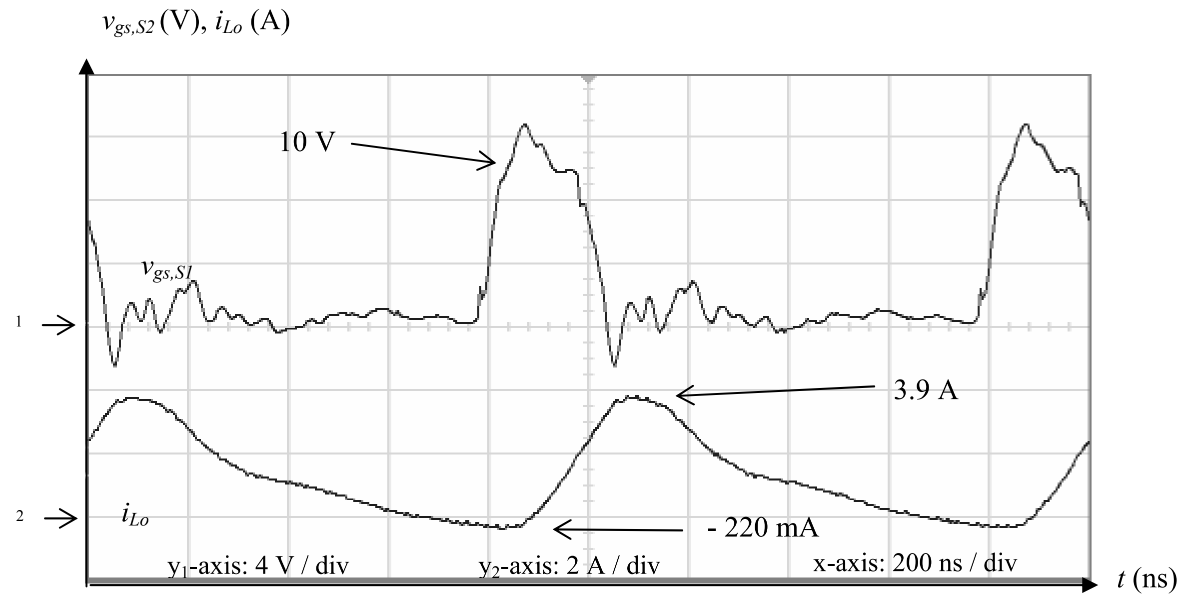

Figure 4.28 Gate Voltage of S_1 and Inductor Current Experimental Waveforms of New SRBC

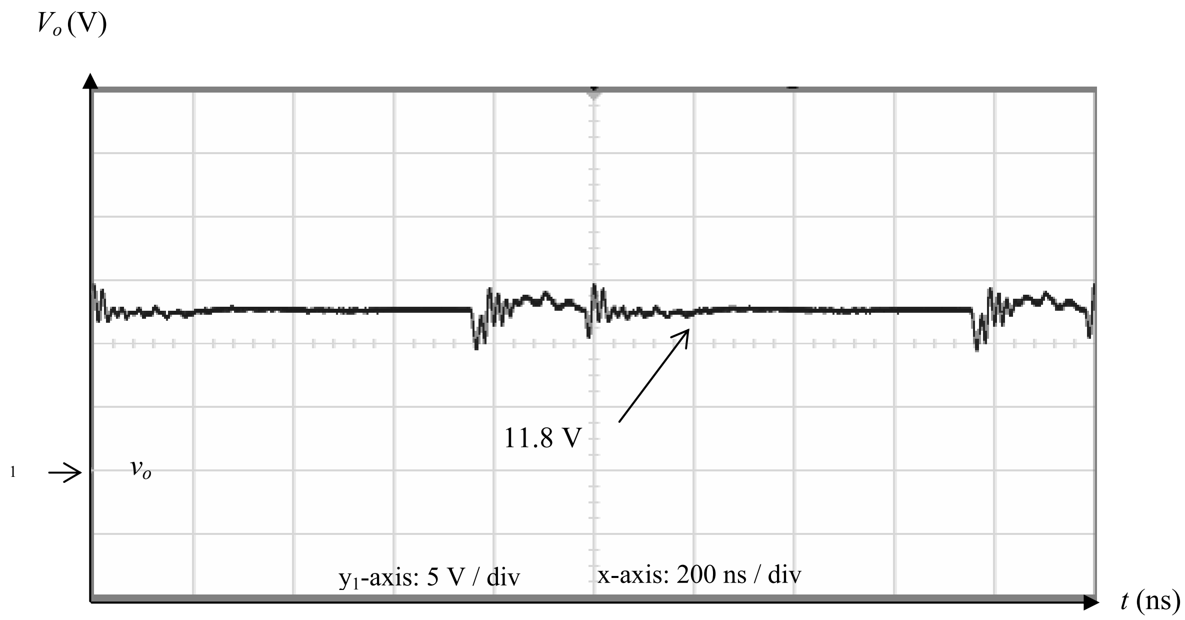

Figure 4.29 Output Voltage Experimental Waveform of New SRBC

Figure 4.28 and Figure 4.29 show the experimental results where i_{Lo} operates in accordance to S_1 switching. The output voltage is also about the value as found in the simulation that is 9.6 V.

Table 4.3 New SRBC: Comparison of Simulated and Experimental Results

Parameters	Simulation	Experiment	% Diff
$i_{ds,S1(peak,max)}$ (A)	8.05	9.0	10.56
$i_{ds,S2\ (peak,max)}$ (A)	5.61	5.80	3.28
$i_{ds,S2\ (peak,min)}$ (A)	- 3.32	- 3.20	3.75
$i_{Lo\ (peak,max)}$ (A)	3.97	3.90	1.79
$i_{Lo\ (peak,min)}$ (mA)	- 930.58	- 220	BIG Δ
V_o (V)	10.6	11.80	10.17

In summary, the differences in simulation and experimental results are tabulated in Table 4.3. The experimentally measured of i_{Lo} minimum peak is lower than the simulated result. This is obviously caused by higher output load total resistance generated within the wire resistance in circuit board and measurement tools. The rest of the data differ within only 5 % of each other.

4.7 Chapter Summary

The optimization of S-CRGD reveals the limiting parameter values which are later applied in D-CRGD circuit. In addition, the Q-factor of S-CRGD has been determined in the simulation and this value is verified. The new SRBC employ D-CRGD as the gate drive in order to generate low switching loss operating in ZVS-boundary DCM condition. In fact, the on-state drain voltages of S_1 and S_2 have also been reduced leading to the reduction in entire turn-on switching losses.

CHAPTER 5

EXTENDED SIMULATION WORK: RESULTS AND DISCUSSIONS

5.1 Chapter Overview

Upon completing the experimental work, the study continues on the investigations of different SRBC topologies in terms of their switching losses and effect on load variations. In addition, the new SRBC circuit has undergone further analyses in varying T_D and f_s. Also since the driving switches have to operate effectively in megahertz environment, their gate drive control schemes have to be evaluated for optimum SRBC circuit performance.

5.2 Switching Loss Analysis and Loading Effects of Three SRBC

Three different SRBC circuit configurations are investigated in the simulation. All of them use the same D-CRGD circuit shown in Figure 3.3 for consistency in the analyses. The new SRBC circuit (Figure 3.4), the conventional SRBC (Figure 2.11) and the SRBC proposed by [51] (Figure 5.1) are compared and their switching losses are calculated. In addition, the ZVS capability of S_1 and S_2 switches are studied during their switching transitions. Using a fixed load of 10 Ω, the work will also look at the output load currents, i_{Lo}, voltages, v_o and output power of the converter.

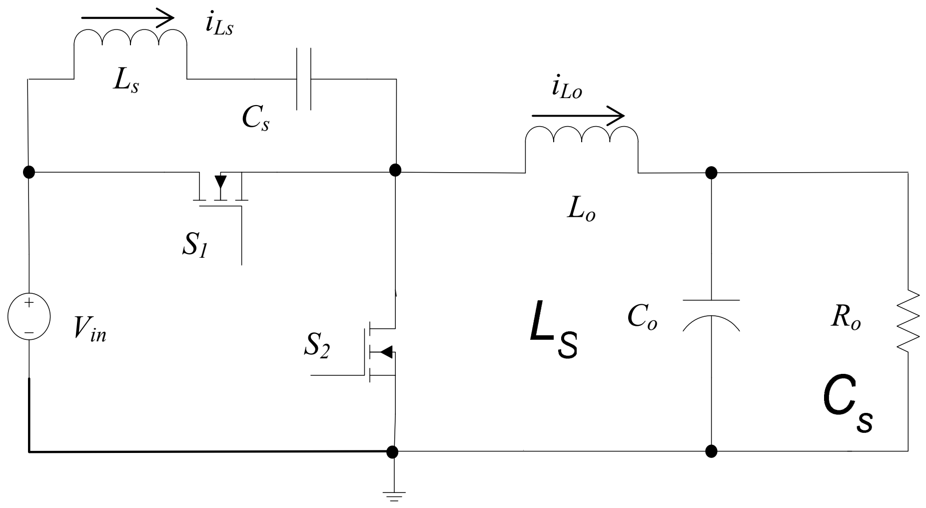

Figure 5.1 SRBC [51]

5.2.1 Switching Loss Analysis

Figure 5.2 shows the turn-off switching losses of all three SRBC circuits for S_1 switch. All of them are studied in terms of their switching losses. In this work, they are simulated using the same D-CRGD circuit topology in Figure 3.3 for the purpose of consistency in the analyses. Conventional SRBC circuit shown in Figure 2.10 presents a mismatch in drain voltage switching transitions during turn-off or turn-on for S_1 and S_2. The new SRBC is referred to Figure 3.4 and the other developed by [51] is shown in Figure 5.1. The switching losses are tabulated in Table 5.1

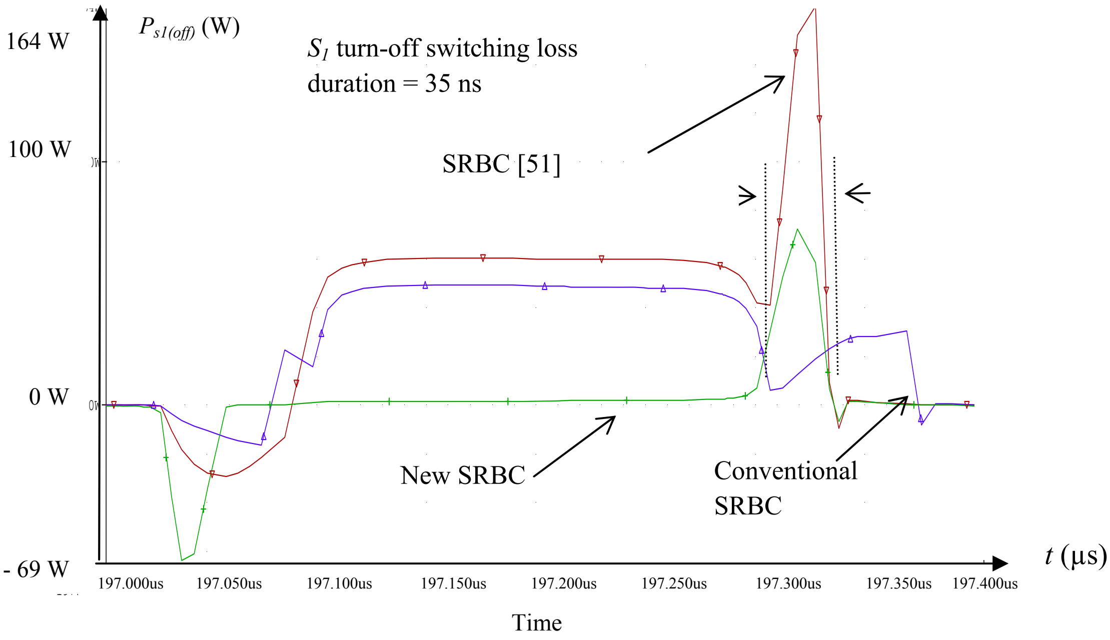

Figure 5.2 Simulated Turn-Off Switching Loss of Three Different SRBC

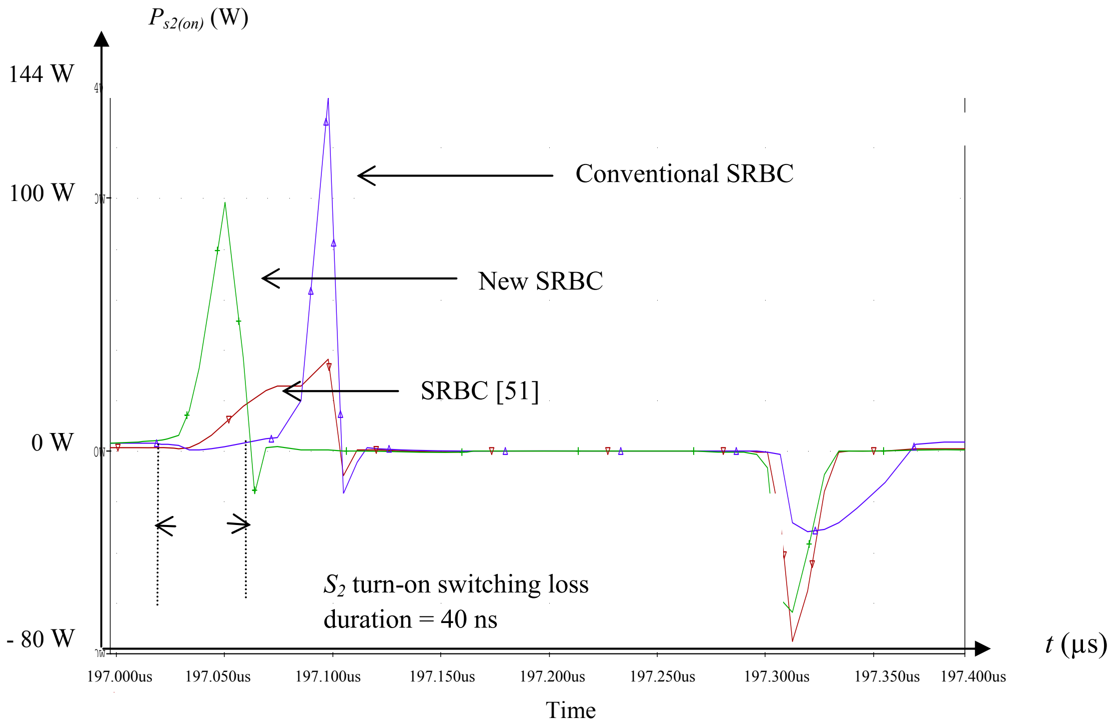

Figure 5.3 Simulated Turn-On Switching Loss of Three Different SRBC

Table 5.1 Comparison of Simulated Switching Losses of SRBC at 10 Ω-Load

Parameters Analyzed	**SRBC [51]**	**New SRBC**	**Loss savings**
S_1 Turn-off Peak V_{ds} * I_{ds} (Figure 5.2)	164 W	65 W	60 %
S_1 Turn-off Switching Losses	2.87 W	1.138 W	60 %
S_2 Turn-on Peak V_{ds} * I_{ds} (Figure 5.3)	-	95 W	-
S_2 Turn-on Switching Losses	-	1.10 W	-

The SRBC [51] is re-simulated using 1-MHz switching frequency and the results are compared. Comparing the turn-off switching loss of S_1, the new SRBC circuit shows an improvement of 60 % in loss savings with the expected reduction in turn-on switching loss. Turn-on switching losses for Figure 5.1 are not able to be measured due to the transient mismatch. In addition, looking from Figure 5.3, high peak power with respect to thermal management of S_1 for Figure 2.10 and Figure 5.1 during turn-on interval is observed in the simulation.

The ZVS behavior during turn-on and off is also important in determining the performance and reliability of the SRBC circuit. Figure 5.4 to Figure 5.6 show the v_{gs} and v_{ds} waveforms for all three SRBC circuits. Based on the parameter settings used, it is determined that the circuit introduced in [51] does not comply entirely with the ZVS condition and in addition, there exists a floating drain voltage of S_1, leading to high switching losses during its turn-on switching cycle. These losses also occur in the conventional and not in the new SRBC circuit.

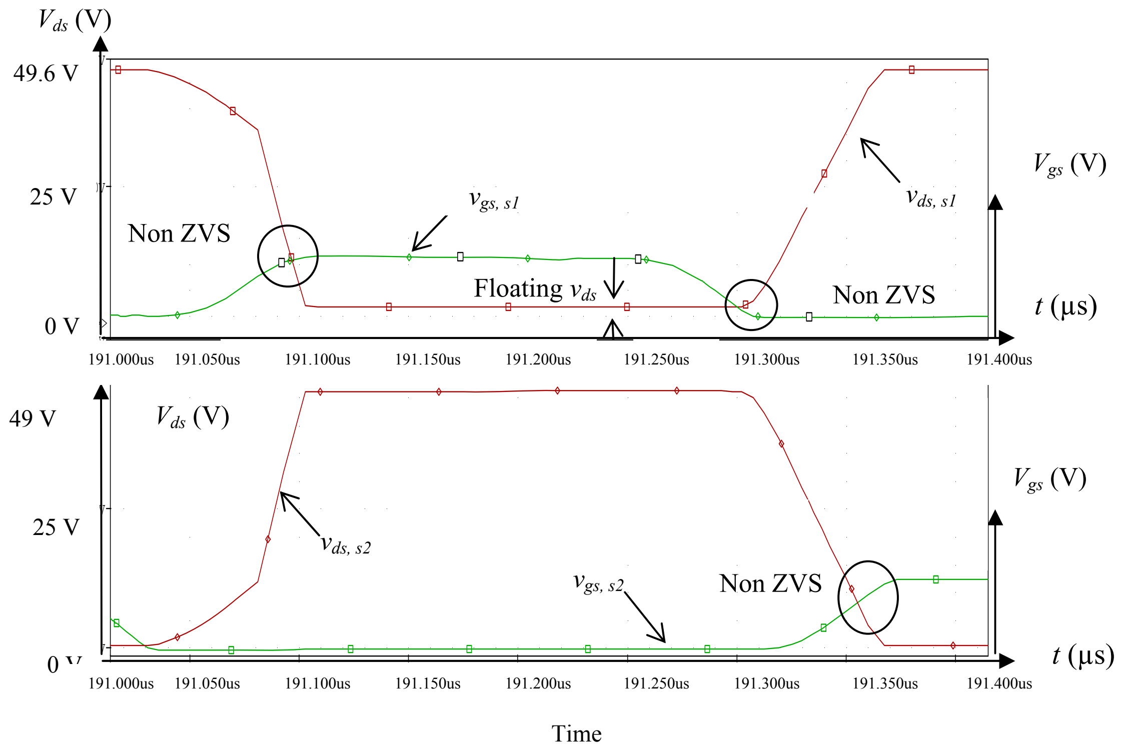

Figure 5.4 Simulated Gate and Drain Voltages of Conventional SRBC

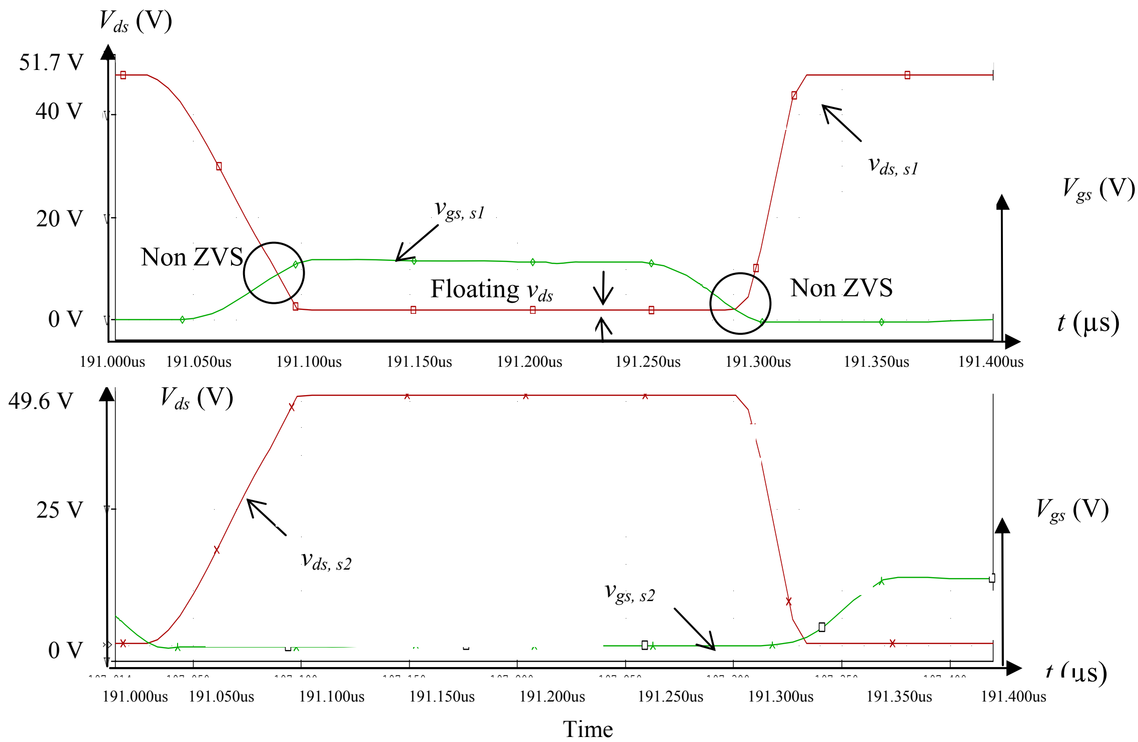

Figure 5.5 Simulated Gate and Drain Voltages of SRBC [51]

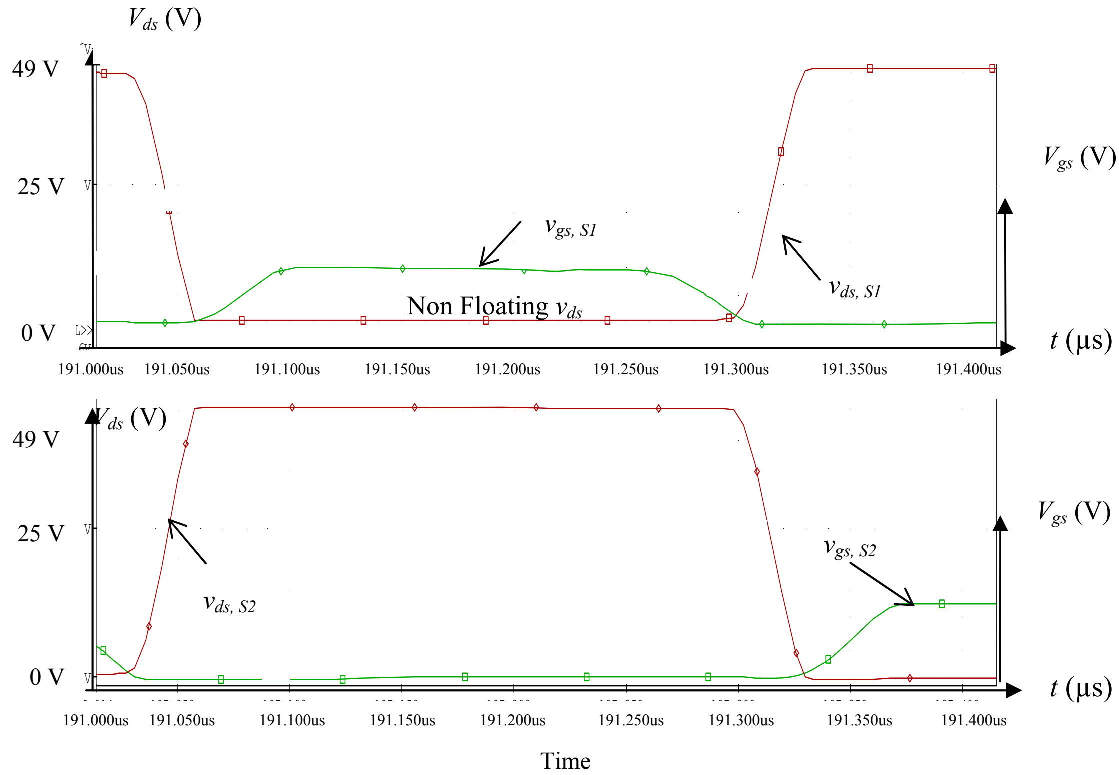

Figure 5.6 Simulated Gate and Drain Voltages of New SRBC

The next analysis discusses the i_{Lo} performance in the SRBC circuit. Figure 5.7 shows i_{Ls}, i_{Lr}, and the three i_{Lo} currents which correspond to V_{gs} of S_1 and S_2. The additional LC configuration which is connected in parallel with S_2 in the D-CRGD circuit slightly influences the i_{Lo} of the SRBC. This is true since an additional current is branched out from the source to the node leading to a drop in i_{Lo} at the load. Comparing with Figure 5.1, i_{Ls} peak in the new SRBC circuit drops 11 % from 5.41 A to 4.81 A and only 3.4 % (4.11 A to 3.97 A) in the i_{Lo}. Nevertheless, the new SRBC circuit operating in DCM has shown an improvement of switching losses in S_1 and S_2 despite the drop in i_{Lo}.

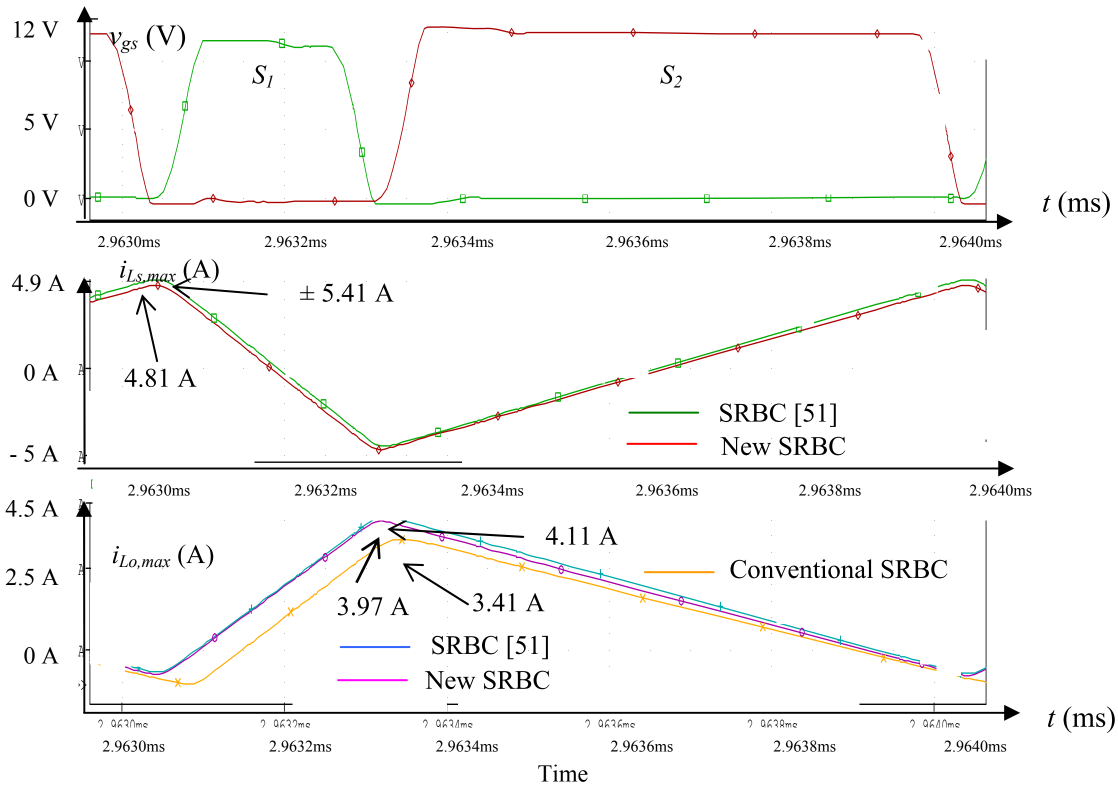

Figure 5.7 Comparison of i_{Ls} and i_{Lo} of Three Different SRBC

Therefore, design compromise has to be made between switching losses and peak i_{Lo} current at the load. With D-CRGD circuit, i_{Lo} is charged and discharged with constant peak value. As a result, the switching time can be reduced leading to lower switching losses. In addition, more power savings in the body diode conduction losses are achieved in S_1 and S_2 during T_D.

5.2.2 Loading Effects Analysis

All SRBC circuits should have the ability to operate in variable load resistance efficiently. In the design where fixed load resistance is used, the level of certain efficiency can be achieved. However, varying load resistances in the SRBC circuit will cause switching loss to vary in S_1 and S_2 as well. This is due to the variation in i_{Lo} that commutates along the S_2 body diode during T_D. In this case, more i_{Lo} has to commutate and a longer time is required to freewheel along the S_2-load path and vice versa. Therefore, this will eventually give impact on the design of D and T_D intervals between switches of the resonant gate drive circuit. The three SRBC topologies are further investigated in terms of their abilities in handling varying load resistances.

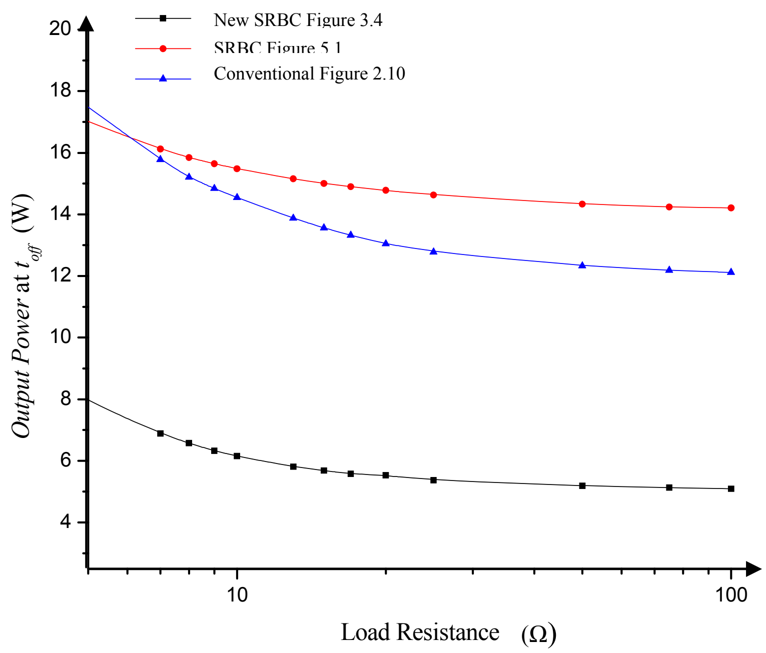

Figure 5.8 Average Turn-Off Power Loss of S_1 at Different Load Resistances

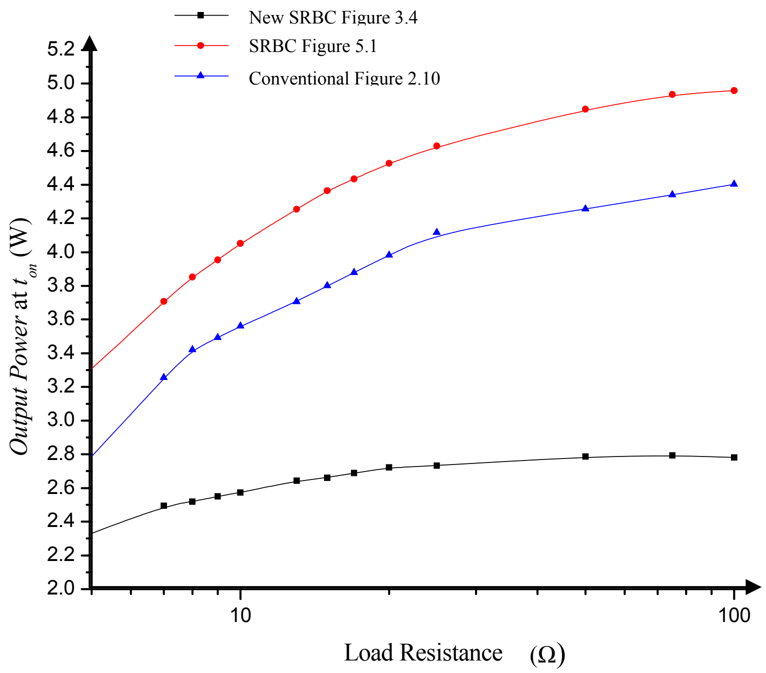

Figure 5.9 Average Turn-On Power Loss of S_2 at Different Load Resistances

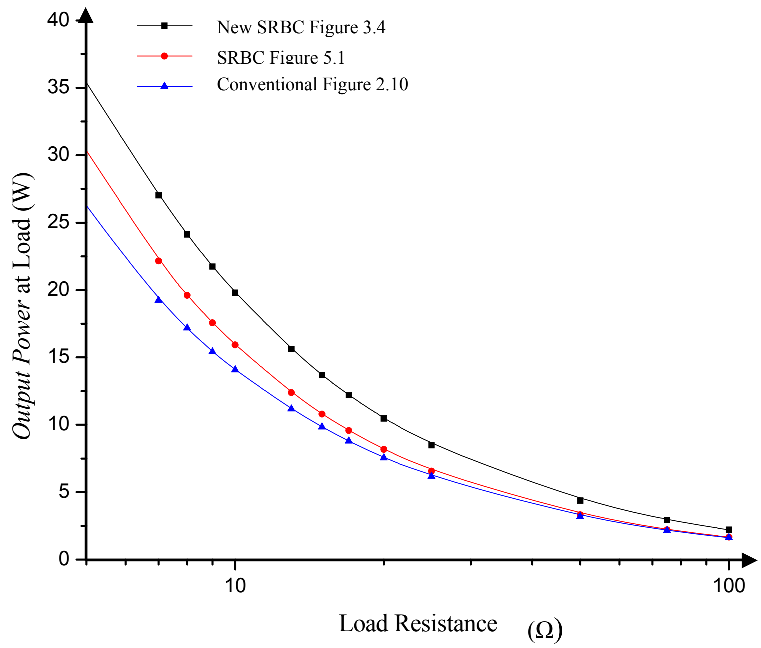

Figure 5.10 Average Load Output Power at Different Load Resistances

Figure 5.8 and Figure 5.9 show the average switching loss of S_1 and S_2

respectively for different load resistance values. Both graphs clearly show that the new SRBC circuit has reduced switching loss significantly. At the same time, the average output power at the load has also been improved significantly, as shown in Figure 5.10.

Taking the load resistance of 10 Ω, the numerical data is tabulated in Table 5.2. This is load resistance value chosen for the experimental validation purposes. However, if the inductive load is used, the average output voltage is normally half of resistive load.

Therefore, in order to evaluate the significant of output load, the suitable application has to be given. In this case, the output power is only 15.9 W at 10 Ω due to the nature the application which is the battery charger, (9.5 V / 1.5 A).

Table 5.2 Average Switching Loss and Output Power of SRBC at 10 Ω Load

Parameter Analyzed	**New SRBC**	**SRBC [51]**	**% Diff.**	**Conventional SRBC**	**% Diff.**
S_1 Turn-off Loss (W)	6.15	15.48	60.28	14.54	57.71
S_2 Turn-on Loss (W)	2.57	4.05	36.48	3.56	27.81
Output Power (W)	19.79	15.92	19.57	14.07	28.10

There shows a pattern of decreasing and increasing values for S_1 turn-off and S_2 turn-on switching losses for different load resistances. The decreasing pattern is also seen in Figure 5.8 where the new SRBC has shown a significant improvement in S_1 turn-off switching losses by more than 60 % as compared to SRBC [51] and almost 58 % to the conventional at 10-Ω load. The switching losses in S_2 and output power have also improved and they are also observed at different load resistances.

5.3 Dead Time Variation in New SRBC Circuit

The pulse settings of the four MOSFETs, $Q_1 - Q_4$ in the D-CRGD circuit shown in Figure 3.3 are adjusted carefully resulting in different values of T_D. The T_D is varied to evaluate the switching losses in the switches and hence the performance of the circuit. The results are then measured, compared and analyzed. Table 5.3 shows the T_D and pulse width settings in the generator.

Table 5.3 Dead Time Variation Settings for f_s = 1 MHz

Dead time		**Initial delay time,** $t_{d,\ initial}$ (ns)	**Delay time for each voltage pulse**				**Pulse Width**					
$T_D = T_{D1} = T_{D2}$ (ns)	T_{D3} (ns)		t_{d1} (ns)	t_{d2} (ns)	t_{d3} (ns)	t_{d4} (ns)	V_{p1} (ns)	V_{p2} (ns)	V_{p3} (ns)	V_{p4} (ns)	PW_{S1} (ns)	PW_{S2} (ns)
5	23	15	15	222	284	947	200	786	654	331	201	769
15	15	15	15	232	284	955	200	765	654	312	211	759
30	5	15	15	247	284	969	200	740	654	286	229	741

For different T_D, the initial delay time, $t_{d,initial}$ is set to be constant at 15 ns. Therefore, the first delay time for voltage pulse one, t_{d1} is equal to $t_{d,initial}$. For example, by taking T_D = 15 ns as reference, it can be observed that only delay time for voltage pulse 1 and 3, t_{d1} and t_{d3} , and pulse width of voltage pulse of 1 and 3, V_{p1} and V_{p3}, are changed in order to obtain the dead times of 5 ns and 30 ns. Table 5.3 also shows that when $T_{D1} = T_{D2}$ increases, T_{D3} decreases instead.

5.3.1 Circuit Performance for Several Dead Times of New SRBC

With circuit parameter values remain unchanged except for T_D, the overall performance of the circuit is analyzed for theoretically output voltage of 9.6 V. The circuit performances at T_D of 5 ns, 15 ns, and 30 ns are shown in Table 5.4 and Table 5.5.

Table 5.4 Parameter Evaluation for Different Dead Time Values of New SRBC for V_{in} = 48 V and D = 0.20

T_D (ns)	V_o (V)	I_o (A)	t_{bd} (ns)	P_{COND} (W)	P_{BD} (W)
5	14.061	1.406	30	0.102	0.135
15	10.128	1.520	24	0.068	0.026
30	14.155	1.41	18	0.103	0.082

Table 5.5 Comparison in Power Losses for Different Dead Time Values of New SRBC for V_{in} = 48 V and D = 0.20

T_D (ns)	P_{S1} (W)	P_{S2} (W)	$P_{loss,total}$ (W)
5	1.538	1.145	2.920
15	1.138	1.100	2.238
30	1.707	1.823	3.715

$P_{loss,total}$ is the total of all losses consisting conduction loss, P_{COND} , body diode loss, P_{BD}, and also switching losses, P_{S1} and P_{S2} . From Table 5.5, it indicates that T_D at 15 ns gives the lowest total power loss, $P_{loss,total}$ of 2.238 W. When compared to T_D = 5 ns and T_D = 30 ns, it shows using T_D = 15 ns is the most energy saving setting to be used. The switching losses, P_{sw} of the circuit are the major contributors of losses. They come from the two switches, S_1 and S_2, in the SRBC circuit. This means that the faster the MOSFETs can turn off, the more switching power loss can be reduced.

Therefore, the shorter the time taken for a switch to turn off, the more energy can be saved. This is because a switch which has a smaller conduction time will produce less switching loss. In addition, an increase in L_s also gives an impact on decreasing P_{ave}. Therefore, in this work, several values of L_s are used in the simulation to get an optimum power loss in the two switches. As shown in Table 5.6, it can be concluded that L_s = 0.9 µH verifies the lowest total switching loss. If L_s is reduced further, the inductance will not be able to withstand the maximum current flow to the load.

Table 5.6 Total Switching Loss for Different L_s of New SRBC at T_D = 15 ns

L_s (µH)	Positive peak		Switching Time		S_1 turn-off switching losses (W)	S_2 turn-on switching losses (W)	Total switching loss (W)
	Switching loss of S_1 (W)	Switching loss of S_2 (W)	S_1 (ns)	S_2 (ns)			
0.9	65.000	95.000	35	40	1.138	1.100	2.238
1.1	61.694	71.383	35	40	1.080	1.428	2.508
1.2	57.118	64.790	35	40	1.000	1.296	2.296
1.4	55.601	55.306	40	45	1.112	1.244	2.356
2.0	47.294	44.399	52	61	1.230	1.354	2.584

5.4 Resonant Inductor Current and Gate Voltage Analyses for Different Dead Times

Table 5.7 records the $i_{L1,avg}$, t_{rise}, t_{rec} and di_{L1}/dt at several T_D of inductor current for D-CRGD circuit. The measurements are taken during steady state of the i_{L1} which can be referred back to Figure 4.2. From the tabulated results, T_D at 15 ns shows the steepest slope compared to others. It also shows the fastest t_{rise} as well as t_{rec}. The importance of t_{rise} is that, the faster the inductor current rises, the faster the circuit performance will be.

Table 5.7 $i_{L1,avg}$, Rise Time, Recovery Time and di_{L1}/dt of L_1 for Different T_D of New SRBC

T_D (ns)	**I_{L1} (A) average**	**Rise time, t_{rise} (ns)**	**Recovery time, t_{rec} (ns)**	**di_{L1}/dt (A/ns)**
5	3.202	35.399	61.972	0.124
15	3.570	25.760	56.645	0.173
30	3.068	33.502	71.685	0.122

On the other hand, t_{rec} means the time taken for the energy to recover back in the gate driver of the circuit. If the time taken for the circuit to recover the energy is shorter, the efficiency of the circuit would be higher. With the D-CRGD circuit, the rate of charged and discharged current are the fastest at T_D of 15 ns leading to the reduction in the switching time and hence switching loss.

Table 5.8 Rise Time, Fall Time and dv/dt of S_1 and S_2 for Different T_D of New SRBC

T_D (ns)	**$t_{rise,S1}$ (ns)**	**$t_{fall,S1}$ (ns)**	**$t_{rise,S2}$ (ns)**	**$t_{fall,S2}$ (ns)**	**dv_{S1}/dt (V/ns)**	**dv_{S2}/dt (V/ns)**
5	46.05	47.29	58.10	60.60	0.35	0.75
15	41.56	40.26	49.35	50.70	0.40	0.78
30	44.23	45.64	54.87	55.97	0.38	0.67

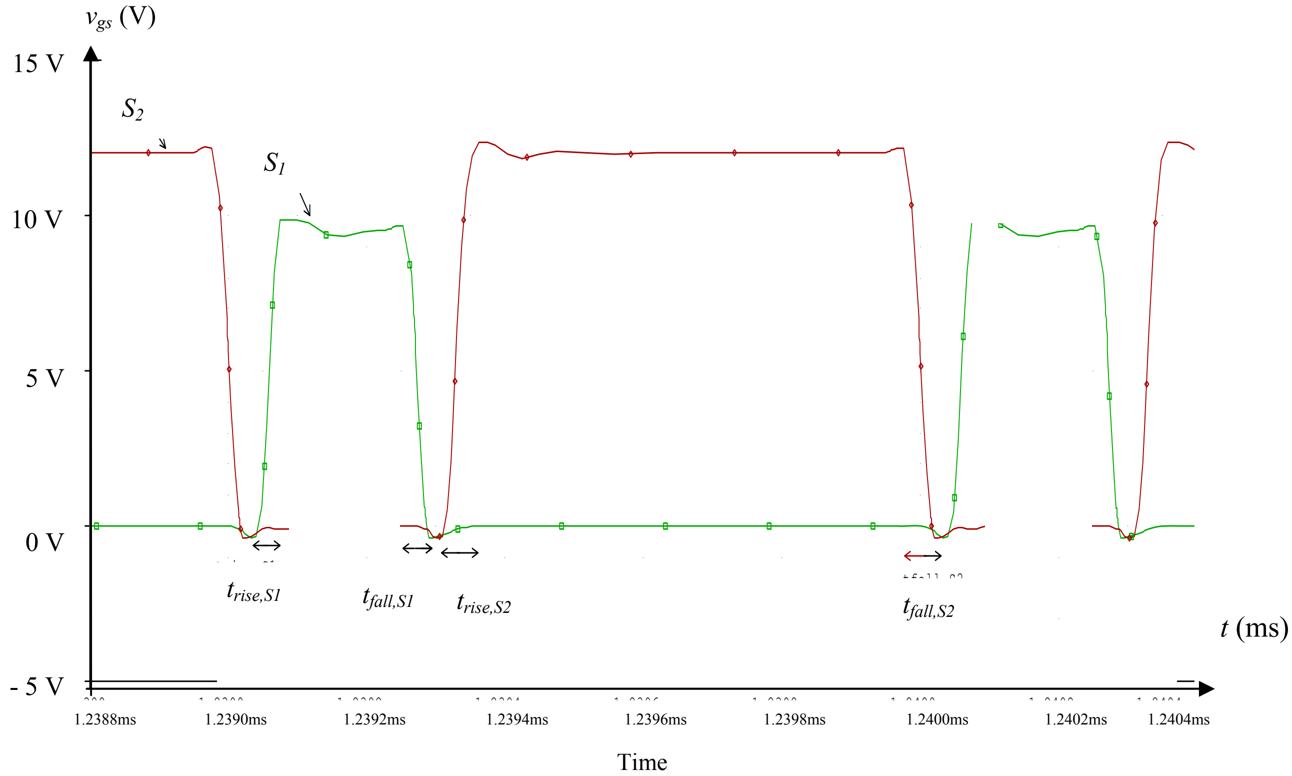

Figure 5.11 Simulated Gate Voltages of S_1 and S_2 at T_D = 15 ns of New SRBC

Table 5.8 shows the t_{rise} and t_{fall} of both switches at new SRBC circuit while Figure 5.11 indicates where they are measure as well as $dv_{S1}/_{dt}$ and dv_{S2}/dt. From the results obtained, again T_D = 15 ns shows the fastest t_{rise} and t_{fall} for both switches. It indicates that the circuit gives better performance at this T_D. In terms of the gradient of the slope, the rising edge of v_{gs} is equal to the falling edge for both switches shown in the simulation. The conventional SRBC does not pose this trait showing higher switching losses compared to the new SRBC circuit as shown in Figure 5.4.

5.5 Effects of Switching Frequency on New SRBC Circuit

By utilizing the FDT scheme and maintaining T_D to be 15 ns, the settings for Figure 3.4 are referred to Table 5.3 for 1 MHz switching frequency. Where all parameter values remain unchanged, the f_s is then varied from 250 kHz to 1.25 MHz.

Here, as frequency is set differently, all settings for V_{p1} to V_{p4} are also changed accordingly.

Switching loss, body diode conduction loss analyses, the T_D delay and effects on cross conduction are measured. Switching losses are measured during the overlapping of turn-on and turn-off in each switching cycle of S_1 and S_2. On the other hand, the switch v_N is tapped to observe the conduction of S_2 body diode. In high switching frequency, cross conduction between switches is inevitable and has to be monitored closely to avoid high power dissipation.

5.5.1 Simulation Data: Effect of Switching Frequency

The results are presented in accordance to variation of f_s. The overlapping switching time may vary as well as body diode conduction loss. The effects on switching and body diode related losses are discussed in relation to the application of T_D.

Table 5.9 Switching Time Comparison of Conventional and New SRBC

Frequency f_s	**S_1 Turn-Off (ns)**			**S_2 Turn-On (ns)**		
	Conv. SRBC	**New SRBC**	**% Diff**	**Conv. SRBC**	**New SRBC**	**% Diff**
250 kHz	29.56	24.10	18.5	83.91	29.78	64.5
500 kHz	45.19	28.44	37.1	80.51	28.20	65.0
750 kHz	56.15	28.44	49.3	91.63	30.71	66.5
1 MHz	62.70	35.00	44.2	88.58	40.00	54.8
1.25 MHz	63.71	33.87	46.8	88.89	43.08	51.5

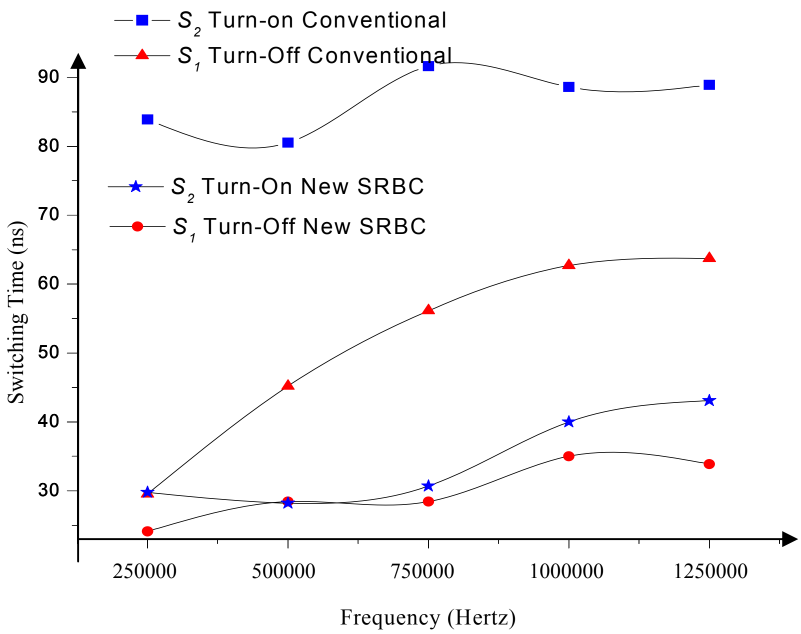

Figure 5.12 Turn-On and Turn-Off Switching Times of Conventional and New SRBC

As shown in Table 5.9, the turn-off and turn-on time are much faster in the new SRBC compared to the conventional by 44.2 % and 54.8 % respectively at 1 MHz switching frequency. The graphical representation of Table 5.9 is shown in Figure 5.12. The switching time increases slightly against frequency and this applies to both switches in SRBC circuit. By increasing the frequency, the device's electrical charges will travel with high velocity and hence prolong the relaxation time upon turn-off due to vibration and heat dissipation and vice versa. The switching speed in the new SRBC circuit has therefore increased by at least 40 % resulting from the new ZVS topology design.

Table 5.10 Average Switching Loss Comparison of Conventional and New SRBC

Frequency f_s	Average S_1 Switching Turn-Off Loss (W)			Average S_2 Switching Turn-On Loss (W)		
	Conv. SRBC	**New SRBC**	**% Diff**	**Conv. SRBC**	**New SRBC**	**% Diff**
250 kHz	11.03	11.79	6.4	5.19	2.08	59.9
500 kHz	12.06	10.47	13.2	4.46	1.42	68.2
750 kHz	12.64	10.32	18.4	4.38	1.21	72.4
1 MHz	14.56	6.19	57.5	3.57	1.23	65.5
1.25 MHz	16.39	12.34	24.7	5.43	1.23	77.3

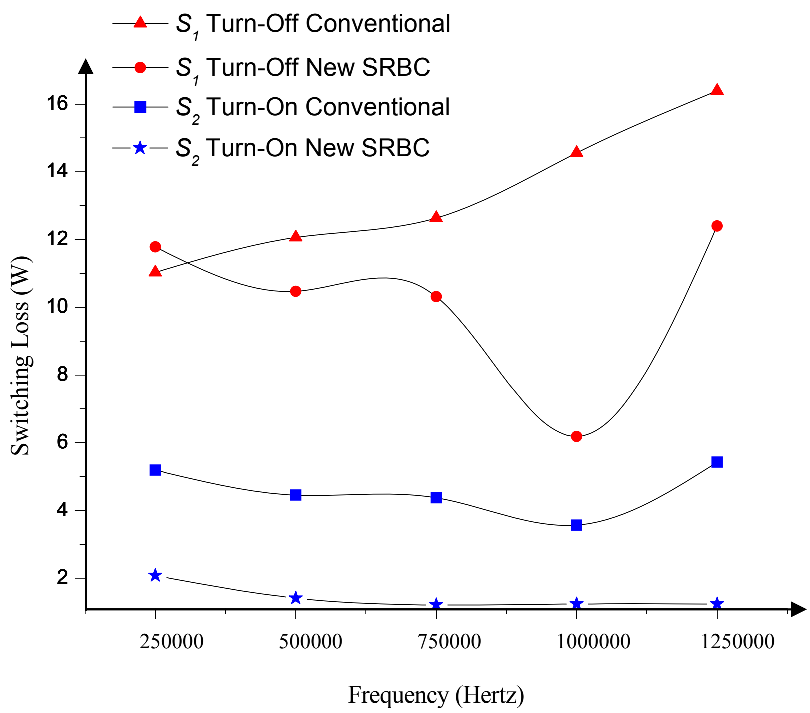

Figure 5.13 Average Turn-On and Turn-Off Switching Losses of Conventional and New SRBC

As for the switching loss, the similar pattern is observed. The loss increases with respect to frequency during turn-off. Looking at Table 5.10, the turn-off switching loss is minimal at f_s of 1 MHz showing the suitability of new SRBC operating at high frequency based on the conditions set in the simulation.

Another distinguishing feature is that the average turn-on S_2 loss of the new SRBC is consistent as frequency increases particularly where more than 65 % of power loss is recovered compared to the conventional at 1 MHz. Figure 5.13 shows the graphical waveforms of Table 5.10.

When both MOSFETs are off, the i_{Lo} flows in the body diode of S_2. Here the body diode conducts and therefore produces additional loss to the circuit. The switching loss in the new SRBC circuit is minimized within the S_2 turn-on duration. Table 5.11 illustrates that the t_{bd} reduces when f_s increases. However, when f_s increases beyond 1 MHz, so does the t_{bd}. This is significant in high switching frequency operation. Unlike the new SRBC circuit, switching loss in conventional SRBC is dominant for the entire switching cycle where t_{bd} does not give any impact to the operation.

Table 5.11 Average Output Current and Body Diode Conduction Comparison of Conventional and New SRBC

Frequency f_s	**Average I_{Lo} (A)**			**New SRBC**		
	Conv. SRBC	**New SRBC**	**% Diff**	**t_{bd} (ns)**	**Peak V_{BD} (V)**	**P_{BD} (W)**
250 kHz	1.68	1.99	15.6	101	-1.42	0.081
500 kHz	1.53	1.81	21.0	38	-0.59	0.055
750 kHz	1.51	1.86	18.8	33	-0.39	0.074
1 MHz	1.21	1.51	19.9	24	-0.24	0.026
1.25 MHz	1.65	1.92	14.1	27	-0.20	0.104

Table 5.11 also indicates that i_{Lo} is inversely proportional to f_s which is due to the vibration produced as heat dissipation at the load. This is similar to t_{bd} where i_{Lo} is also increasing beyond 1 MHz. Nevertheless, i_{Lo} improves by at least 19 % for 1 MHz in the new SRBC circuit. Also it is shown that body diode conduction time, t_{bd} is also inversely proportional to frequency. Having a low peak reverse voltage, V_{BD}, this gives result in low body diode conduction loss. Therefore, from the evaluation of t_{bd}, i_{Lo} and V_{BD}, they have shown that the new SRBC circuit has improved switching loss and hence the entire system operation compared to the conventional SRBC.

5.6 Effects of Duty Ratio on New SRBC Circuit

Referring to new SRBC circuit as shown in Figure 3.4, S_1 has the primary function of a buck converter, used to convert high input voltage to low output voltage at the load. On the other hand, S_2 has a longer conduction time compared to S_1. The switching losses are recorded in Table 5.12.

Table 5.12 Switching Loss Analysis for Different S_2 Duty Ratio of New SRBC at T_D = 15 ns in DCM Operation

$V_{gs,S1}$ duty ratio, D	$V_{gs,S2}$ duty ratio, D	S_1 Turn-off Peak (W)	S_2 Turn-on Peak (W)	S_1 Turn-off Switching Loss (W)	S_2 Turn-on Switching Loss (W)
0.20	0.20	91.617	109.726	1.603	2.195
0.20	0.55	87.060	98. 760	1.524	1.975
0.20	0.70	66.132	79.336	1.389	1.483
0.20	0.75	57.118	64.790	1.000	1.296

From the results, the D of S_2 at 0.75 gives the lowest switching losses compared to others. Therefore, it can be concluded that in order to reduce the conduction loss in the circuit, the conduction time of S_2 has to be at 0.75 for low switching loss. From the variation of S_2 duty ratio and constant S_1 conduction time, the results are plotted in line chart as shown in Figure 5.14.

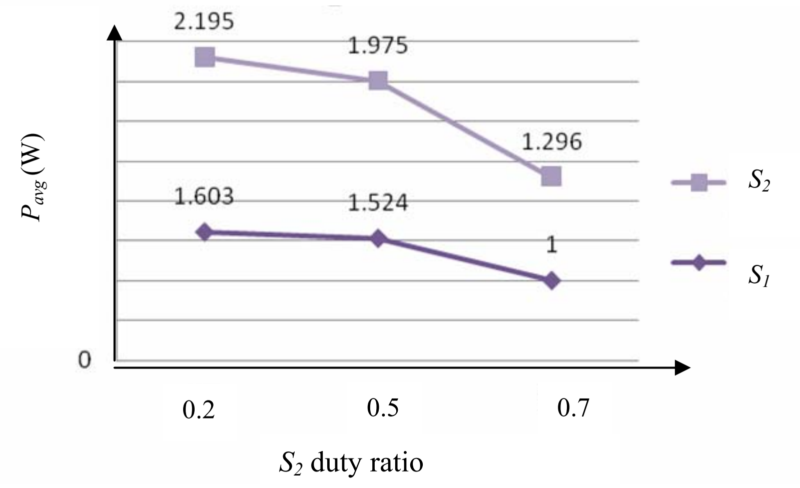

Figure 5.14 S_1 Turn-Off and S_2 Turn-On Power Losses at Different S_2 Duty Ratio in DCM Operation

5.7 Numerical Verifications on New SRBC Performance for T_D of 15 ns

Utilizing MathCAD, which is the tool to numerically calculate based on formulas, the results are compared with PSpice measurements as shown in Table 5.13.

Table 5.13 Comparison of MathCAD Calculations and PSpice Measurements at T_D = 15 ns of New SRBC

Parameters	**Method**		
	MathCAD	**PSpice**	**% Diff**
Rise time, t_{rise} (ns) (40)	25.81	25.76	0.19
Recovery time, t_{rec} (ns) (37)	51.62	56.64	8.87
Peak current, $i_{L1}(t_{peak})$ (A) (38)	3.572	3.24	9.29
Total switching loss, $P_{sw,total}$ (W) (16)+(17)	2.52	2.24	11.01
Conduction loss of S_2, P_{COND} (mW) (20)	100	68	32.00
Body diode loss, P_{BD} (mW) (14)	49	25.7	47.55

The difference in the results obtained from PSpice and MathCAD show significant big margin in the conduction and body diode losses. Other than these, the simulation results are acceptable. Nevertheless this extended work has successfully verified that T_D of 15 ns is the best value to be used for the lowest switching loss in the converter.

5.8 Comparative Assessment of Gate Drive Control Schemes

In this part of work, dual-channel function generators are again used to fix the pulse widths and T_D of Q_1 to Q_4 switches for FDT scheme in Figure 3.3. On the other hand, a set of combinational discrete components and transistor-transistor logic (TTL) gates are employed for the generation of ADG and PGD schemes. All three schemes are compared to determine the effectiveness in terms of switching loss, output power distribution, body diode conduction loss and efficiency of the converter. Figure 5.15 and Figure 5.16 show the proposed AGD and PGD schemes respectively.

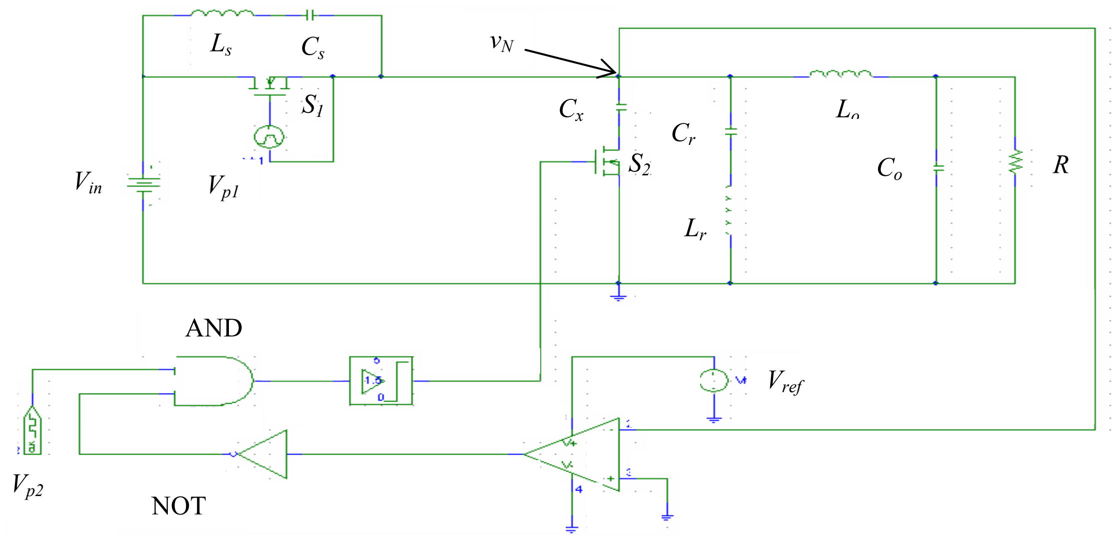

Figure 5.15 SRBC AGD Circuit

The digital control block is included in the AGD scheme for the SRBC circuit shown in Figure 5.15. In this scheme, S_1 is applied with a fixed PWM signal. S_2 switch is actually controlled by the scheme. Here, the v_N is first captured and compared with V_{ref}. The digital clock will then be fed to the AND gate so that when the clock triggers with input 1, S_2 switch will not turn on until node voltage is zero. The T_D is measured along side with the body diode conduction time of S_2. As a result, the conduction loss, body diode conduction loss and total switching losses can be calculated. The digital delay line settings are shown in Table 5.14.

Table 5.14 Digital Delay Line Settings of Adaptive SRBC Gate Drive

Parameters	**Value**
Delay (ns)	340
On Time (ns)	645
Off Time (ns)	355
Start value	0
Opposite Value	1

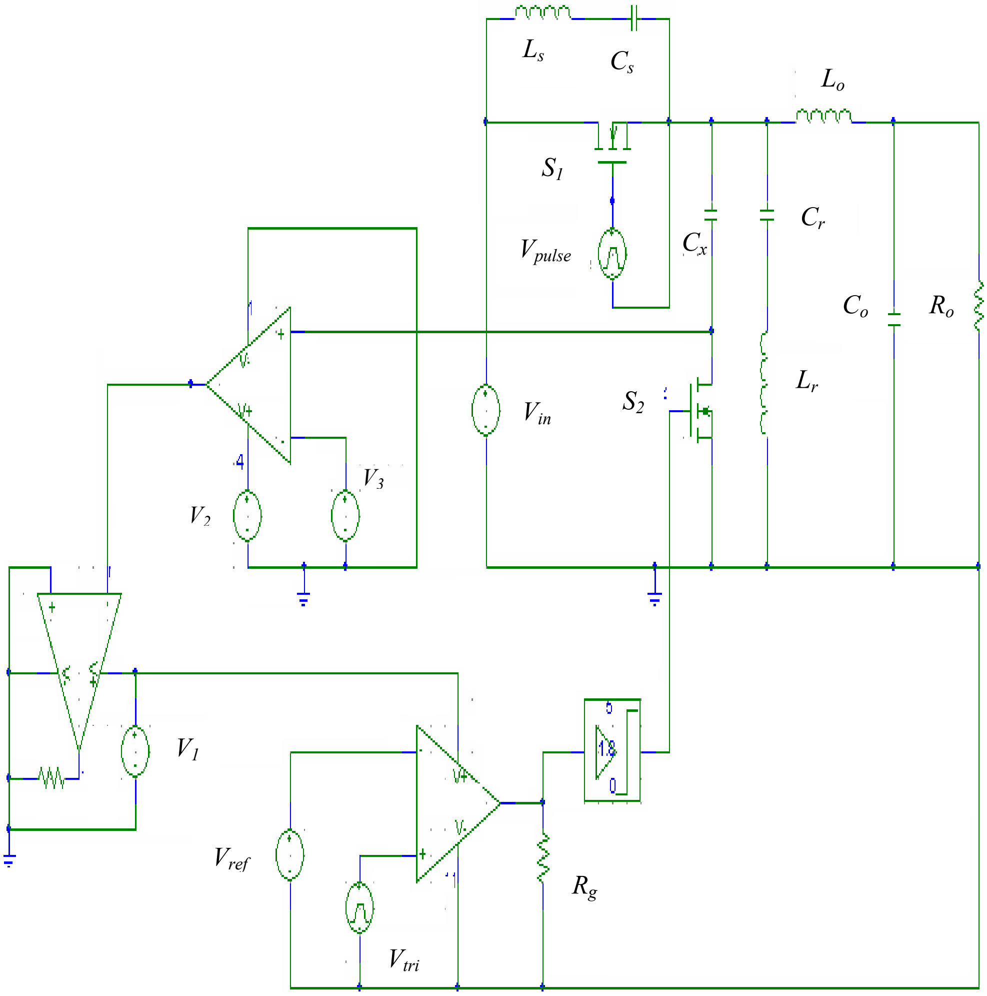

Figure 5.16 SRBC PGD Circuit

On the other hand, in PGD control scheme as shown in Figure 5.16, the PWM technique using comparator is used where an equal pulse width will be generated from the comparison between the triangular waveform, V_{tri} and V_{ref}. The comparator will produce an output voltage each time V_{tri} goes above V_{ref}. In this work, the pulse width will be varied by adjusting V_{ref} in between 0.2 V and 0.8 V, to find out the capability of T_D reduction in SRBC circuit.

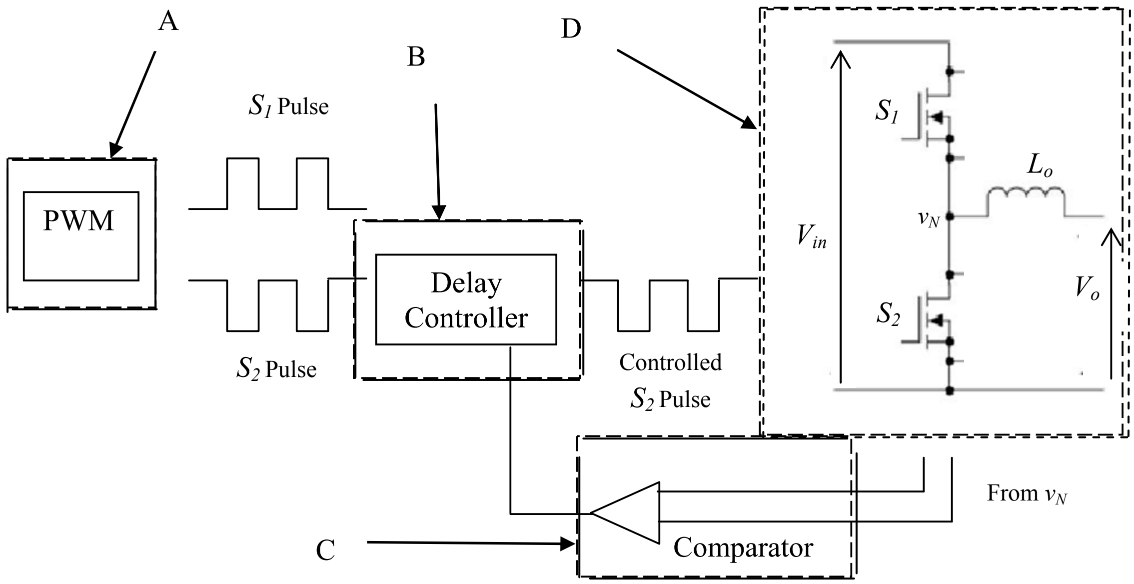

Figure 5.17 PGD Control Block Diagram

The Block Diagram of the PGD is shown in Figure 5.17. Note that it is constructed from several circuits constituting PWM circuit (A), Delay Controller Circuit (B), Circuit to sense the body diode conduction (C) of S_2, and SRBC Circuit (D). The PWM circuit (A) will generate the pulse that is used to turn on and off the MOSFET. The S_1 pulse will directly use to drive S_1. The S_2 pulse will be the input of the delay controller (B) before it drives the S_2. Circuit (C) will perform the feedback operation and generate output signal to the delay controller. Block A and D have already been explained in previous section 3.3 and 3.4 respectively. The operating details of block B and C are described below.

5.8.1 Delay Controller Circuit

The delay controller circuit will adjust the S_2 pulse before the output drives the switch S_2. The adjustment is based on the prediction concept where the width of the pulse will be adjusted by the controller according to the feedback signal it receives. In Figure 5.18, the *D[n]* pulse is currently turned on the S_2. During this turn-on period, the feedback circuit will sense the conduction at S_2 due to the inductive load and it will generate a signal to the Delay Controller. Based on this signal, the controller will make an adjustment for the next pulse, *D[n+1]* so that the dead time, $T_{D[n+1]}$ for next switching cycle can be minimized while preventing the cross conduction.

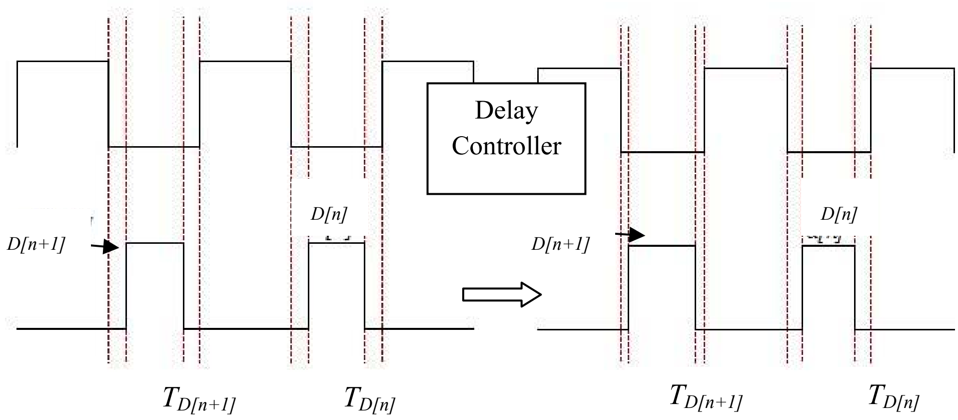

Figure 5.18 S_2 Pulse Width Delay Adjustment

The adjustment made by the controller can be either to maximize or minimize the pulse width. Note that the T_D for $T_{D[n+1]}$ is adjusted by the delay controller. It has the ability to vary the reference voltage according to the received input from the feedback circuit. Figure 5.19 illustrates how the pulse width can be adjusted based on the feedback circuit.

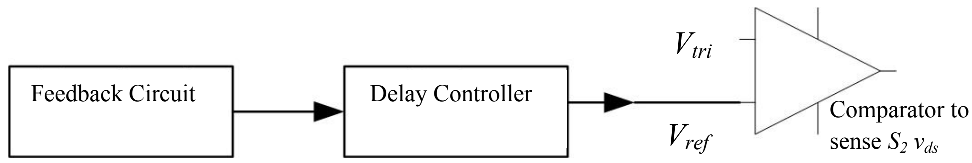

Figure 5.19 PGD Delay Controller Block Diagram

This is a circuit where the feedback operation is performed. The output generated from this circuit will be used as the input for the Delay Controller. During S_1 pulse transition from HIGH to LOW, the comparator will sense the v_{ds} of S_2. If body diode conduction is detected, the comparator will generate HIGH output and the delay controller will reduce the delay of low side pulse for the next switching cycle. If the comparator output generates a LOW output, the delay controller will increase the delay for the next switching cycle of S_2. As long as the SRBC operates, this shifting process will continue to avoid the cross conduction while ensuring the T_D delay introduced is small.

The feedback circuit is connected to the delay controller. Based on the signal received, the delay controller will adjust the V_{ref}. Since the width of the pulse generated depends on the comparison between the V_{tri} and V_{ref}, the variation in V_{ref} will change the T_D between the pulses accordingly. The parameter setting for V_{tri} and V_{ref} are given in Table 5.15 and Table 5.16 respectively. Using the required frequency of 1 MHz, the frequency of the V_{tri} must also be same. As previously mentioned, the duty ratio of S_1 is determined to be 0.20.

Table 5.15 PSpice Parameter Settings for V_{tri} of Predictive Gate Drive

Parameter	Value
Max Voltage, V_1	0
Min Voltage, V_0	1
Rise Time, t_r	0.5 ìs
Fall Time, t_f	0.5 ìs

Table 5.16 PSpice Parameter Settings for V_{pulse} of Predictive Gate Drive

Parameter	Value
Max Voltage, V_1	5 V
Min Voltage, V_0	0 V
Rise Time, t_r	5 ns
Fall Time, t_f	5 ns
Time Delay, t_d	893 ns
Pulse Width, *PW*	200 ns
Time Taken for a Complete Cycle, *PER*	1 µs

The steady-state simulation analysis is repeated with different V_{ref} values in order to investigate the effect in T_D on SRBC circuit's performance. The study on the $P_{COND} - P_{BD}$ and $T_D - t_{bd}$ relationships with respect to V_{ref} are also carried out in addition to switching related losses in the converter.

5.8.2 Comparison between FDT and AGD Control Schemes

Table 5.17 shows the comparison and the analysis of FDR and AGD circuit operations. The initial study concentrated on the AGD scheme which was applied directly to the gate terminal of Q_4 (AGD-Q_4) in the D-CRGD circuit as shown in Figure 5.20. It is found that this implementation does not show significant improvement in new SRBC except only for the V_o compared to FDT. In addition, this also adds up the t_{bd} of S_2 caused by the delay in cross coupling loops during T_D detections in Q_3-Q_4 and S_1-S_2. As a result, S_2 will take a longer time to conduct. Moreover, the AGD-Q_4 scheme requires a precise control on gate charge compensation delay of the switch or else this leads to switching loss of 2.52 W, which is 7.54 % higher than FDT scheme.

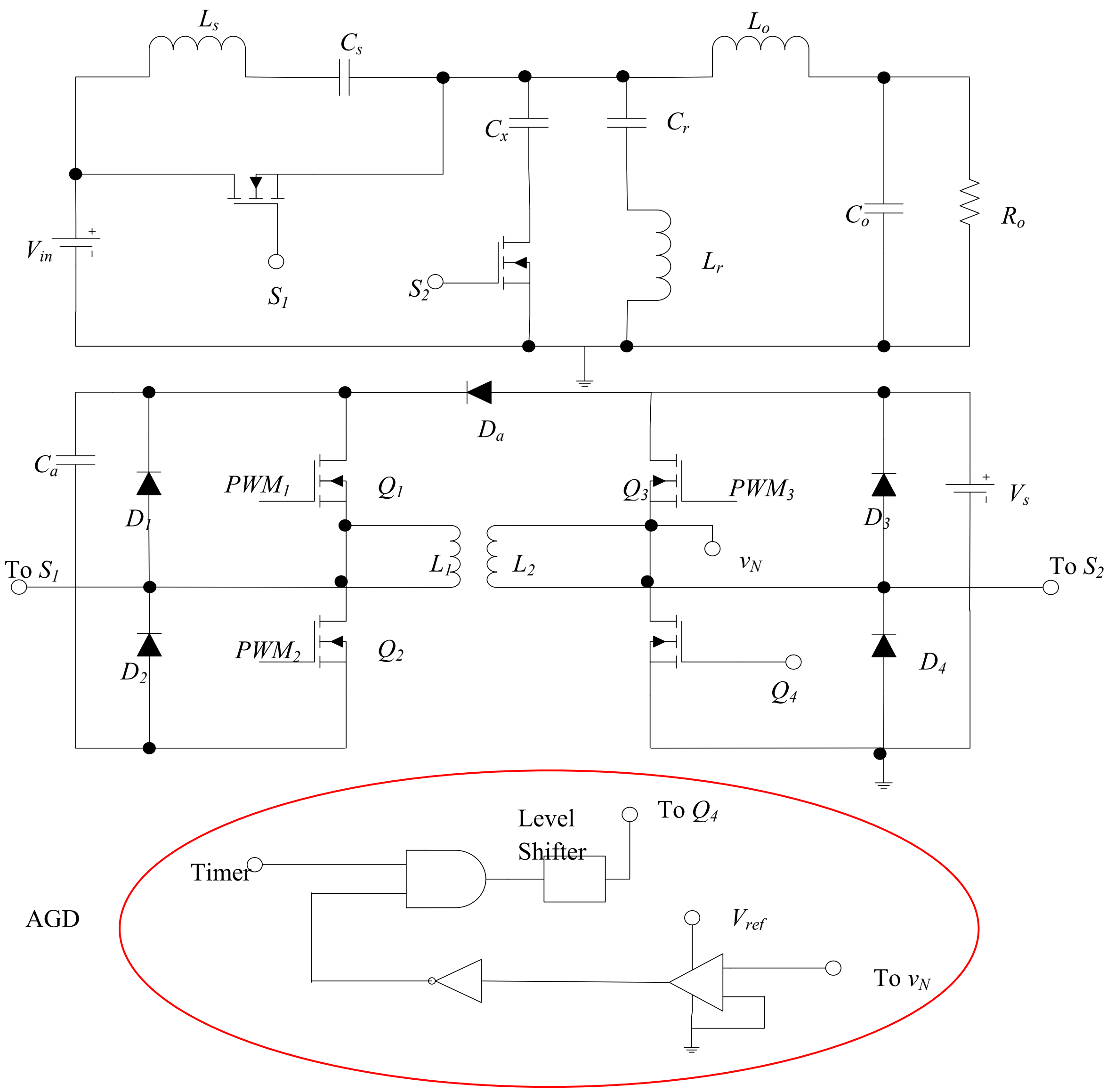

Figure 5.20 D-CRGD Circuit with AGD Control Scheme at Switch Q_4

Table 5.17 FDT, AGD-Q_4 and AGD-S_2 Analysis for D = 0.20 in D-CRGD Circuit

Parameters	FDT	AGD-Q_4	% Δ to FDT	AGD-S_2	% Δ to FDT
V_o (V)	10.18	10.41	2.21	10.27	0.88
I_{Lo} (A)	1.51	1.27	15.89	1.28	15.23
t_{bd} (ns)	24	27	11.11	28	14.28
P_{COND} (mW)	68.30	86.90	21.40	87.40	21.85
P_{BD} (mW)	25.73	26.11	1.46	28.62	10.10
P_{sw} (W)	2.33	2.52	7.54	3.09	24.60

In the other implementation, the AGD scheme is fed to the gate of S_2 (AGD-S_2) of SRBC shown in Figure 5.15. It is found that the P_{sw} is higher in AGD-S_2 compared to AGD-Q_4. This is due to the impact of C_x in the converter which prolongs the detection of T_D by the controller and hence reduces the efficiency. When comparing with FDT, the P_{sw} in AGD-S_2 has increased by 24.6 %.

Therefore, this clearly indicates that using the D-CRGD helps solve issues related to T_D, reduce P_{COND} to 68.30 mW and hence P_{sw}. In other words, by applying the digital delay control directly to S_2 will not give much advantage in SRBC performance. It is found that the new D-CRGD network can generate better loss savings to the converter.

5.8.3 Comparison between FDT and PGD Control Schemes

The simulation of PGD control scheme is carried out based on the variation of reference voltage, V_{ref} as shown in Figure 5.16 and it is applied directly to the gate of S_2 (PGD-S_2) in the new SRBC circuit through delay controller. The simulation data are presented in Table 5.18. From the variation of V_{ref} in the PGD-S_2 control block, the SRBC's P_{sw} in both S_1 and S_2 are measured. As V_{ref} is decreased from 0.8 V to 0.27 V, all parameter values except i_{Lo} have reduced with respect to T_D. Then once V_{ref} is below 0.27 V, the results are no longer valid since T_D is negative. It is also found that low P_{sw} lies between 0.27 V and 0.3 V. If V_{ref} is applied with less than 0.27 V, the pulses will overlap and eventually leads to cross-conduction. A high V_{ref} yields a greater V_o which is favorable in the design but the P_{COND} will increase resulting in high total switching loss, $P_{sw,Total}$ in the circuit.

Table 5.18 Switching Loss Measurement Adopting PGD-S_2 for D = 0.20 in New SRBC

V_{ref} (V)	V_o (V)	I_{Lo} (A)	T_D (ns)	t_{bd} (ns)	P_{COND} (mW)	P_{BD} (mW)	$P_{sw,S1}$ (W)	$P_{sw,S2}$ (W)	$P_{sw,Total}$ (W)
0.8	11.60	1.12	260	350	103.90	109.0	1.64	1.03	2.88
0.6	11.23	1.25	170	220	115.65	77.0	1.96	1.42	3.34
0.4	10.23	1.31	66	82.5	92.51	54.9	1.42	1.25	2.82
0.35	10.41	1.48	40	48	81.15	48.8	1.61	1.20	2.94
0.33	10.35	1.50	27	33	71.24	36.8	1.56	1.15	2.82
0.3	**10.24**	**1.52**	**15**	**24**	**68.27**	**24.6**	**1.16**	**1.10**	**2.35**
0.29	10.22	1.53	10	25	67.27	24.0	1.17	1.09	2.35
0.285	10.11	1.54	4	24	62.43	23.5	1.15	1.10	2.33
0.28	**10.07**	**1.56**	**0**	**24**	**61.89**	**23.7**	**1.18**	**1.11**	**2.38**
0.27	**10.02**	**1.58**	**0**	**27**	**60.25**	**23.2**	**1.20**	**1.15**	**2.43**
0.26	10.95	1.29	-7.5	28	59.57	28.5	1.28	1.90	3.26
0.25	11.89	0.98	-11	32	66.93	30.7	1.32	2.35	3.76
0.20	12.38	0.64	-34	46	71.68	33.1	1.56	3.10	4.76

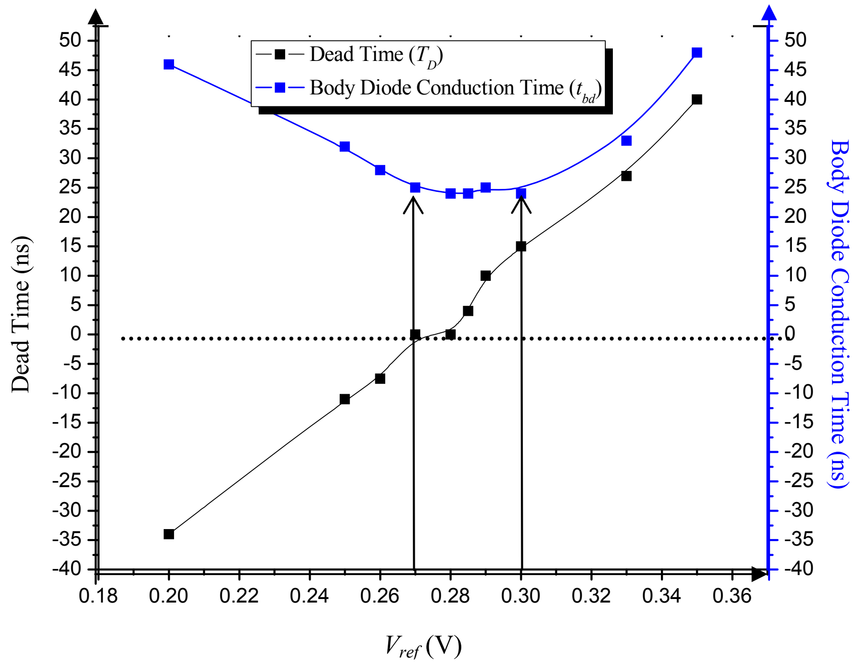

Figure 5.21 Relationship between T_D and t_{bd} versus V_{ref} of PGD-S_2

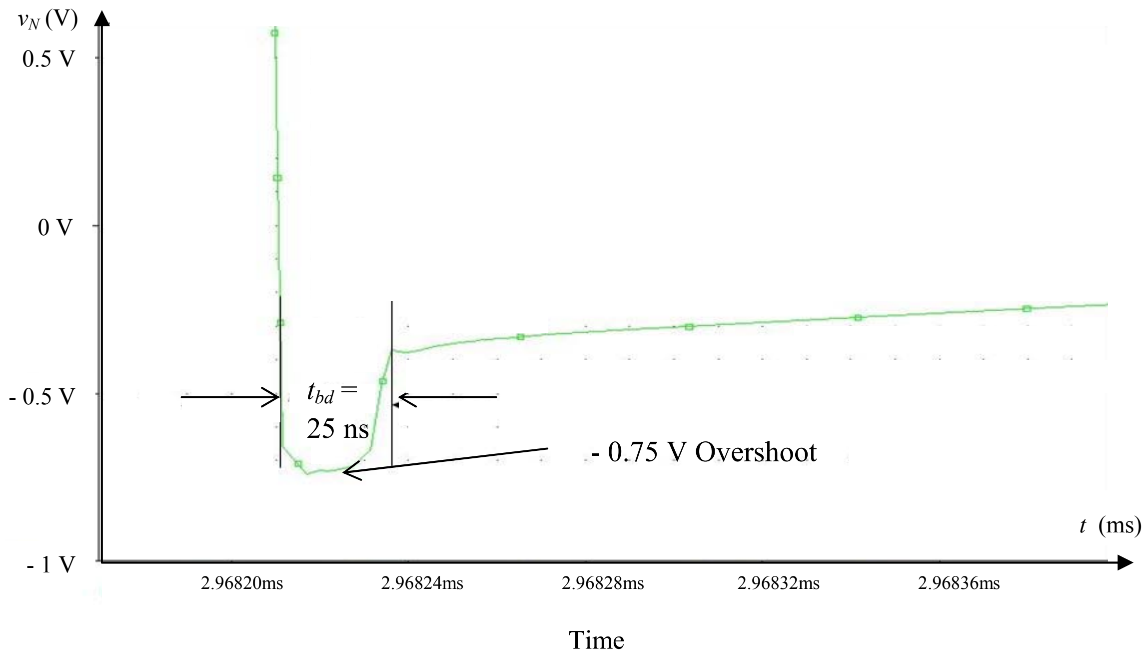

Figure 5.22 Negative Overshoot of v_N in PGD-S_2 at V_{ref} of 0.29 V

Figure 5.21 explains that the t_{bd} increases linearly with T_D starting from V_{ref} at 0.27 V. The faster free-wheeling i_{Lo} flows into the body diodes during T_D, the lower

P_{sw} in the converter will be. For instance, at V_{ref} = 0.29 V, the t_{bd} is measured at 25 ns with - 0.75 V overshoot which indicates the duration of on-state conduction of body diode as shown in Figure 5.22. Here, t_{bd} has to be minimized and this can be realized by reducing T_D. However, due to the fact that T_D cannot be negative, the best applicable V_{ref} is 0.28 V to achieve the lowest t_{bd}.

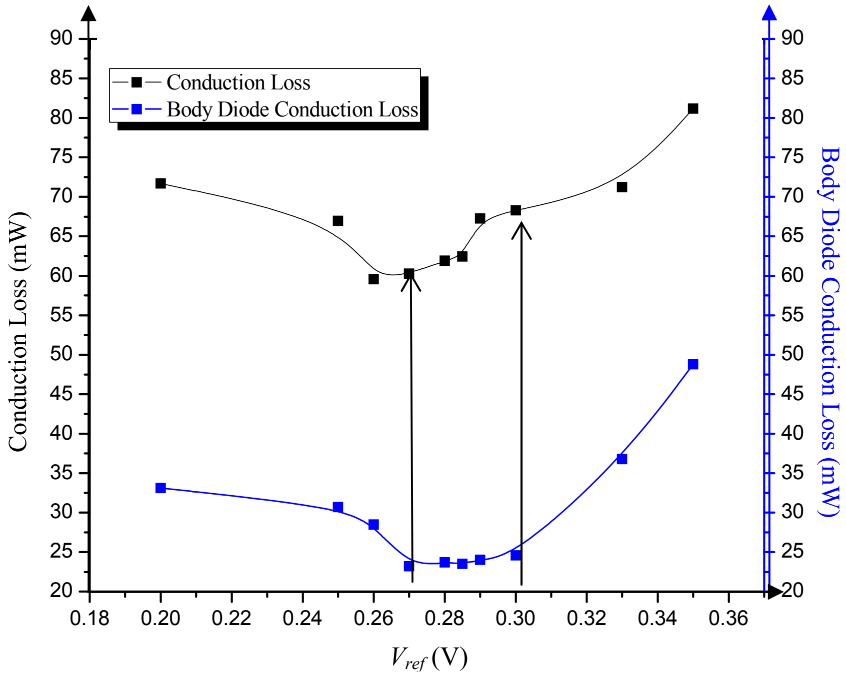

Figure 5.23 Relationship between P_{COND} and P_{BD} versus V_{ref} of PGD-S_2

In Figure 5.23, the P_{COND} and P_{BD} losses are minimum at V_{ref} = 0.27 V. Here, when V_{ref} is less than 0.27 V or greater than 0.3 V, these losses will increase. It is also seen that P_{COND} is slightly higher at V_{ref}= 0.3 V due to the presence of T_D = 15 ns. The role of the controller is to minimize the T_D for the lowest possible P_{COND} by detecting it before S_2 can be turned on. However, this is valid only if T_D is positive. The t_{bd} is slightly higher at V_{ref} = 0.27 V compared to 0.3 V because of the existence of cross-conduction. Other related graphs extracted from Table 5.18 are compiled in Appendix C.

Next, the application of PGD control scheme is applied to the Q_4-switch (PGD-Q_4) of the D-CRGD circuit. The process in determining the new

SRBC's P_{sw} is similar to the PGD-S_2 implementation. Table 5.19 gives the simulated assessments between PGD-Q_4 and PGD-S_2 for V_{ref} = 0.27 V at T_D = 0 ns.

Table 5.19 Comparison of PGD-Q_4 and PGD-S_2 for V_{ref} = 0.27 V, D = 0.20 at T_D = 0 ns

Parameters	**PGD-Q_4**	**PGD-S_2**	**% Diff**
V_o (V)	10.20	10.02	1.76
$I_{Lo,avg}$ (A)	1.56	1.58	1.27
t_{bd} *(ns)*	26	27	3.70
P_{COND} (mW)	62.30	60.25	3.29
P_{BD} (mW)	23.65	23.20	1.90
$P_{sw,S1}$ (W)	1.25	1.20	4.00
$P_{sw,S2}$ (W)	1.18	1.15	2.54
$P_{sw,Total}$ (W)	2.52	2.43	3.57

Table 5.19 reveals the impact on D-CRGD network with PGD control block. The P_{COND} is seen slightly higher in PGD-Q_4 scheme of 62.30 mW which gives a reduction in 3.29 % compared to PGD-S_2. Also, since the T_D is assumed to be zero at V_{ref} = 0.27 V, ideally, P_{BD} can be minimized. However, this slightly increases t_{bd} compared to V_{ref} at 0.3 V and hence shoots up $P_{sw,S1}$. In spite of this drawback, the PGD controller is still able to control and adjust S_2 gate signal and maintain P_{COND} and P_{BD} losses at acceptable levels.

By introducing a small T_D interval of 15 ns for V_{ref} = 0.3 V as given in Table 5.20, the issue in signal overlapping can be avoided. In fact, the PGD controller can have a longer safe time margin to detect the T_D before $V_{gs,S2}$ can turn on. The application of non-zero T_D produces higher P_{COND} and P_{BD} compared to T_D = 0 ns. Remarkably, $P_{sw,S1}$ is reduced compared to V_{ref} at 0.27 V leading to lower $P_{sw,Total}$ for a shorter duration in t_{bd}.

Table 5.20 Comparison of FDT and PGD-S_2 at V_{ref} = 0.3 V for D = 0.20 at T_D = 15 ns

Parameters	**FDT**	**PGD-S_2**	**% Diff**
V_o (V)	10.18	10.24	0.59
I_{Lo} (A)	1.51	1.52	0.65
t_{bd} *(ns)*	24	24	-
P_{COND} (mW)	68.30	68.27	0.04
P_{BD} (mW)	25.73	24.60	4.39
$P_{sw,S1}$ (W)	1.14	1.16	1.72
$P_{sw,S2}$ (W)	1.10	1.10	-
$P_{sw,Total}$ (W)	2.33	2.35	0.85

In addition, the use of the D-CRGD in FDT circuit can also be considered as an independent gate drive control option to bias S_1 and S_2 gates. The $P_{sw,Total}$ in FDT is only 0.85 % lower than PGD-S_2. However, PWM signals have to be generated with precise control to avoid cross conduction even though it is known for its simplicity. From the simulation, PGD-S_2 is found to be the best option for the gate drive control scheme. Apparently, all simulation results have indicated positive remarks and brought to successful analyses in the comparison of different PGD driving techniques with FDT control scheme.

5.9 Efficiency Analyses of S-CRGD, SRBC and Gate Drive Control

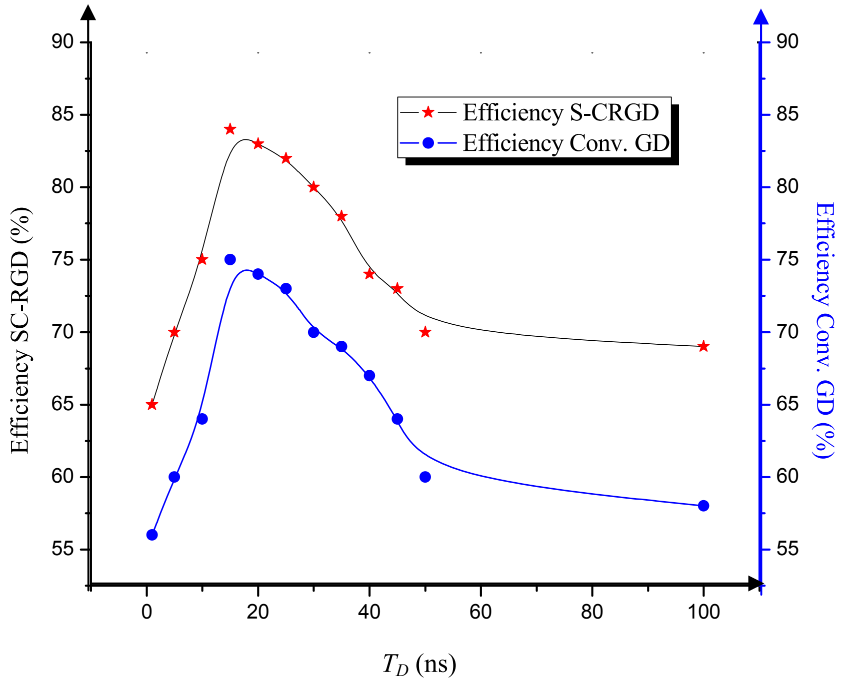

Figure 5.24 Efficiency versus T_D for $L_r = 9$ nH and $D = 0.20$ of S-CRGD

Figure 5.24 shows that the efficiency of S-CRGD circuit is better than the conventional gate driver by at least 12 %. It is also observed that the efficiency is at maximum when T_D is around 20 ns. When T_D is increased or decreased beyond this value, the efficiency drops significantly. This is true since when T_D is applied too small, this will lead to cross conduction and consequently increase the switching loss. On the other hand, when T_D is too big, there will be a possibility in overshoot voltage at the gate voltage of S_1 and S_2 and this leads to the increase in the conduction losses. So the T_D of around 18 ns produces the least loss and eventually improves the efficiency of the driver.

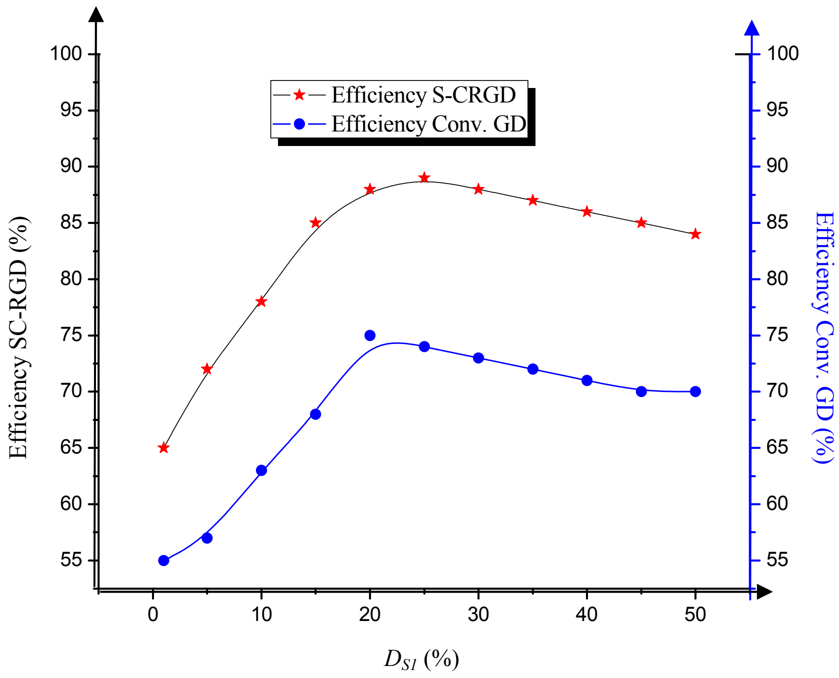

Figure 5.25 Efficiency versus Duty Ratio of Q_1 for L_r = 9 nH and T_D = 15 ns of S-CRGD

Based on the design benchmark of S-CRGD circuit, L_r and T_D have been optimized to round 9 nH to 10 nH and 15 ns respectively. By varying D of Q_1 and 1-D on Q_2, the efficiency of S-CRGD and conventional gate driver are compared. As shown in Figure 5.25, S-CRGD circuit performs better having a higher efficiency of around 85 % at D = 0.20 compared to conventional of only around 75 %. Since D is important in determining the rate of inductor current flow in the driver, the variation in D will influence the efficiency significantly. When D is reduced below 0.20, the figure clearly shows the steep drop in efficiency in both converters. This is caused by the increase in oscillation during discharging of current. Therefore, gate drive loss increases. Interestingly, an increase in D will not cause significant reduction in efficiency. This is the remarkable feature of the gate driver where the operating condition is not dependent on duty ratio.

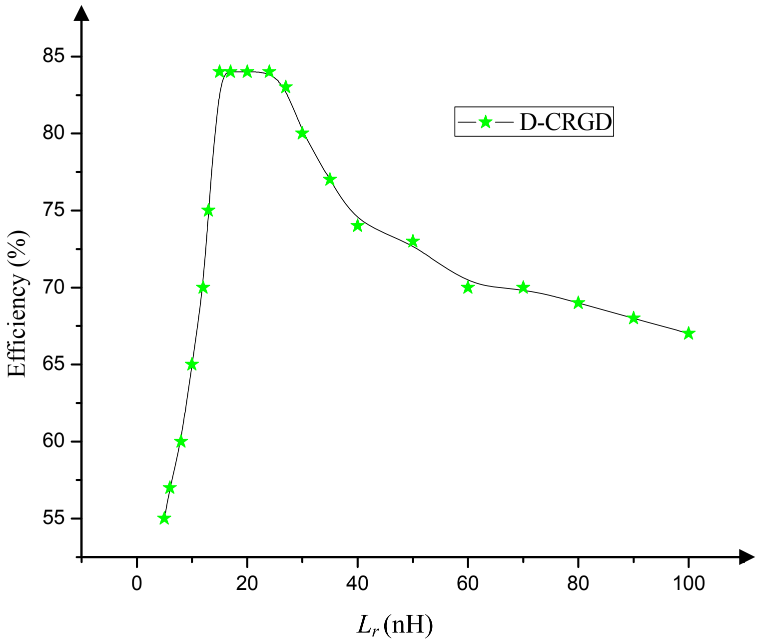

Figure 5.26 Efficiency versus Resonant Inductor for D = 0.20 and T_D = 15 ns of New D-CRGD

In Figure 5.26, it is observed that the efficiency of the D-CRGD varies with respect to L_r. The efficiency is about 83 % when L_r is around 9 nH - 25 nH. When L_r is reduced, the efficiency drops tremendously. This is because L_r cannot sustain high level of peak current during charging phase. This results in high power dissipation and possible circuit malfunction. Besides, as L_r increases, more time is needed for the current to flow. Here, the efficiency will drop to around 68 % in case of L_r = 100 nH since a high L_r will lead to high oscillation in current and gate voltage of the switch during turn-off.

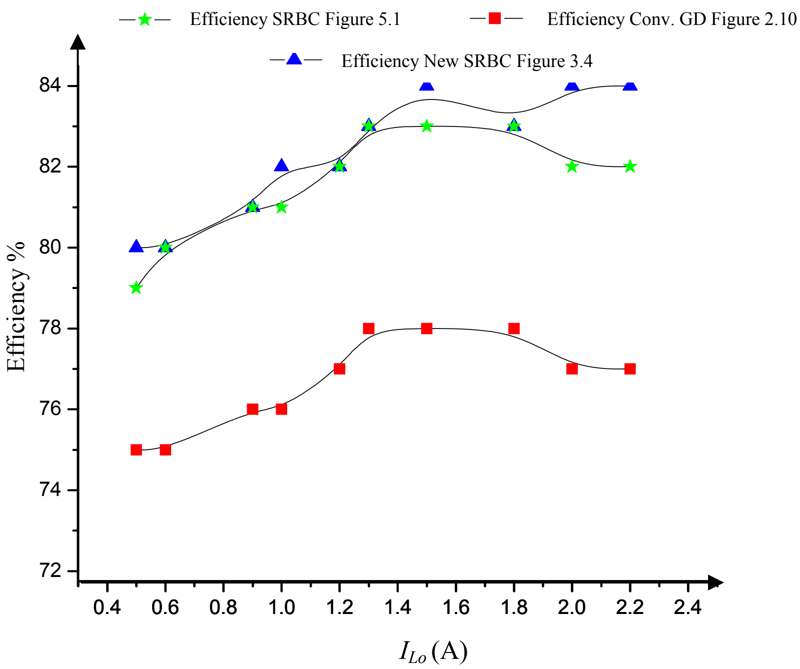

Figure 5.27 Efficiency versus Inductor Load Current for D_{S1} = 0.20, D_{S2} = 0.75 and T_D = 15 ns of Three SRBC

Three different SRBC circuits are studied and their efficiencies are measured with respect to various load resistances. In Figure 5.27, the range of I_{Lo} is small since the converter is designed for the application of low power applications. It is obvious to understand that the conventional SRBC does not perform with a high efficiency (η = 77 % at I_{Lo} of 1.5 A) because of unavailability of ZVS mechanisms to reduce the switching losses.

The efficiency of the SRBC introduced by [51] is slightly lower compared to the new SRBC since the floating turn-on voltage of S_1 has not been reduced. This adds to the additional switching loss during the entire turn-off of S_1. In comparison, the efficiency of the new SRBC circuit has indicated a small improvement of approximately 3 % to [51] and 8 % to the conventional.

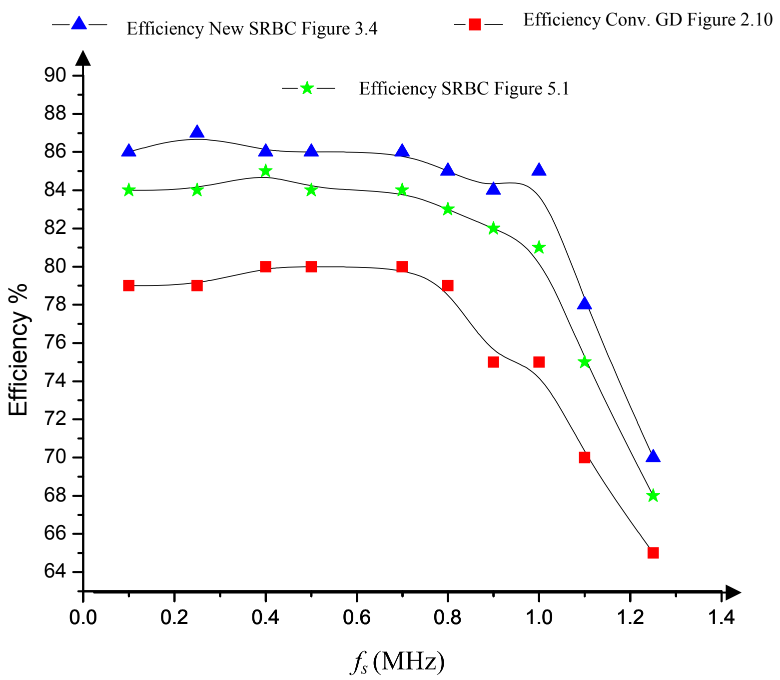

Figure 5.28 Efficiency versus Switching Frequency for $D_{S1} = 0.20$, $D_{S2} = 0.75$ and $T_D = 15$ ns of Three SRBC

When switching frequency increases, the SRBC circuit experiences high power dissipation and energy loss. However, with the aid of soft-switching operation, these losses can be reduced. This is shown in Figure 5.28 where the efficiency of new SRBC is higher compared to [51] and conventional. At a lower switching frequency below 500 kHz, the conventional SRBC operates efficiently at 80 %. As f_s increases, its efficiency drops drastically due to high switching loss in S_1 and S_2.

For new SRBC circuit, the efficiency is 86 % within 1 MHz range compared to [51] of only 84 %. Due to the fact that the high power switch used in the simulation inhibits a maximum f_s rating of only 1 MHz, a higher applicable f_s will impair the efficiency.

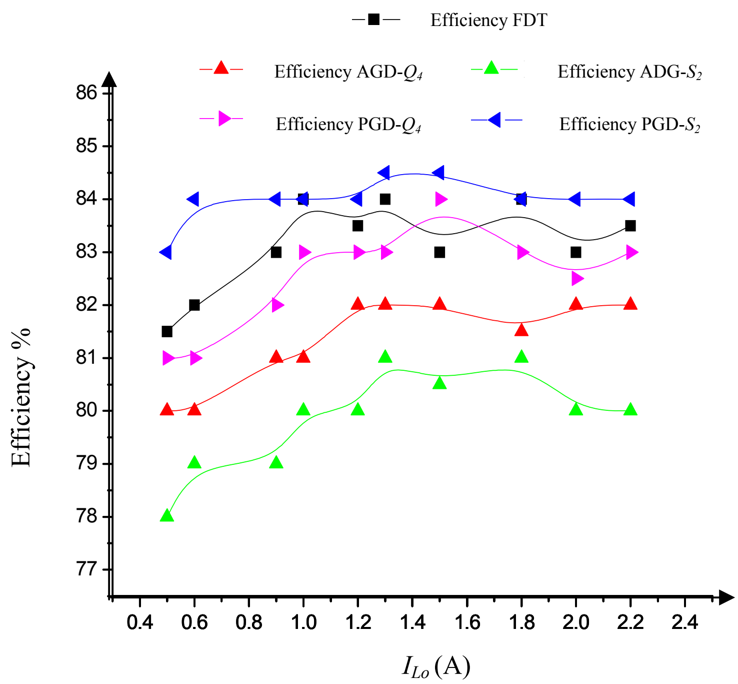

Figure 5.29 Efficiency versus Inductor Load Current for $D_{S1} = 0.20$, $D_{S2} = 0.75$ and $T_D = 15$ns on New SRBC of Three Gate Drive Control Schemes

It is observed in Figure 5.29 that the use of PGD control scheme produces higher efficiency of more than 82 % at I_{Lo} of 1.5 A compared to AGD and FDT. In addition, the application of AGD-Q_4 produces better efficiency compared to AGD-S_2 by only 2 % because D-CRGD helps control $V_{gs,Q4}$ turn-on for S_2 pulses. This indicates the necessity of gate drive circuit in SRBC. However, PGD control scheme does not require any intermediate D-CRGD circuit to achieve high efficiency. The application of PGD-S_2 can reduce the switching loss effectively as S_2 gate can intelligently be adjusted and controlled with respect to the detection of T_D in the circuit.

In FDT scheme, the driving pulses given to Q_1-Q_4 switches can be precisely controlled by independent PWM generators. It is found that FDT scheme can also manage to cap the efficiency as high as 83 % which is comparable to PGD-S_2 implementation. Due to its simplicity, the complemented signals generated at the gates of S_1 and S_2 are easy to control and monitor on new SRBC circuit.

5.10 Chapter Summary

The extension simulation work looks into several factors which influence the performance of new SRBC circuit. It is found that the new SRBC can operate effectively at 1 MHz compared to conventional. The S_2-duty ratio of 0.75 has shown the least switching loss in the switch.

Several gate drive control schemes have been simulated and the results indicate superior performance of FDT and PGD-S_2. FDT is simple and can be driven correctly with small dead time. Therefore, the duration of body diode conduction has been minimized. Nevertheless, PGD-S_2 is the best option whilst AGD can also maintain high level of efficiency of new SRBC. However, AGD scheme generates more switching loss due to longer adaptation time between the controller and the detection of dead time.

CHAPTER 6

CONCLUSIONS

6.1 Resonant Gate Drive Circuit

Switching losses are the major contributor in RGD circuit design especially when operating in megahertz frequency. Based on the design parameters used in the S-CRGD, several limiting parameters have been identified which affect the performance of the circuit. Using PSpice simulator, the D, T_D and L_r have been thoroughly studied to identify the best operating values for the driver. The simulated results have shown close proximity with the experimental except for the i_{Lr}.

The L_r can be used to verify the performance of the S-CRGD circuit by optimizing the Q-factor. Q-factor is a quality indicator which characterizes the rate of energy dissipation in resonant system. It depends on circuit topology, f_s and type of power switch used. For example, a higher L_r will result in more energy to dissipate and more area consumption on electronic board respectively. By interpolating the gate resistance power loss and L_r, this leads to the selection of optimized Q-factor value. Hence, the optimization of power losses and switching capability are then justified.

Well defined pulses contribute to a high accuracy of T_D between switches for the application of D-CRGD circuit. Utilizing the optimized parameter values, each of the resulting gate voltages of S_1 and S_2 switch has generated well defined pulses for the new SRBC operation.

6.2 Synchronous Buck Converter Circuit

A new SRBC circuit has been proposed having the capability in ZVS operation with respect to new configuration of series L-C connected in parallel to the switch. From this, the traditional turn-off drain voltage of the switch has been reduced. Consequently, this has improved loss savings of the converter significantly. Using a constant load value of 10 Ω and switching frequency of 1 MHz, both simulation and experimentation results in terms of drain current of switches and load current have presented small difference in margin.

The study is extended to evaluate the impact of varying load, f_s and T_D of switching MOSFETs on the performance of the new SRBC circuit. Three different SRBC circuits are chosen in the investigation. In the experiment, the switching losses in the new SRBC circuit are the lowest compared to others. Similarly, this justifies for the different load resistances using simulation.

6.3 Gate Drive Control Schemes

The FDT, AGD and PGD schemes are used to evaluate the performance of the new SRBC circuit. A direct square-waved pulse generated by the function generator is used as FDT scheme whereas the AGD and PGD are derived from the combinational logic and analog circuits. It is found that the D-CRGD has managed to solve issues pertaining T_D and body diode conduction loss and hence reduce switching loss.

When using PGD as control scheme, the switching loss has improved slightly compared to the FDT. However, this scheme is not easy to implement. It is determined that FDT can manage a low body diode conduction time before the shoot-through current can occur.

On the other hand, the AGD and PGD schemes are beneficial to improve the gate driving loss but their implementations are more complex. Comparatively, FDT scheme is easy to apply and eventually gives better advantages in converter's performance. Therefore, the stand-alone FDT control or a direct implementation of PGD-S_2 schemes can be chosen in the design of high frequency SRBC circuit.

6.4 Contribution of Work

This work has introduced several contributions, which are as follow:

a) If incorrect value of L_r is chosen in S-CRGD circuit, the oscillation of i_{Lr} will be generated and consequently induces additional loss. Here, the L_r has been optimized of which is then applied to the D-CRGD network.

b) The new SRBC employing paralleled LC-switch has reduced losses. Having this similarity in the previous design for the controlled switch, S_1, the LC parallel link is also applied in the new design to S_2 as well as reducing the turn-on drain voltage. This can be seen from the non-intersected gate and drain voltages of S_1 and S_2. In addition, the on-state drain voltages of both switches have also been reduced to minimum compared to the conventional SRBC. This eventually reduces the entire turn-on switching losses.

c) Using simulation, the new SRBC has proven the capability in sustaining variable load conditions and switching frequencies when using precise T_D and D conditions. The different in gate drive control schemes have also been introduced to evaluate the performance of new SRBC. The finding has suggested that the FDT scheme is the easiest solution.

6.5 Future Work

This work has yet to require further improvement in terms of following:

a) Even though the work has been experimentally verified as explained in Chapter 5, the simulation results discussed in Chapter 6 have yet to be verified experimentally.

b) In addition, the implications of the new SRBC operating in three different regions such as in below, at and above resonant are the other important parameters to be studied.

c) At such, the frequency has to be pushed higher than 1 MHz. To do this, the selections of components have to be correct and the implementation of chip-based low-loss devices, thermal management and programmable gate drive and feedback control systems are necessary.

d) Moreover, in order to have a high power density module, the new SRBC has to come in a small board size having higher efficiency, especially when the components in terms of chip-based surface-mount are used.

e) In fact, the components' and pcb/wiring parasitic effects will be considered to allow for lesser EMI and harmonic effects. This will require further detailed analysis and complex on-board measurement.

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1. N. Z. Yahaya, K. M. Begam and M. Awan "Simulation of an Inductive Coupled High Frequency Resonant Gate Driver" in *IEEE Ind. Informatics*, Jul. 2008, pp. 1523-1527.

2. N. Z. Yahaya, K. M. Begam and M. Awan "Switching Loss Analysis of a Diode-Clamped Resonant Gate Driver Network" in *UMS Science and Tech. Sem.*, Oct. 2008, pp. 471-475

3. N. Z. Yahaya and T. M. Dung "Design and Improvement of Soft-Switched Quasi-Resonant Boost Converter" in *2nd UMS Eng. Conf.*, Dec. 2008, pp. 582-587.

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2. N. Z. Yahaya, K. M. Begam & M. Awan. "A Review on Design Considerations & Limitations of Resonant Gate Drive Circuit in VHF Operations", *IAENG Eng. Lett.*, Vol. 17, Iss. 2, pp. 54-62, Jun 2009.

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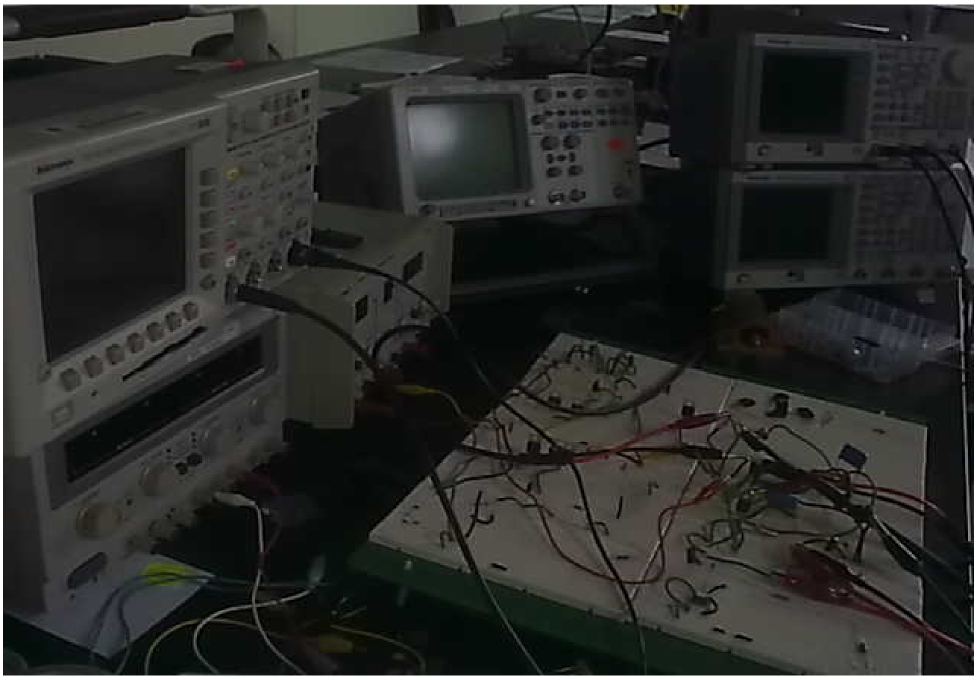
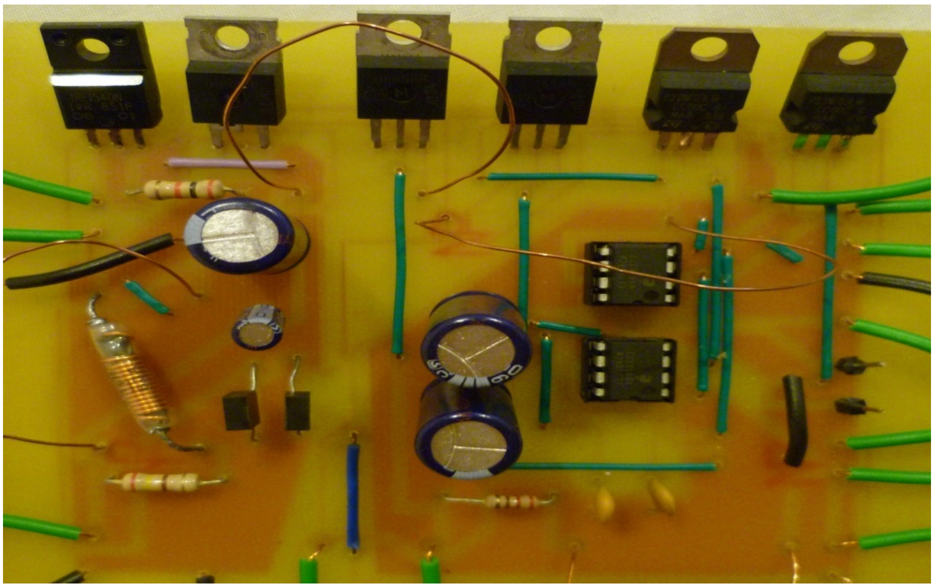
APPENDIX A

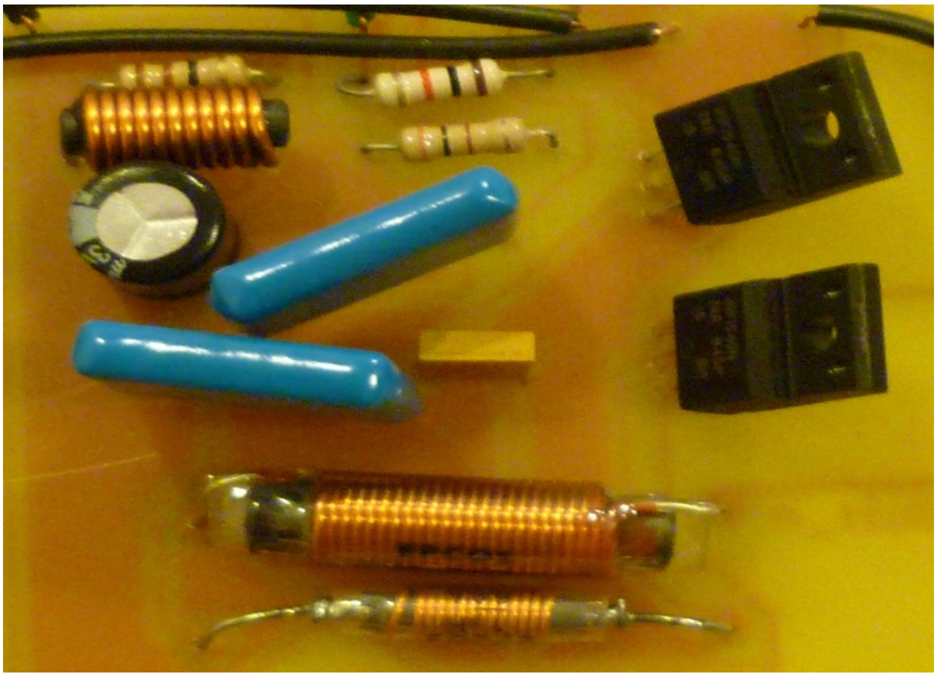


App. A1 Measurement Setup

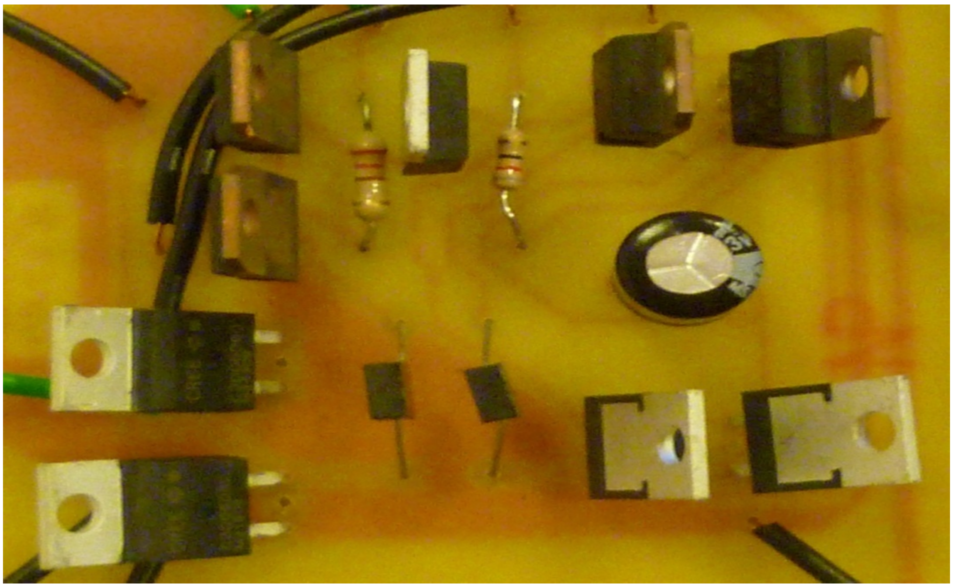


App. A2 S-CRGD Circuit on PCB

APPENDIX B

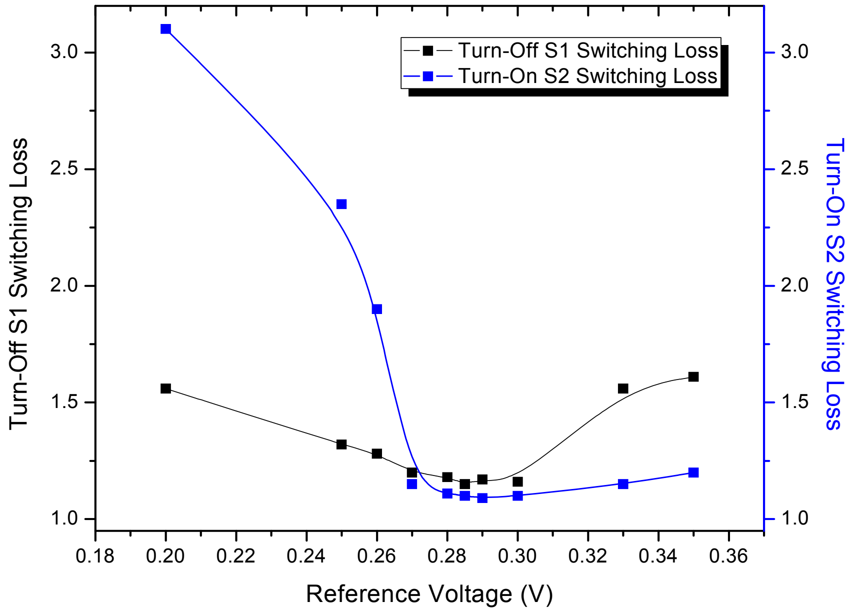


App. B1 New ZVS-SRBC Circuits on PCB

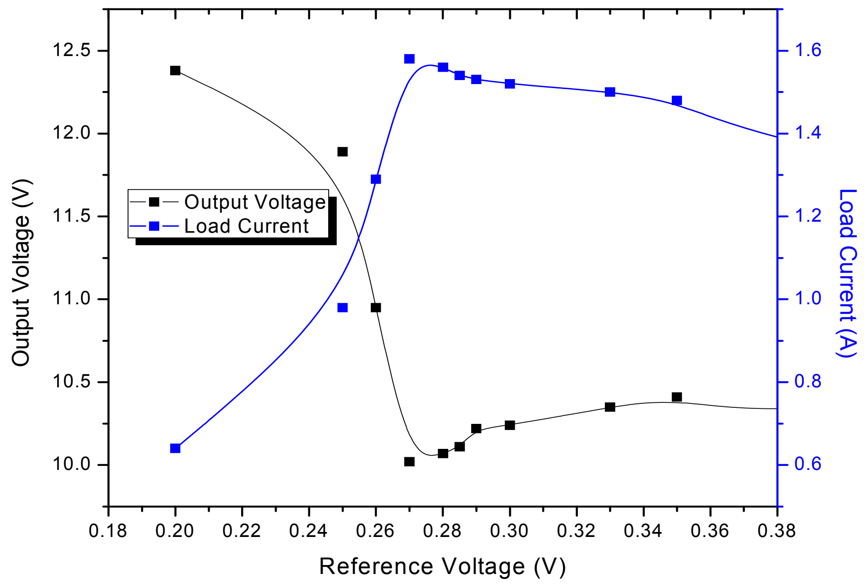


App. B2 D-CRGD Circuit with Bootstrap Units

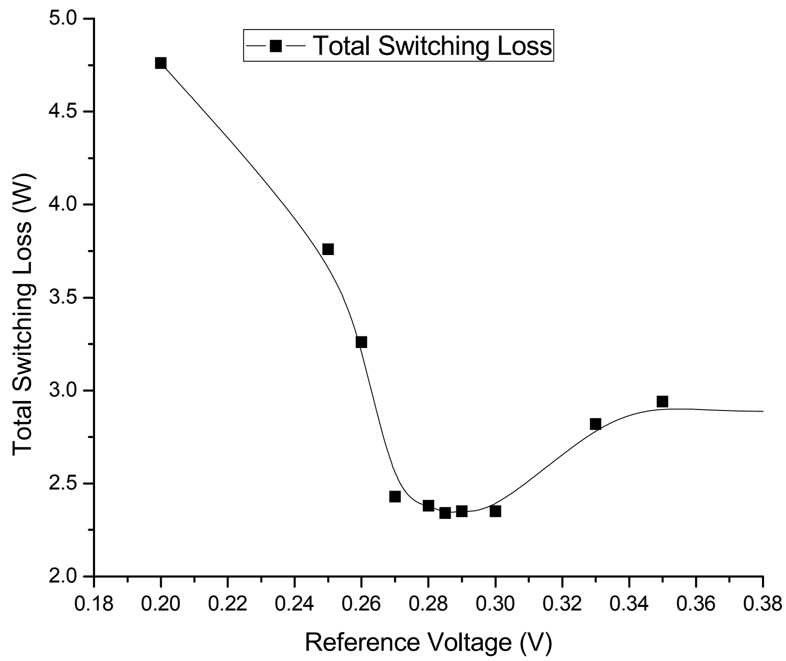
APPENDIX C



App. C1 Relationship between P_{S1} and P_{S2} Versus V_{ref}



App. C2 Relationship between Output Voltage and Load Current Versus V_{ref}



App. C3 Total Switching Loss Versus V_{ref}