EXPERIMENTAL VERIFICATION OF A DIODE-CLAMPED RESONANT GATE DRIVER NETWORK

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By

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CERTIFICATION OF APPROVAL

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TRONOH, PERAK

June 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

KHAIRUL AZHAR BIN ISHAK

ABSTRACT

A Diode-Clamped Resonant Gate Driver Network is popular in high switching frequency applications. The objective of this project is to perform analysis on the overall performance and efficiency of converter by doing experiment. The duty ratio, resonant inductor value and the dead time are the parameters that influence on the switching losses and other losses in the gate drivers. From the previous work which is done through simulation, it is found that optimized value of inductor is 9nH. By doing experiment work, to maximize capability of RGD circuit, the varied duty ratio by constructing PWM generation network, fixed inductance value of almost 9nH and varied the dead time has been chosen. In the end, it is found that the overall performance for high switching frequency converter are easily influenced by the low capability of the equipments and circuit constructions in the experiment that may lead to the switching losses in the network.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

PWM	Pulse Width Modulation
MOSFET	Metal Oxide Field Effect Transistor
DC-RGD	Diode Clamped-Resonant Gate Driver
D	Duty Ratio
DC	Direct Current

CHAPTER 1
INTRODUCTION

1.1 Background of study

The purpose of resonant gate driver is to improve the gate drive efficiency by means of recovering the energy stored in the input capacitance of the power MOSFET. Usually, to accomplish this task, a resonant circuit is used. Hence, at least an inductor is necessary to be included in the gate drive network [1]. In recent years, there are many resonant gate drive have been introduced such as the diode-clamped resonant gate driver. This network is studied to explore the limitations of resonant current based on fixed inductance value.

1.2 Problem statement

In order to achieve high efficiency in high switching applications such as resonant gate driver, to be more specific the diode-clamped Resonant Gate Driver (RGD), too many parameters should be considered even though this network is recognized successfully in recovering the energy in the circuit without high dissipation at the input source [2]. Hence, there are some restrictions in RGD circuit design which is inductor value and its current must be optimized and followed to certain factors. The study is to verify and determine the effects on the inductor and its current value by varying the applied pulse width to the switches (gate drivers) in the diode-clamped RGD network, whether it will create higher switching losses that may lead to the low efficiency of this network.

In this project, Pulse width modulation (PWM) is generated within its duty cycle of 20% to 60%, by considering the dead time value and effects of pulse width to the resonant current in the RGD network. The selection of pulse width modulator

should be clear and it operates in high frequency range of 1MHz in order to get the best result of PWM signal that will be used together in RGD network analysis.

1.3 Objectives

During completing the work, there are some objectives need to be achieved, which are:

- To do study and understand about diode-clamped resonant gate driver network.
- To design the PWM generation network.
- To integrate PWM generation network with DC-RGD
- To validate the diode-clamped RGD network by experimentally.

1.4 Scope of study

Throughout this project, the study listed as follows:

- Conceptual and theory.

  In this stage, all information related with the diode clamped resonant gate driver network are collected and reviewed.

- Construction and experimenting.

  After all ideas and information gathered, PWM generation network will be constructed and tested. Next, it will be integrated with the diode clamped resonant gate driver before the experiment of the whole circuits can be implemented based on the specifications in the voltage supply and in the switching frequency.

- Overall analysis

  Throughout the experiment, all results obtained should be analyzed and discussed. Then, its performance assessment will be handled and validated according to the Pspice simulation results.

CHAPTER 2
LITERATURE REVIEW

2.1 Pulse width modulation

A modulation technique that generates variable-width pulses to represent the amplitude of an analog input signal. Like its fixed-width pulse density modulation (PDM) cousin, the output switching transistor is on more of the time for a high-amplitude signal and off more of the time for a low-amplitude signal. PWM is widely used in the common "switch-mode" power supplies that convert AC power to DC for computers and other electronic devices. It is also used to control the speed of a DC motor [3].

Pulse width modulation is used to reduce the total power delivered to a load without resulting in loss, which normally occurs when a power source is limited by a resistive element. The underlying principle in the whole process is that the average power delivered is directly proportional to the modulation duty cycle. If the modulation rate is high, it is possible to smooth out the pulse train using passive electronic filters and recover an average analog waveform[4].

High frequency pulse width modulation power control systems can be realized using semiconductor switches such as MOSFET. Here, the discrete ON or OFF state of the modulation itself can be used to control the switches, thereby controlling the voltage or current across the load. The major advantage with these types of switches is that the voltage drop across it during conducting and non-conducting states, is ideally zero[4]. Figure 1 is the example of consistent PWM signal:

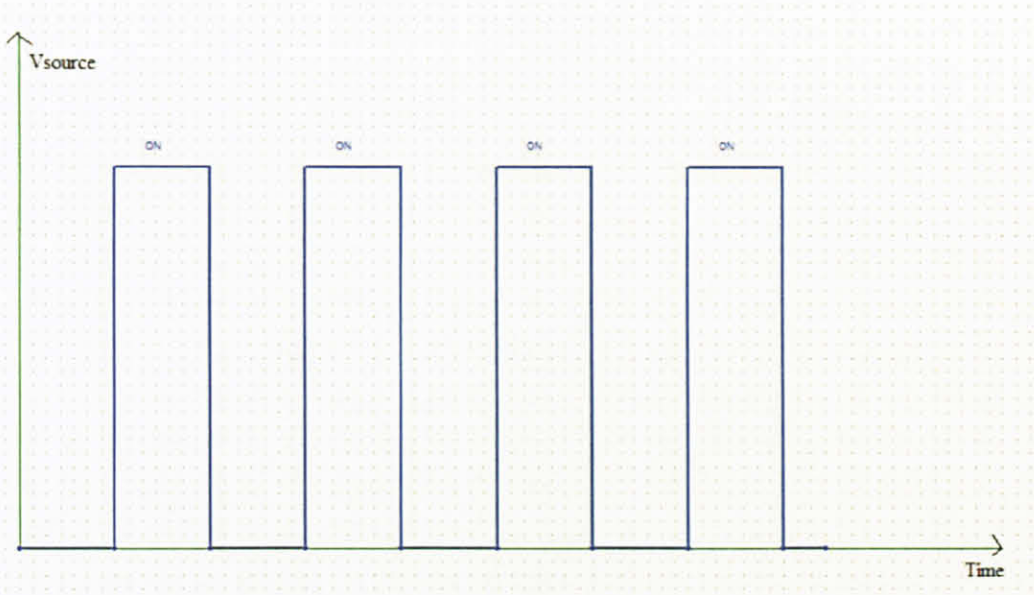

Figure 1 The example of PWM signal

In this project, PWM will be applied to the gate driver of diode clamped resonant gate driver with the different duty ratio (20%-60%). Basically, there are two pulses as in figure applied to the MOSFET Q_1 and Q_2 that is complementary turn-on and turn-off. For this circuit, supposed that both MOSFETs do not turn-on at the same time to avoid shoot-through [5].

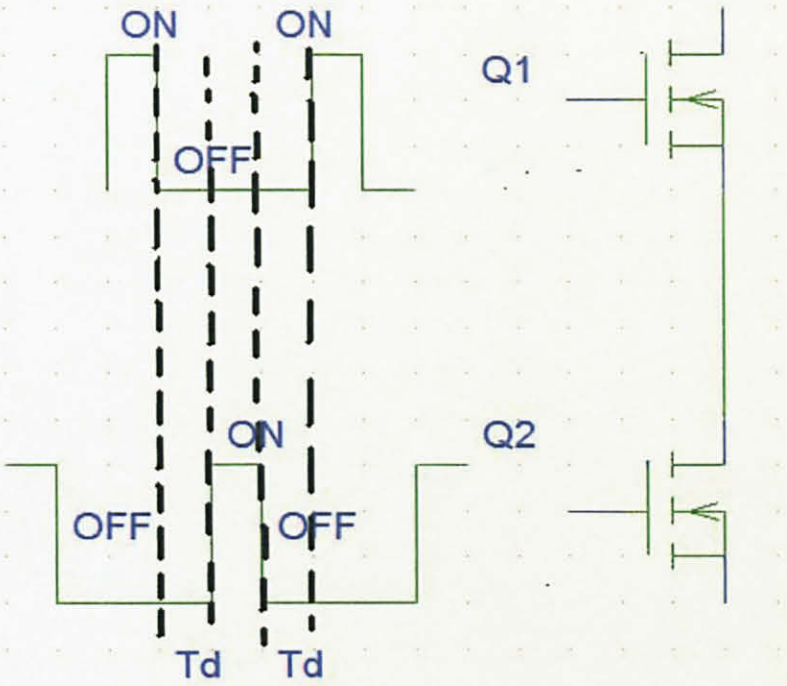

Figure 2 Synchronous switching using PWM

2.2 Duty ratio or duty cycle

Duty cycle is the proportion of time during which a component, device, or system is operated. In the switch duty cycle, this is defined as the ratio of the on duration of the switch to the switching time period.

Duty cycle,

$$D = \frac{t_{on}}{T_s} \qquad (1)$$

Where t_{on} is duration that the switch ON and T_s is the switching time [6].

Duty cycle also can describe as the duration of ON-time in one complete switching cycle [5]. In this project, by varying duty ratio, D will determine the charging and discharging current time of the resonant inductor, τ_c as given in (2) where C_{in} is the input capacitance of S_1 in DC-RGD circuit.

$$\tau_c = \frac{L_r}{\sqrt{\frac{L_r}{C_{in}}}} \qquad (2)$$

2.3 Dead time, t_d

The dead time is the period of none of the switch (MOSFET) is in turn-on condition. It is between the turn-on time of MOSFET Q_1 and MOSFET Q_2. During this period, there is no signal generated and applied to any switches. The important of the dead time is to avoid shoot-through or cross conduction between the gates of Q_1 and Q_2, since both switches conducting complementarily [5]. Practically, the significance of applied the dead time in the signal is to make sure that the pulses applied must be complement to each other. It is shown in figure 3.

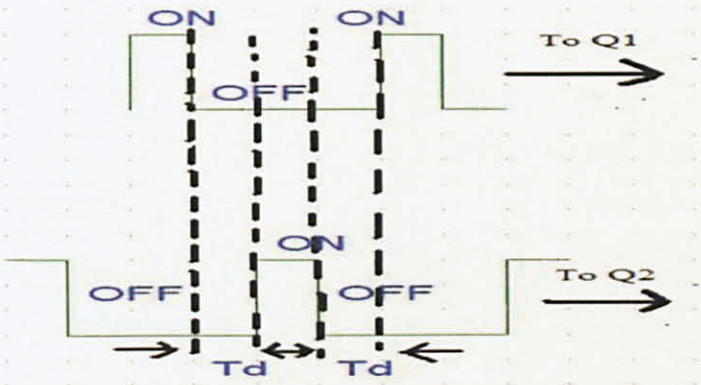

Figure 3 The effect of dead time on driving pulses

2.4 Cross conduction

Cross conduction is a phenomenon which Q_1 and Q_2 are either fully or partially turned on when it provides a path for current to shoot-through from supplied voltage to the ground [9]. It is also can happen if the induced voltage is larger than gate threshold voltage of Q_2, which could be turned-on while Q_1 is turn-on. This may lead to the excessive power dissipations on both switches and make the devices failure to operate [5]. Hence, choosing the right MOSFET and the right dead time will eliminate this phenomenon.

2.5 Synchronous buck-converters

Buck converter is a step-down converter produces a lower output voltage than the DC input voltage, V_s. It is widely used in electronics field as its main application is in regulated DC power supplies and DC motor speed control [6]. A DC-RGD circuit is one of the synchronous buck-converter designs. Synchronous rectification increases the efficiency of a buck converter by replacing the Schottky diode with a low-side N-channel MOSFET because the resultant voltage drop accross MOSFET can be smaller than forward voltage drop of Schottky diode[9]. Its topology as shown in figure 4:

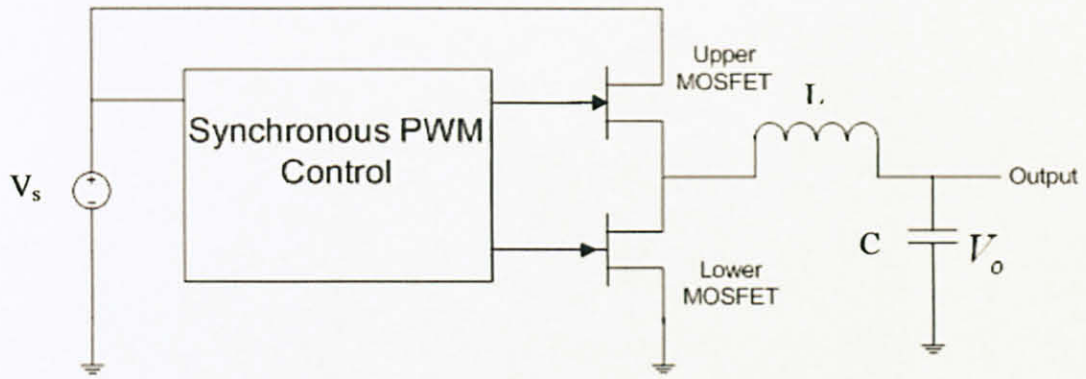

Figure 4 Synchronous buck-converter topology [10].

The average output voltage of buck converter can be calculated as:

$$V_o = \frac{t_{on}}{T_s} = DV_s \qquad (3)$$

By varying the duty ratio, D the output voltage can be controlled. Usually, two controlled switches, upper MOSFET and lower MOSFET, to achieve unidirectional

power flow from input to output. The converters also use one capacitor and one inductor to store and transfer energy from input to output. They also filter or smooth voltage and current. When the switch, upper MOSFET is on in ON-time, t_{on} the switch conducts the inductor current, i_L. When it is in OFF-time, the lower MOSFET will take over to turn-ON to circulate inductor current and make path for inductor current to discharge. The average inductor current must be equal to the DC current through the load [6]. It is express as in (4).

$$i_{L,average} = I_0 = \frac{v_0}{R} \qquad (4)$$

Where,

I_0= output current

V_0= output voltage

R= load for converter

The output capacitor is assumed to be so large as to yield $vo\ (t) = Vo$ .However, the ripple in the output voltage with a practical value of capacitance can be calculated as in (5) and (6).

$$\frac{\Delta v_0}{V_0} = \frac{\pi^2}{2} t_{off} \left(\frac{f_c}{f_s}\right) \qquad (5)$$

Where f_s is a switching frequency,

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad (6)$$

From the equations above, the voltage ripple can be minimized by selecting a corner frequency, f_c of the low pass filter at the output such that $f_c << f_s$. Besides, the ripple is not depend on output load power, as long as the converter is operates in continuous conduction mode [9].

2.6 Limitations and implications on diode-clamped RGD circuit

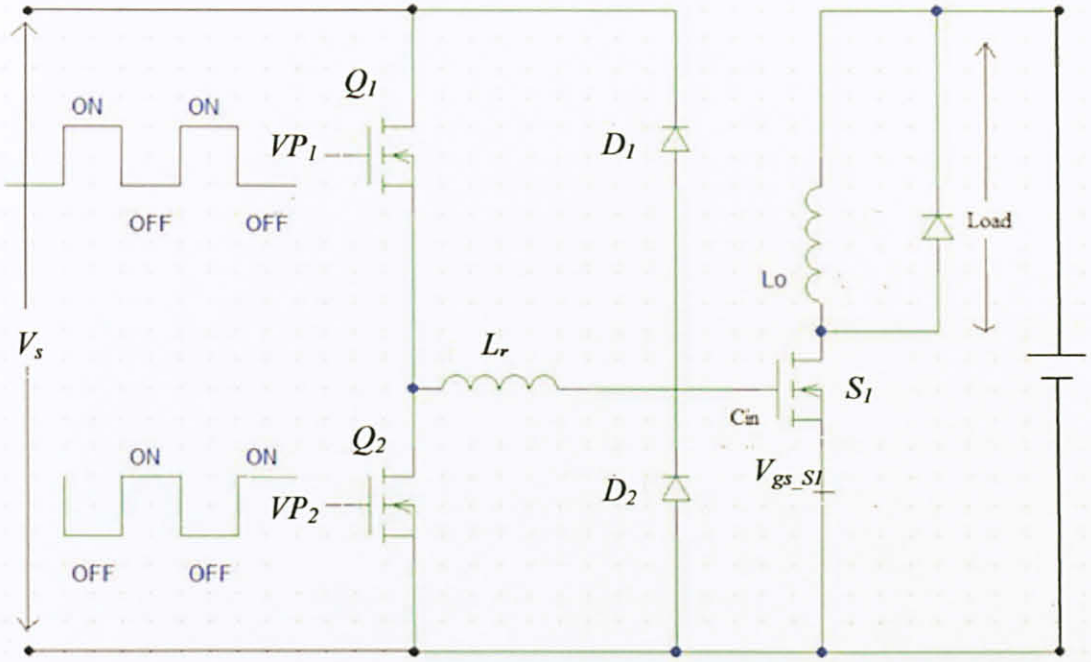

Figure 5 The diode-clamped resonant gate driver with voltage pulses[2]

Based on [5], high power MOSFET is chosen as a switch because it could operate up 5MHz. But, there are limitations and implications of duty ratio, D, dead time, t_d and resonant inductor, L_r in RGD circuit. In many RGD network, driving switches contribute more losses compared to losses due to conduction and gate [5]. Based on figure 5, the gate is driven by a voltage source, V_s of 12V. By applying pulse VP_1 and VP_2 to Q_1 and Q_2 respectively will cause switch Q_1 and Q_2 conducting complementarily. The period of turn-on of switch Q_1 will cause the inductor current to increase and it is charged to the maximum value as well as V_{gs_S1}. Hence, it will exponentially clamp up the V_{gs_S1} at 12V. The duration time of charging current through the inductor is depends on the value of L_r. Once Q_1 is turn-OFF, Q_2 will turn-ON after some specified time. This duration of time is called dead time, t_d . The clamped voltage of 12V at V_{gs_S1} will discharge back to zero. The resonant inductor current is charged again to its maximum value but in negative direction. With the considerations of the duty ratio, D, L_r and t_d are varied in order to get optimized switching losses in the circuit.

2.6.1 *Effect of duty ratio, D*

With the operating frequency of 1MHz, duty ratio of V_{gs_S1} can be determined by providing pulse width of VP_1 and VP_2. However, there is very limited in the literature discussing on the effects on the resonant current, i_{Lr} and its time taken to charging and discharging and the effects on V_{gs_S1}. In order to achieve this, the variable duty cycle should be applied in generating the pulse width. The sufficient ON-time switching is also important because the sufficient time will enables i_{Lr} to flow without disruption [5]. By increasing the pulse widths in VP_1 and VP_2 will cause the duty ratio of V_{gs_S1} to increase and reducing the pulse widths may results i_{Lr} forced discharging and generated unwanted oscillation at the end of V_{gs_S1}. As a result, this will increases dissipation and gives rise to stress in the DC-RGD circuit according to [5]. In this project, the intentions are to provide pulse widths applied to Q_1 and Q_2 with variable duty ratio of 20%, 30%, 40%, 50% and 60%.

2.6.2 *Resonant inductor effects, L_r*

As L_r value increases, the charging and discharging time of i_{Lr} [2]. The relationship between i_{Lr} and R_g is given in (7), where R_g is the total gate resistance in the RGD circuit and its value is estimated around 1.3Ω to 1.7Ω whereas, C_{in} is internal input capacitance of S_1 .When the turn-ON duration, the current of resonant inductor, i_{Lr} will increase to its maximum value before it is discharging. The fixed value of resonant inductor has been optimized to 9nH for its simplicity during the experiment work. For all t_ds, it is found that optimized value is around 9nH according to [5].

$$i_{L_r}(t) = \frac{2V_s}{\sqrt{\frac{4L_r}{C_{in}} - R_g^2}} e^{-\frac{R_g}{2L_r}t} \sin\left(\frac{\sqrt{\frac{4L_r}{C_{in}} - R_g^2}}{2L_r}t\right) \qquad (7)$$

2.6.3 *Effects of dead time, t_d*

The dead time for this project is not specified because resonant inductor value has been optimized to the fixed value. From the previous explanation, dead time is set up to avoid shoot-through or cross conduction between Q_1 and Q_2 in the

RGD circuit. By fixing the value of L_r and varying the dead time, i_{Lr} will be observed whether it will cause in power losses at V_{gs_S1}.

2.7 Power MOSFET

It is voltage controlled device that is used in many electronics application circuit. In DC-RGD circuit, switches Q_1 and Q_2 both are MOSFET that require the continuous of a gate source voltage in order to be in the ON-state. MOSFET is used because it can operate in much higher frequency at a lower voltage. However, at high voltage MOSFET still has some limitations. According to the intrinsic characteristic of MOSFET, it is produce a large on-resistance which increases excessively when the devices breakdown voltage is raised [6]. Figure 6 and figure 7 is shown the symbol and circuit model for MOSFET.

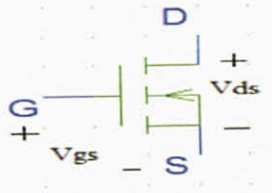

Figure 6 Symbol for N-channel MOSFET [6]

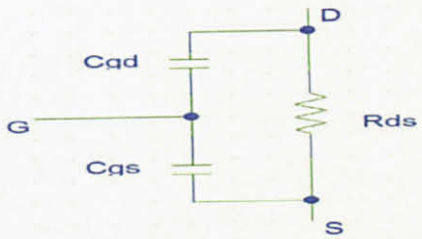

Figure 7 MOSFET equivalent circuit in the ohmic region [6]

2.8 Switching losses

Switching losses has to be considered in the analysis of this RGD circuit because it is important to determine its efficiency. For this RGD circuit, the switching is involving 2 MOSFETs which are turn-on complementarily during each switch

transition. Figure 8 shown the graph of switching losses occurs in MOSFET.

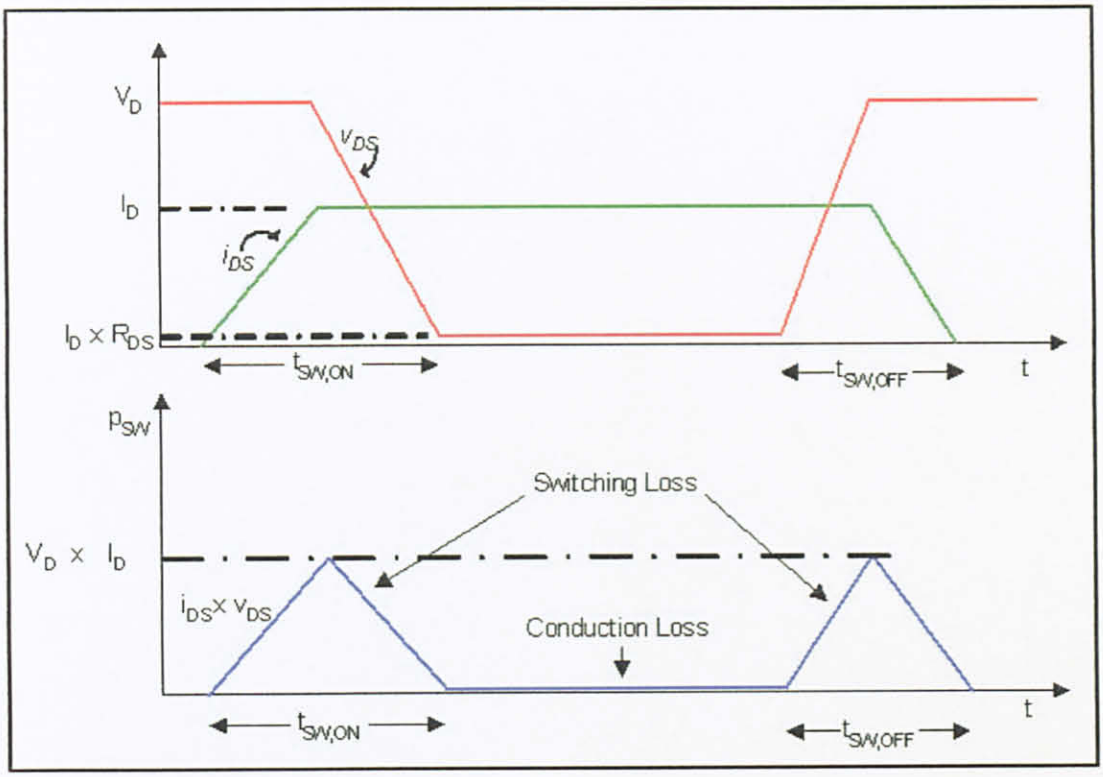

Figure 8 Switching losses occurs as MOSFETs transition between fully ON and fully OFF [8]

The graph of drain-source voltage, V_{DS} and drain-source current, I_{DS} is plotted to explain the switching losses occur in MOSFET. Based on the upper graph in figure 8, during the ON-time and OFF-time of charging and discharging of capacitance in MOSFET, there is non-instantaneous voltage and current transition occurs. As plotted in the graph, I_D must be transferred to MOSFET before V_{DS} decreases to final ON-state which is I_D x R_{DS} [8]. Same goes to the MOSFET in turn-OFF state where V_{DS} will increases to its final OFF-state before current is transferred to MOSFET. As a result, there is overlap between voltage and current waveform that is represented as switching loss in lower graph in figure 8.

The switching loss is calculated using the equation (8), (9), (10) and (11).

$$P_{switching} = \frac{v_D}{2} \times [t_{on} + t_{off}] \times I_D \quad (8)$$

$$P_{on} = D \times I_D^2 \times R_{DS} \quad (9)$$

$$P_{total} = P_{switching} + P_{on} \quad (10)$$

$$n = \frac{P_{in} - P_{total}}{P_{in}} \times 100 \quad (11)$$

Where:

$P_{switching}$= Losses during turn on and turn off (W)

P_{on} = Conduction losses when the switch is on (W)

P_{total}= Total losses (W)

P_{in} = Input Power (W)

n= Efficiency (%)

V_D= drain-source voltage during time off (V)

fs = Switching frequency (Hz)

t_{on} = Time taken for the switch to turn on (s)

t_{off} = Time taken for the switch to turn off (s)

I_D = Conduction current (A)

D = Duty Cycle

R_{DS} = "On" resistance of MOSFET

V_{ds}= Drain-source voltage

CHAPTER 3
METHODOLOGY

3.1 Project planning

This project is about to construct the circuit of two network between PWM generation network and the diode-clamped RGD network. Then, the experiment between these two networks can be implemented. A lot of research has to be done to complete this project. With this report, gantt charts are attached in appendix A and appendix B. Figure 9 shows the flowchart of the methodology.

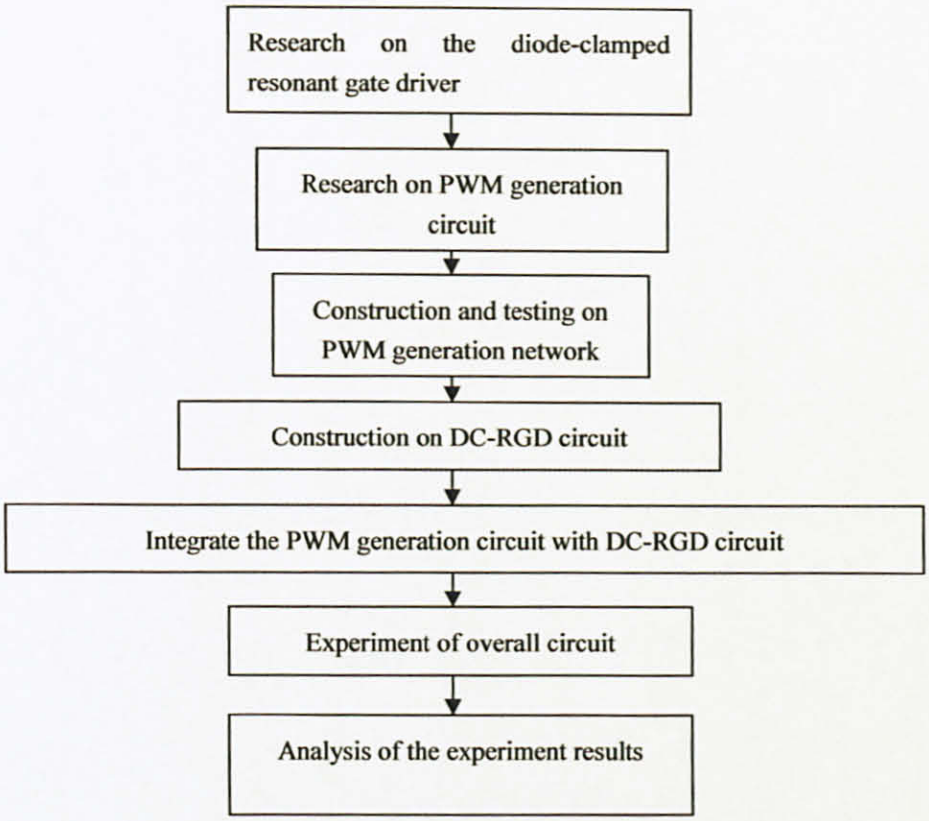

Figure 9 Methodology approach

3.2 Tools and equipments required

Basically, this project is a research based experiment work to validate the simulation. The work has been started by researching all knowledges related to this topic. Hence, there are some specific equipment and components required to implement it.

Table I The detail for the equipments

Equipment/component	Purpose	Details
DC Power supply	To generate wide range of DC signal	Model no. :GPC3030DQ Available in the laboratory
Function generator	Provide signal output to the circuit	Model no. : GPG 8255A Available in the laboratory
Oscilloscope	To display and analyze the waveform	Model no.: CS4125 Available and can be used in the laboratory
PWM generation circuit	To provide wide range of pulse width	Using three main circuits which are PWM generate circuit, synchronization circuit and output buffer to apply adjustable duty ratio
Diode-clamped resonant gate driver	As a test circuit	Using the specified components with fixed inductance value of 10nH and varied dead

		time

3.3 Block diagram

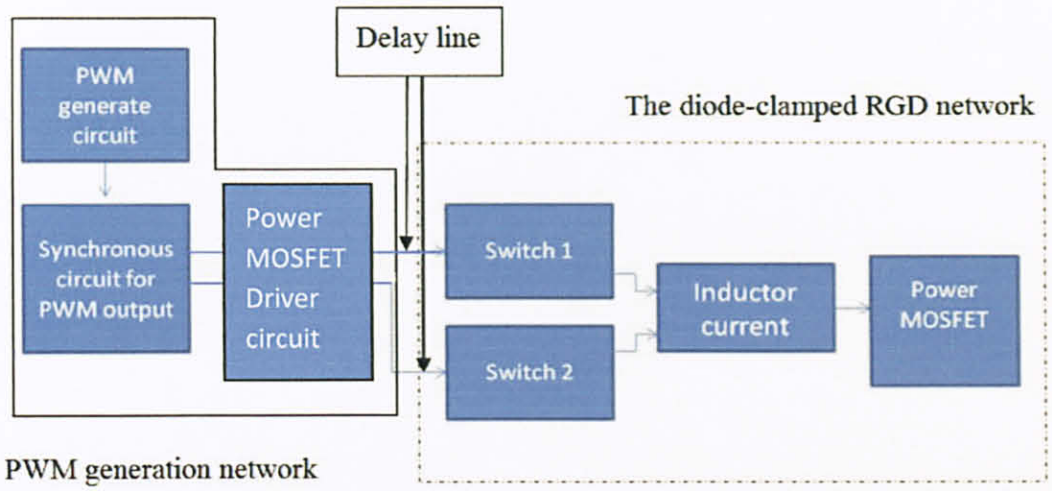

Figure 10 Proposed block diagram for overall circuit

The figure 10 shows the block diagram of the whole network used throughout this project. The entire block diagram has its own specification and proposed configuration. The PWM generation network will generate the pulse widths to be applied to the switch 1 and switch 2 (both are MOSFET). There are two PWM output signals which are used to drive switch 1 and switch 2 respectively. Apart from that, delay line will be applied at the same time to create finite delay time of the pulse width for the RGD network. Hence, the analyses on the resonant inductor current are then performed.

3.3.1 PWM generation network

This section consists of three main circuits, PWM circuit, synchronous circuit for PWM and PWM output buffer. PWM circuit is responsible to provide PWM signals to the switch 1 and switch 2 respectively having different value of pulse width leading to the different generation of duty ratio. Whereas, synchronous circuit for PWM is needed to synchronize the timing of both MOSFETs. This circuit takes both frequency of the converter and frequency of

the synchronization signal. They are then integrated before connected to DC-RGD network.

3.3.2 The diode-clamped resonant gate driver network

The RGD network configuration is the main circuit to be analyzed. The proposed PWM generation circuit will be integrated with this circuit to validate the simulation.

3.4 Recommended circuit

3.4.1 Intersil ICM 7555

The PWM signals can be generated in many ways. Intersil ICM 7555 is a generating IC that uses analogue method to produce PWM signal. This chip has been chosen because of its features in providing adjustable duty ratio in astable operation mode. Furthermore, it can be operated in high speed operation up to 1MHz. Figure 11 shows the astable circuit.

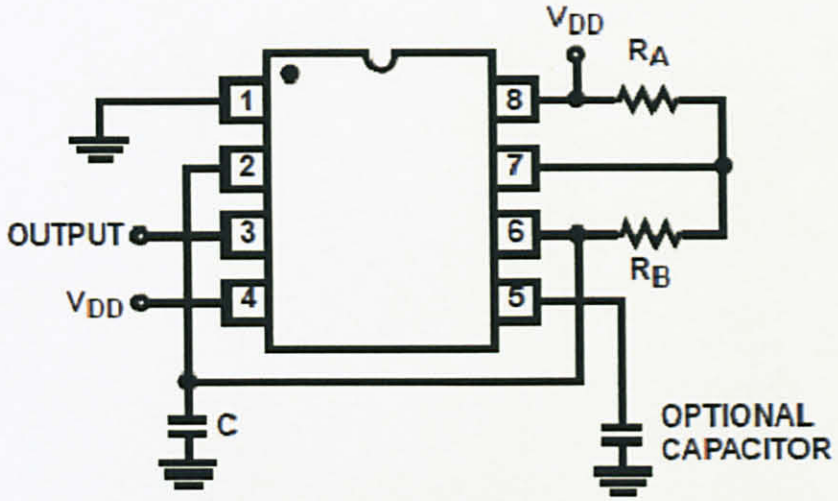

Figure 11 Astable circuit chip [7]

The value of duty ratio is controlled by the value of R_A and R_B. By selecting R_1 and R_2, the duty cycle of the output can be adjusted. Since C charges through $R_1 + R_2$ and discharges only through R_2, duty cycles

approaching a minimum of 50 % can be achieved if $R_2 >> R_1$ so that the charging and discharging times are approximately equal. It is expressed as (12), (13), (14) and (15):

$$t_{on} = 0.7(R_1 + R_2)C_1 \quad (12)$$

Where,

$$R_1 = R_A \, , \; R_2 = R_B$$

$$t_{off} = 0.7R_2C_1 \quad (13)$$

$$T_s = t_{on} + t_{off} = 0.7(R_1 + 2R_2)C_1 \quad (14)$$

$$F = \frac{1}{T_s} = \frac{1.44}{(R_1+2R_2)C_1} \quad (15)$$

For making duty ratio less than 50%, some modification has to be done [7]. By adding the diode such as in figure, C_1 will charge through only R_1 and discharge through R_2. To achieve this, it is necessary to make R_1 less than R_2. Under this specification, the expression for duty ratio, D is:

$$D = \frac{t_{on}}{T_s} \quad (16)$$

The other formula is expressed as:

$$t_{on} = 0.7R_1C_1 \quad (17)$$

Where,

$$R_1 = R_A \, , \; R_2 = R_B$$

$$t_{off} = 0.7R_2C_1 \quad (18)$$

$$T_s = t_{on} + t_{off} = 0.7(R_1 + R_2)C_1 \quad (19)$$

$$F = \frac{1}{T_s} = \frac{1.44}{(R_1+R_2)C_1} \quad (20)$$

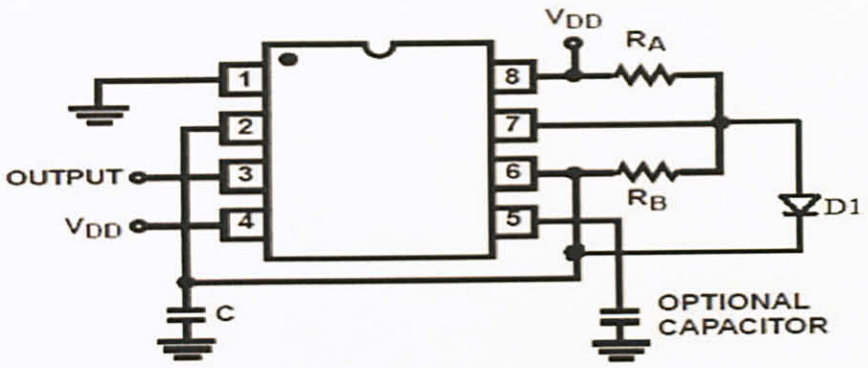

Figure 12 Modified astable circuit chip [7]

3.4.2 Voltage controlled PWM generator

Another way to generate pulses to the MOSFETs is by using PWM generator circuit. In order to make the circuit works, a DC reference level is needed. Hence, 5KΩ potentiometer implementing a voltage divider and 1.5KΩ resistor are added as shown in the figure 13. This resistor will prevent the DC voltage to fall too much under the bottom edge of the shifted triangle waveform. Therefore, the whole range of the potentiometer will have active influence the PWM duty cycle. It is the most important characteristic of this circuit. For this circuit MAX944 (MAXIM) is used as voltage comparator between DC input level voltage and triangular waveform. The layout is shown as in figure 13.

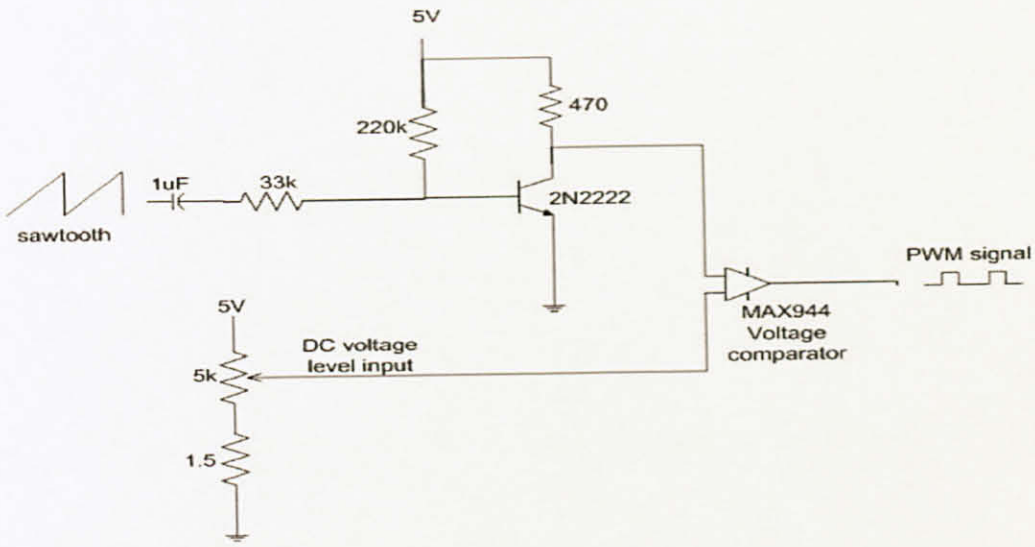

Figure 13 Voltage controlled PWM generator schematic [11]

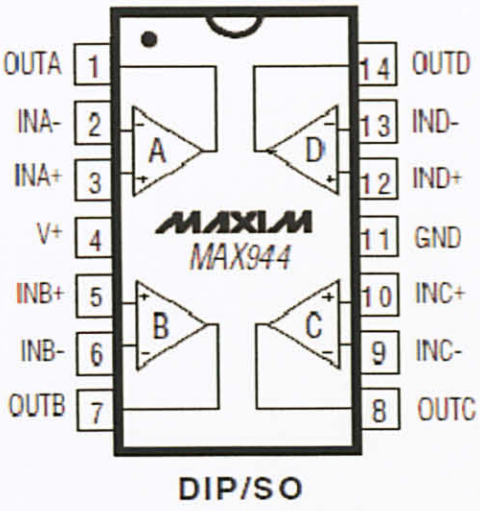

Figure 14 MAX944 pin layout *(see appendix C for details)*

3.4.3 Proposed Synchronization circuit

A synchronization circuit is used to synchronize at least two pulse widths, each producing a respective pulse width modulated output signal comprising an analogue input signal. This means that a synchronization circuit shifts the timing of the two pulse-width modulated output signal from the PWM generate circuit for VP_1 and VP_2. Based on figure 15, *sync* and *CT-BUFFER are* applied as input 1 and input 2 of synchronization circuit. Whereas, OUTA and OUTB will be the output for the gate of switch 1 and switch 2.

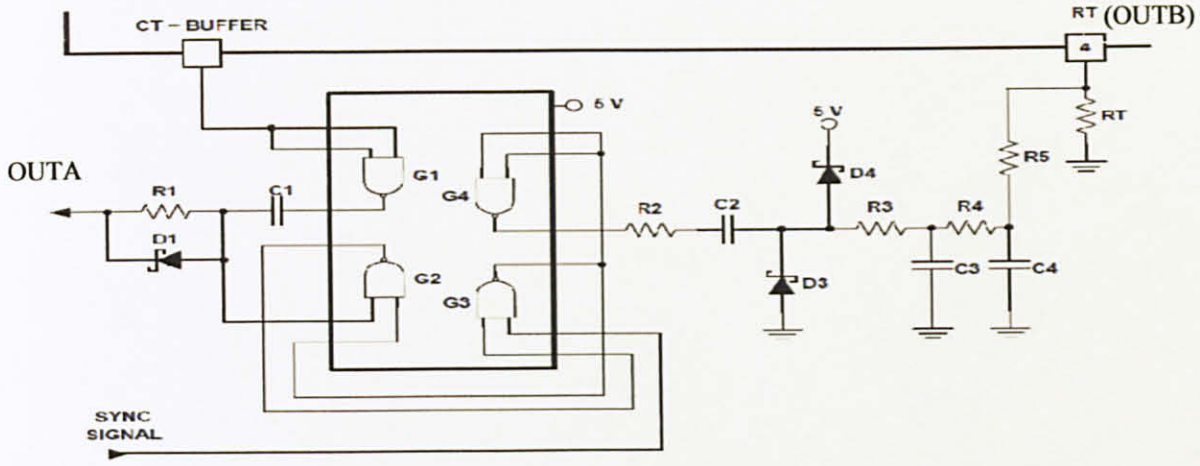

Figure 15 The configuration for synchronization circuit [11]

The list of components involved in synchronization circuit construction is

shown in table II:

Table II All components in synchronization circuit

R1	1kΩ
R2	1kΩ
R3	1kΩ
R4	6.2kΩ
R5	327kΩ
RT	400kΩ
C1	1nF
C2	1nF
C3	1nF
C4	100pF
Zener diode *D1*	5V
Zener diode *D2*	5V
Zener diode *D3*	5V
Zener diode *D4*	5V
CMOS NAND gate	CD4011

3.4.4 Delay line

This circuit is capable to delay any analogue signal such as pulse width. Delay line has many versions. In this project, three types of delay are used in order to generate dead time in between of two pulse widths. The 15A series delay line has been chosen in the experiment. This delay line is built with 8-pin package and it is TTL schottky interfaced. The delay was set up to give a total delay from 25ns to 1000ns. Table III below shows the details about the delay:

Table III Delay lines detail

Part number	Tap delay
15A-1000NL	200ns x 5 tap
15A-050NL	10ns x 5 tap
15A-500NL	100ns x 5 tap

For these delay lines, the configuration of the circuit is the same for each part number. Figure 16 shows the layout for delay line.

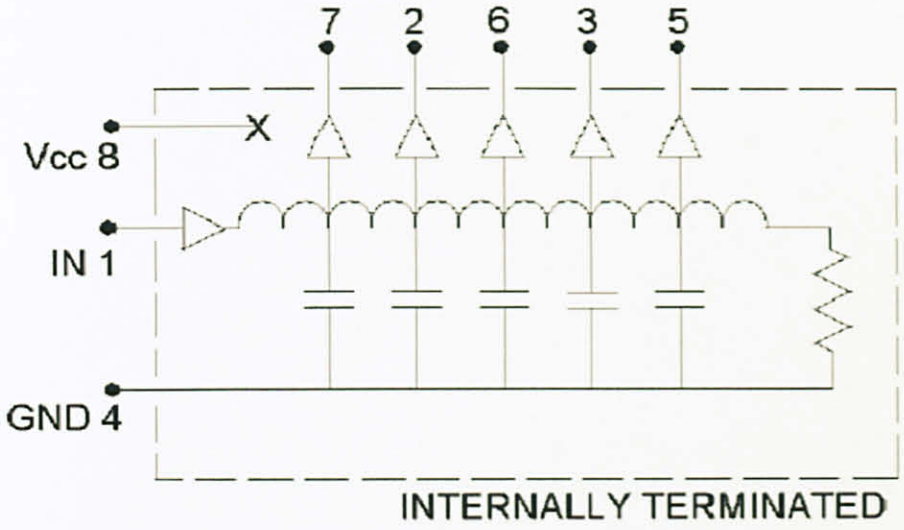

Figure 16 Layout for the delay line *(see appendix D for details)*

3.4.5 Power MOSFET driver circuit

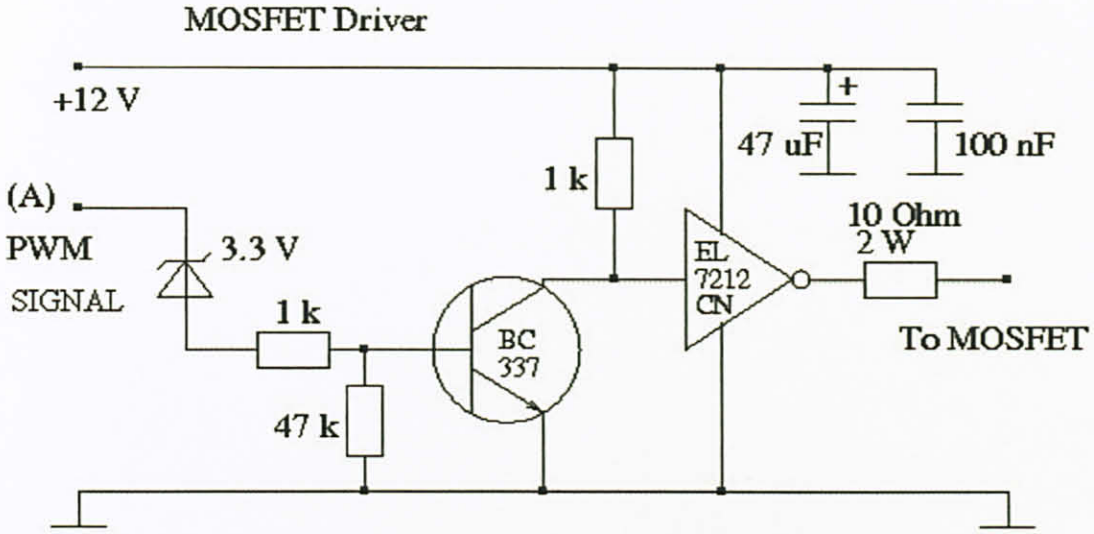

Figure 17 Circuit layout for MOSFET driver [12]

Based on figure 17, it is the layout for MOSFET driver circuit. The MOSFET (switch) in DC-RGD requires a specific driver circuit between PWM generator circuit and the MOSFET itself. The reason for this is the gate voltage of the MOSFET transistor requires high transient current (2 A) due to relatively high capacitive load [12]. Besides, this circuit is used to avoid voltage drop and power losses during the switching in DC-RGD circuit.

3.4.6 Diode-clamped resonant gate driver

The selection of the components used for this circuit construction has been chosen. The table IV shows the list of the components involved and ratings for each component.

Table IV List of the components in DC-RGD network

Components	Role in DC-RGD	Rating	Quantity
International rectifier, IRF620, Power MOSFET (n-channel)	Switches, Q_1 and Q_2	200V/5A, $R_{DS(on)}$=0.8Ω	2
STPS6045CP, Power schottky rectifier	Diodes	45V/60A	2
International rectifier, IRFP250NPbRF, Power MOSFET	S_1, power MOSFET	200V/30A, $R_{DS(on)}$=0.075Ω	1
4445-01M	Inductor	5nH	2

The layout of the analysis circuit has shown in figure 18 below:

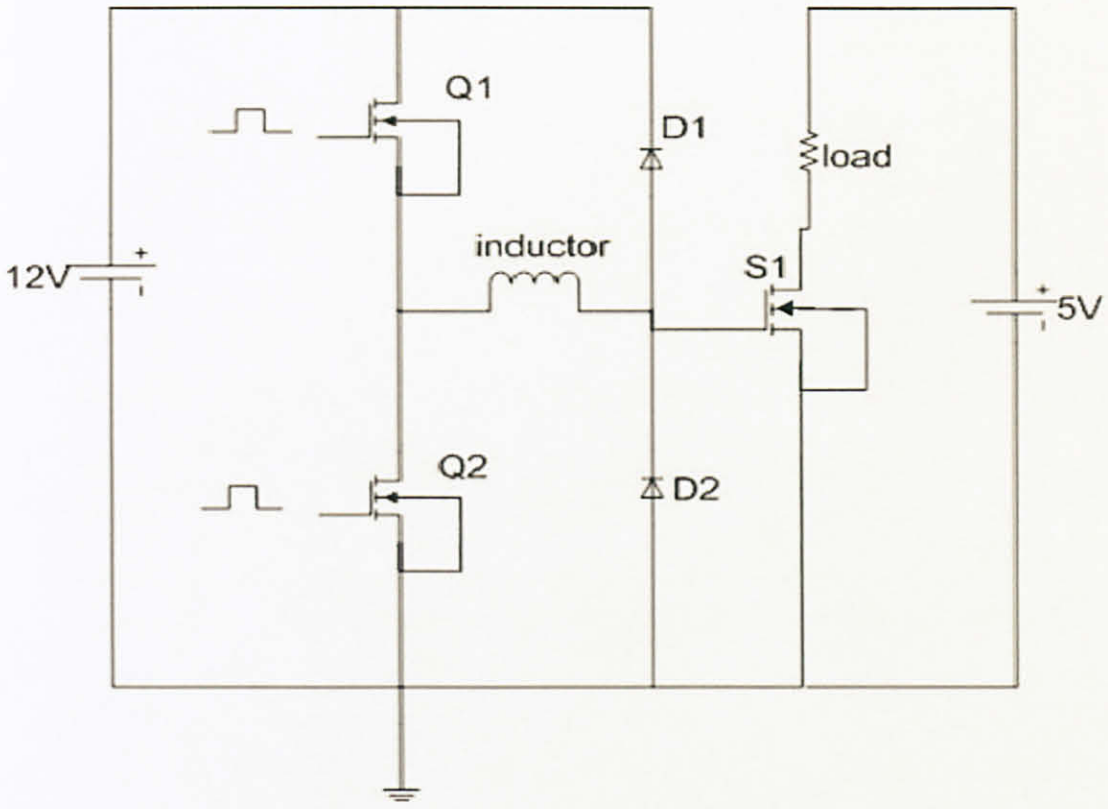

Figure 18 Schematic for DC-RGD circuit

CHAPTER 4
RESULTS AND DISCUSSIONS

4.1 PWM output signal test

PWM output signal generated using two methods which are Intersil ICM 7555 and PWM modulator circuit. Both are using analogue method to produce PWM signal. These circuits already tested practically in order to generate pulse widths to Q_1 and Q_2 in DC-RGD circuit. The circuit configuration and selection of components has been discussed in previous chapter.

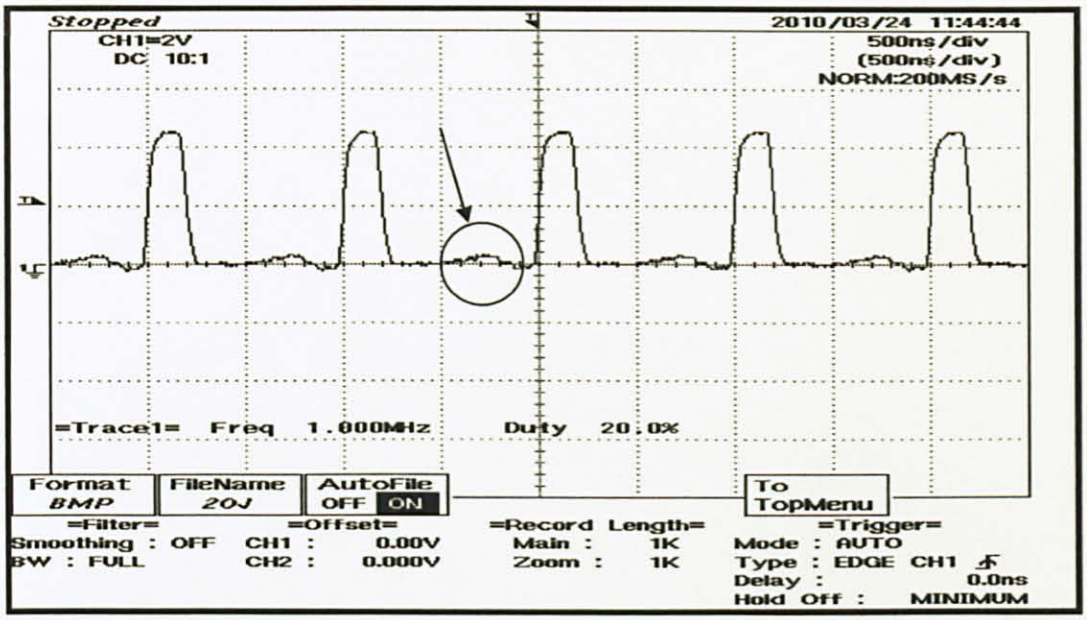

Figure 19 The experiment result showing 20.0% duty ratio [X: 500ns/div, Y: 2V/div]

The result based on the figure 19 is generated from PWM modulator circuit by adjusting the variable resistor of 5k ohm. The pulse width of the ON-time is 200ns whereas, the OFF-time showed 800ns of one complete cycle. Circle portion as in this figure shows that there are slightly undesired signal produced. However, it will not much affect on the work analysis.

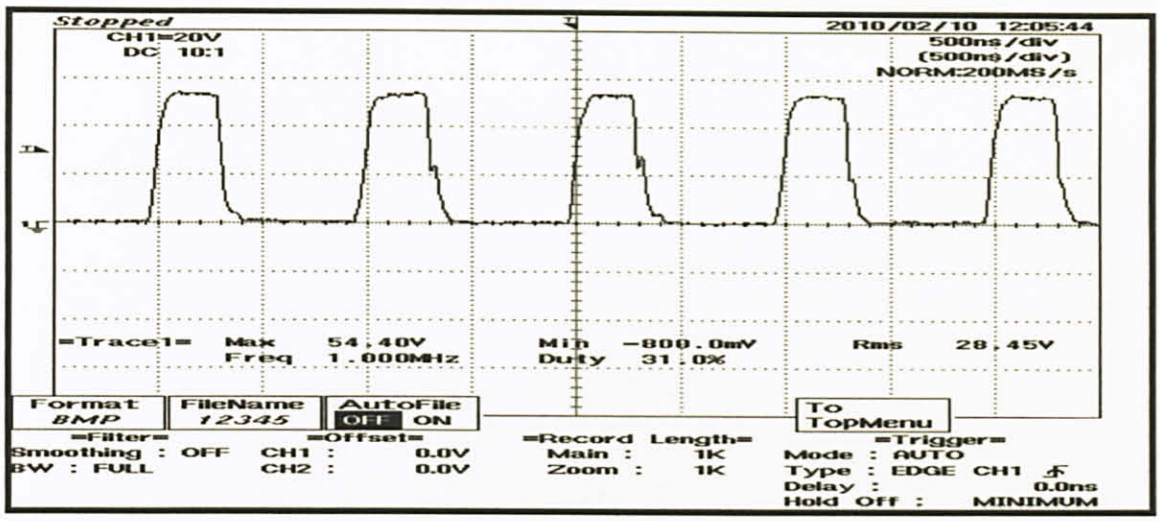

Figure 20 The experiment result showing 31.0% duty ratio [X: 500ns/div, Y: 5V/div]

Figure 20 shows the result of 31.0% duty ratio which is needed for analysis of DC-RGD. The ON-time is 310ns and the OFF-time is 690ns (one period is equal to 1000ns). Eventhough, there is the existence of undesired signal in this graph, it is still acceptable to be used in the analysis work.

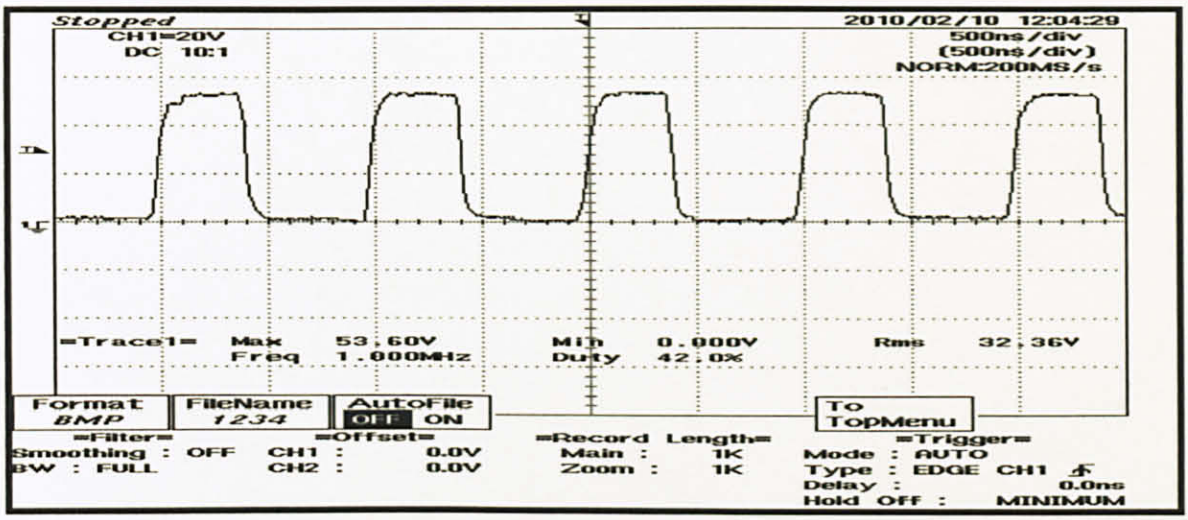

Figure 21 The experiment result showing 42.0% duty ratio [X: 500ns/div, Y: 2V/div]

The graph above shows PWM signal of 42.0% duty ratio. The pulse width period is 420ns out of 1000ns. Based on the figure 21, it is proven that as the duty ratio is increasing, the disturbance and ripple in the signal becomes lesser. This is a

good sign that there is less loss produced in the waveform and applicable in the analysis.

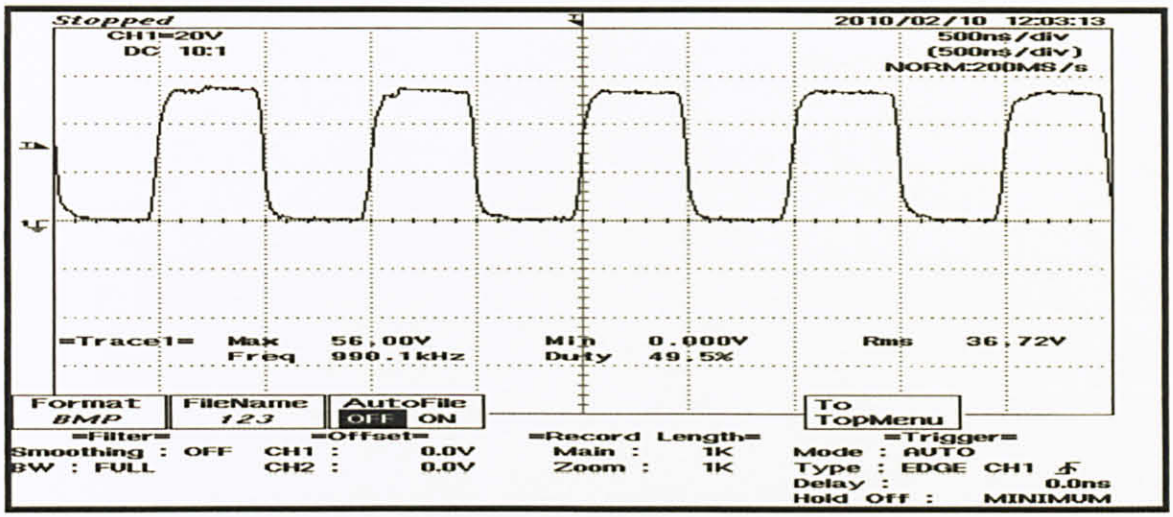

Figure 22 The experiment result showing 49.5% duty ratio [X: 500ns/div, Y: 2V/div]

Similarly like in the previous result, this figure 22 shows the pulse width for 49.5% duty ratio. Based on above result, the ON-time is 495ns and the remaining time will be the OFF-time. It is acceptable to be used in the analysis work.

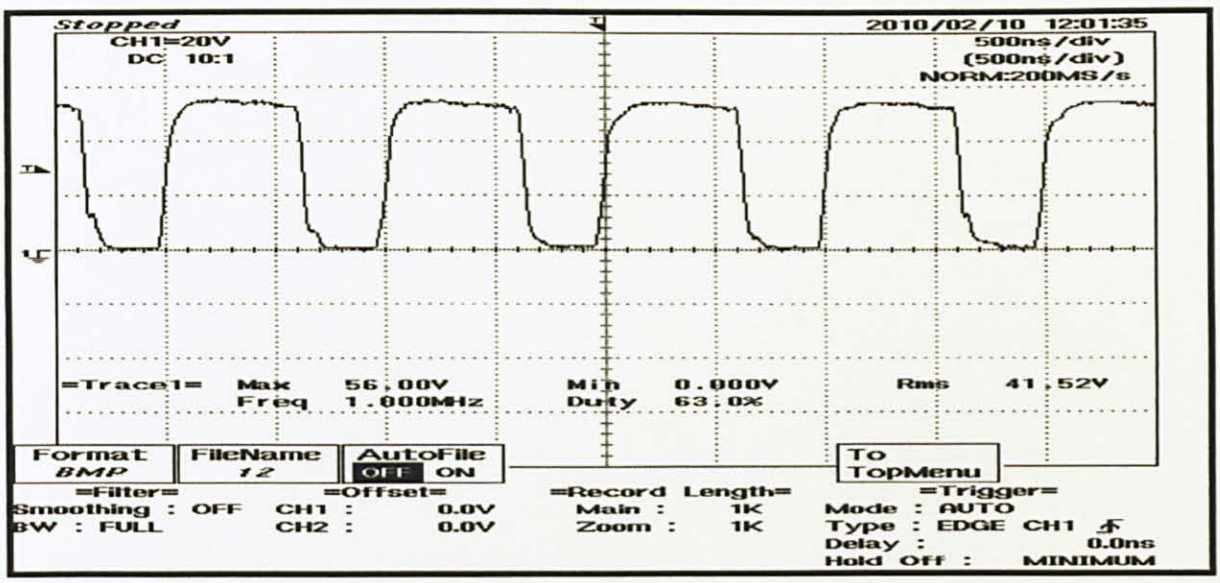

Figure 23 The experiment result showing 63.0% duty ratio [X: 500ns/div, Y: 2V/div]

Figure 23 shows the result of 63.0% duty ratio with ON-time period of 630ns and OFF-time period is 370ns.

4.2 Proposed synchronization circuit output

As the desired PWM output waveforms were generated, this circuit was evaluated and the result of this circuit is shows in figure 24.

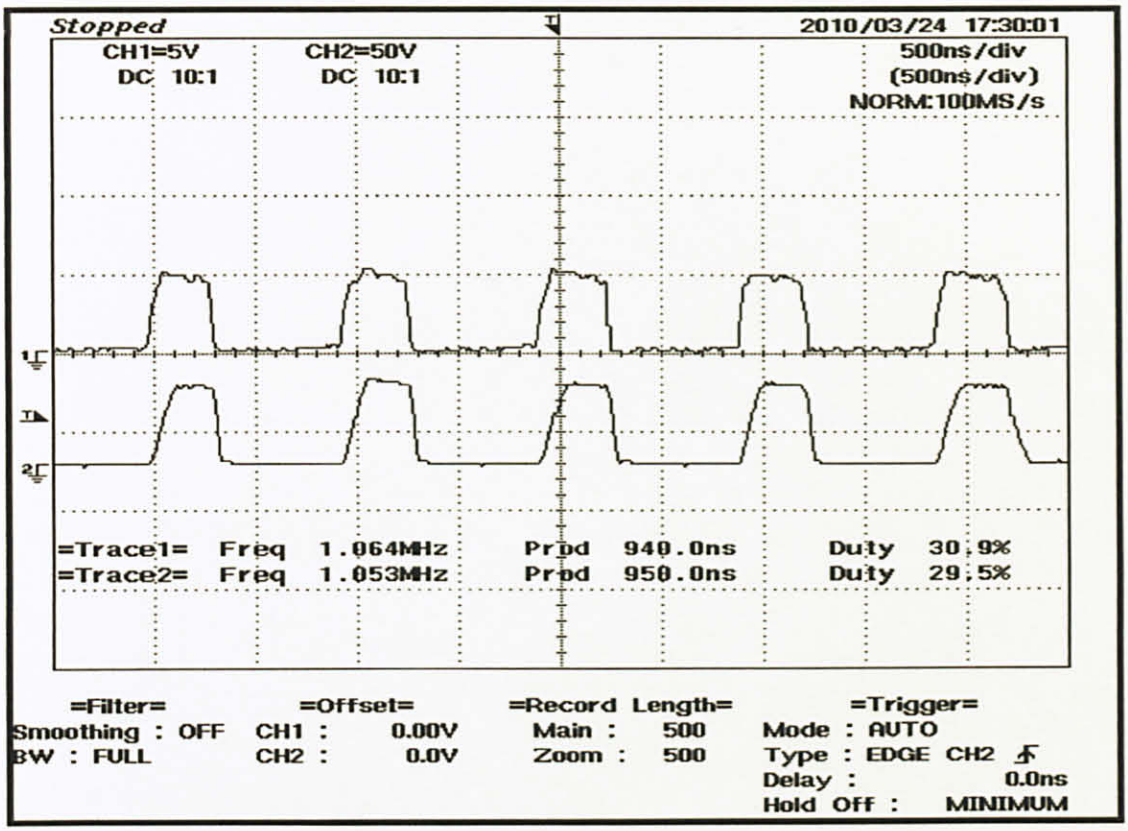

Figure 24 Synchronized PWM output waveform [X: 500ns/div, Y: 5V/div]

The waveforms generated in the graph above shows the synchronized PWM signal output generated from PWM modulator circuit. Two inputs from PWM modulator will be the input for synchronization circuit. The output side of synchronization circuit will generate the synchronize signal of these two PWM inputs. Based on the result obtained, two PWM signals of estimated 30.0% duty ratio were synchronized with frequency of 1MHz. As shown above, trace 1 and trace 2 represented the input to the gate of driving switches Q_1 and Q_2 respectively.

Once these two signals were synchronized, then it can be applied in switches

in DC-RGD circuit. Based on the graph above, the ON-time for both signals are started at the same point as well as the OFF-time. However, Q_1 and $Q2$ should not be conducted at the same time. This is to avoid cross conduction during the switching transition from Q_1 to Q_2. For the time being, these two synchronized signals were analyzed for duty ratio around 30%, examines the capability of this synchronization circuit. After synchronizing the signals, one of two signals either in trace 1 or trace 2 should go through the delay line circuit in order to get the delay waveform of PWM.

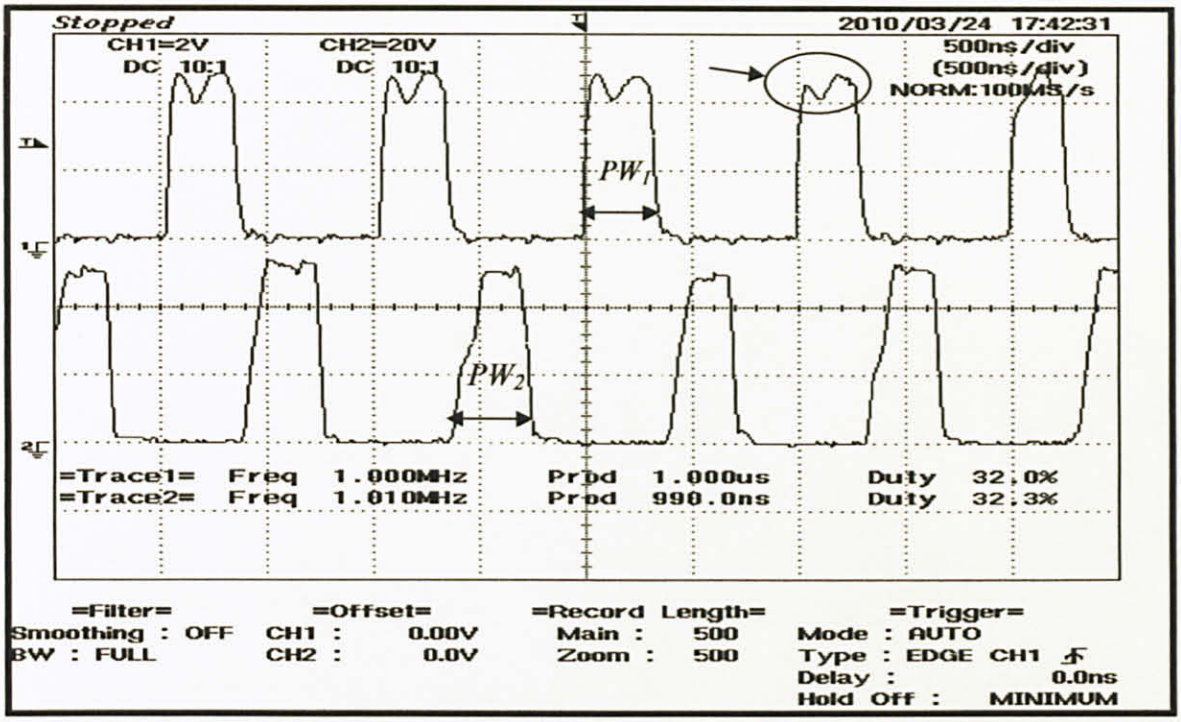

Figure 25 Two synchronized signal after delay line circuit being applied [X: 500ns/div, Y: 2V/div]

Figure 25 shows two signals initially started at the same point and time. However, for analysis purpose it has to make sure that Q_1 and Q_2 will be conducted complimentarily. Delay line will make one of these signals delayed and provide the different ON-time for both switches. Both pulses PW_1 and PW_2 have the same periods which are around 320ns. For that, delay line with delay of 400ns should be enough to delay the signal and applied to trace 1 and result obtained in trace 1 in figure 25. The waveform was shifted from its initial point but still in synchronizing condition.

However, there is a problem occurred after going through the delay. There is

slightly voltage drop in the signal after delayed. To solve this problem, the fixed supply of 5V has to be increased in order to maintain 5V after delayed. Another problem is that the waveform pattern becomes more critical where the ripple and spike produced at the pulse. To solve it, resistor has to be connected to the output of this signal. However, the resistance value has to be as low as possible to avoid the decreasing in current value and create more problems.

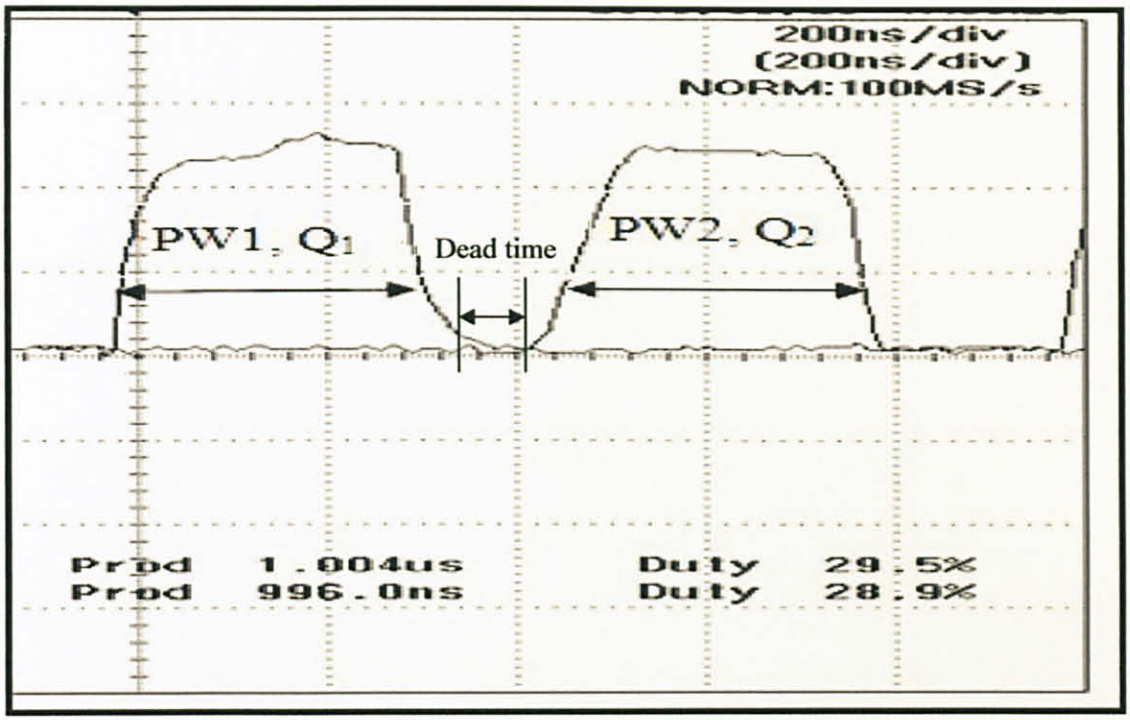

Figure 26 Synchronized signals of PW_1 and PW_2, duty ratio of 30%

Figure 26 shows pulse widths to be applied to Q_1 and Q_2. One of these two signals connected to delay line of ±200ns. Based on figure 26, there is dead time between both signals that is important to make sure the ON-time for both switches do not overlap and cause cross conduction and more losses to be produced.

4.3 Results of integration between DC-RGD circuit and PWM generation network

The experiment works for the whole network was not using switching frequency of 1MHz. This is due to the problem with high frequency which is become more critical to implement in the experiment. Because of that problem, the switching frequency has reduced to 500kHz as the maximum frequency and it is used for analyzing the whole network and it has been done for the experiment work. The duty ratio used for this experiment was around 20% (Pulse width of ±400ns) and dead time around 50ns.

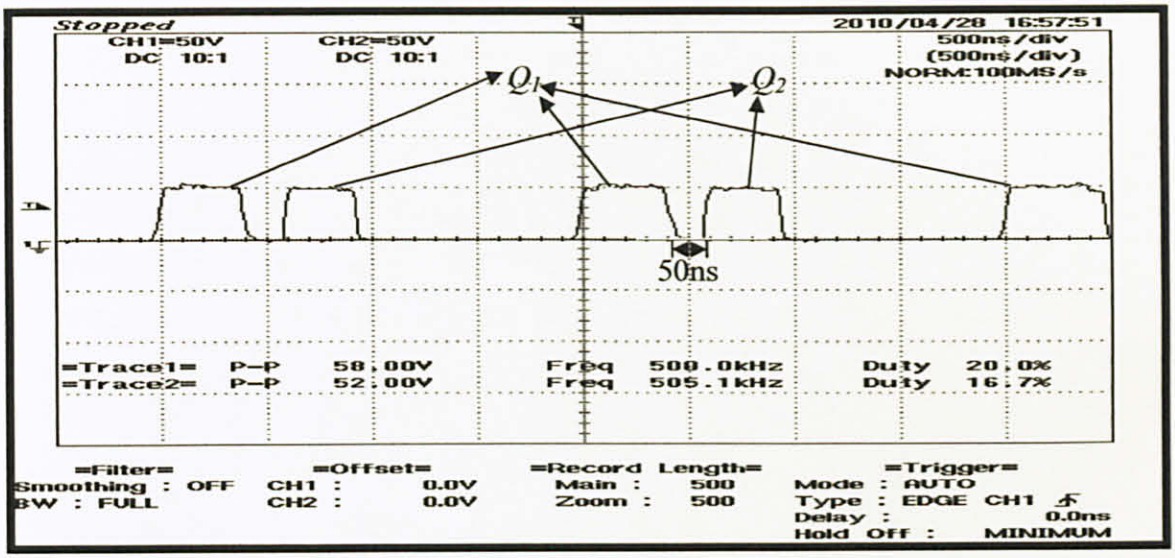

Figure 27 V_g applied respectively to both switches Q_1 and Q_2 [X:500ns/div, Y:5V/div]

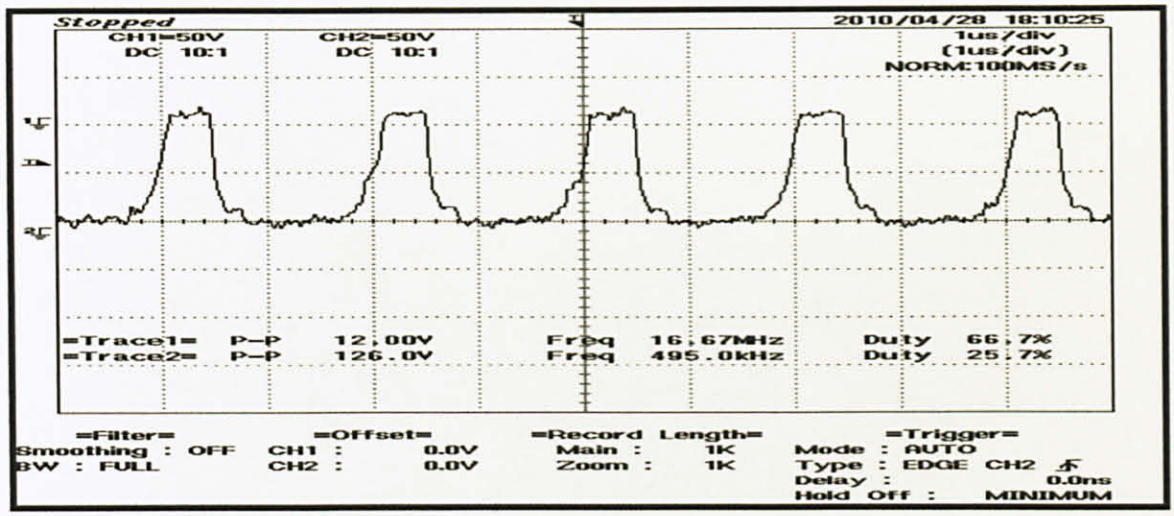

Figure 28 Pulse width 1 (VP_1) applied to the driving gate of switch Q_1 [X:1us/div, Y: 5V/div]

Figure 28 shows the output from the MOSFET driver circuit that has been amplified until 12.6V to turn-ON gate of the switch Q_1 . This is because of the problem where the MOSFET could not turned-ON by simply integrated to the DC-RGD network. Drive circuits for power MOSFET is needed for both networks to get function. According to appendix, gate voltage should be at 10V or more and MOSFET of IRF620 *(see appendix E for details)* will be turned-ON only when $I_{d(ON)}$ ≥5.0A.

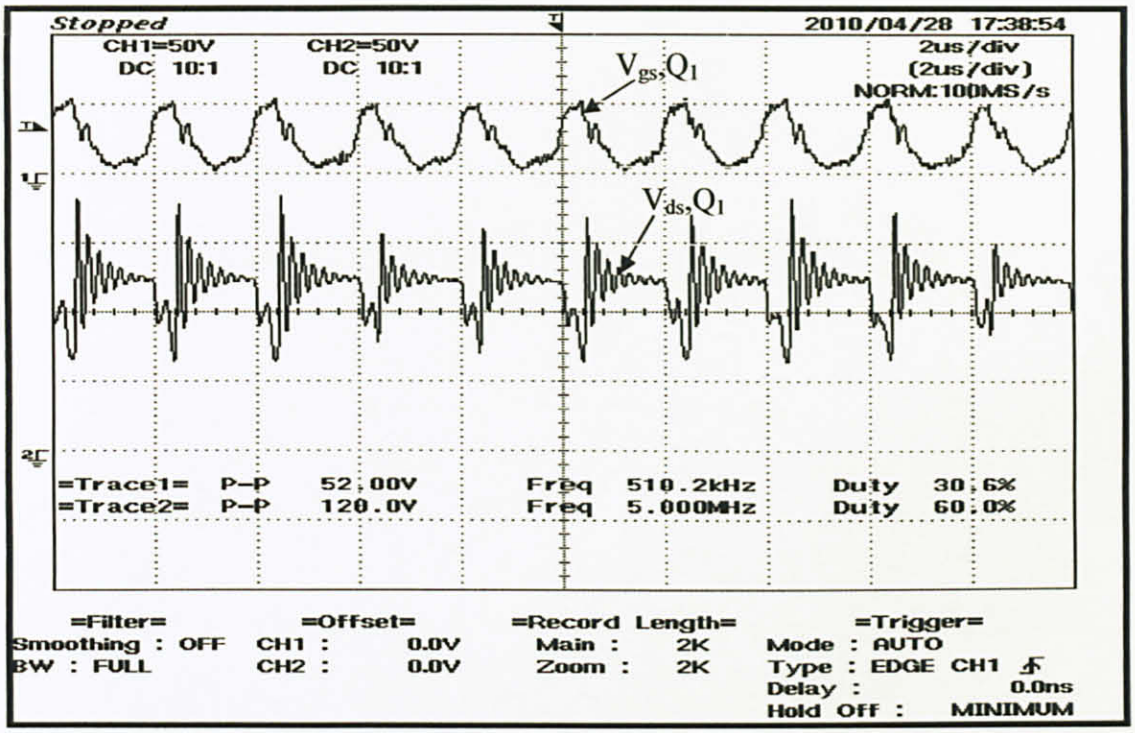

Figure 29 V_{gs},Q_1 and V_{ds},Q_1 for switching frequency of 510.2kHz

Figure 29 shows gate voltage exhibits like a '*step*', maintaining at a constant voltage level of 5V (maximum of 5.2V) while the drain voltage rises and falls complementarily with switching. The voltage at which the gate voltage remains during the switching is called Miller voltage, V_{gm}. In most applications, this voltage is around 4V and 6V depending on the current being switched [13].

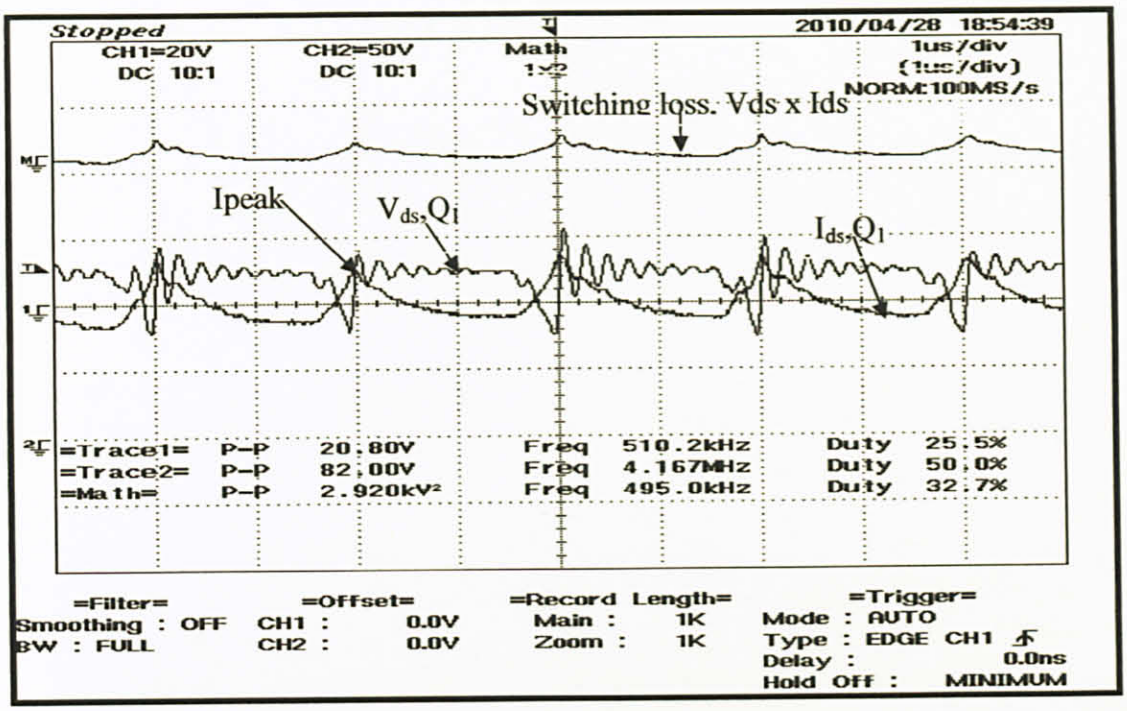

Figure 30 V_{ds}, I_{ds} and switching loss for Q_1

Referring to figure 30, current peak value of I_{ds} , I_{peak} is around 1.8A which is very high. In DC-RGD experimental works, the optimized value of inductor 10nH, varied dead time (within range of 50ns), switching frequency of 500kHz and 400ns pulse width being used. There is relationship between I_{peak} and turn-ON speed of the switches. As I_{peak} goes higher, causing the decrease turn-ON speeds for the switches. Means that, the lower the value of I_{peak} indicates a higher turn-ON speed and improving the efficiency of the network. Below is the equation (21) to determine power losses for both switches Q_1 and Q_2.

$$P_{sw} = V_{ds} \times I_{ds} \qquad (21)$$

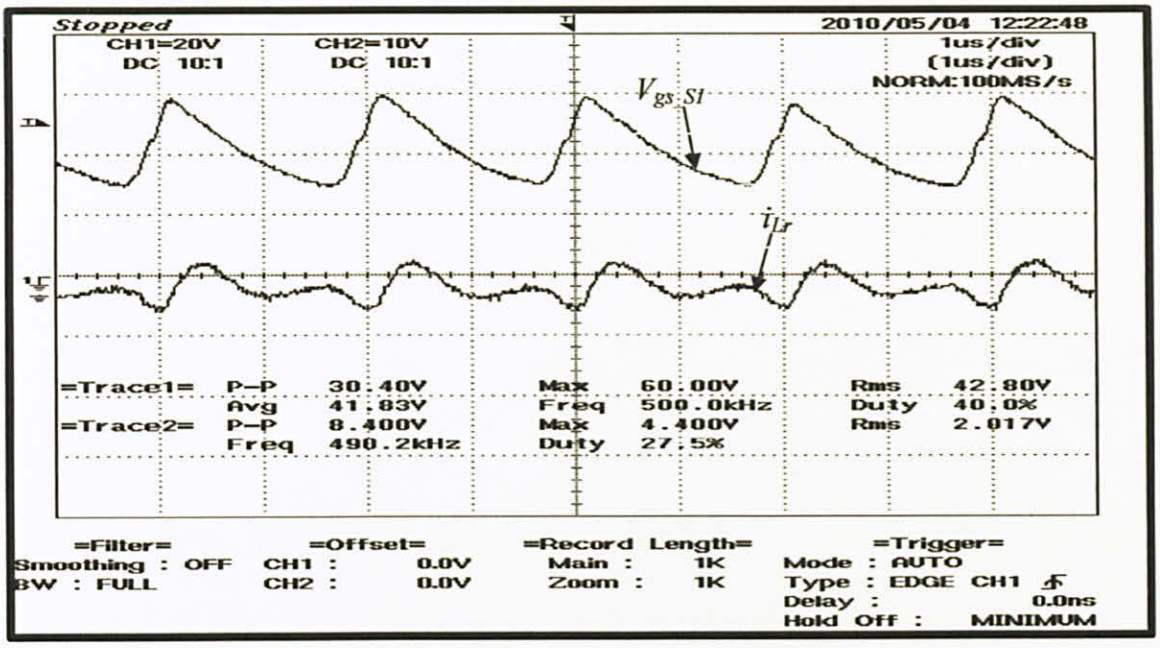

Figure 31 Graph of i_{Lr} of 10nH and V_{gs_S1}, within 400ns pulse width

Figure 31 shows that voltage, V_{gs_S1} of 6.0 is clamped. It is a large drop around 6.0V compared to the simulation work. This problem occurred because of the current flows through its gate, i_{Lr} is low as (maximum charging current of 0.44A) as per shown above. The selection of MOSFET also influences the results in the experiment works. The MOSFET has to be able to function as the current through inductor goes higher. When switch of Q_1 is turn-ON, i_{Lr} will be charged up the inductor, L_r and discharged back as in figure 28. The duration of charging the inductor seen shorter than discharging. Besides that, V_{gs_S1} is dependent on the value of i_{Lr} and C_{in}, internal capacitance for switch. This C_{in} can be obtained using a simple equation in (22). Given in (23) is the equation to get the time taken for current of the inductor to reach its maximum value.

$$C_{in} = \frac{Q}{V_{gs\_S1}} \tag{22}$$

$$t_{peak} = \frac{\tan^{-1}\left(\frac{2L_r \times \sqrt{\frac{4L_r}{C_{in}} - R_g^2}}{R_g}\right)}{2\sqrt{\frac{4L_r}{C_{in}} - R_g^2}} \tag{23}$$

4.4 Simulation results on diode-clamped RGD with 500kHz switching frequency

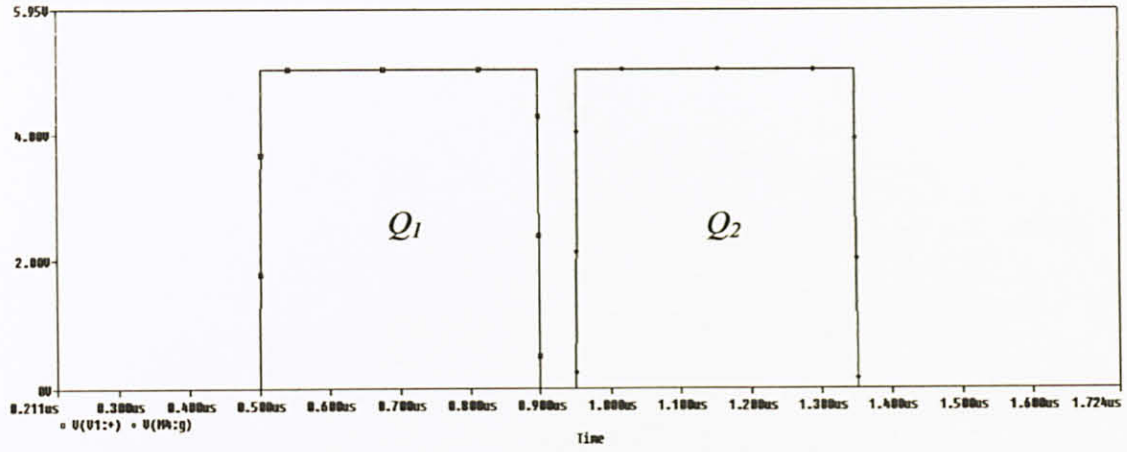

Figure 32 Pulse width of Q_1 and Q_2 within 400ns each (20% duty ratio)

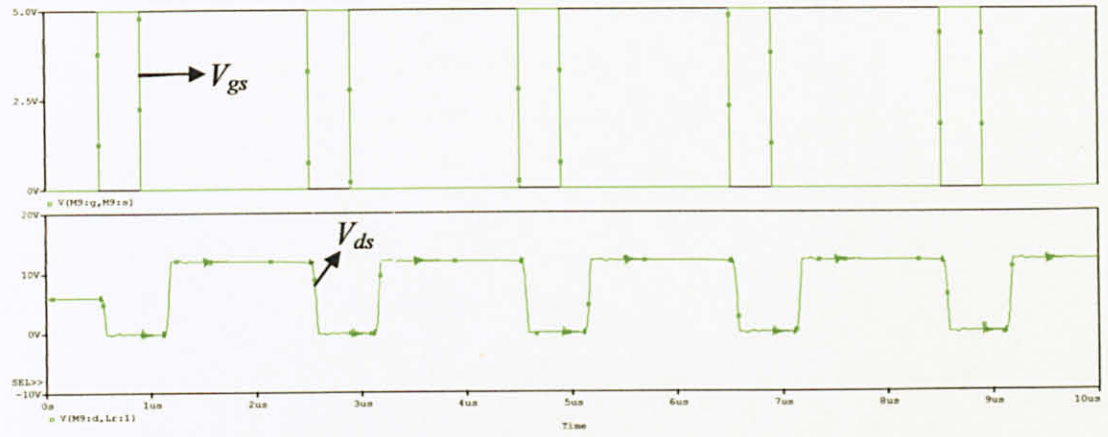

Figure 33 V_{gs} and V_{ds} of switch Q_1 in DC-RGD circuit

Figure 32 shows the VP_1 and VP_2 respectively that connected to the gate source for both switches Q_1 and Q_2. By using switching frequency of 500kHz, the dead time of 50ns was set up and figure 33 shows the graph of V_{gs},Q_1 and V_{ds},Q_1 which are the maximum value of 5.0V and 12.0V respectively.

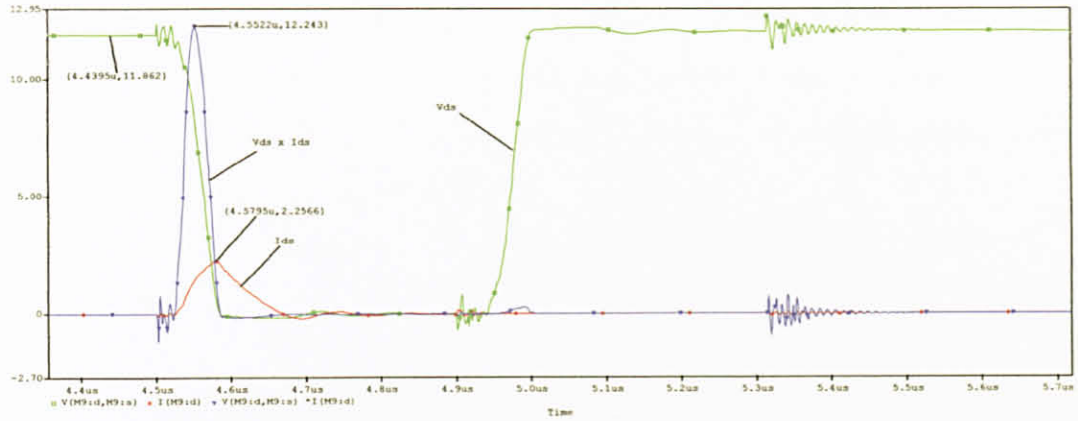

Figure 34 Simulation of V_{ds} and I_{ds} for Q_1 and switching loss

From the waveforms in figure 34, maximum value for V_{ds} reached 12V as the input source being used. The switch Q_1 starts to conduct when V_{ds} is in OFF state which means that it works in complimentary pattern with the V_{gs}. As switch Q_1 turn-ON, the current will start to increase until its maximum value and decrease until the switch Q_1 in OFF position as seen in both graphs above. Current for I_{ds} must reach its maximum value before ON state of V_{ds} has ended. Hence, the overlapping between I_{ds} and V_{ds} represented as a switching losses which is around 12.243W.

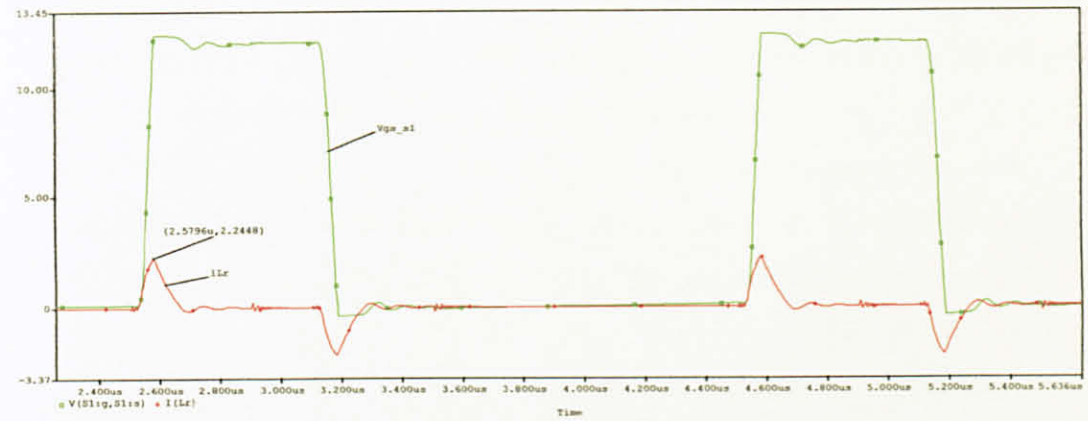

Figure 35 Graph of V_{gs_S1} and resonant inductor current, i_{Lr}

Figure 35 shows the combination graph of driving gate voltage source, V_{gs_S1} and resonant inductor current, i_{Lr} or gate current to the switch S_1. This V_{gs_S1} increases exponentially and is clamped 12V as the input source [5]. The current will start to charge to its maximum value when Q_1 is turn-ON and the time taken to charge

depends on L_r and the impedance of the network, Z_o of the network and it is discharged to zero as the V_{gs_S1} discharged to zero. The discharging time is longer compared to the charging time. This is due to the ON resistive charging effects through gate and driving resistance [5].

4.5 Discussions

4.5.1 PWM generator circuit analysis

The experiment work for PWM output signal testing has been done and working for range between 20% and 60% of duty ratio which are required in this project. The experiment work used 5V DC (peak to peak) voltage supply and switching frequency of 1MHz (almost 1MHz for each test). However, 10% duty ratio is quiet difficult to generate the smooth signal and not recommended to use it in full work analysis of this project. It might be not possible to produce short ON-time in high frequency unless the equipments and components used in the experiment are reliable and capable to make it.

In this experiment work to generate PWM signal, it is possible to generate adjustable duty ratio from 0-100% in low frequency of between 1Hz and 600 kHz with a smooth signal and clean pulses. As frequency gets higher, the gate driving losses will increase that can lead to high power dissipation. For 1MHz switching frequency, the chances of clean pulses generated is low because of distortion and ripple produced due to the internal resistance as well as wire resistance. According to all results above, proved that good PWM signals of duty ratio in range of 30% and above achieved. It is due to the capability of these PWM circuit and equipment used for the experiment work. Take note that the ON-time for each pulses generated is suitable to allow the MOSFET to turn-ON by analyzing the starting point at the voltage of ON-time pulse is match with the ON condition of the switch (MOSFET).

4.5.2 Synchronization circuit analysis

Based on the results for synchronization circuit, the objective to produce

synchronization between two signals was achieved but there is still noise and disturbance produced in the waveform. However, it is not a big problem to proceed to the next step which is generating finite dead time. For that, delay line circuit was connected to one of two signals. Apart from that, ripple and noise still occurred that make the measurement are not accurate. The main reason due to this problem is that in high frequency of 1MHz, this circuit cannot withstand and produce high ringing (noise) to the circuit eventhough a clean signal of oscillator is applied from function generator to this circuit. This is because of the loose connection used on the breadboard during the testing. The experiment work improved by using the right components value as well as the connection itself.

4.5.3 Comparison between simulation results and experiment results

This section discusses the data for experiment and simulation results in order to verify the overall performance of DC-RGD network. With considering 50ns dead time, 10nH resonant inductor and 20% duty ratio within 500kHz switching frequency, the comparison could be made.

Table V Comparison results from experiment and simulation

Parameter	Experiment result	Simulation result	Difference
V_{gs}, Q_1	5.2V	5.0V	0.2V
V_{ds}, Q_1	Max. voltage:12.0V	Max. voltage:12.0V	0V
I_{ds}, Q_1	Peak current=1.8A	Peak current=2.2566A	0.4566A
$V_{ds} x\ I_{ds}$	Maximum loss=2.920W	Maximum loss=12.243W	9.323W
$V_{gs,S1}$	Max. clamped voltage=6.0V	Max. clamped voltage=12.0V	6.0V
i_{Lr}	Max.charging current=0.44A	Max. charging current=2.2448A	1.8048A

Based on the experiment result for I_{ds}, Q_1, peak current only achieved at 1.8A compared to the simulation result, 2.2566A. It may due of the specification of MOSFET used in the experiment which is not the same with the

simulation work. As in the experiment, the MOSFET used for the switches are not be able to function properly as the current goes higher. When $I_{ds,}Q_1$ is measured inaccurate value, the switching loss for the switch Q_1 or Q_2 also increases. As a result, the measurement in the experiment will not be accurate too. Hence, it is still an issue for the selection of the right MOSFET used in the high switching frequency circuit because it is important while doing the analysis through the experiment work.

Moreover, from the table V shows that $V_{gs,S1}$ only clamped-up until 6V for its maximum value because of the maximum charging current only achieved at 0.44A. By referring to (24), value of $V_{gs,S1}$ is depending on C_{in} and the integral of i_{Lr} when i_{Lr} is charging. So, the value of the resonant inductor current, i_{Lr} influences the voltage clamps for $V_{gs,S1}$. For $V_{gs,S1}$, it is supposed to clamp up the voltage until 12V as the input voltage source. Hence, the right value of inductor must be used in the experiment in order to get the best analysis in this network.

$$V_{gs\_S1}(t) = \int_0^t \frac{1}{C_{in}} i_{Lr}(t)dt \qquad (24)$$

CHAPTER 5
CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

The study is about to experiment and analyze the overall performance of a diode-clamped resonant gate driver network by considering the parameter of duty ratio, resonant inductor and the dead time. In the design of diode-clamped resonant gate driver circuit with range MHz switching frequency is very crucial. Experiment work with voltage pulses of 20% duty ratio, 50ns dead time (limited dead time generated) and 10nH resonant inductor within 500kHz switching frequency validated with based on Pspice simulation result. Throughout the project, it is found that the construction and the testing of the whole networks required a lot of time before the overall analysis has been done. From the analyses for high switching frequency converter, its performance and reliability are easily influenced by the low capability of the equipments and circuit constructions in the experiment that may lead to the switching losses in the network.

5.2 Recommendation

Since the PWM generation network and DC-RGD network is completed and discussed in this project, improvement is necessary in the experiment work so that the overall analysis for 1MHz switching frequency could be done in future and validation for Pspice simulation will be more relevant and accurate. For future work, analysis for the network with duty ratio of 30%-60% with switching frequency of 1MHz can be implemented.

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APPENDICES

Appendix A: Gantt chart FYP 1

Appendix B: Gantt chart FYP 2

Appendix C: Datasheet of MAX 944

Appendix D: Datasheet of delay line

APPENDIX A

Activities/Milestone \ Week Number	1 20/07-26/07	2 27/07-02/08	3 03/07-09/07	4 10/08-16/08	5 17/08-23/08	6 24/08-30/08	7 31/08-06/09	8 07/09-13/09	9 14/09-20/09	 21/09-27/09	10 28/09-04/10	11 05/10-11/10	12 12/10-18/10	13 19/10-25/10	14 26/10-01/11	15 02/11-08/11
Confirmation of Title selection			H1N1 EMERGENCY BREAK							MID SEMESTER BREAK						
Literature Review																
Preparation and Submission of the Preliminary Report																
Project Works (Research and Circuit Design)																
Preparation and Submission of Progress Report 1																
Continue on Project (Circuit Construction)																
Seminar of FYP1																
Submission of Draft Report																
Preparation and Submission of Interim Report																
Oral Presentation																

Gantt chart for FYP 1

APPENDIX B

Week 1 / Activities/Milestone	1 25/1 – 31/1	2 1/2 – 7/2	3 8/2-14/2	4 15/2 – 21/2	5 22/2 – 28/2	6 1/3 – 7/3	7 8/3 – 14/3	8 15/3 – 21/3	9 22/3 – 28/3	10 29/3 – 4/4	11 5/4 – 11/4	12 12/4 – 18/4	13 19/4 -25/4	14 26/4 – 2/5	15 3/5 – 9/5	17 10/5 – 16/5	21 7/6 – 13/6	22 14/6 – 20/6	23 21/6 – 26/6
Continuation of Project								MID SEMESTER BREAK											
Literature Review and Methodology																			
Preparation and Submission of Progress Report 1																			
Preparation and Submission of Progress Report 2																			
Preparation and Submission of Draft																			
Preparation and Submission of Final Report (Soft)																			
Technical Report																			
Oral Presentation																			
Preparation and Submission of Thesis (Hard)																			

Appendix B: Gantt Chart For FYP II

APPENDIX C

19-0229; Rev 9; 3/09

MAXIM

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

General Description

The MAX941/MAX942/MAX944 are single/dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator.

The input common-mode range of the MAX941/MAX942/MAX944 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail.

Internal hysteresis ensures clean output switching, even with slow-moving input signals. The MAX941 features latch enable and device shutdown.

The single MAX941 and dual MAX942 are offered in a tiny µMAX® package. Both the single and dual MAX942 are available in 8-pin DIP and SO packages. The quad MAX944 comes in 14-pin DIP and narrow SO packages.

Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

Sampling Circuits

Features

- Available in µMAX Package for Automotive Applications
- Optimized for 3V and 5V Applications (Operation Down to 2.7V)
- Fast, 80ns Propagation Delay (5mV Overdrive)
- Rail-to-Rail Input Voltage Range
- Low 350µA Supply Current per Comparator
- Low, 1mV Offset Voltage
- Internal Hysteresis for Clean Switching
- Outputs Swing 200mV of Power Rails
- CMOS/TTL-Compatible Outputs
- Output Latch (MAX941 Only)
- Shutdown Function (MAX941 Only)

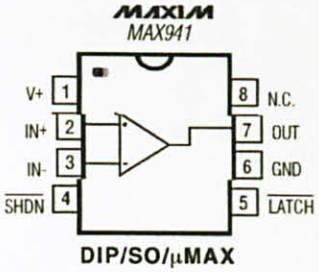
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX941CPA	0°C to +70°C	8 Plastic DIP
MAX941CSA	0°C to +70°C	8 SO
MAX941EPA	-40°C to +85°C	8 Plastic DIP
MAX941ESA	-40°C to +85°C	8 SO
MAX941EUA-T	-40°C to +85°C	8 µMAX
MAX941AUA-T	-40°C to +125°C	8 µMAX

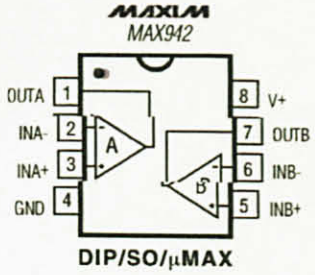
Ordering Information continued at end of data sheet.

Pin Configurations

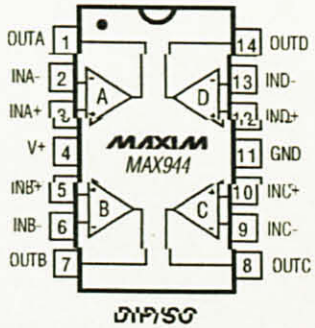
TOP VIEW



DIP/SO/µMAX



DIP/SO/µMAX



DIP/SO

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
- Supply Voltage V+ to GND ..... +6.5V
- Differential Input Voltage ..... -0.3V to (V+ + 0.3V)
- Common-Mode Input Voltage ..... -0.3V to (V+ + 0.3V)
- $\overline{LATCH}$ Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)
- $\overline{SHDN}$ Control Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)
- Current Into Input Pins ..... ±20mA

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
- 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
- 14-Pin SO (derate 8.33mW/°C above +70°C) 667mW

Operating Temperature Ranges
- MAX94_C_ _ ..... 0°C to +70°C
- MAX94_E_ _ ..... -40°C to +85°C
- MAX94_AUA ..... -40°C to +125°C
- MAX942MSA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Positive Supply Voltage	V+				2.7		5.5	V
Input Voltage Range	V_{CMR}	(Note 1)			-0.2		V+ + 0.2	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = 0 or V_{CM} = V+ (Note 2)	T_A = +25°C	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		1	3	mV
				MAX941_UA/MAX942_UA		1	4	
			T_A = T_{MIN} to T_{MAX}	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA			4	mV
				MAX941_UA/MAX942_UA			6	
Input Offset Voltage	V_{OS}	V_{CM} = 0 or V_{CM} = V+ (Note 3)	T_A = +25°C	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		1	2	mV
				MAX941_UA/MAX942_UA		1	3	
			T_A = T_{MIN} to T_{MAX}	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA			3	mV
				MAX941_UA/MAX942_UA			5.5	
Input Bias Current	I_B	V_{IN} = V_{OS}, V_{CM} = 0 or V_{CM} = V+ (Note 4)		MAX94_C		150	300	nA
				MAX94_E/A, MAX942MSA		150	400	
Input Offset Current	I_{OS}	V_{IN} = V_{OS}, V_{CM} = 0 or V+				10	150	nA
Input Differential Clamp Voltage	V_{CLAMP}	Force 100µA into IN+, IN- = GND, measure V_{IN+} - V_{IN-}, Figure 3				2.2		V
Common-Mode Rejection Ratio	CMRR	(Note 5)		MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		80	300	µV/V
				MAX941_UA/MAX942_UA		80	800	
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V+ ≤ 5.5V, V_{CM} = 0V		MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		80	300	µV/V
				MAX941_UA/MAX942_UA		80	350	
Output High Voltage	V_{OH}	I_{SOURCE} = 400µA			V+ - 0.4	V+ - 0.2		V
		I_{SOURCE} = 4mA			V+ - 0.4	V+ - 0.3		
Output Low Voltage	V_{OL}	I_{SINK} = 400µA				0.2	0.4	V
		I_{SINK} = 4mA				0.3	0.4	
Output Leakage Current	I_{LEAK}	(Note 6)					1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current per Comparator	I_{CC}	V+ = 3V	MAX941		380	600	µA
			MAX942/MAX944		350	500	
		V+ = 5V	MAX941		430	700	
			MAX942/MAX944		400	600	
		MAX941 only, shutdown mode (V+ = 3V)			12	60	
Power Dissipation per Comparator	PD	(Note 7)	MAX941		1.0	4.2	mW
			MAX942/MAX944		1.0	3.6	
Propagation Delay	t_{PD+}, t_{PD-}	(Note 8)	MAX94_C		80	150	ns
			MAX94_E/A, MAX942MSA		80	200	
Differential Propagation Delay	dt_{PD}	(Note 9)			10		ns
Propagation Delay Skew		(Note 10)			10		ns
Logic Input Voltage High	V_{IH}	(Note 11)		$\frac{V+}{2}$ + 0.4	$\frac{V+}{2}$		V
Logic Input Voltage Low	V_{IL}	(Note 11)			$\frac{V+}{2}$	$\frac{V+}{2}$ - 0.4	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0 or V+ (Note 11)			2	10	µA
Data-to-Latch Setup Time	t_S	(Note 12)			20		ns
Latch-to-Data Hold Time	t_H	(Note 12)			30		ns
Latch Pulse Width	t_{LPW}	MAX941 only			50		ns
Latch Propagation Delay	t_{LPD}	MAX941 only			70		ns
Shutdown Time		(Note 13)			3		µs
Shutdown Disable Time		(Note 13)			10		µs

Note 1: Inferred from the CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

Note 2: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone (see Figure 1).

Note 3: V_{OS} is defined as the center of the input-referred hysteresis zone (see Figure 1).

Note 4: The polarity of I_B reverses direction as V_{CM} approaches either supply rail. See *Typical Operating Characteristics* for more detail.

Note 5: Specified over the full common-mode range (V_{CMR}).

Note 6: Applies to the MAX941 only when in shutdown mode. Specification is for current flowing into or out of the output pin for V_{OUT} driven to any voltage from V+ to GND.

Note 7: Typical power dissipation specified with V+ = 3V; maximum with V+ = 5.5V.

Note 8: Parameter is guaranteed by design and specified with V_{OD} = 5mV and C_{LOAD} = 15pF in parallel with 400µA of sink or source current. V_{OS} is added to the overdrive voltage for low values of overdrive (see Figure 2).

Note 9: Specified between any two channels in the MAX942/MAX944.

Note 10: Specified as the difference between t_{PD+} and t_{PD-} for any one comparator.

Note 11: Applies to the MAX941 only for both $\overline{SHDN}$ and $\overline{LATCH}$ pins.

Note 12: Applies to the MAX941 only. Comparator is active with $\overline{LATCH}$ pin driven high and is latched with $\overline{LATCH}$ pin driven low (see Figure 2).

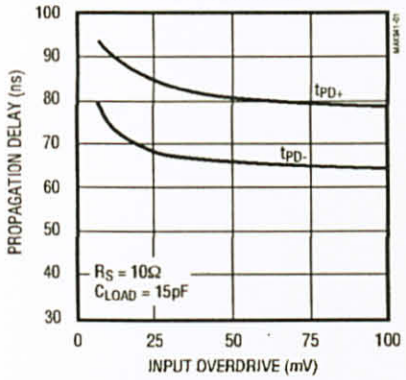
Note 13: Applicable to the MAX941 only. Comparator is active with $\overline{SHDN}$ pin driven high and is in shutdown with $\overline{SHDN}$ pin driven low. Shutdown disable time is the delay when $\overline{SHDN}$ is driven high to the time the output is valid.

Note 14: The MAX941_UA and MAX942_UA are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

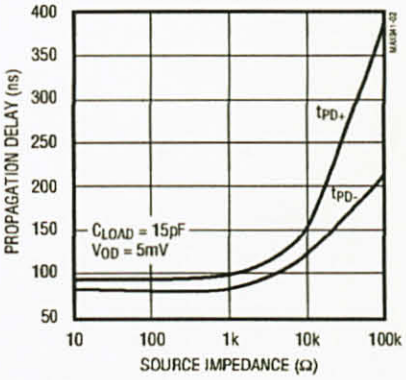
Typical Operating Characteristics

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

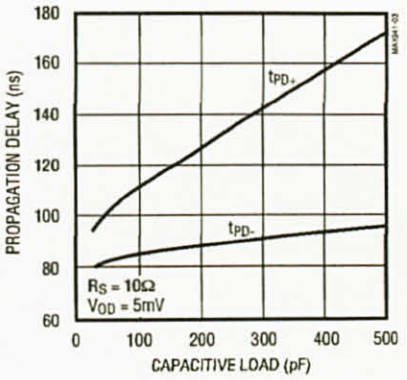
PROPAGATION DELAY vs. INPUT OVERDRIVE



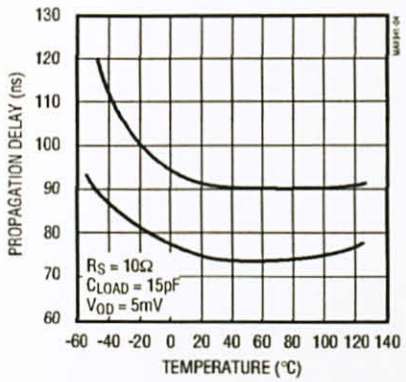
PROPAGATION DELAY vs. SOURCE IMPEDANCE



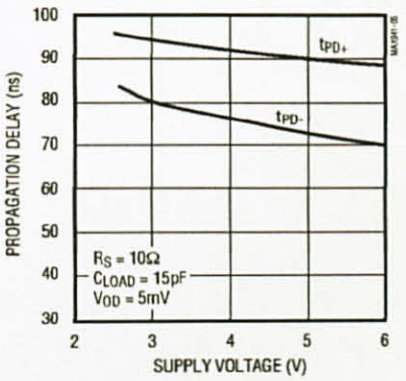
PROPAGATION DELAY vs. CAPACITIVE LOAD



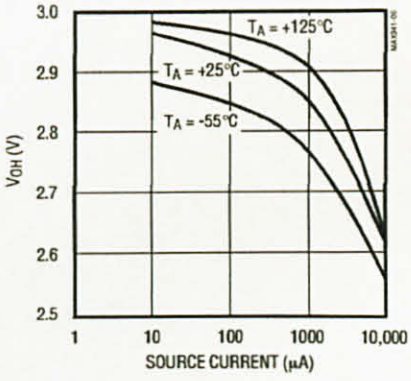
PROPAGATION DELAY vs. TEMPERATURE



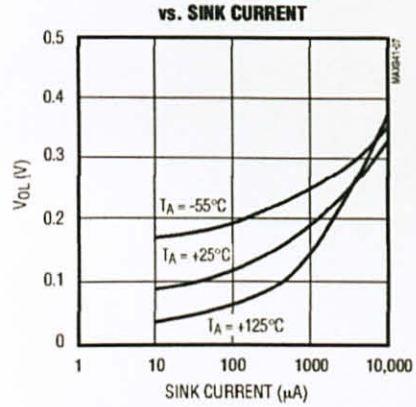
PROPAGATION DELAY vs. SUPPLY VOLTAGE



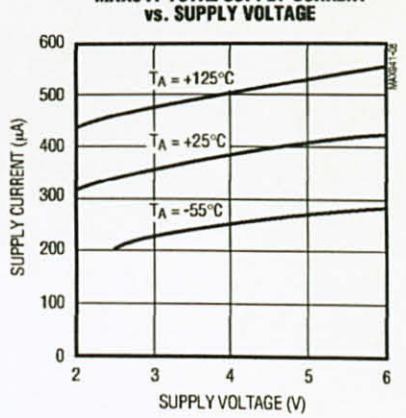
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



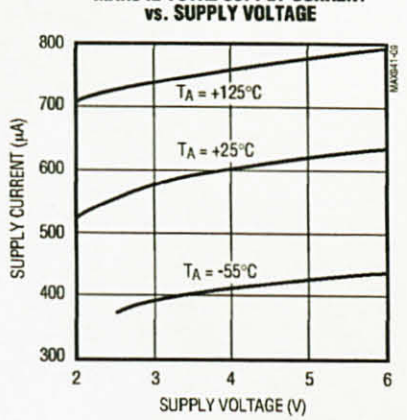
OUTPUT LOW VOLTAGE vs. SINK CURRENT



MAX941 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



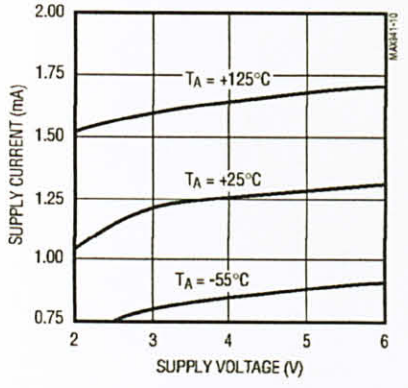
MAX942 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



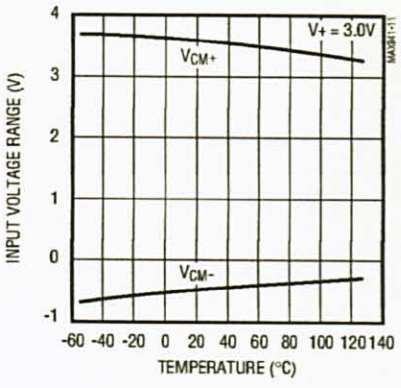
Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

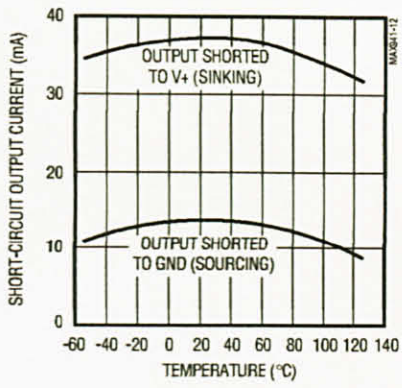
MAX944 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



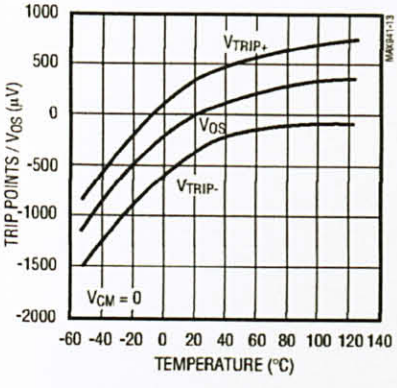
INPUT VOLTAGE RANGE vs. TEMPERATURE



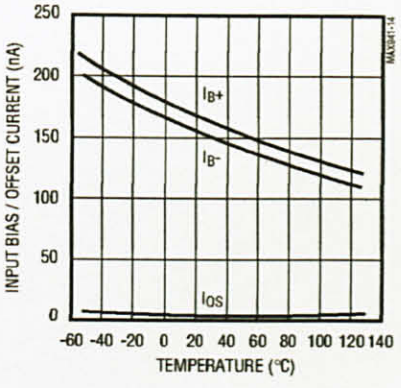
SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



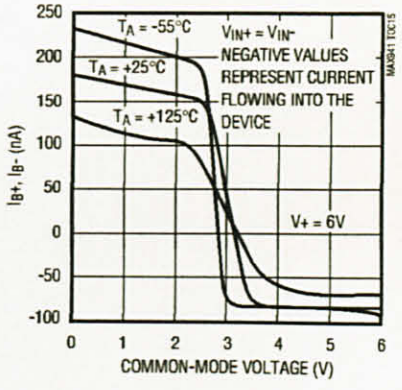
VOLTAGE TRIP POINTS/INPUT OFFSET VOLTAGE vs. TEMPERATURE



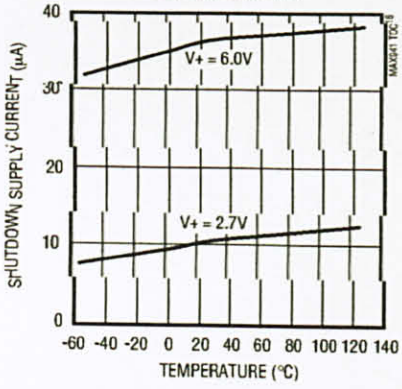
INPUT BIAS CURRENT/INPUT OFFSET CURRENT vs. TEMPERATURE



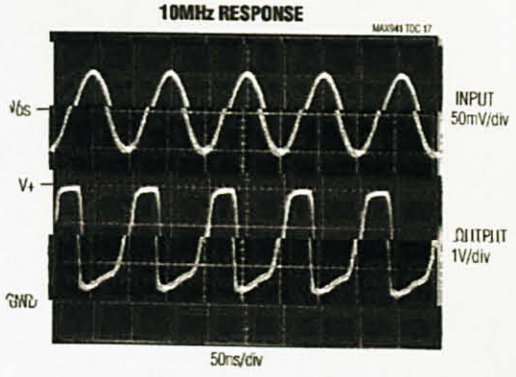
INPUT BIAS CURRENT (I_{B+}, I_{B-}) vs. COMMON-MODE VOLTAGE



MAX941 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

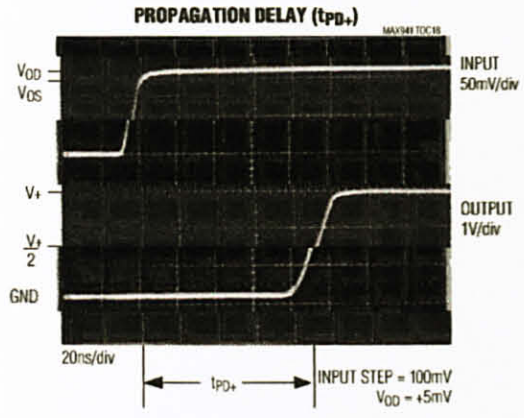


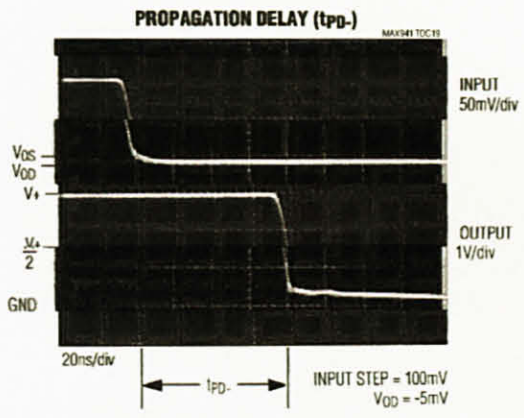
10MHz RESPONSE



Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN			NAME	FUNCTION
MAX941	MAX942	MAX944		
—	1	1	OUTA	Comparator A Output
—	2	2	INA-	Comparator A Inverting Input
—	3	3	INA+	Comparator A Noninverting Input
1	8	4	V+	Positive Supply (V+ to GND must be ≤ 6.5V)
—	5	5	INB+	Comparator B Noninverting Input
—	6	6	INB-	Comparator B Inverting Input
—	7	7	OUTB	Comparator B Output
—	—	8	OUTC	Comparator C Output
—	—	9	INC-	Comparator C Inverting Input
—	—	10	INC+	Comparator C Noninverting Input
6	4	11	GND	Ground
—	—	12	IND+	Comparator D Noninverting Input
—	—	13	IND-	Comparator D Inverting Input
—	—	14	OUTD	Comparator D Output
2	—	—	IN+	Noninverting Input
3	—	—	IN-	Inverting Input
4	—	—	$\overline{SHDN}$	Shutdown: MAX941 is active when $\overline{SHDN}$ is driven high; MAX941 is in shutdown when $\overline{SHDN}$ is driven low.
5	—	—	$\overline{LATCH}$	The output is latched when $\overline{LATCH}$ is low. The latch is transparent when $\overline{LATCH}$ is high.
7	—	—	OUT	Comparator Output
8	—	—	N.C.	No Connection. Not internally connected.

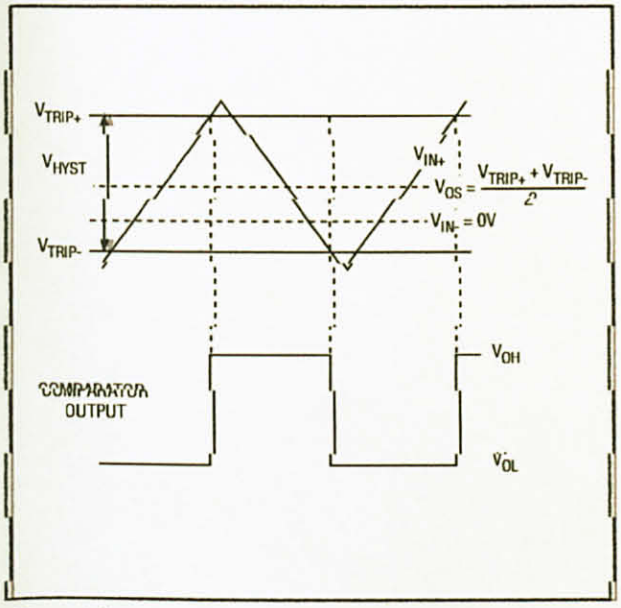


Figure 1. Input and Output Waveform, Noninverting Input Varied

Detailed Description

The MAX941/MAX942/MAX944 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.4V of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX941/MAX942/MAX944 interface directly to CMOS and TTL logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX941/MAX942/MAX944 have internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX941/MAX942/MAX944's fixed internal hysteresis eliminates these resistors and the equations needed to determine appropriate values.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX941 includes an internal latch that allows storage of comparison results. The $\overline{LATCH}$ pin has a high input impedance. If $\overline{LATCH}$ is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when $\overline{LATCH}$ is pulled low. All timing constraints must be met when using the latch function (Figure 2).

Shutdown Mode (MAX941 Only)

The MAX941 shuts down when $\overline{SHDN}$ is low. When shut down, the supply current drops to less than 60µA, and the three-state output becomes high impedance. The $\overline{SHDN}$ pin has a high input impedance. Connect $\overline{SHDN}$ to V+ for normal operation. Exit shutdown with $\overline{LATCH}$ high; otherwise, the output will be indeterminate.

Input Stage Circuitry

The MAX941/MAX942/MAX944 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two 4.1kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than $2V_F$, where V_F is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(IN+ - IN-) - 2V_F}{2 \times 4.1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I_B). As long as the differential input voltage is less than $2V_F$, this input current is equal to I_B. The protection circuitry also allows for the input common-mode range of the MAX941/MAX942/MAX944 to extend beyond both power-supply rails. The output is in the correct logic state if one or both inputs are within the common-mode range.

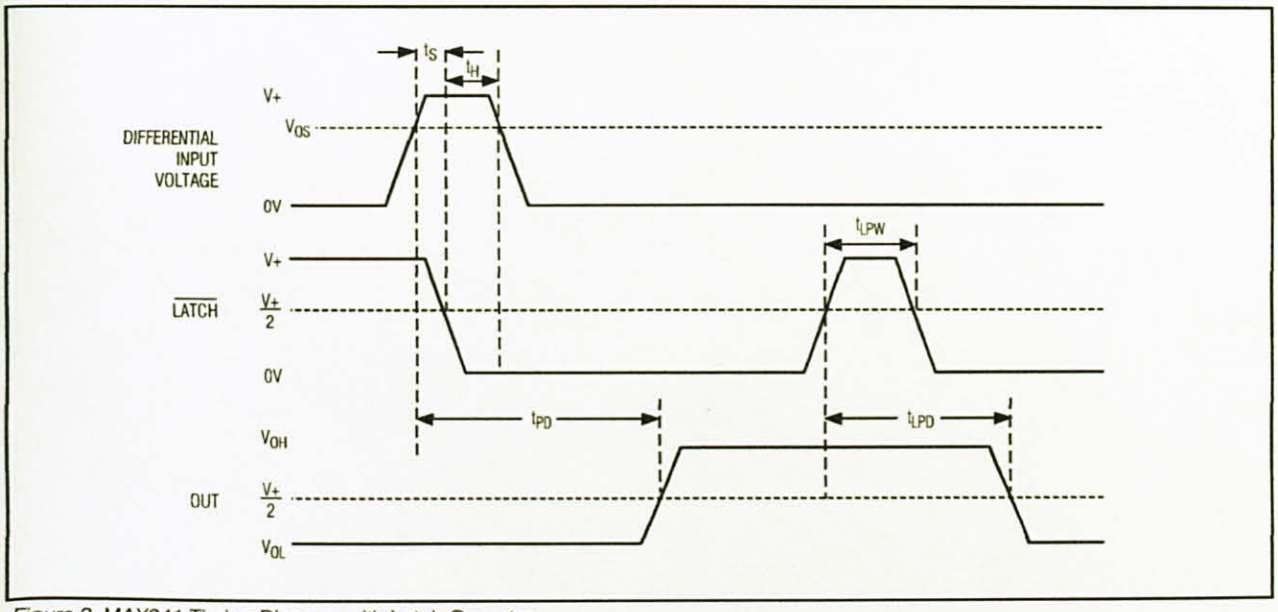


Figure 2. MAX941 Timing Diagram with Latch Operator

Output Stage Circuitry

The MAX941/MAX942/MAX944 contain a current-driven output stage as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noise-sensitive applications where fast edges may cause interference.

Applications Information

Circuit Layout and Bypassing

The high gain bandwidth of the MAX941/MAX942/MAX944 requires design precautions to realize the comparators' full high-speed capability. The recommended precautions are:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V+ as possible.
3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
5) Solder the device directly to the printed circuit board instead of using a socket.

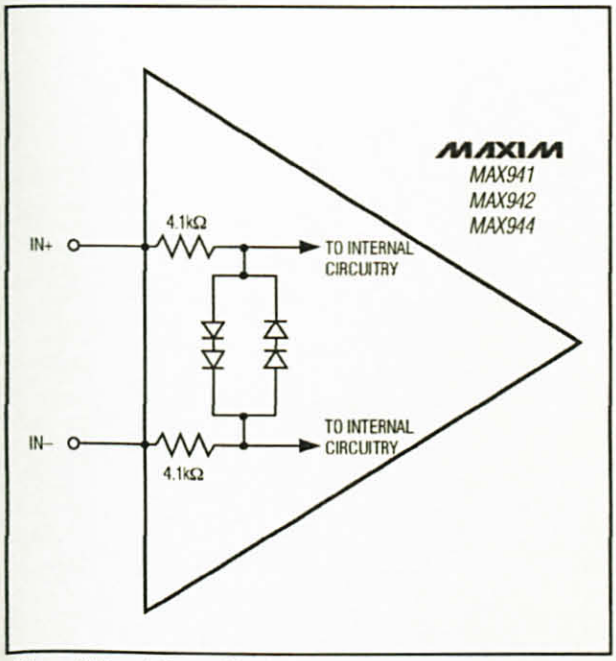


Figure 3. Input Stage Circuitry

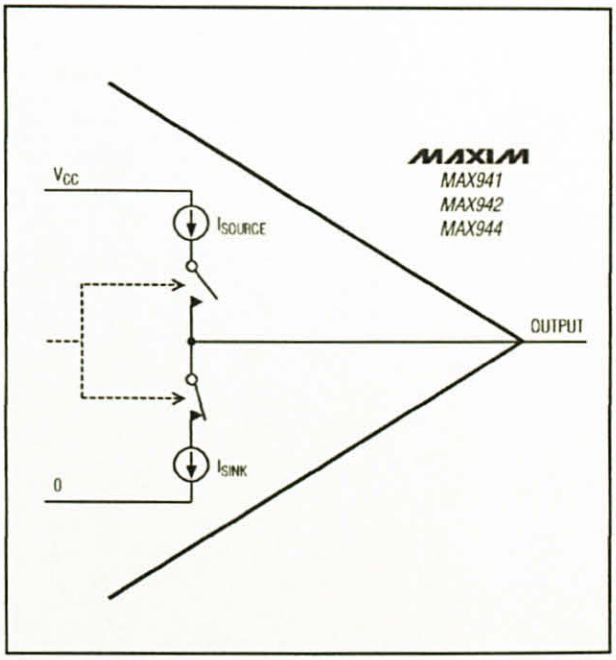


Figure 4. Output Stage Circuitry

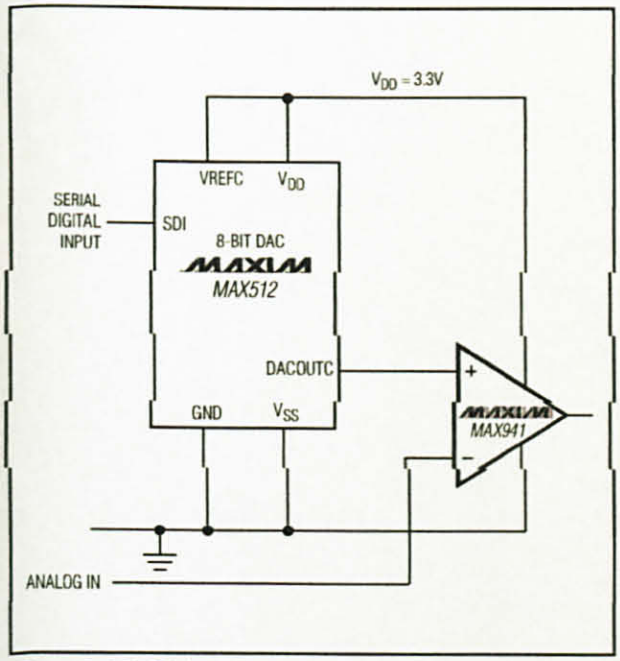


Figure 5. 3.3V Digitally Controlled Threshold Detector

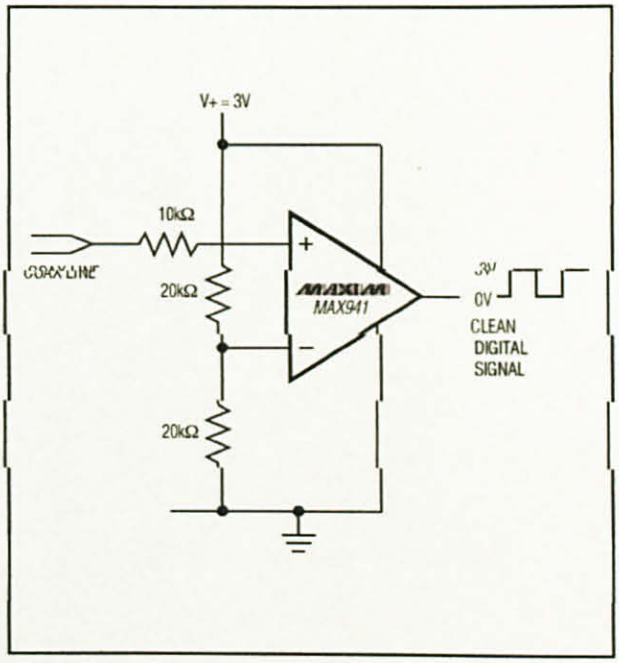


Figure 6. Line Transceiver Application

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX942MSA/PR	-55°C to +125°C	8 SO
MAX942CPA	0°C to +70°C	8 Plastic DIP
MAX942CSA	0°C to +70°C	8 SO
MAX942EPA	-40°C to +85°C	8 Plastic DIP
MAX942ESA	-40°C to +85°C	8 SO
MAX942EUA-T	-40°C to +85°C	8 µMAX
MAX942AUA-T	-40°C to +125°C	8 µMAX
MAX944CPD	0°C to +70°C	14 Plastic DIP
MAX944CSD	0°C to +70°C	14 SO
MAX944EPD	-40°C to +85°C	14 Plastic DIP
MAX944ESD	-40°C to +85°C	14 SO

Chip Information

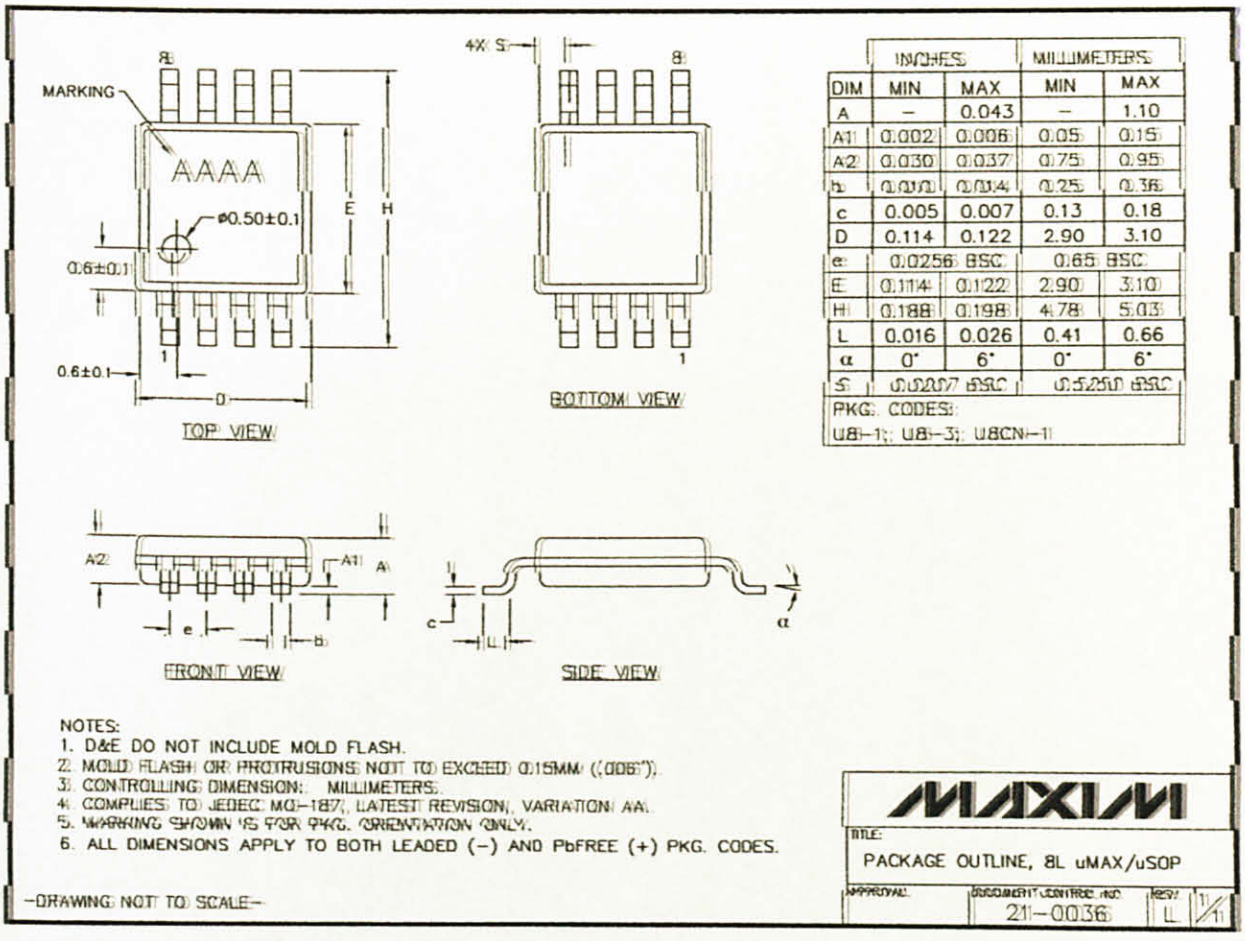
PROCESS: BiPOLAR

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

Package Information

(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 µMAX	U8-1	21-0036
8 Plastic DIP	P8-1	21-0043
8 SO	S8-2	21-0041
14 Plastic DIP	P14-3	21-0043
14 SO	S14-1	21-0041



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8-1; U8-3; U8CN-1

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO-187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

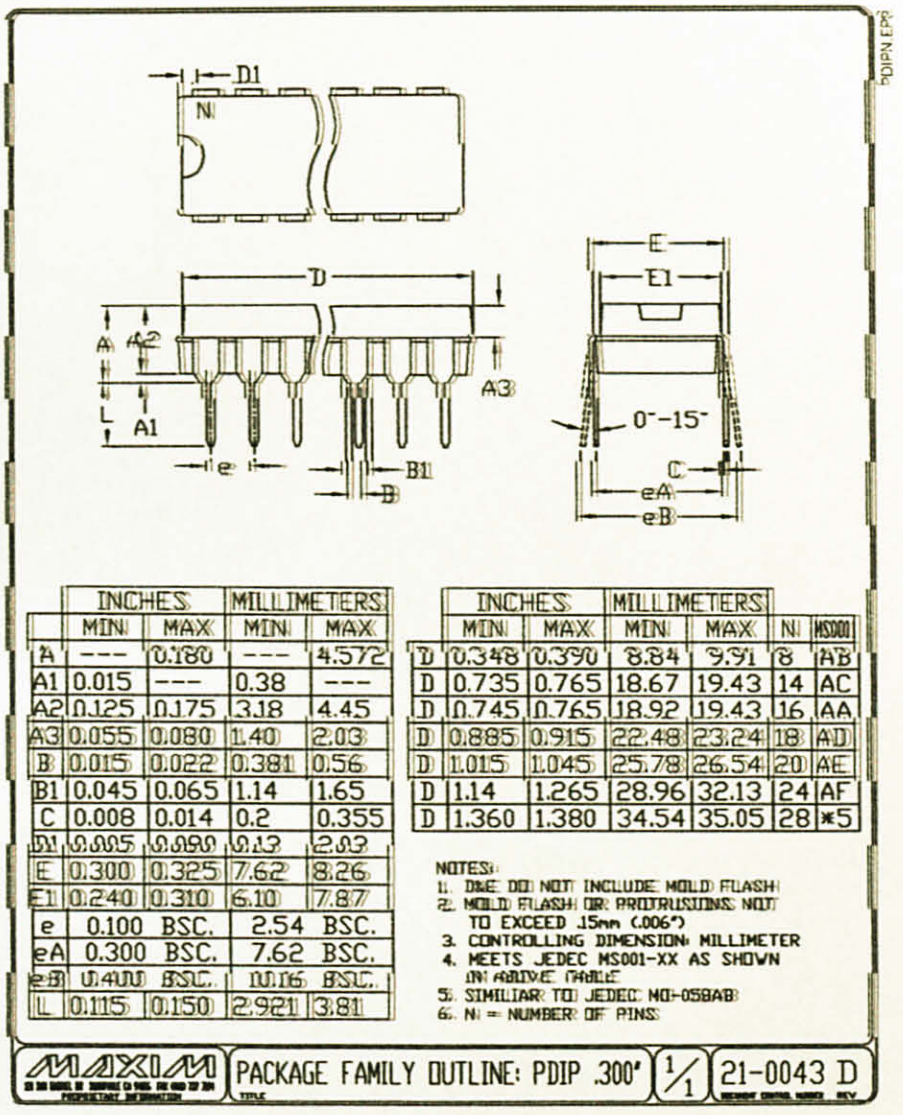
MAXIM

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV. L | 1/1

Package Information (continued)

(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 D

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

Package Information (continued)

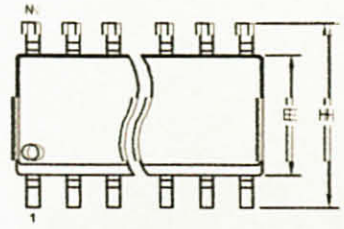
(For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.)

SOICN .EPS

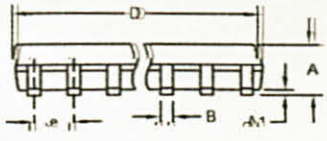
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

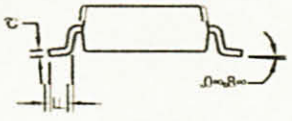
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. DIES DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
8	12/08	Added SO package diagram and removed transistor count	10
9	3/09	Corrected *Ordering Information* for MAX944ESD	10

APPENDIX D

Yuan Dean Scientific CO.,LTD

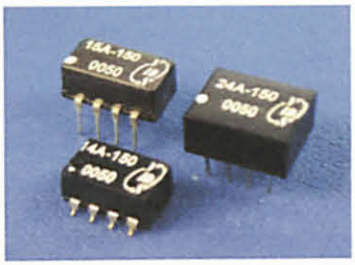
15A/14A/24A SERIES

RoHS Compliant

8 PIN LEADING & TRAILING TTL ACTIVE DELAY LINE

FEATURES

- 8-PIN PACKAGE.
- 5EQUALLY-SPACED TAPS.
- TTL SCHOTTKY INTERFACED.
- TOTAL DELAYS FROM 25-1000nS.



ELECTRICAL CHARACTERISTICS

IIH LOGIC"1" INPUT CURRENT	:50UA MAX
IIL LOGIC"0" INPUT CURRENT	:-2mA MAX
VOH LOGIC"1" OUTPUT VOLTAGE	:2.7V MIN
VOL LOGIC"0" OUTPUT VOLTAGE	:0.5V MAX
VIH LOGIC"1" INPUT VOLTAGE	:2.0V MIN
VIL LOGIC"0" INPUT VOLTAGE	:0.8V MAX
TA OPERATING TEMPERATURE	:0℃ TO 70℃
NH FANOUT"1" OUTPUT	:20 TTL LOAD
NL FANOUT"0" OUTPUT	:10 TTL LOAD
SUPPLY CURRENT	:75mA TYP.

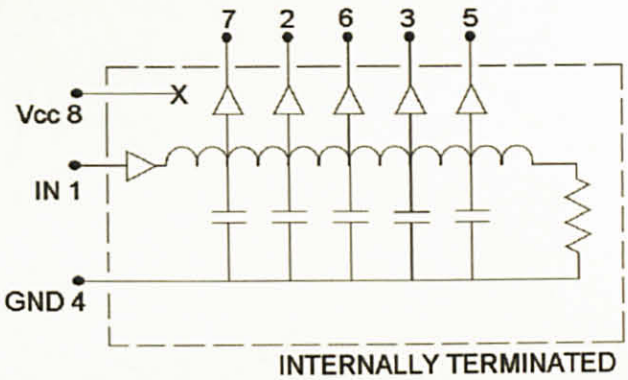
INPUT PULSE TEST CONDITION

PULSE VOLTAGE	:3.2V
PULSE WIDTH	:50NS MIN. OR 100%TD
DUTY CYCLE	:<50%
PULSE RISE TIME	:2NS(0.75 TO 2.4V)
TIME DELAY MEASURED	:@1.5V level
SUPPLY VOLTAGE VCC	:5.0±0.25VDC

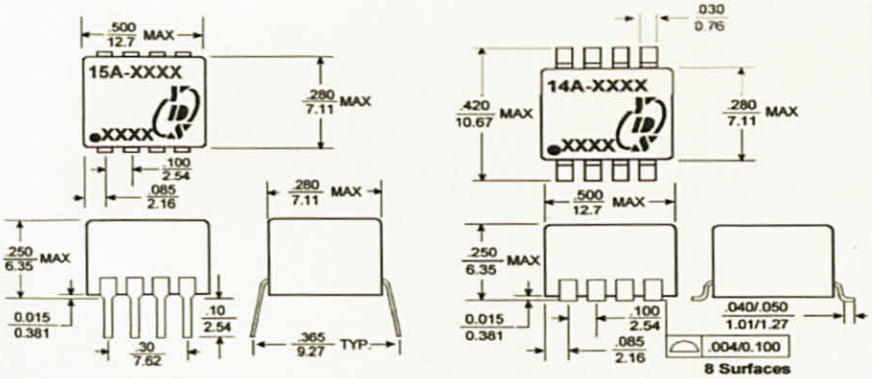
ELECTRICAL SPECIFICATIONS

PART NO.	DELAY TIME Td(nS)	TAP DELAY (nS)	RISE TIME Tr(nS)max
15A/14A/24A-025	25±2	5±2	4
15A/14A/24A-050	50±5%	10±2	4
15A/14A/24A-075	75±5%	15±2	4
15A/14A/24A-100	100±5%	20±2	4
15A/14A/24A-150	150±5%	30±2	4
15A/14A/24A-200	200±5%	40±2	4
15A/14A/24A-250	250±5%	50±5%	4
15A/14A/24A-300	300±5%	60±5%	4
15A/14A/24A-500	500±5%	100±5%	4
15A/14A/24A-1000	1000±5%	200±5%	4

PIN CONNECTIONS



MARKINGS AND DIMENSIONS



Dimensions:inches/mm Unless otherwise specified, all tolerances are ±.010/±0.25

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http://www.yds.com.tw E-mail:yds@yds.com.tw Fax:886-6-2511858

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