STUDY OF DEFORMATION AND CRACK PROPAGATION ON COMPONENT DURING REFLOW SOLDERING PROCESS

by

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DECLARATION

I hereby declare that the work reported in this thesis is the result of my own investigation and that no part of the thesis has been plagiarized from external sources. Materials taken from other sources are duly acknowledged by giving explicit references.

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LIST OF ABBREVIATIONS

3-D	Three dimensions
AHP	Analytic hierarchy process
$BaTiO_3$	Ceramic
BC	Boundary condition
BGA	Ball grid array
CSP	Chip scale package
CT	Crack tip
CTE	Coefficient of thermal expansion
CTOD	Crack tip opening displacement
DCB	Double cantilever beam
DOF	Degree of freedom
FCP	Fatigue crack propagation
FEM	Finite element method
FTEMP	Facet temperature
GA	Genetic algorithm
G_C	Critical strain energy release rate
HFL	Heat flux factor
HTP	Time integral heat flux factor
IC	Integrated circuit
IMC	Intermetallic
IR	Infrared
LEFM	Linear elastic fracture mechanics
MLCC	Multi layered ceramic capacitor

NT	Nodal temperature
PBI	Pseudo boundary integral
PCB	Printed circuit board
PCBA	Printed circuit board array assembly
PHILSM	Level set value phi
PSILSM	Level set value psi
PWB	Printed wiring board
QFP	Quad flat package
RFL	Reaction flux
SERR	Strain energy release rate
SIF	Stress intensity factor
VCCT	Virtual crack closure technique
WARP3D	Three-dimension finite element programme
XFEM	Extended finite element method

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Appendix A	Table of Hashin data used
Appendix B	The Stress intensity factor

STUDY OF DEFORMATION AND CRACK
PROPAGATION ON COMPONENT DURING REFLOW SOLDERING PROCESS

ABSTRAK

Elemen khas yang terdapat dalam pemasangan dan peranti elektronik adalah kapasitor seramik berlapis (MLCC). Walau bagaimanapun, kecacatan mekanikal MLCC seperti kekosongan, keretakan, dan penghapusan akan mengurangkan kegunaan, kebolehpercayaan, dan umur panjang peranti dengan ketara. Kecacatan mekanikal ini adalah salah satu faktor penting yang akan berkembang di permukaan permukaan kapasitor seramik berlapis, terutama lapisan antara dua bahan berbeza yang dipasang bersama. Oleh itu, tujuan kajian ini adalah untuk mengkaji penyebaran retak yang akan dijumpai di sempadan lapisan tembaga dan tembaga-epoksi kapasitor seramik berlapis semasa pematerian reflow proses. Kaedah simulasi berangka untuk proses reflow termal model MLCC dan penyebaran retak dari void mikro awal kerana pencemaran kelembapan tinggi pada lapisan itu didekati. Selain itu, aliran suhu dan pencemaran kelembapan pada lapisan tembaga dan tembaga-epoksi diperiksa semasa simulasi untuk penyebab penyebaran retak pada MLCC. Dari hasil simulasi yang dijalankan, penyebaran retak di antara lapisan tembaga dan tembaga-epoksi disebabkan oleh ketidakcocokan termal dan pertumbuhan penyebaran cecair mikro semasa proses pematerian reflow. Akibat tekanan tinggi wap yang diserap dalam jurang antara lapisan tembaga dan tembaga-epoksi, ia akan mempunyai kapasiti yang lebih besar untuk menyerap kelembapan dan menyebabkan keretakan retak, mengakibatkan suhu yang lebih tinggi diperlukan untuk memulakan retakan pada 270 ° C semasa proses reflow. Pada 284.2 (mm / mg3), kepekatan berada pada tahap tertinggi. Oleh kerana itu, kapasitor seramik berlapis menghasilkan ubah bentuk 0.077218 mm antara tembaga dan tembaga-epoksi. Tekanan sekitar yang lebih tinggi, faktor intensiti tekanan mod I, dan kadar pemanjangan retak akan berlaku akibat kekosongan yang lebih besar ini. Sebab utama reflow suhu yang berkaitan dengan masalah penyebaran patah pada kapasitor telah dikenal pasti, dan penyelesaian yang dapat dilaksanakan telah dicadangkan. Ini akan membantu pengguna akhir dengan meningkatkan prestasi dan kebolehpercayaan peralatan elektronik, serta meminimumkan kos pembuatan tambahan dan masa petunjuk yang diperlukan dalam mencari dan menyelesaikan masalah.

STUDY OF DEFORMATION AND CRACK

PROPAGATION ON COMPONENT DURING REFLOW SOLDERING PROCESS

ABSTRACT

A typical element found in electronic assemblies and devices is the multi-layered ceramic capacitor (MLCC). However, MLCC mechanical defects such as voiding, cracking, and delamination would significantly reduce the device's usefulness, dependability, and longevity. This mechanical defect is one of the significant factors that will develop in the surface mount of the multi-layered ceramic capacitor, especially the layer between the two different materials that are mounted together. Therefore, the purpose of this study is to study the crack propagation that will be found in the boundary of the copper and copper-epoxy layers of the multi-layered ceramic capacitor during the reflow soldering process. The numerical simulation method for the thermal reflow process of the MLCC model and the crack propagation from the initial micro voids due to the high moisture contamination on that layer was approached. Besides, the temperature flow and the moisture contamination on the copper and copper-epoxy layers were examined during the simulation for the causes of the crack propagation on the MLCC. From the results of the simulation conducted, the crack propagation in between the copper and copper-epoxy layers was caused by the thermal mismatch and propagation growth of micro voids during the reflow soldering process. As a result of the high pressure of vapour absorbed in the gap between the copper and copper-epoxy layer, it will have a greater capacity to absorb moisture and cause crack delamination, resulting in the higher temperatures required to commence the crack at 270 °C during the reflow process. At 284.2 (mg/mm3), the concentration is at its highest. Because of this, a multi-layered ceramic capacitor results in a 0.077218 mm deformation between copper and copper-epoxy. Higher vicinity stress, mode I stress intensity factor, and crack elongation rate would result from this greater void. The main reason for the temperature reflows that is related to the fracture propagation problems in capacitors has been identified, and workable solutions have thus been suggested. This would help the end-users by enhancing the performance and dependability of the electronic equipment, as well as minimizing the additional manufacturing costs and lead times required in locating and resolving the problems.

CHAPTER 1

INTRODUCTION

1.1 Surface Crack Technology

Manufacturing fault and in-service damage most commonly reveal themselves as early cracks, fracture and failure are particularly important in the damage tolerance assessment of advanced metallic joints. A finite element study is often performed for different type crack shapes, sizes, and locations to analyse the censorious of an initial defect and its impact on residual strength and the life of the materials. Even though, the changes in the physiography of the fracture need remeshing of the domain, the finite element approach has several limitations in such investigations (Shi et al., 2010). This is a significant limitation that makes fracture growth simulations in complex geometries difficult.

Thermal stress is dominated in solder reflow processes on printed circuit boards (PCBs). Thermal cycling is used on the solder joints, and the crack lengths at different thermal cycles are measured. Many researchers have proved the thermal-fatigue resilience of flip chips on low-cost PCBs with an underfill encapsulant using thermal cycling tests and mathematical modelling (Akbari et al., 2019). Fracture mechanics using the finite element method was used to calculate the stress intensity factors at the crack tip of varied crack lengths in the solder reflow process. Crack initiation and propagation in solder reflow of a PCB assembly was subjected to thermal cycling. While most studies on the thermal cycling reliability of single-grained solder junctions have concentrated on area array components, the current study investigates the effect for ceramic resistors.

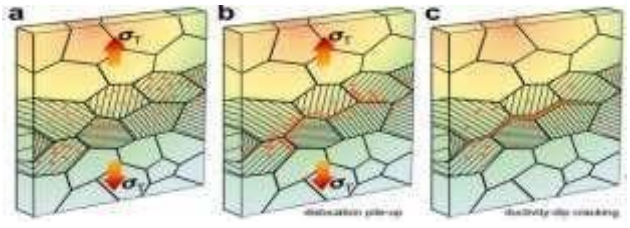


Figure 1.1 (a)Thermal stresses are applied to the sample in all feasible directions because of the temperature gradient, with dislocations mostly active in the XZ plane.

(b) Dislocations accumulate at the GBs, resulting in localised excessive deformation.

(c) Elevated local deformation causes voids and cracks to occur.

The extended finite element method (XFEM) has provided considerable improvements over other approaches such as boundary element methods, remeshing methods, and element deletion methods in reducing the computing burden associated with the insertion of arbitrary fractures into a finite element model. While the boundary element technique could accurately capture near-tip singularities, its application to elastoplastic fracture issues is cumbersome due to the employment of fictional body forces in the domain integration. Aside from that, XFEM has a few appealing properties in terms of the damage tolerance evaluation and modelling of curved crack propagation path in a complex 3D geometry, and sustainable development initiatives to combine XFEM with existing commercial FEM solvers have been promoted. The Abaqus Version 6.14.5 is used for evaluation of crack propagation parameters on static or growing crack fronts in metallic constructions using crack tip opening displacement (CTOD) and life forecasts for constant or varying fatigue load. The Figure 1.2 shows the crack analysis of XFEM by two mesh which is a free mesh, or an unstructured mesh, and a structured mesh. In unstructured meshes, each cell must hold the indices of its neighbouring cells. This is not essential in a structured mesh because it has a structure that makes it simple to determine the indices of nearby cells. Therefore, structured mesh much better to the formation of the crack. (Shi et al., 2010).

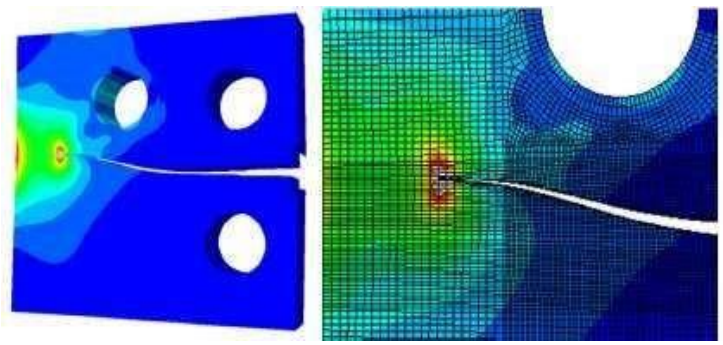


Figure 1.2 Mesh sensitivity study of crack growth patterns for the miss-hole CT specimen

It should be noted that, the operational performance of electronics systems used in safety-critical applications such as aircraft, defence, oil and gas drilling applications,

automobiles, medical devices, and power grids has now become increasingly dependent on solder joint dependability. Solder joint dependability refers to the capacity of solder joints to remain in compliance with their mechanical, electrical, and visual standards for a certain period and under a specific set of operational conditions. Multiple factors can influence the reliability of these joints, including shear strength, creep resistance, drop shock, thermal fatigue, and vibration resistance (Dušek et al., n.d.,2020).

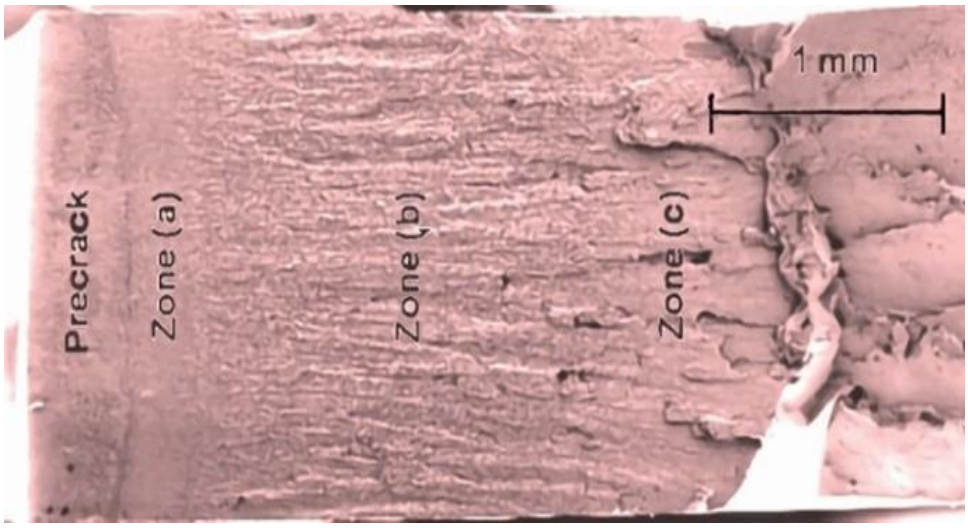


Figure 1.3 The Crack scanning electron micrographs of the fracture surface

1.2 Vapour Pressure Deamination

For a growing crack, instead of nodal degree-of-freedom (DOF) enrichment with discontinuous functions, a ghost node idea has been used, and crack formation is governed by de-cohesion rules rather than fracture mechanics requirements. Gurson's porous material model as well as the cohesive law have been updated to include vapour pressure effects on void formation. With these models' crack growth resistance-curve calculations reveal that high vapour pressure paired with high porosity results in a significant loss in fracture toughness (Kastratović et al., 2020). High vapour pressure can speed up void formation and coalescence, resulting in brittle like interface delamination in some circumstances. In an otherwise shear-dominated interface loading, vapour pressure introduces a substantial tensile mode component (Guo et al., 2009).

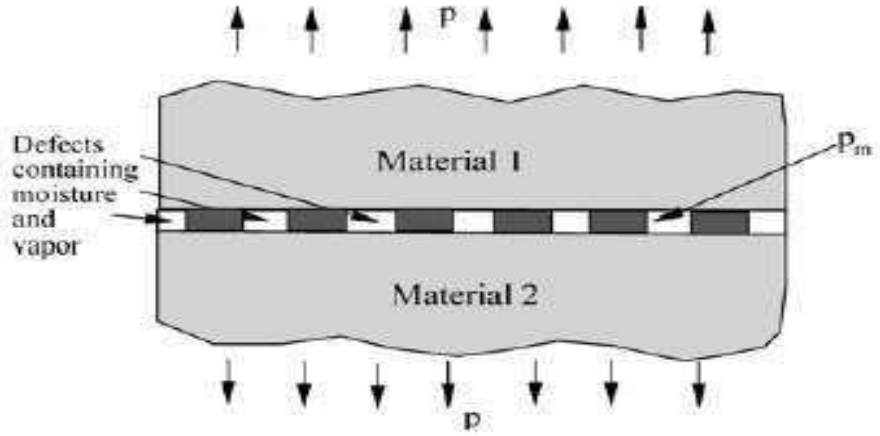


Figure 1.4 Crack formation due to the vapor pressure

The effects of vapour pressure can be seen in a variety of ways. The process of void formation and coalescence is accelerated by high vapour pressure within cavities. Vapor pressure also exerts tractions on crack faces and defects at interfaces, as well as shifting interface mode mixity from shear-dominated to tensile-dominated stress fields, potentially increasing the risk of brittle delamination.

1.3 Surface Crack Challenges

The deformation and crack on a component are deals with the fracture machine which is the involvement in field of mechanics with the study of propagation of crack formed in certain material. It is also actually deals with the fracture and failure process in materials and construction. Many manufacturing problems cause failures, including mechanical or thermal loading uncertainty, the environment, early cracks, material deficiencies, and design flaws. Fracture and failure are common issues in engineering materials, where even a minor crack can jeopardise structural integrity (Jiang et al., 2019). The analysis of stresses and strains near the crack tip is the foundation for understanding crack behaviour. Despite the presence of a plastic and damaged zone at the crack's tip, the linear elastic analysis will give an accurate mapping of reality for materials like steel. Elastic-plastic behaviour laws are fully considered for high ductility materials or excessive stresses.

Crack is formed in materials due to the overloading, stress concentration, existing flaw, or thermal expansions and by the vapour pressure. When evaluating the structural

integrity of a component, fracture initiation and growth must be examined. The widening, extending, or increase in the number of cracks on a specific surface is referred to as crack growth. Crack growth, which can occur in a range of materials including metal, wood, and concrete, can dramatically diminish a structure's load carrying capacity (Kastratović et al., 2020).

The main fracture parameters to assess the performance of structures with cracks and singular stress fields are the Stress Intensity Factor (SIF), K, and Strain Energy Release Rate (SERR), G. When a load is applied to the structure, SIF displays the stress field intensity measurement in the fracture-tip region in Figure 1.2 as well as the ability to analyse crack growth or failure. In general, SIF can be determined both analytically and numerically. Besides that, when SERR exceeds the material property critical strain energy release rate, G_C, for example when $G > G_C$, a fracture will propagate. The Virtual Crack Closure Technique (VCCT) is an energy release rate-based method in which the crack expands indefinitely(Shahwan, n.d.,2004). When a fracture length extension is imposed, the energy variation is used to calculate SERR using VCCT. Rybicki and Kanninen proposed this approach in 1977.

For crack analysis, numerical calculation is one of the most effective and general methods for solving partial differential equations of applied mechanics. In the engineering sector, the Finite Element Method (FEM) has established itself as a powerful and effective tool for modern engineering design and stress field analysis. When compared to traditional crack modelling methodologies, the ANSYS software improved the numerical method by using the Extended Finite Element Method (XFEM), which allows cracks to be represented by finite elements without the need for mesh alteration to follow crack propagation. The crack is geometrically independent of the mesh in XFEM (Shi et al., 2010)(Belytschko & Black, 1999).

According to the Western Digital crack experiment, the failure was made under the thermal shock test. Issues with the pressing or sintering processes, such as insufficient binding strength, trapping of air or foreign material, and internal sublimation of burnout material, can result in cracks that run parallel to the electrodes. Insufficient base termination thickness could more than double the percentage of MLCC failures during wave soldering. The robustness of capacitors is significantly increased thanks to the base

terminal materials and processes being optimised, and the probability of failures during high humidity operations is decreased.

1.4 Problem Statement

A 3-D displacement measuring method is required to perceive and measure all three modes (i.e., opening, sliding, and tearing fracture modes) of crack propagation on a concrete structure at the same time. Despite the fact that the diffraction pattern method has demonstrated its potential for simultaneous 3-D displacement measurement.

One of the most important criteria in determining the solder joint fault rate is reflow soldering. Traditional approaches for obtaining reflow thermal profiles rely on destructive experimental observations and trial-and-error method. However, measuring the temperature for fine pitch dimensions of a package is problematic. Only the substrate of the constructed PCB was checked when the temperature was detected using the thermocouple. A solder joint's real temperature remained unknown. Furthermore, the experimental trial-and-error method is time-consuming and costly. A thorough qualification of a new product, for example, could take up to six months of testing time.

Modelling and simulations provided further insight into the reflow process and helped the electronic manufacturing sector to solve reliability issues. Using a Finite Element Method (FEM) model, the temperature distribution of a BGA package during the reflow process was identified. The average heat-transfer coefficient was calculated using experimental formulas for a number of impinging jets. However, some reflow soldering parameters, such as track speed, flux quantity, soldering temperature, and preheat temperature, cannot be changed using the suggested approach in order to propagate the crack delamination. The solder joint reliability throughout the reflow process was significantly impacted by the process environment. In the early stages of numerical modelling, the computing power and software capability limited how well the thermal response could be predicted.

Most literature focused on the crack that emerged when it was tested electrically among the study conducted. The shock test was one of the methods employed. A similarly comparable problem, according to this, is interface cracking in electronic packing caused by vapour pressure that assisted void growth process. This happens when

the electronic packages are surface mounted on the printed circuit board at a high temperature. The plastic packaging is exposed to a humid environment where moisture is absorbed into pores and crevices. The electronic packages experiences vapour pressure because of the trapped moisture caused by the base's porosity and the conductive epoxy's hygroscopic characteristics at the high temperature. As a result, the interfacial de-adhesion at the thin layer of copper was brought on by the trap vapour pressure. Hence, research will be undertaken on this issue using data and a modelling technique to understand the causes that cause this fracture.

Aside from that, the reflow soldering process may be categorized into four stages which are preheating, soaking, reflowing, and cooling. The solder joint fault is affected by each stage of the reflow process. The cost of the experiment for the crack delamination was high, and it took more time for the crack to form between the boundary layers. With the enhanced optimization technique, solder joint flaws could be identified earlier in the production process and were more cost-effective. Production experts claim that a number of quality factors, such as thermal uniformity, reflow time, thermal stress produced, and peak temperature of a solder junction, were utilised to evaluate the effectiveness of the reflow soldering process. In order to reduce the solder connection defect of multi-layered ceramic capacitors, the current study describes a well-designed optimization methodology to enhance the many quality attributes of reflow soldering.

1.5 Objective

The precise aim of the thesis study are as follows, set against the investigated background of deformation and fracture propagation during the reflow soldering process:

1. To simulate using the Extended Finite Element Method (XFEM) of the growth and propagation of a micro-crack/delamination gap between the copper and copper-epoxy layers.
2. To investigate the damage characteristic due to moisture in the base termination and due the presence of hygroscopic properties of conductive epoxy and large void between base metal and conductive epoxy.

3. To study the effect of moisture that trapped in the void at different temperature including the vapor pressure on the conductive epoxy/base metal joint and crack initiation

1.6 Scope of Project

In this research work, the investigation of the vapor pressure on the moisture and the temperature within the epoxy/base metal joint and the solder joint are focused on the reflow soldering process through the simulation and experiment. The extended finite element method was used to simulate on the crack propagation of the metal joint by performing the thermal flow that increases the vapor pressure on the assembly which will initiate the micro void on the epoxy/base metal joint. The thermal profiling experiment and the study produced by previous researchers were used to validate the numerical method. The parametric case studies were also employed in this study to better understand board configurations, reflow oven parameter settings, and solder materials. Furthermore, the Hashin's damage approach was used to optimise the reflow soldering of a multi-layered ceramic capacitor to analyse the interactive relationship of the factors to consider distinct damage initiation mechanisms in the reflow soldering process. This research also focuses on the parametric case studies to enrich the understanding of board configurations and the crack simulations for several cases by proposing micro-voids of different sizes and shapes

1.7 Thesis Outline

The five parts of this work include the introduction, literature review, methodology, results, and discussion, as well as the conclusion. The introduction covers the study's background, problem description, and purpose of solving the problem.

In Chapter 2, crack measurement methods from the literature as well as commercially accessible technologies are discussed. The merits and limits of existing crack growth measurement approaches are thoroughly reviewed. Chapter 2 presents detailed literature evaluations of BGA technology, the reflow soldering process, and modelling and optimization methodologies for the reflow process. The structure and mechanism of fracture standards have been studied by a few researchers, and the results are reported below. The extended finite element method (XFEM) and crack tip opening

displacement were the main topics in this section (CTOD). A few papers also explain how using this method has significant limits in such investigations because changes in the topology of the fracture necessitate domain remeshing. Finally, this chapter reviews and discusses several research papers.

In chapter 3, the methodological section of this paper is covered. The flow chart shows the project's overall process flow as well as its essential steps. This chapter also investigated the effect of vapour pressure on moisture and temperature within the epoxy/base metal joint and the solder junction during the reflow soldering process using simulation and experiment. In Chapter 3, the devised method for measuring 3-D displacement components for crack growth monitoring is demonstrated. A crack model was created to crack propagation in three dimensions. The created approach uses the Hashin's damage criterion to determine the 3-D outputs (x-, y-, and z- displacement) which was applied and were extended to include the boundary condition that was applied to the multi-layered ceramic model.

Chapter 4 contains the results and comments of the experiments and demonstrations. Based on the acquired outputs and error analysis, the suggested graphical analysis approach is compared to the Western Digital experimental method. For 3-D displacement estimation, a better approach for determining 2-D displacement information is drawn by analysing experimental method that is observed from different directions. This chapter includes contains the results and discussion for the experiment employing the proposed 3-D displacement of MLCC component measurement. This chapter next discusses the results of the demonstrations utilising the devised approach to measure crack initiation and propagation on a multi-layered ceramic model.

Finally, in Chapter 5, the thesis' findings are explored, and a conclusion is formed for further research. A few suggestions were made, and a few ideas were considered for future works and initiatives.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

Various materials will deal with the deformation and the crack propagation. This can be said one of the demanding research areas learnt by many researchers. As electronic product technologies get more intricate and miniaturised, the margin of solder joint and pitch dimensions in electronic components will continue to shrink as a future trend. Besides, the high temperature storage tests, temperature flow testing, and thermal shock tests were performed on the researched soldering reflow method, as well as the vapour pressure that aids crack deformation. As a result, researchers must seek out innovative ways to analyse and improve the performance of the crack deformation in the reflow soldering process for modern packaging. Significant prior works relating to basic information about the reflow soldering method will be discussed in this chapter. In addition, before examining process in the literature linked to the analysis and simulation of the reflow soldering process, the next section provides an overview of electronic technology and delamination due to high vapour pressure during reflow.

2.2 Electronic Technology

The need for portable modern technology for instance the tablet computers, laptop computers, and smart phones is increasing at an exponential rate. As a result, there is a significant need for packaging solutions that can match customer expectations and market demands both now and in the future. The Printed board Circuit (PCB) and Ball Grid Array (BGA) are the most known technology that are prone to the crack deformation on the material. The formation of cracks in the solder joints of a PCB assembly subjected to high-speed cyclic bending has been thoroughly investigated. Lead-free tin-based alloys are often stiffer than lead-based solders, resulting in higher stress being transferred to printed circuit boards (PCBs) during thermal cycling. This could result in PCB laminate breaking around the soldering joints, which would increase PCB flexibility, relieve strain on the solder joints, and improve solder fatigue life. The first primary stress is constantly greater on the inner side of the junctions under the components, regardless

of solder grain orientation. This is in line with the findings of PCB breaking on the inside surface shown in Figure 2.1. ((Akbari et al., 2019)

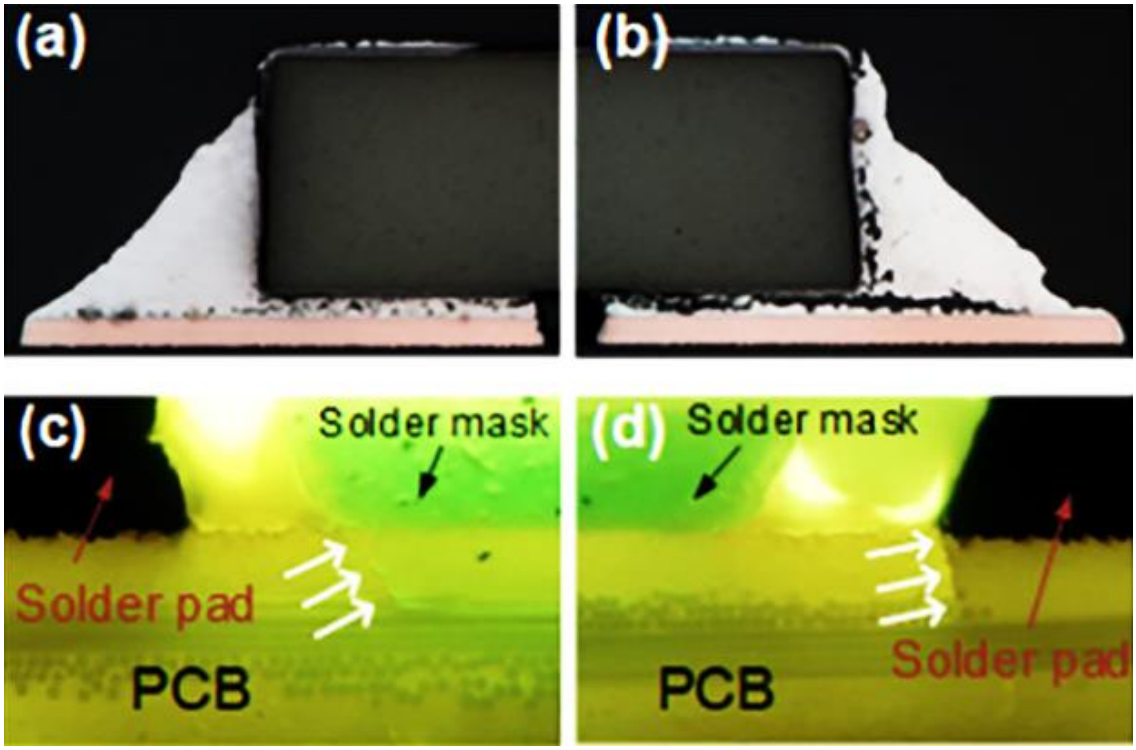


Figure 2.1 Cross-sections of the solder joints to a thermally cycled resistor showing (a–b) cracks in the two solder joints and (c–d) cracks in the PCB laminate**.**

Besides that, with applied electronics components becoming smaller, modern electronics devices have been evolving towards fine line and thin meshing nodes. Furthermore, a growing number of electronics components with fine-pitch Integrated circuit (IC) packaging, particularly Ball Grid Array (BGA) and Chip-scale package (CSP) components, have been assembled on PCB. The total separation of a solder ball can result in a break in the electrical connection between the BGA and the electronic board, which is known as a crack. Under the general coefficient of thermal expansion (CTE) mismatch, numerous studies have demonstrated that the joint with the most damage in the form of a crack that fails first for a ball grid array (BGA) component is not always situated at the site of the highest strain. This happens due to the temperature in the temperature cycle test. Figure 2.2 shows the crack deformation that is formed after the temperature cycle test that has been performed with two temperatures at relatively high-rate changes (Rahko, n.d.,2011).

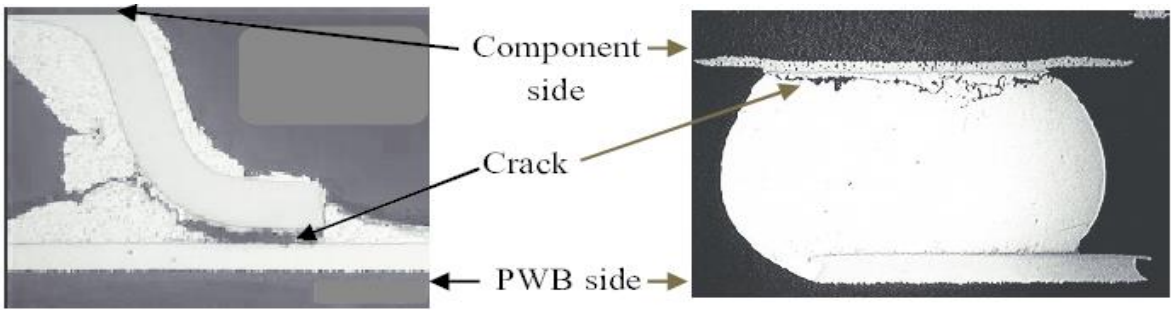
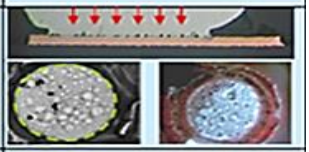
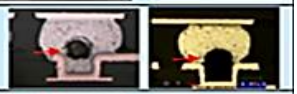
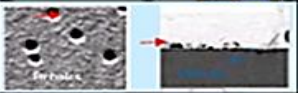


Figure 2.2 Typical QFP and BGA solder joint crack after a Temperature Cycle Test

2.2.1 Void and Crack

Voids act as stress concentrators, limiting solder joint fatigue life, and they can also act as stress relievers, slowing fracture development. The fatigue life of voids on BGA/CSP solder junctions was found to be related to voids and worse thermal cycling performance. Equivalent plastic strain and shear strain of solder junctions with voids of varied sizes at various places were computed in another early study based on finite element technique analysis. It was discovered that the existence of voids does not necessarily have a negative impact on solder joint thermal fatigue (Ribas et al., n.d.,2017).

Table 2.1 Types of voids in solder joints

Type of Voids	Description	Photos
Macro Voids	Voids generated by the evolution of volatile ingredients of the fluxes within the solder paste; typically 4 to 12 mils (100 to 300 µm) in diameter, these are usually found anywhere in the solder joint; IPC's 25% max area spec requirement is targeted toward process voids; NOT unique to LF solder joints. Sometimes referred to as "Process" voids	
Planar Micro Voids	Voids smaller than 1 mil (25 µm) in diameter, generally found at the solder to land interfaces in one plane; though recent occurrence on Immersion Silver surface finish has been highlighted these voids are also seen on ENIG and OSP surface finishes; cause is believed to be due to anomalies in the surface finish application process but root cause has not been unequivocally determined. Also called "champagne" voids	
Shrinkage Voids	Though not technically voids, these are linear cracks, with rough, 'dendritic' edges emanating from the surface of the solder joints; caused by the solidification sequence of SAC solders and hence, unique to LF solder joints; also called sink holes and hot tears	
Micro-Via Voids	4 mil (100 µm) and more in diameter caused by microvias in lands; these voids are excluded from 25% by area IPC spec; NOT unique to LF solder joints	
Pinhole Voids	Micron sized voids located in the copper of PCB lands but also visible through the surface finish; Generated by excursions in the copper plating process at the board suppliers	
Kirkendall Voids	Sub-micron voids located between the IMC and the Copper Land; Growth occurs at High Temperatures; Caused by Difference in Inter-diffusion rate between Cu and Sn. Also Known as "Horsting" Voids.	

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I. Macro Voids: These voids are very common because they are caused by the evolution of volatiles from the paste flux during reflow. Process voids are another name for them.

II. Intermetallics (IMC) Micro Voids or Kirkendall Voids: Situated between the copper coating and the intermetallic layer. The voids are caused by variations in the rates of Cu and Sn's diffusion.

III. Shrinkage Voids: These are induced by contraction strains on solidifying interdendritic eutectic solder in Pb-free alloys.

IV. Planar Micro Voids: These voids, often known as "champagne “, voids, are typically smaller than 25 μm. This can happen at any time throughout the surface finish plating process.

V. Micro-via Voids: Pb-free alloys aren't the only ones with this problem. Micro-vias in the ground are to blame.

VI. Pinhole voids: Improper copper plating is to blame. Generally, it has a diameter of 1-3 μm and are found in PCB land. (Aspandiar, n.d.,2018)

2.2.2 Vapour Pressure Crack Propagation

At high temperature, crack growth of the material was typically assisted by the vapour pressure. Moisture-induced popcorn cracking of packages during surface mounting of electronic packages onto the printed circuit board continues to be a major reliability risk in IC packaging. There are three types of cracking by vapour that have been studied extensively using conventional fracture mechanics. The die pad/moulding compound interface delamination causes the package crack in Type I. Package cracks arising from the die attach/die pad interface delamination are classified as Type II, whereas package cracks originating from the moulding compound interface delamination are classified as Type III. Figure 2.3 shows the Type 1, Type II, and Type III cracking of the die/pad moulding compound. The external and internal moisture effects on interface delamination and package cracking can be classified. The extrinsic level includes two interconnected impacts. The quickly vaporising moisture exerts tractions on the delaminated interface, resulting in a mode I crack driving force that increases as the fracture size increases. Background stresses in IC packages, on the other hand, which are mostly thermal in nature, cause a mode II loading component on polymer-silicon contacts. The increasing amplitude of vapour pressure-induced driving force shifts the

interface loading from mode II to mode I dominant as the crack grows. Both impacts are extremely damaging to the interface's integrity (Wong et al., 2014).

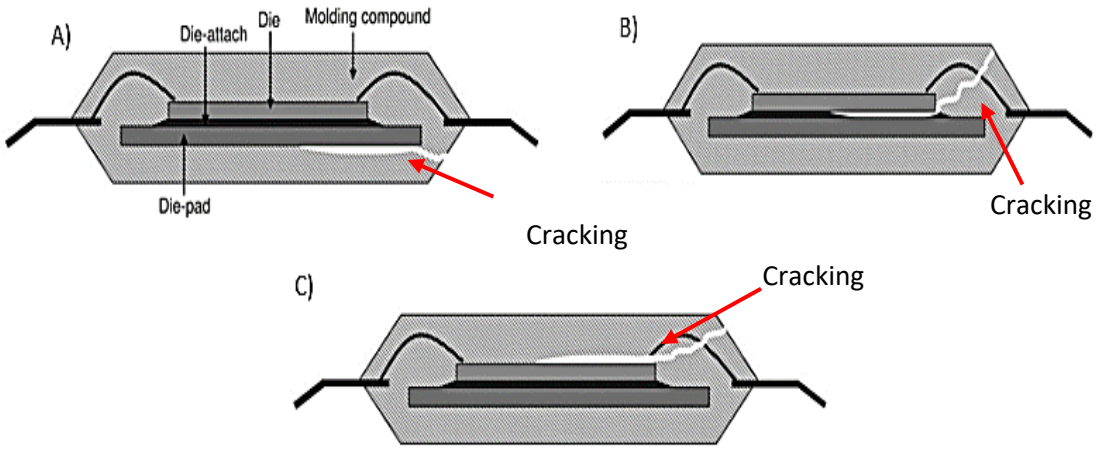

Figure 2.3 A) Type I cracking B) Type II cracking B) Type III cracking

Using a micromechanics method, interface delamination in plastic IC packages has been achieved. (Chew et al., 2008) used a cohesive law that included vapour pressure effects to simulate the die pad/moulding compound contact. Their simulations indicated that when interface delamination is predominantly driven by background thermal stress, it will be stopped after a certain amount of fracture propagation. Thermal stress and vapour pressure, on the other hand, can generate unstable delamination, resulting in Type I popcorn cracking (Wong et al., 2014).

A strip of cell elements is used to model the interface in their work. A Gurson constitutive relation is used in the cell model, with vapour pressure as an internal variable. It was discovered that high vapour pressure increases void formation, resulting in a significant drop in the toughness of the die-attach or die pad contact. Type II popcorn cracking is extremely vulnerable to the weaker joint. They conducted a full field IC package study, demonstrating the potential of the mechanism-based approach in simulating the complete failure process usually from debonding to macrocrack formation and propagation without a prior information of the essential interface for delamination (Chew et al., 2008).

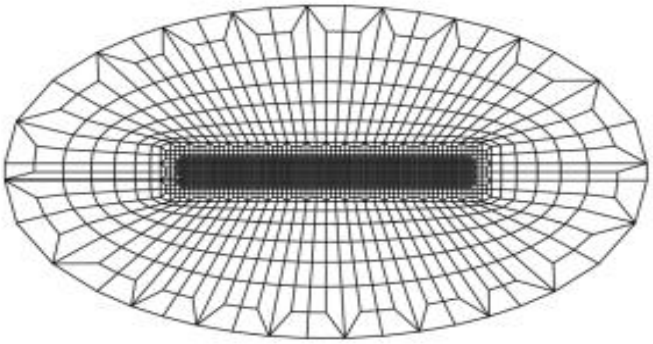

Figure 2.4 Finite element mesh for small scale yielding analysis refined mesh of inner region

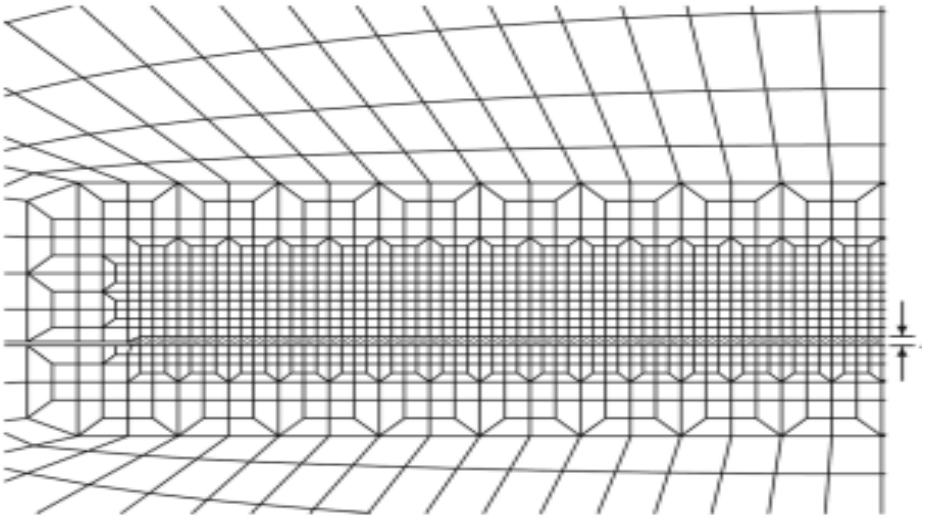

Figure 2.5 Finite element mesh for small scale yielding analysis the near-tip mesh with a strip of cell elements

The finite element mesh of the inner region of the crack geometry in Figure 2.2 is displayed in Figure 2.4. Before the initial crack tip, Figure 2.5 shows a single row of cell elements embedded in the highly refined mesh region. A vacuum of initial volume fraction linked with initial vapour pressure exists in each cell element. 3450 three-dimensional, eight-node linear elements, including 120 cell elements, make up the mesh. WARP3D, a 3D finite element programme, was used to perform the calculations. Plane strain criteria are enforced by requiring all nodes to have vanishing out-of-plane displacements (Wong et al., 2014).

2.3 Reflow Soldering Process

Reflow soldering is the procedure used to join the PCB and two different surface mount components. Currently, the main method for attaching electrical components to printed circuit boards is reflow soldering (PCBs). The component pads on the PCB are coated with solder paste beforehand (usually using a stencil printing process), and the solder paste deposits are then covered with the components. When an electrical component is inserted into the circuit board, the solder connection is made by the moulted solder paste, resulting in a strong bond (Whalley, 2004).

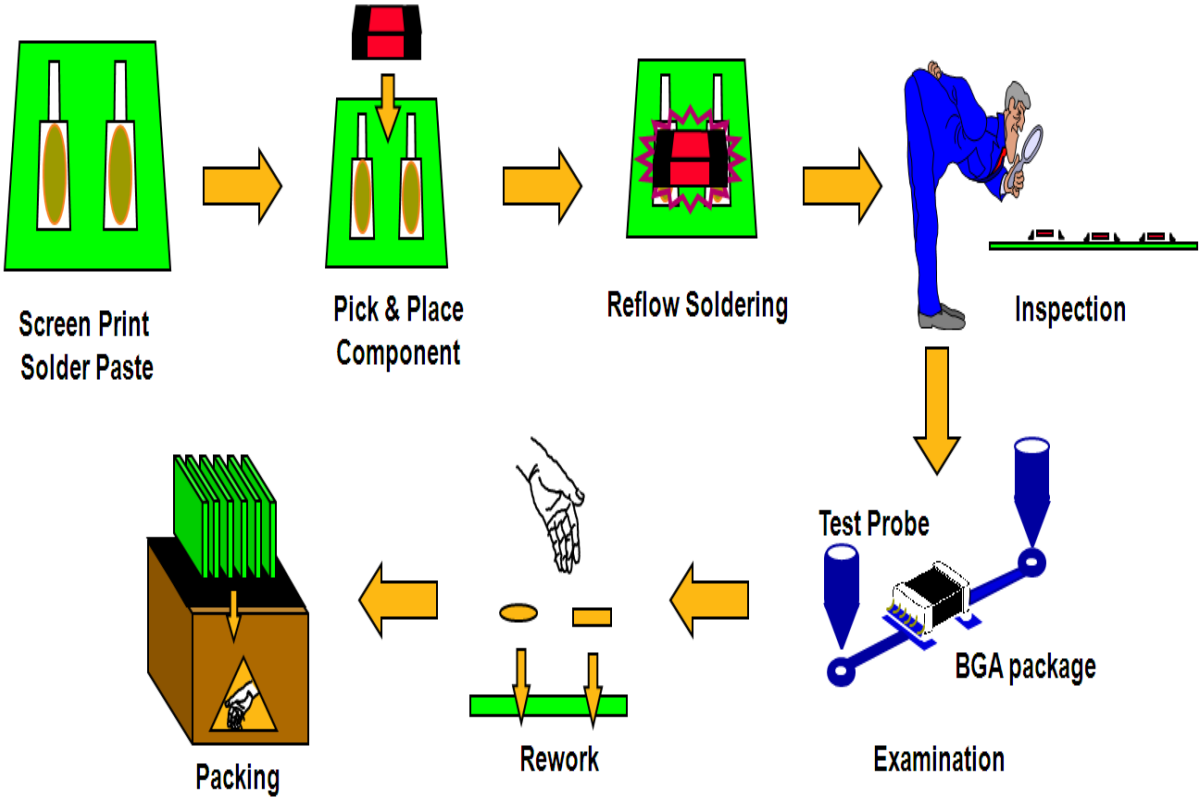

Figure 2.6 The reflow soldering process

Solder paste is screen printed onto the PCB bond pads as part of the preliminary procedures. The terrain pattern is created using a stencil during the solder paste print process. The bulk solder paste is then positioned in front of the squeegee, and the actuated squeegee blade strikes and generates hydrodynamic pressure simultaneously for both rolling and translational action, as shown in Figure 2.7 (Amalu et al., 2011). Following the separation of the PCB from the stencil, the PCB pads have deposits of paste. A

different technique involves pumping solder paste via a needle for paste registration and volume control during the dispensing operation, which deposits the solder paste. The dispensing procedure is ideal for meeting the requirements of reflow soldering on a curved surface. The arbitrary image inspection was performed after the printing process

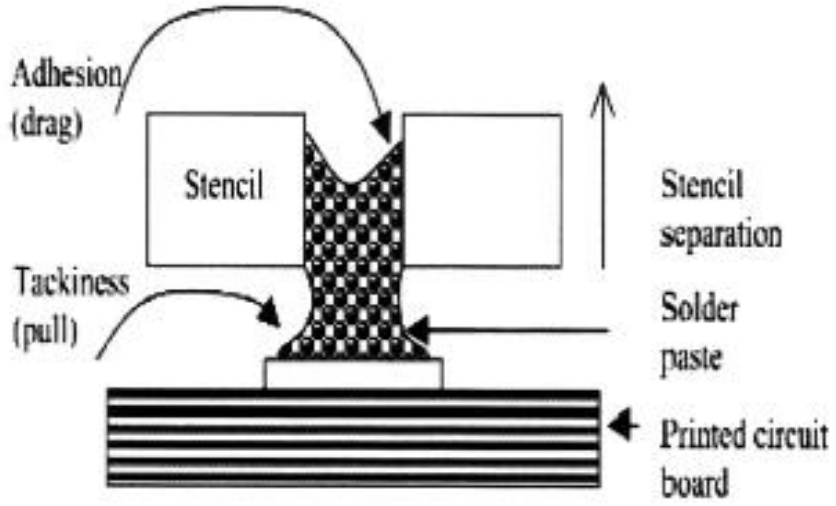

Figure 2.7 Stencil printing process

2.3.1 Reflow Oven

A reflow oven is a machine used primarily for reflow soldering of surface mount electronic components to printed circuit boards (PCBs). There are two types of reflow ovens which is batch-type and conveyor continuous-process ovens, depending on the desired production capacity. The heat-transfer mechanism, however, is another way to divide up the reflow oven. Conduction, convection, and radiation are the three types of heat transmission mechanisms that oven manufacturers typically employ. The most popular types of ovens used today are infrared (IR) reflow, forced convection reflow, and combinations of the two, but many early ovens were of the vapour phase type (Bi et al., 2006). Infrared radiation is the form of energy transfer in radiation furnaces. In the beginning, surface mount device boards were soldered using this technology. Convection ovens have almost entirely taken their place in modern manufacturing.

Recently discovered that the modified IR oven proposed by Son and Shin (2005) with the addition of the process air and retrieved from the porous panel heaters is the force convection-infrared reflow soldering process. The initially proposed adding air

(i.e., forced convection) into the soldering process through the porous panel heater to dampen the temperature fluctuations in the IR oven(Son & Shin, n.d.,2015). Force convection infrared reflow soldering with mixed air injection is recognised to have the stability of air flow and temperature fields as well as thermal control of the assembly based on the analytical results for the standard operating state. The oven operating conditions, such as the conveyor speed, temperature, and air velocity, have been properly used since they were the key factors in ensuring the dependability of the forced convection-infrared reflow soldering. Figure 2.8(a) illustrates the placement of the IR emitter panels or quartz heater in the top and bottom temperature zones of the IR reflow oven. The IR reflow oven's drawback is the potential for uneven heating of the PCB assembly, which depends on its surface characteristics and body colours. In addition, it was challenging to monitor and adjust the source temperature (Powell & Woodruff, 2006). Figure 2.8(b) illustrates the simultaneous application of convection and radiative heating or cooling to the PCB assembly. The forced convection-IR oven concept is also well suited for batch-type reflow ovens and is frequently employed in scientific research and multi-variety production.

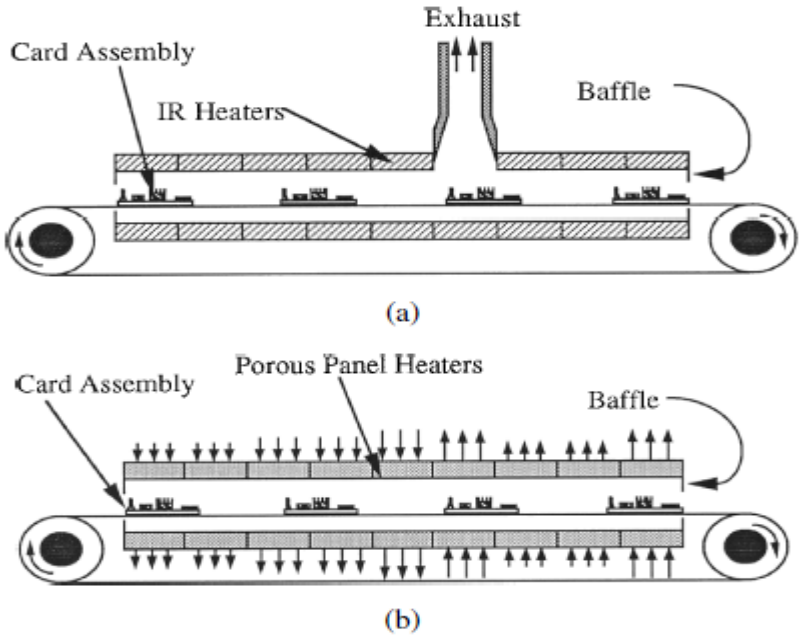

Figure 2.8 Schematic of a convectional infrared reflow oven (a) and forced convection-infrared oven (b)

A heating zone at the entry, a cooling zone at the exit, and an entrance section typically make up this kind of reflow oven. Each heating zone has two convectional heaters, one each in the top and bottom layers. As the constructed board moves through the oven, the conveyor speed can be used to modify the dwell time for each zone

2.3.2 Reflow Thermal Characterize

When attempting to increase the first pass yields in the electronics assembly, reflow soldering was the predominant method utilised to create many different sorts of contemporary electronics products which was a critical factor to consider. Additionally, it deals with the proper way to set a specific temperature profile for each solder joint in a PCBA (PCB Assembly) during the reflow process (J. Gao et al., 2007). To attach the electrical components on the PCB with solder joints, an infrared (IR) solder reflow technique with precisely controlled heating and cooling temperatures has been adopted (Liao et al., 2017). Based on that, SnAgCu solder was chosen as an alternative to traditional lead-based solder since it is lead-free (Sn63Pb37). In contrast to lead-based solder, lead-free solder often required a smaller process window and a higher melting temperature, ranging from 35 to 40 °C. Reflow thermal profiling now faces more difficulties because of the usage of lead-free soldering. In addition, the reflow thermal profiling is significantly impacted by the thermal characteristics of the various packages (Schüßler et al., 2009).

Previously, (Jin Gang Gao Yi Ping Wu Han Ding Nian Hong Wan, (2008),") propose a reference recipe, a step-by-step process to consider the specific condition of the reflow process in order to optimise the heating factor, and an analysis of the particular form of the thermal reflow profile that is accomplished by adjusting the heating factor's range (J. G. Gao et al., 2008). To achieve excellent reliability and soldering quality, the heating factors of all the solder connections in a PCBA should be controlled within a specific range (such as 200-700 s °C) during the reflow thermal process. Then, the total length was then calculated by adding up each heating zone's n value (i = 1, 2, 3, …, n) during the reflow process. The 1809EXL oven has a total of 9 heating zones. The intended reflow profile shown in Table 2.2 is taken into consideration and implemented in Figure 2.9 along with the temperature increase, dH^i (i = 1, 2, ..., n), within each t_i. The reference setting for the oven recipe is the last heating zone temperature setting Hn,

which is close to the cooling section. dHi, which should represent the temperature increase of each solder junction, particularly the hot point in the PCBA, is utilised to approximate to [(1 - exp (- (t_a - t_o/t)) (T_a - T_i)] while Hn is momentarily assumed to be a known value. In addition, the ε (plus to the compensate for the differences between the actual temperature and the thermal source temperature) was in the range of 5 to 25 °C and finally the cooling zone temperature was fixed to 110 °C. If the PWB temperature vs. time plot is assumed to be linear, then the heating rate of the PWB can be obtained by taking the slope of the measured temperature profile (Powell & Woodruff, 2006). Generally, the cold point's temperature profile's maximum rising slope is acceptable as shown in Figure 2.10. It indicates that some solder joints on the PCBA may just barely exceed the specification (2.0 °C/s) since the h point exceeds the top limit of the specification. In general, given that 2.3 is just slightly larger than 2.0, it is likewise tolarable in thermal profiling.

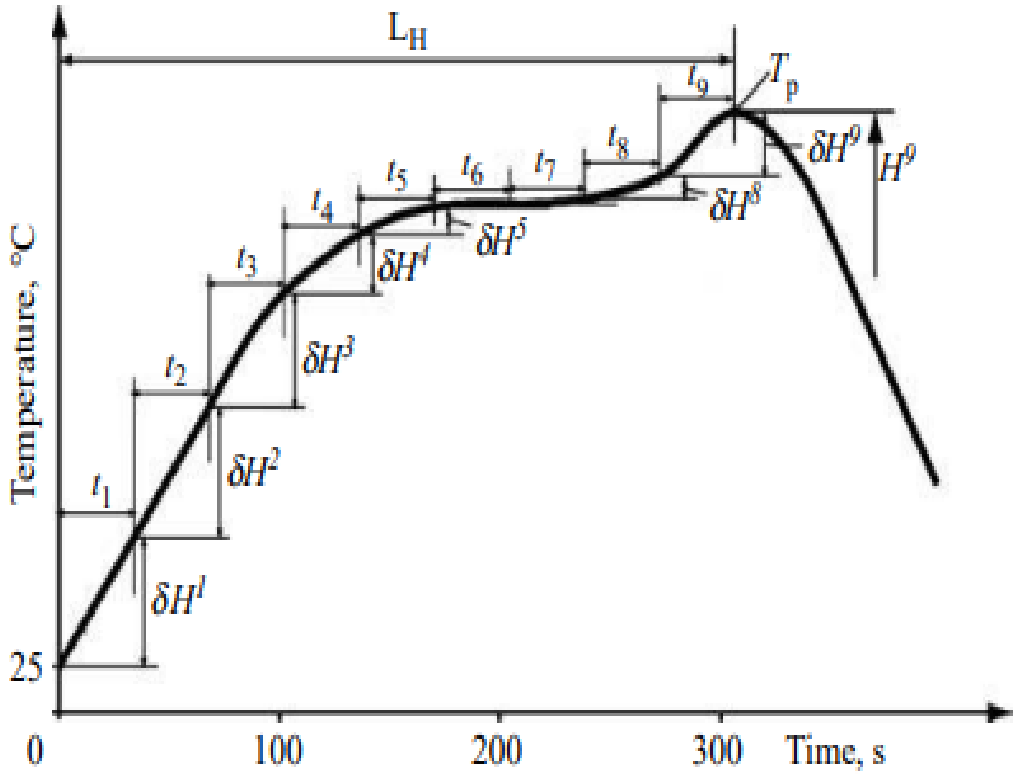

Figure 2.9 Illustration of thermal profiling

Table 2.2 The profile specifications of the critical points

	Max rising slope (°C/s)	Max soak time (s)	The heating factor (s °C)
The target profile	*2.0*	*100*	*200-700*
The hot profile	2.3	73	949
The cold profile	1.7	49	327

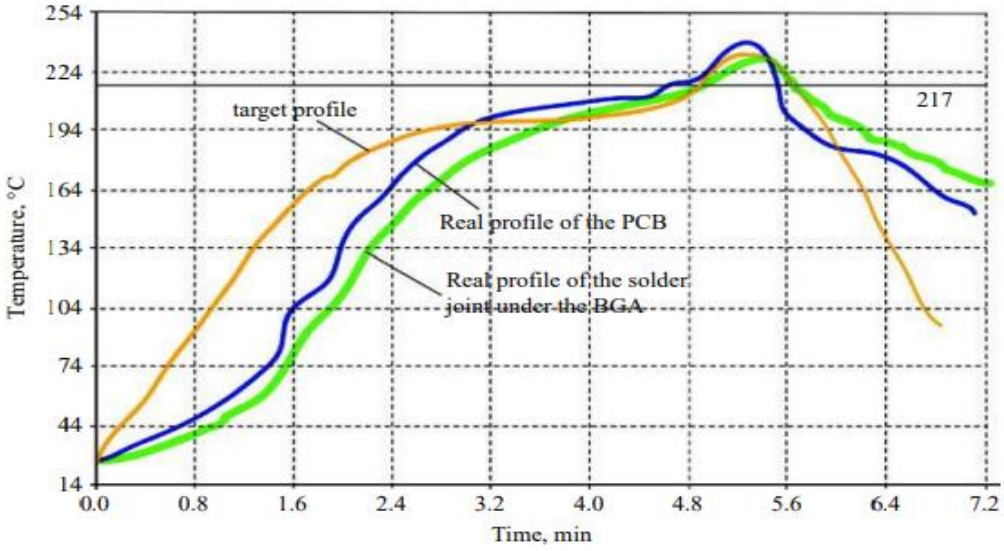

Figure 2.10 The thermal profile in response to the reference recipe

The behaviour of various cooling periods toward temperature and heat transfer efficiency in a BGA IC package was examined using the simulation mode (Srivalli et al., 2015). Two optimization technique were compared for tackling the reflow thermal profiling problem for various PCB densities, with and without merging the various performance attributes into a one measure of desirability. To identify the ideal combination of thermal profiling parameters optimised using a desirability function approach in the context of the Analytic Hierarchy Process (AHP) weighting method, the trained propagation neural network is first applied as an objective function for the evolutionary genetic algorithm operation (Tsai, 2009).

2.4 Review of Fracture Mechanism

With an existing crack or fault, a part's failure can be predicted and diagnosed using the fracture mechanics methodology. The stress around a crack in a part is increased and may cause failure earlier than would be expected using typical strength-of-materials procedures. Traditionally, strength of materials ideas have been used in the design and analysis of a part. The stresses resulting from the applied loading are computed in this instance. Once the material's strength (either the yield strength or ultimate strength, depending on the failure criterion) is exceeded by the amount of applied stress, failure is declared to have occurred.

Based on a previous study, (Zhang et al., 2010) took an approach to examining the fatigue fracture behaviours in a variety of copper/lead-free solder junctions that had been thermally aged and as soldered as well as deformed under monotonic and cyclic loads. Cu substrate material was utilised to test with the tensile test of the bulk solder in order to achieve the fatigue fracture and examine how thermal ageing affected the tensile properties of solders. An Instron E1000 fatigue testing machine was used to conduct the tensile tests at a strain rate of 1.25 s^{-1} in air at 20 °C. Additionally, fatigue tests were carried out with the loading axis vertical and parallel to the interface according to the parameter listed in Table 2.3, interrupted at various deformation cycles, for the purpose of observing the interfacial deformation and cracking behaviours to identify the fracture causes. Epoxy composite have been widely modified with various fillers, and the results have been carefully examined (Zhou et al., 2019). The period that passes between the solder junction solidifying and the point at which its maximal thermal stress exceeds its tensile stress is known as the solder joint fracture time.

Table 2.3 Reflowing, aging temperatures, and times of different solder joints

Solder joints	Reflowing Temperature (°C)	Reflowing time (min)	Aging temperature (°C)	Aging time (day)
Sn-4Ag/Cu	260	5	180	4,16
Sn-37Pb/Cu	220	5	160	7
Sn3,8Ag0.7Cu/Cu	240	5	170	7
Sn-58Bi/Cu	200	3	120	4,7,9

Under the propagation of the initial voids and the crack growth rate, fracture mechanics is employed to explain the observed crack growth phenomena. The PCB, IC component, and solder joints were constructed using a coarse mesh in the global model, which is depicted in the picture (Hofmeister et al., 2008). The accumulated voids and cracks that result from thermo-mechanical and shock stresses in solder-joint fatigue degradation grow in size and number (Huang et al., 2019). A fractured solder ball that leads to the crack happens that will result in the accumulated fatigue damage, is shown in Figure 2.11. The separation between the BGA package and solder ball was known as the fracture. Figures 2.12 show a cracked solder ball of a BGA package attached to an electronic printed circuit board (PCB). A fracture occurs when a solder ball completely separates, which can cause the electrical connection between the BGA and the electronic board to break (Hofmeister et al., 2008).

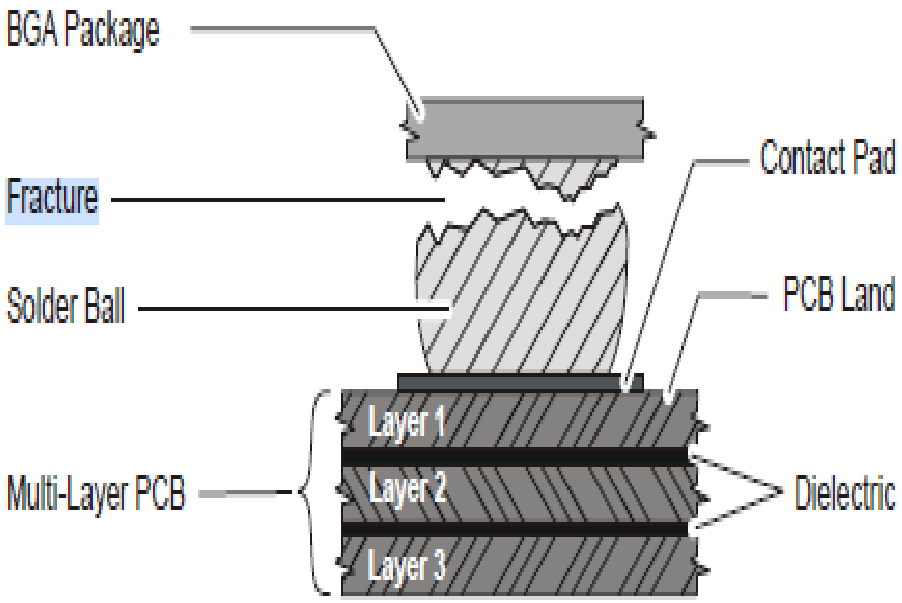

Figure 2.11 Fractured Solder Ball.

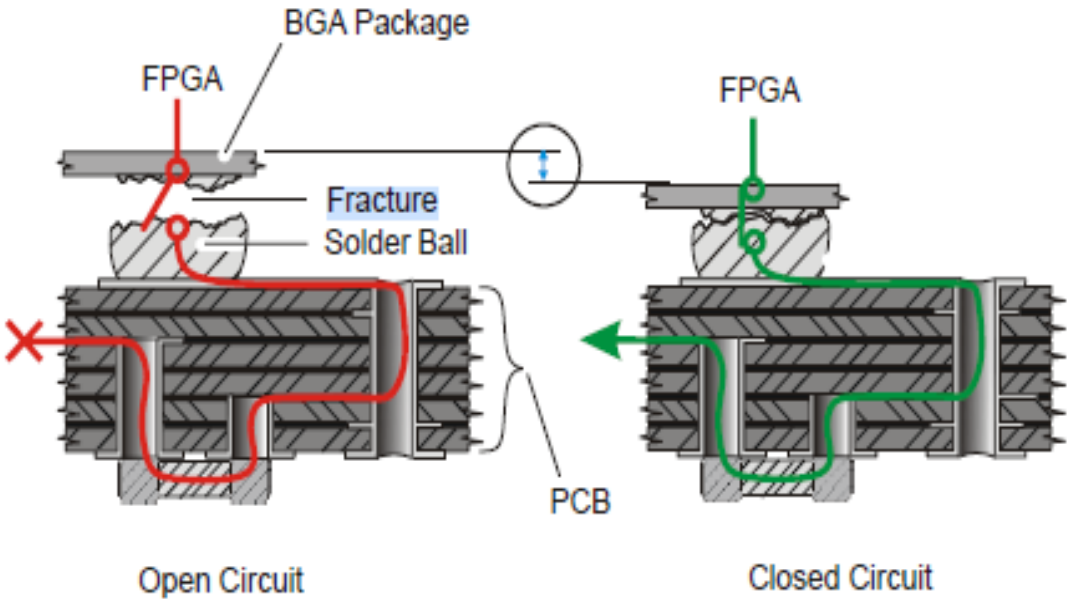

Figure 2.12 Intermittent Open and Closed Connection**.**

To mesh the tube, second order hexahedral elements are used. As illustrated in Figure 2.13, a group of hexahedral elements are compressed to create a ring of wedge elements that perfectly matches the singularity at the crack tip in order to get a