Admittance-Based Stability Analysis of Resistance-Emulating Controlled Grid-Connected Voltage Source Rectifiers

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***Abstract*—Due to low cost and high reliability, resistance-emulating control (REC) is an emerging approach for grid-connected voltage source rectifiers (VSRs). However, small-signal stability issues of the grid-connected VSR with REC are currently rarely studied. In this paper, the small-signal dq-admittance model of the grid-connected VSR with REC is first built and the small-signal stability superiority of the VSR with REC in weak-grid connection is revealed. First, a dq-admittance model of the grid-connected VSR with REC is established. The admittance characteristics of the grid-connected VSR with REC and the grid-connected VSR with traditional dual closed-loop control (DCC) are analyzed and compared. Then, the influence of short circuit ratio (SCR), voltage-loop bandwidth and the output power on the stability of the VSR with REC and DCC is analyzed based on the generalized Nyquist criterion. The stability comparison results indicate that the VSR with REC has better adaptability to the weak grid and can achieve a higher bandwidth at the voltage loop. Besides, it is found that the DCC controlled VSR is more suitable for light-load operation than the REC controlled VSR. Finally, the correctness of the analysis is verified by experiments.**

***Index Terms*—Resistance-emulating control (REC), weak grid, small-signal stability.**

I. Introduction

DUE to high controllability and improved efficiency, voltage source rectifiers (VSRs) have been widely used as the interface for power conversion systems which can provide constant DC-link voltage and achieve sinusoidal input currents [1]–[3]. However, various stability issues are introduced by the interactive dynamics between VSRs and the power grids, particularly when the short circuit ratio (SCR) is relatively small [4]–[7]. Such stability issues need to be carefully evaluated when considering the entire stable operation of power systems.

The dual closed-loop control (DCC), which owns fast dynamic response and flexible power regulation, has become one of the most dominated control methods for grid-connected VSRs [8]–[10]. The DCC usually requires a phase-locked-loop (PLL) to achieve the grid synchronization [11]. The prior-art research indicated that the PLL has a significant influence on system stability, especially in a weak grid [12]–[14]. According to the impedance-based stability analysis, a negative resistor effect near the fundamental frequency was identified, which tends to cause small-signal instability under weak grid conditions [15], [16].

To address those stability issues led by the PLL, some research efforts have been made [17]–[21]. One solution is to modify the control scheme. In [17], a pre-filter was added in the critical loop that improves the phase margin of the system. To introduce an additional damping feedback path, a feedforward compensator is proposed in [18]. Furthermore, using advanced PLLs is another good solution. Based on the adaptive filtering technique, a fast and robust PLL algorithm is presented in [19]. A more-stable enhanced PLL (MsEPLL) is developed in [20], which improves stability by adding additional nonlinear damping terms. A linear active disturbance rejection controller (LADRC)-based PLL is proposed in [21], enhancing the system damping under weak grid conditions. Although the above-mentioned solutions can improve the stability under adverse grid conditions, they all compromise on the design complexity and computation burden.

Some researches have thus been devoted to the PLL-less control to avoid the undesirable effect caused by the PLL [22]. Among them, the resistance-emulating control (REC) emerges as a promising way for the grid-connected converters [23]–[26], which is characterized by easy-to-implement and clear physical insight. The basic idea of the REC is to make the VSR imitate the external characteristics of the resistor, where the value is regulated by the outer loop. According to the passive circuit theory, the current caused by the interaction between the AC grid and the resistor is synchronized with the AC grid [23]. As a result, the synchronization of the grid current is realized naturally under the REC, which thus abolishes the PLL.

At present, the REC has shown great potentials in many applications [23]–[30]. In the earlier time, the REC was

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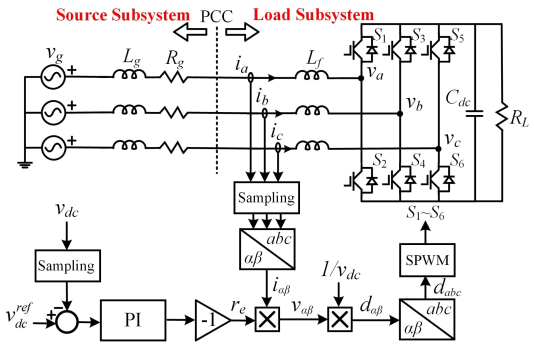

Fig. 1. Diagram of grid-connected rectifier with REC.

mostly used in the grid-connected VSRs [23]–[26]. To improve the power factor under the REC, an extremum-seeking-based power factor compensator was presented in [27]. Furthermore, following the same idea of the passive circuit emulation, the REC was extended to applications of active power decoupling [28] and three-phase unbalanced grid voltages [29] with introducing some unique concepts (e.g., the harmonic impedance, common-mode and differential-mode resistances). In the latest work [30], a negative resistance stabilized control was proposed to tackle the instability of the REC for the grid-connected inverter. All these researches validate the effectiveness of the REC for grid-connected converters. However, to the best knowledge of the authors, the small-signal stability of the VSR systems using the REC has not been studied before. Moreover, there is no comprehensively comparative analysis about the frequency-domain characteristics and the stability of the grid-connected VSRs with REC and DCC. Therefore, this paper aims to fill this void.

The main contributions of this paper are summarized as follows:

1) The dq-frame admittance model for the VSR with REC is established, and the admittance characteristics of the VSR with REC and DCC are compared and analyzed.

2) The influence of the SCR and the voltage-loop bandwidth on the stability of grid-connected VSRs with REC and DCC is studied. From the system stability viewpoint, the REC is shown to be more preferable than the DCC in a weak grid or high voltage-loop bandwidth.

The rest of this paper is organized as follows: In Section II, the concept and the control scheme of resistance-emulating technique are elaborated. Section III is devoted to deriving the dq-frame small signal admittance of the VSR with REC. The admittance characteristics of the grid-connected VSR with REC and DCC is verified and compared in Section IV. Section V gives the comparisons of the stability analyses of the system with REC and DCC. Finally, in Section VI, the results are verified by experiments.

II. Concept of Resistance-Emulating Control

Fig. 1 depicts a three-phase voltage-source rectifier (VSR) with REC. According to the idea of REC, the reference voltage to the PWM is given as

$$\mathbf{v}_{ref}^{s} = \mathbf{i}^{s} r_e \tag{1}$$

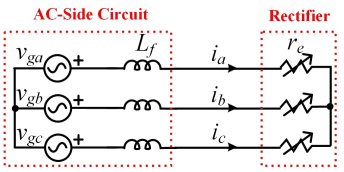

Fig. 2. The equivalent circuit of the VSR based on resistance-emulation.

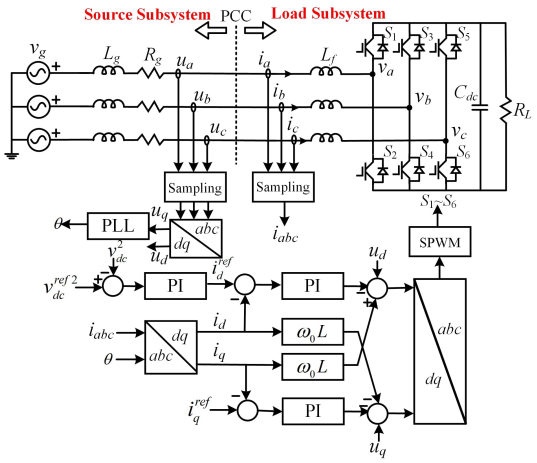

Fig. 3. Diagram of grid-connected rectifier with DCC.

where the superscript 's' is used to express the complex vector in the stationary $\alpha\beta$-frame, $e.g.$, $\mathbf{v}_{ref}^{s} = v_{ref}^{\alpha} + jv_{ref}^{\beta}$ and $\mathbf{i}^{s} = i_{\alpha} + ji_{\beta}$.

Based on (1), the equivalent schematic diagram of the three-phase VSR with REC is drawn as Fig. 2. The equivalent resistance r_e is regulated by a DC voltage controller. Then $r_e i_{\alpha}$ and $r_e i_{\beta}$ are taken as the voltage reference of the rectifier. It is emphasized that the grid current will self-synchronize with the grid because the current through any branch of a linear passive circuit will synchronize with the excitation voltage.

In the REC scheme, the AC current control loop and the PLL are eliminated. Besides, only two AC current sensors and one DC voltage sensor are used. Therefore, this control scheme is easy-to-implement and low-cost, which makes it suitable for practical application.

III. Admittance Modeling of the Grid-Connected Rectifier with REC

A. Modeling Conventions

In this paper, we use boldface letters to express complex space vectors. For example, $\mathbf{E} = E_d + jE_q$, $\mathbf{v} = v_d + jv_q$ and $\mathbf{i} = i_d + ji_q$ are the point of common coupling (PCC) voltage vector, converter voltage vector and inductor current vector, respectively. The grid impedance and the converter input admittance are denoted as $\mathbf{Z_g}(s) = Z_{gd}(s) + jZ_{gq}(s)$ and $\mathbf{Y}(s) = Y_d(s) + jY_q(s)$, respectively.

Let italic letters represent real space vectors. For instance, $v = [v_d, v_q]^T$ and $i = [i_d, i_q]^T$ for voltage and current, respectively. The relation between v and i can be described as

$$i = Y(s)\, v, \qquad Y(s) = \begin{bmatrix} Y_{dd}(s) & Y_{qd}(s) \\ Y_{dq}(s) & Y_{qq}(s) \end{bmatrix} \tag{2}$$

Notably, E_0, i_d^0 and i_q^0 are denoted as the steady-state value of PCC voltage, input current in d axis and q axis, respectively.

In our derivation, physical quantities such as voltage and current are expressed in grid dq frame, which is based on angle θ_g

$$\frac{d\theta_g}{dt} = \omega_g \tag{3}$$

where ω_g is the angular synchronous frequency and $\omega_g = 100\pi$ rad/s. The converter dq frame is based on θ, which would be consistent with the grid dq frame at steady state.

In Fig. 1, L_g, L_f, C, R_g and R_L are the grid inductance, filter inductance, DC side capacitance, grid resistance and DC load, respectively. The direct-voltage controller has two inputs for the measured DC-link voltage v_{dc} and the reference voltage v_{dc}^{ref}, one output for emulated resistance R_e. The superscripts 's' and 'c' are used to express vectors in the stationary $\alpha\beta$ frame and the converter dq frame, respectively.

B. AC Loop Modeling

The dynamic differential equation of AC loop in converter dq frame can be written as

$$L_f \frac{d\mathbf{i}^c}{dt} + j\omega_g L_f \mathbf{i}^c = \mathbf{E}^c - \mathbf{v}^c \tag{4}$$

Transforming (4) into frequency domain, whose small-signal form is written as

$$L_f s\Delta\mathbf{i}^c + j\omega_g L_f \Delta\mathbf{i}^c = \Delta\mathbf{E}^c - \Delta\mathbf{v}^c \tag{5}$$

The reference voltage to the PWM is

$$\mathbf{v}_{ref}^s = \mathbf{i}^s r_e \tag{6}$$

Rewriting (6) in the converter dq frame yields

$$\mathbf{v}_{ref}^c = \mathbf{i}^c r_e \tag{7}$$

The linearized form of (7) is

$$\Delta\mathbf{v}_{ref}^c = R_e\Delta\mathbf{i}^c + \mathbf{i}_0^c\Delta r_e \tag{8}$$

where R_e is the steady state operating point of the emulated resistance r_e and $\mathbf{i}_0^c = i_d^0 + ji_q^0$.

Considering the zero-order hold effect and calculation delay, it is obtained that

$$\Delta\mathbf{v}^c = \underbrace{\frac{\left(1 - e^{-sT_s}\right)e^{-sT_d}}{sT_s}}_{G_d}\Delta\mathbf{v}_{ref}^c \tag{9}$$

where T_s is the switching period and T_d is the dead time of the PWM switching.

Substituting (8) and (9) into (5), the AC loop model can be derived as

$$L_f s\Delta\mathbf{i}^c + j\omega_g L_f \Delta\mathbf{i}^c = \Delta\mathbf{E}^c - G_d\left(R_e\Delta\mathbf{i}^c + \mathbf{i}_0^c\Delta r_e\right) \tag{10}$$

Then (10) can be written in matrix form as follows

$$H_1\Delta i^c = \Delta E^c + G_1\Delta r_e \tag{11}$$

where

$$H_1(s) = \begin{bmatrix} L_f s + G_d R_e & -\omega_g L_f \\ \omega_g L_f & L_f s + G_d R_e \end{bmatrix} \tag{12}$$

$$G_1(s) = \begin{bmatrix} -G_d i_d^0 \\ -G_d i_q^0 \end{bmatrix} \tag{13}$$

C. DC Loop Modeling

The instantaneous active power flowing into the converter can be described as

$$P = \frac{3}{2}\mathrm{Re}(\mathbf{v}^c\mathbf{i}^{c*}) \tag{14}$$

where $\mathrm{Re}\{\cdot\}$ represents the real part of a complex number. Substituting (4) into (14) yields

$$P = \frac{3}{2}\mathrm{Re}(\mathbf{E}^c - L_f\frac{d\mathbf{i}^c}{dt} - j\omega_g L_f\mathbf{i}^c)i^{c*} \tag{15}$$

Linearizing (15) gives

$$\begin{aligned} P = {} & 1.5\left(E_0 i_d^0 + i_d^0\Delta E_d + i_q^0\Delta E_q + E_0\Delta i_d\right) - \\ & 1.5\left(L_f i_d^0\frac{d\Delta i_d}{dt} - L_f i_q^0\frac{d\Delta i_q}{dt}\right) \end{aligned} \tag{16}$$

Assume that the power losses on the switches of the rectifier are neglectable, the DC-link voltage dynamic is obtained as

$$\frac{1}{2}C_{dc}\frac{dv_{dc}^2}{dt} = P - \frac{v_{dc}^2}{R_L} \tag{17}$$

The small-signal form of (17) is

$$\Delta P = \underbrace{\left(C_{dc}v_{dc}^{ref}s + \frac{2v_{dc}^{ref}}{R_L}\right)}_{F_c}\Delta v_{dc} \tag{18}$$

Combining (16) with (18), then we obtain

$$\Delta v_{dc} = G_2\Delta E^c + H_2\Delta i^c \tag{19}$$

where

$$G_2 = \begin{bmatrix} \dfrac{3i_d^0}{2F_c} & \dfrac{3i_q^0}{2F_c} \end{bmatrix} \tag{20}$$

$$H_2 = \begin{bmatrix} \dfrac{3\left(E_0 - L_f i_d^0 s\right)}{2F_c} & -\dfrac{3L_f i_q^0 s}{2F_c} \end{bmatrix} \tag{21}$$

With the emulated resistance r_e as the controller output, the DC-link voltage controller is described as follows

$$r_e = -\underbrace{\left(k_{pd} + \frac{k_{id}}{s}\right)}_{F_{dc}}\left(v_{dc}^{ref} - v_{dc}\right) \tag{22}$$

The small-signal form of (22) is

$$\Delta r_e = \underbrace{\left(k_{pd} + \frac{k_{id}}{s}\right)}_{F_{dc}}\Delta v_{dc} \tag{23}$$

Substituting (24) into (11) to get

$$\Delta r_e = F_{dc}G_2\Delta E^c + F_{dc}H_2\Delta i^c \tag{24}$$

$$Y_{dd}=\frac{H_{i1}F_c-1.5\left(i_d^0\right)^2H_{i1}G_dF_{dc}-1.5i_d^0i_q^0H_{i2}G_dF_{dc}}{sL_fH_{i1}F_c+1.5i_d^0H_{i1}A_{i1}G_dF_{dc}+H_{i1}F_cG_dR_e+\omega_1L_fH_{i2}F_c+1.5i_q^0H_{i2}A_{i1}G_dF_{dc}} \tag{35}$$

$$Y_{qd}=\frac{-1.5i_d^0i_q^0H_{i1}G_dF_{dc}+H_{i2}F_c-1.5\left(i_q^0\right)^2H_{i2}G_dF_{dc}}{sL_fH_{i1}F_c+1.5i_d^0H_{i1}A_{i1}G_dF_{dc}+H_{i1}F_cG_dR_e+\omega_1H_{i2}L_fF_c+1.5i_q^0H_{i2}A_{i1}G_dF_{dc}} \tag{36}$$

$$Y_{dq}=\frac{-1.5i_d^0i_q^0G_dF_{dc}\left(sL_fF_c+1.5i_d^0A_{i1}G_dF_{dc}+F_cG_dR_e\right)+\left(F_c-1.5\left(i_d^0\right)^2G_dF_{dc}\right)\left(\omega_1L_fF_c+1.5i_q^0A_{i1}G_dF_{dc}\right)}{sL_fH_{i1}F_c+1.5i_d^0H_{i1}A_{i1}G_dF_{dc}+H_{i1}F_cG_dR_e+\omega_1H_{i2}L_fF_c+1.5i_q^0H_{i2}A_{i1}G_dF_{dc}} \tag{37}$$

$$Y_{qq}=\frac{\left(F_c-1.5\left(i_q^0\right)^2G_dF_{dc}\right)\left(sL_fF_c+1.5i_d^0A_{i1}G_dF_{dc}+F_cG_dR_e\right)+1.5i_d^0i_q^0G_dF_{dc}\left(\omega_1L_fF_c+1.5i_q^0A_{i1}G_dF_{dc}\right)}{sL_fH_{i1}F_c+1.5i_d^0H_{i1}A_{i1}G_dF_{dc}+H_{i1}F_cG_dR_e+\omega_1H_{i2}L_fF_c+1.5i_q^0H_{i2}A_{i1}G_dF_{dc}} \tag{38}$$

D. Closed-Loop Admittance Modeling

Substituting (24) into (11) to eliminate Δr_e, we have

$$\begin{bmatrix}M_{11}&M_{12}\\M_{21}&M_{22}\end{bmatrix}\begin{bmatrix}\Delta i_d\\\Delta i_q\end{bmatrix}=\begin{bmatrix}N_{11}&N_{12}\\N_{21}&N_{22}\end{bmatrix}\begin{bmatrix}\Delta E_d\\\Delta E_q\end{bmatrix} \tag{25}$$

where

$$M_{11}=L_fs+\frac{1.5i_d^0(E_0-L_fi_d^0s)G_dF_{dc}}{F_c}+G_dR_e \tag{26}$$

$$M_{12}=-\omega_gL_f-\frac{1.5L_fi_d^0i_q^0sG_dF_{dc}}{F_c} \tag{27}$$

$$M_{21}=\omega_gL_f+\frac{1.5i_q^0(E_0-L_fi_d^0s)G_dF_{dc}}{F_c} \tag{28}$$

$$M_{22}=-L_fs-\frac{1.5L_fi_q^{02}sG_dF_{dc}}{F_c}+G_dR_e \tag{29}$$

$$N_{11}=\frac{F_c-1.5i_d^{02}G_dF_{dc}}{F_c} \tag{30}$$

$$N_{12}=-\frac{1.5i_d^0i_q^0G_dF_{dc}}{F_c} \tag{31}$$

$$N_{21}=-\frac{1.5i_d^0i_q^0G_dF_{dc}}{F_c} \tag{32}$$

$$N_{22}=\frac{F_c-1.5i_q^{02}G_dF_{dc}}{F_c} \tag{33}$$

From (25), the dq-frame input admittance of the VSR with REC can be calculated as:

$$Y(s)=\begin{bmatrix}M_{11}&M_{12}\\M_{21}&M_{22}\end{bmatrix}^{-1}\begin{bmatrix}N_{11}&N_{12}\\N_{21}&N_{22}\end{bmatrix}=\begin{bmatrix}Y_{dd}&Y_{qd}\\Y_{dq}&Y_{qq}\end{bmatrix} \tag{34}$$

Then Y_{dd}, Y_{qd}, Y_{dq} and Y_{qq} can be solved, whose detailed expression is given in (35)-(38), shown at the top of this page.

For comparisons, the DCC shown in Fig. 3 is also considered. The VSR admittance model with DCC is developed as

$$\begin{cases}Y_{dd}^{dcc}=y_{i1}+g_{c1}G_{dc}^d\\Y_{qd}^{dcc}=y_{i2}-y_{i2}E_0G_{PLL}+g_{c1}G_{dc}^q-i_q^0G_{PLL}\\Y_{dq}^{dcc}=y_{i3}+g_{c2}G_{dc}^d\\Y_{qq}^{dcc}=y_{i4}-y_{i4}E_0G_{PLL}+g_{c2}G_{dc}^q+\dfrac{P_0}{E_0}G_{PLL}\end{cases} \tag{39}$$

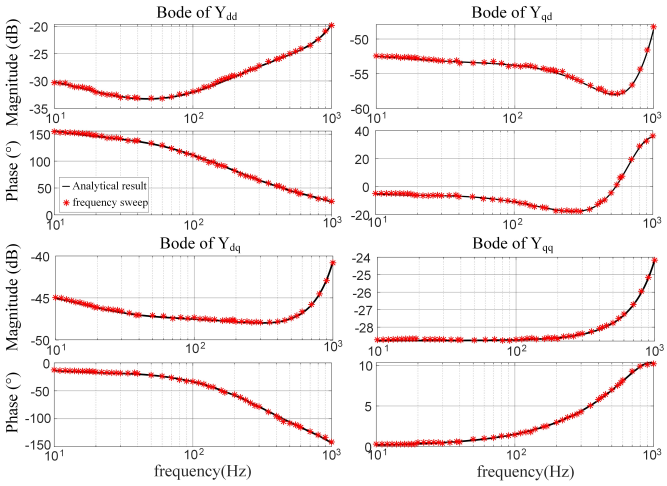

Fig. 4. The input-admittance measurement of the VSR with REC.

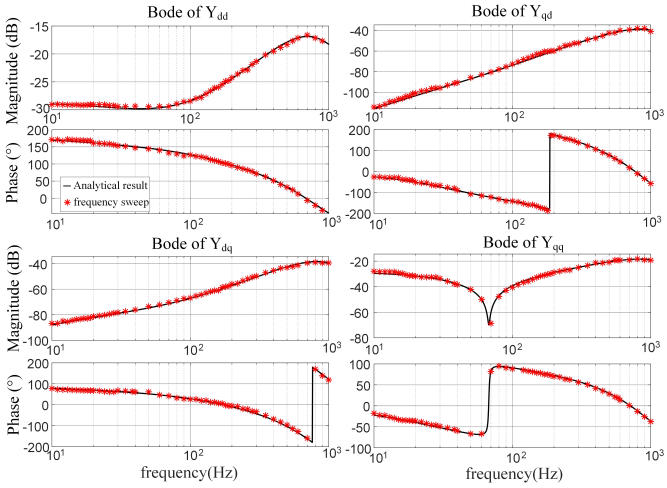

Fig. 5. The input-admittance measurement of the VSR with DCC.

where y_{i1}, y_{i2}, y_{i3}, y_{i4}, g_{c1}, g_{c1}, G_{dc}^d and G_{dc}^q are given in appendix B. The principles of controllers design for REC and DCC are presented in appendix A.

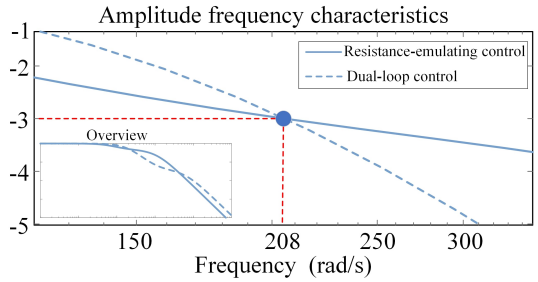

Fig. 6. The closed-loop amplitude frequency characteristic diagram of REC and DCC.

IV. Verification and Characteristic Analysis of the Admittance Model

A. Frequency Scan Validation

The input-admittance models of the VSR using REC and DCC are validated by the point-by-point frequency scanning in Matlab/Simulink. The parameters of the VSR are shown in Table I and Table II. The principles of controller design are elaborated in [10]. The measurement objects are four unknown admittance elements ($Y_{dd}, Y_{dq}, Y_{qd}, Y_{qq}$). The amplitude of the voltage perturbation is 0.02 pu and the harmonic frequency is set at 10 Hz-1000 Hz with an interval of 1 Hz-100 Hz. The perturbation is small enough to maintain the system in steady state but large enough for the system admittance identification. The admittance measurement results are drawn in Fig. 4 and Fig. 5. The black solid lines show the established admittance models of the grid-connected rectifier with REC and DCC. The red marks represent the admittance measurement results. As observed, the admittance measurement results are in good agreement with the established admittance models, which validates the accuracy of the built admittance models.

B. Comparative Results of Admittance Characteristics

Observing the dq-frame admittance characteristics shown in Fig. 4 and Fig. 5, some observations are given as follows:

1) The amplitude of Y_{dd} of REC is lower than Y_{dd} of DCC, which indicates that the REC shows a better voltage disturbance suppression capability;

2) In the low-frequency regions, the negative resistor effect is identified in both $Y(s)$ and $Y_{DCC}(s)$, which tends to cause small-signal instability;

3) Compared with $Y_{DCC}(s)$, the $Y(s)$ has a narrower negative-resistor frequency regions. Therefore, the REC is more preferable in terms of stability.

V. Stability Analysis and Comparison

In this section, the stability of grid-connected VSR with REC and DCC are carried out and compared. The system stability is identified by applying the Nyquist criterion to $Y(s)Z(s)$. Fig. 6 shows the small-signal description of a VSR connected with a grid. The VSR is modeled in Norton representation as a current source in parallel with an admittance $Y(s)$. The grid is modeled in a voltage source $v_g(s)$ in series with a grid impedance $Z_g(s)$, whose equation is given as follows.

$$Z_{\mathrm{g}}(s) = \begin{bmatrix} sL_g + R_g & -\omega_g L_g \\ \omega_g L_g & sL_g + R_g \end{bmatrix} \tag{39}$$

The relationship between voltage source and input current can be described as:

$$\Delta i(s) = \left(I + Y(s)Z_g(s)\right)^{-1}\left(Y(s)\Delta v_g(s) - \Delta i_c(s)\right) \tag{40}$$

where the grid voltage $\Delta v_g(s)$ is stable and $Y(s)\Delta v_g(s) - \Delta i_c(s)$ is also stable for properly designed converters. Therefore, whether the system is stable depends on $(I + Y(s)Z_g(s))^{-1}$, Due to the system is presented by a multi-input multi-output (MIMO) transfer matrix, the Generalized Nyquist Criterion can be applied [31]. Stability can be examined by checking the eigen loci of the eigenvalues $\lambda_1(s)$ and $\lambda_2(s)$ of open-loop gain $Y(s)Z_g(s)$. If the eigen loci do not encircle (-1, j0), then the system is stable.

The fairness of the comparison between REC and DCC is guaranteed by analyzing them under a equal voltage loop

TABLE I
Main Circuit Parameters

Symbol	Description	Value
V_g	Grid voltage (line to line)	311 V
ω_g	Grid angular frequency	100π rad/s
L_f	Filter inductor	3 mH
C	DC side capacitor	50 μF
R_L	Resistance load	80 Ω
L_g	Grid inductance	6 mH
R_g	Grid resistance	0 Ω

TABLE II
Control Parameters

Symbol	Description	Value
	(I) REC method	
v_{dc}^{ref}	DC-link voltage reference	650 V
P_0	Steady-state active power	5.28 kW
ω_{ci}	Bandwidth of voltage loop	205 rad/s
k_{pd}	Proportional gain of voltage controller	0.18
k_{id}	Integral gain of voltage controller	20
f_{sw}	switching frequency	10 kHz
f_s	Control frequency	10 kHz
	(II) DCC method	
ω_{ci}	Bandwidth of current loop	3140 rad/s
k_{pa}	Proportional gain of current controller	9.42
k_{ia}	Integral gain of current controller	1
ω_d	Bandwidth of voltage loop	205 rad/s
k_{pd}	Proportional gain of voltage controller	6.5×10^{-5}
k_{id}	Integral gain of voltage controller	0.0174
ω_p	Bandwidth of PLL	210 rad/s
k_{pp}	Proportional gain of PLL	0.6752
k_{ip}	Integral gain of PLL	0.001

bandwidth and circuit parameters. The amplitude frequency characteristic diagram of REC and DCC is shown in Fig. 7, which indicates that the voltage loop control bandwidth of REC and DCC are equal. For the comparison purpose, the following cases are studied.

A. Effect of Grid Inductance

The first case study tests the system stability with different grid inductances which determine the grid strength. Four different grid inductances for each method are tested to analyse the impact of the grid inductance: $L_{g1} = 6$ mH, $L_{g2} = 9$ mH, $L_{g3} = 12$ mH, $L_{g4} = 15$ mH.

Fig. 8 shows the Nyquist plots of the impedance ratios $Y(s)Z_g(s)$ of REC and DCC with different values of grid inductance. For a VSR with DCC, increasing grid inductance makes the Nyquist curves more easily encircle the critical point (-1, j0), the stability is therefore reduced. When $L_g \geq 12$ mH, the Nyquist plots encircle (-1, j0) and the system becomes unstable, which is shown in Fig. 8(a).

For a VSR using REC, when L_g changes from 6 mH to 15 mH, the Nyquist curves move towards to the left half plane but do not encircle (-1, j0) from the Nyquist diagram in Fig. 8(b).

Though the increase of grid inductance makes the system unstable with both control methods, when L_g increases to 12 mH the system with DCC becomes unstable while the system with REC keeps still stable. Therefore, the system with REC has better adaptability to weak grid.

To compare the effect of REC and DCC on the system stability under weak grid conditions intuitively, Fig. 9 shows the stable boundaries of R_g and L_g for both control, where the points right below the stable boundary are stable. Clearly, the stability domain of the REC is wider than the DCC.

B. Effect of Voltage Loop Bandwidth

This case is performed to study the impact of the DC voltage loop bandwidth. The comparison is carried out when both of the circuit parameters are equal. Four different voltage loop bandwidth values are tested for each method: $\omega_{d1} = 500$ rad/s, $\omega_{d2} = 654$ rad/s, $\omega_{d3} = 781$ rad/s, $\omega_{d4} = 900$ rad/s.

Fig. 10 shows the Nyquist plots of the impedance ratios $Y(s)Z_g(s)$ of REC and DCC with different values of voltage loop bandwidth. For a VSR with DCC, increasing ω_d makes the Nyquist curves move towards to the left plane to encircle the critical point (-1, j0). The instability happens when $\omega_d \geq 781$ rad/s, as shown in Fig. 10(a).

For a VSR using REC, when ω_d changes from 500 rad/s to 900 rad/s, the Nyquist curves move towards to the left plane but do not encircle (-1, j0) from the Nyquist diagram in Fig. 10(b).

The increase of voltage loop bandwidth makes the system unstable with both control methods. Nevertheless, the Nyquist curves of DCC encircle the critical point (-1, j0) more easily with the increase of ω_d. Therefore, the rectifier with REC is

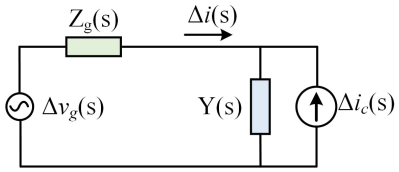

Fig. 7. Small-signal representation of the grid-connected VSR system.

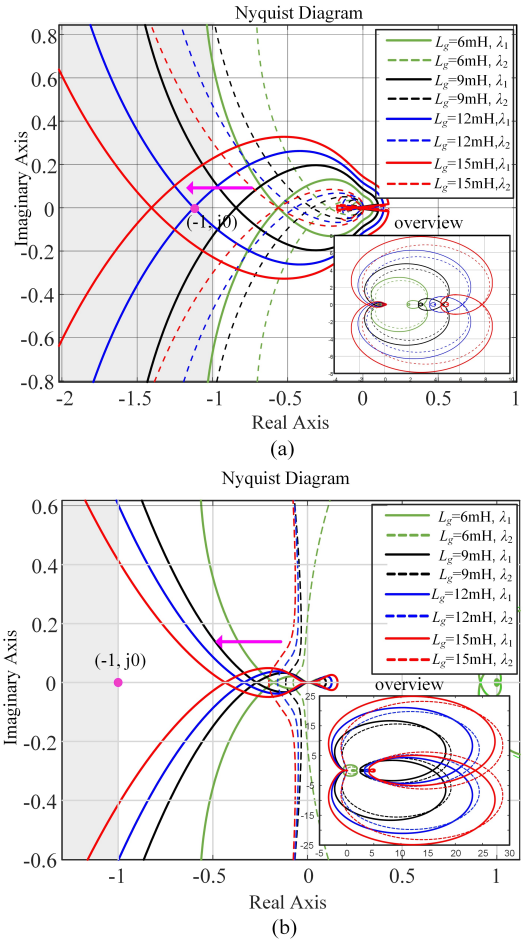

Fig. 8. Nyquist diagram of system with various DC-link voltage loop bandwidth under both control methods. (a) DCC; (b) REC.

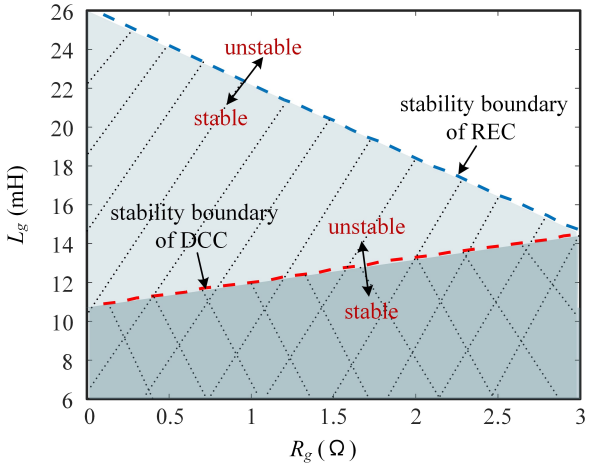

Fig. 9. The stability boundary of L_g and R_g for both control methods.

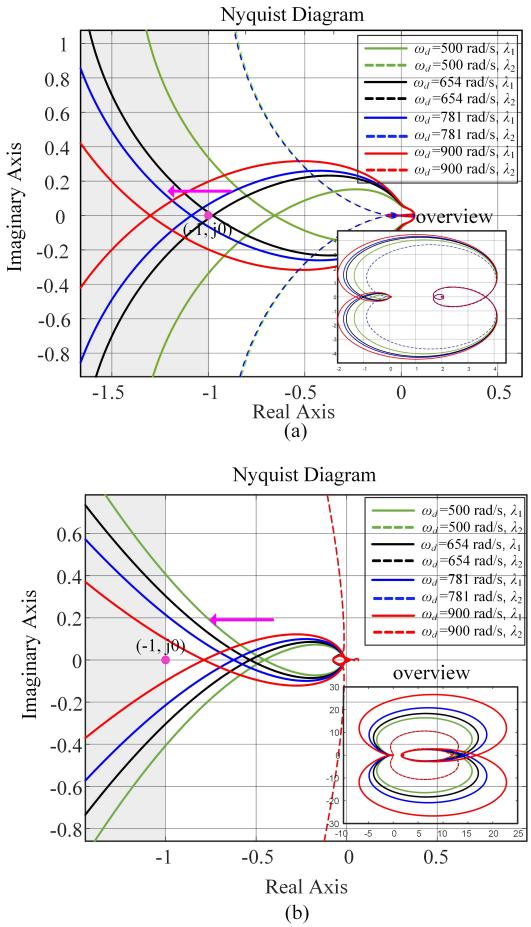

Fig. 10. Nyquist diagram of system with various DC-link voltage loop bandwidth under both control methods. (a) DCC; (b) REC.

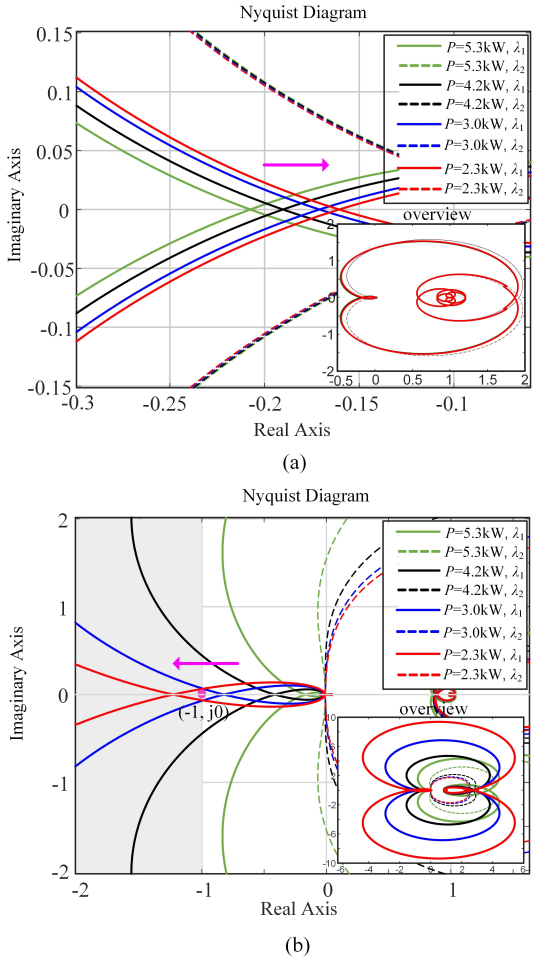

Fig. 11. Nyquist diagram of system with various DC-link voltage loop bandwidth under both control methods. (a) DCC; (b) REC.

more stable with high voltage loop bandwidth.

C. Effect of Output Power

In this case study, the effect of the output power P on system stability is studied. Four different output power values are tested to analyse the impact of P: $P_1 = 4.2$ kW, $P_2 = 3.0$ kW, $P_3 = 2.3$ kW, $P_4 = 1.9$ kW.

Fig. 11 shows the Nyquist plots of the impedance ratios $Y(s)Z_g(s)$ of REC and DCC with different values of the output power. For a VSR with DCC, reducing P makes the Nyquist curves move away from the left plane in Fig. 11(a).

For a VSR with REC, reducing P makes the Nyquist curves move towards to the left plane to encircle the critical point (-1, j0). When $P = 2.3$ kW, the system is unstable, as shown in Fig. 11(b).

Reducing P helps to stabilize the VSR with DCC. Conversely, increasing P helps to stabilize the VSR with REC. Therefore, the VSR with REC is more preferable for heavy-load condition while the VSR with DCC is more applicable for light-load condition.

VI. Experimental Results

In this section, the stability analysis and the advantages of REC are validated by experiments based on a two-level three-phase PWM rectifier built in the laboratory, as shown in Fig. 12. The controller board is mainly composed of a floating-point DSP (TMS320F28335) and a field-programmable gate array (FPGA EP2C8J144C8N). The DSP is used to accomplish the control process and output duty ratios to the FPGA. And the FPGA is used to achieve the outputs switching driving signals. The related experimental specifications are provided

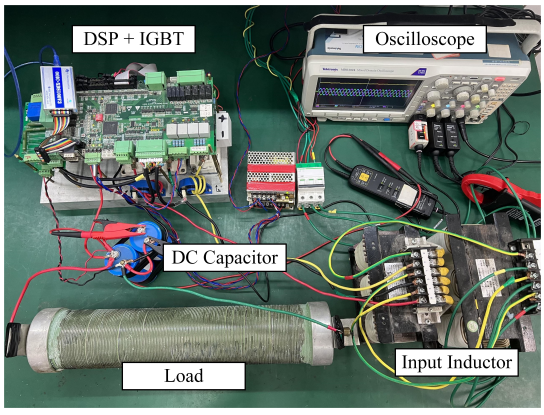

Fig. 12. Configuration of experimental setup.

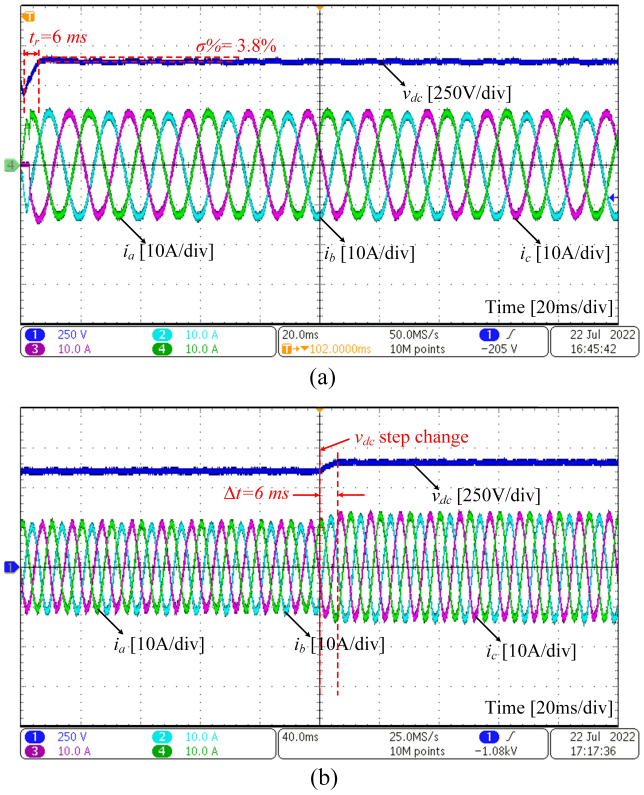

Fig. 13. Experimental results of dynamic response of the VSR with REC. (a) Dynamic response under stable operating conditions; (b) Dynamic response when DC-link voltage suddenly changes.

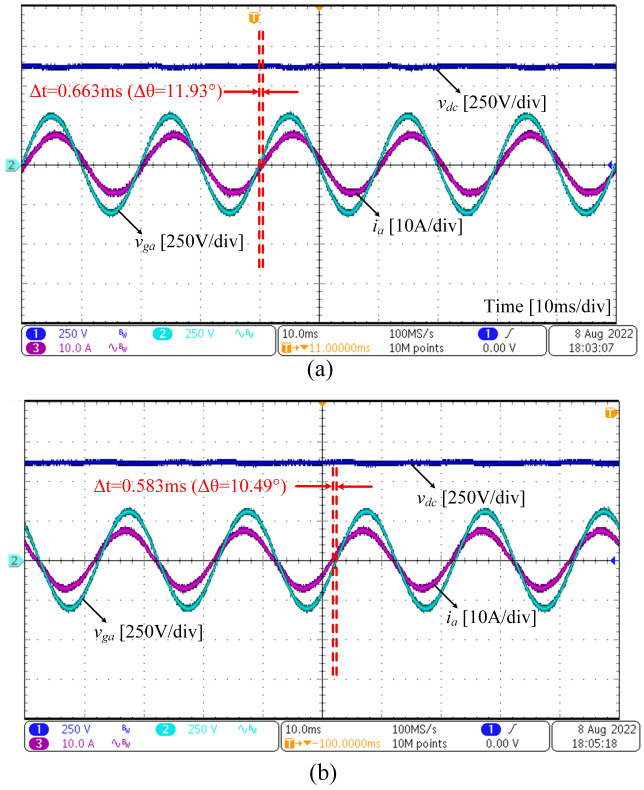

Fig. 14. Experimental results of lagging and leading power factor. (a) Lagging power factor; (b) Leading power factor.

in Table I and Table II.

Fig. 13 shows the experimental waveforms of input currents i_{abc} and DC-link voltage v_{dc} under stable operating conditions to observe the dynamic response of the VSR with REC. The dynamic response of REC method is shown in Fig. 13(a). From Fig. 13(a), we can obtain that the rise time of the system with REC is about 6 ms and the over shoot is 3.8%. Fig. 13(b) shows the transient process when the DC-link voltage reference rises from 600 V to 650 V suddenly. It can be observed that the whole transient process can be completed within 6 ms. The input current remains sinusoidal and the dc-link voltage tracks its reference at steady state. Therefore, the proposed REC can achieve a satisfying dynamic response.

The lagging and leading power factor results for the VSR with REC with the emulated fundamental frequency steady-state inductance proposed in [27] are presented in Fig. 14. Fig. 14(a) shows the experimental results with emulated inductance L_e = 1 mH (L_g + L_f = 4 mH), the lagging power factor is 0.9784. In Fig. 14(b), the experimental results show that the leading power factor is 0.9833 with emulated inductance L_e = -8 mH (L_g + L_f = 4 mH). The experimental results verify that the control strategy is effective with both inductive reactive power and capacitive reactive power.

Next, the comparative experiments between REC and DCC in weak grid are carried out. For the VSR with DCC, a stable response is observed in Fig. 15(a) when L_g = 9 mH, while an unstable response is observed in Fig. 15(b) when L_g = 12 mH. The experimental results agree with the stability analysis in Fig. 8(a). Fig. 16 depicts the experimental waveforms for the REC. When L_g is 9 mH or 12 mH, the system can keep stable, which conforms to the stability analysis in Fig. 8(b). The above experimental results demonstrate that the REC significantly extends the stability regions of the grid-connected VSR compared with DCC.

The experimental waveforms under different voltage-loop bandwidth are shown in Fig. 17. Fig. 17(a) shows the step change of the DC-link voltage loop bandwidth from 654 rad/s to 781 rad/s with DCC. The system becomes unstable at ω_d =781 rad/s, which conforms to the stability analysis in Fig. 10(a). Fig. 17(b) shows the step change of the DC-link voltage loop bandwidth from 654 rad/s to 781 rad/s with REC. When ω_d changes to 781 rad/s, the system keeps stable, which verifies the stability analysis in Fig. 10(b). The above experimental results demonstrate that the REC has better adaptability to high voltage-loop bandwidth.

The impact of the output power P on the system stability is verified by experiments. The VSR with DCC keeps stable when P = 2.3 kW as shown in Fig. 18(a), which agrees with the stability analysis in Fig. 11(a). For the VSR with REC, when P = 2.3 kW, the system becomes unstable as shown in Fig. 18(b), which conforms to the stability analysis in Fig. 11(b). The above experimental results demonstrate that the VSR with DCC is more suitable for light-load operation than the VSR with REC.

The computational effort of the proposed REC and the

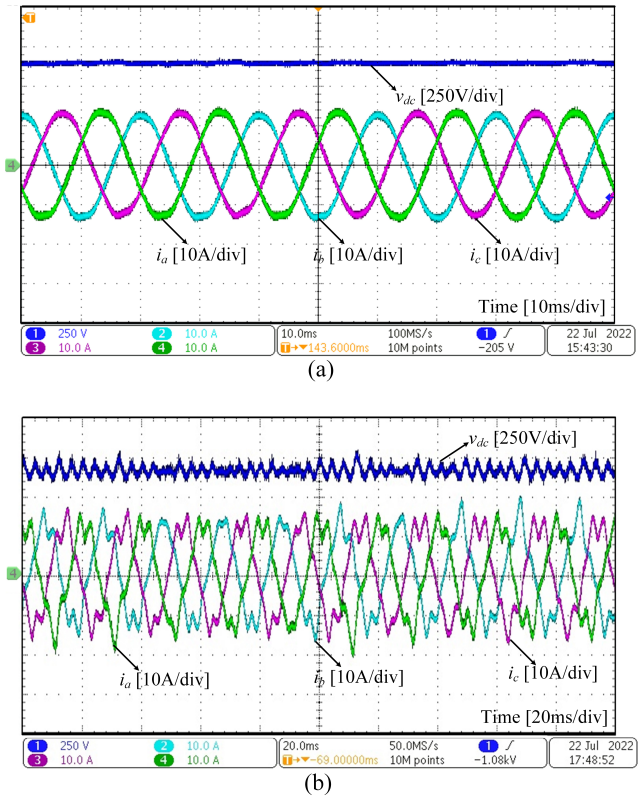

Fig. 15. Experimental results of the VSR with DCC when grid inductance changes. (a) L_g = 9 mH; (b) L_g = 12 mH.

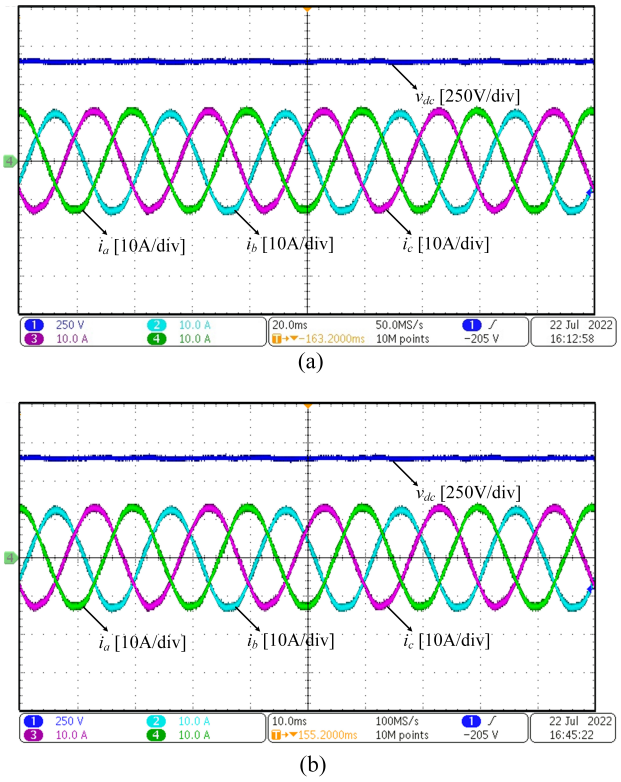

Fig. 16. Experimental results of the VSR with REC when grid inductance changes. (a) L_g = 9 mH; (b) L_g = 12 mH.

DCC are measured based on DSP TMS320F28335, and the measured results are 8.57 μs and 24.18 μs, respectively. The measured execution time of each link of REC and DCC is shown in Fig. 19. It is found that the execution time required by the proposed REC is lower than DCC, verifying the superiority of the REC in the computational effort.

Table III summarizes the comparative results between the traditional controllers and the proposed REC. Both DCC and direct power control (DPC) [6] require grid voltage sensors and PLL to achieve grid synchronization. But REC in [29] and REC in our manuscript can achieve control objects without grid voltage sensors and PLL. From the perspective of system stability, the VSR with REC can operate stably under weaker grids or higher voltage bandwidth, which reflects that the VSR with REC has a wider stability region compared to DCC and DPC. As for REC in [29], the effect of grid inductance and voltage bandwidth on stability are not analyzed and proved. Moreover, the control algorithms of DCC, DPC, REC in [29] are more complicated than that of REC, thereby, leading to a higher computational cost.

VII. Conclusion

In this paper, the dq-frame admittance model of the grid-connected VSR with REC was proposed. By using the dq-frame admittance-based approach, the stability comparison between REC and DCC was carried out. The influences of the SCR and the bandwidth of the DC-link voltage loop on the grid-VSR system stability were discussed and compared. The conclusions are drawn as follows:

1). The application of REC significantly enlarges the stability regions of VSR under weak grid conditions. From the perspective of system stability, The REC is more preferable to DCC in a weak grid.
2). The bandwidth of DC-link voltage controller is the key factor to impact the system stability. The grid-connected

TABLE III
Comparison of the DCC and the Proposed REC

Method	Grid voltage sensors	Grid synchronization method	Short SCR	High bandwidth	Stable region	Computational cost
DCC	Required	PLL	Unstable	Unstable	Narrow	High
DPC in [6]	Required	PLL	Unstable	Unstable	Narrow	High
REC in [29]	No Required	Self	Not Proved	Not Proved	Not Proved	High
Proposed	No Required	Self	Stable	Stable	Wide	Low

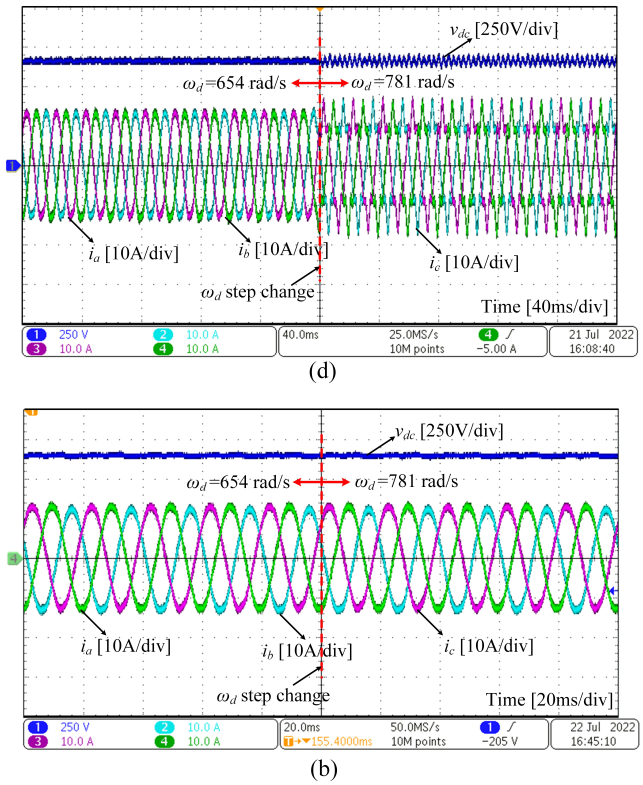

Fig. 17. Experimental results of the VSR when voltage loop bandwidth changes. (a) DCC; (b) REC.

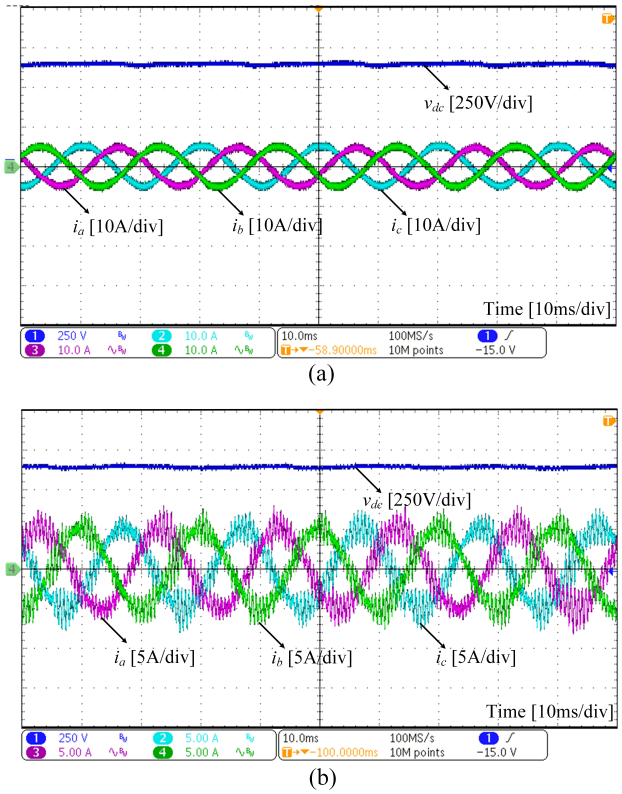

Fig. 18. Experimental results of the VSR with both method when P = 2.3kW. (a) DCC; (b) REC

VSR with the REC has better adaptability to high voltage-loop bandwidth.

3). The grid-connected VSR with REC has better flexibility to the high output power while poorer flexibility to the low output power.

APPENDIX

A. Principles of controller design of REC and DCC

1) DC Control Loop of REC: In the direct-voltage controller loop, a PI voltage controller is employed:

$$r_e = -\underbrace{\left(k_{pd} + \frac{k_{id}}{s}\right)}_{F_{dc}}\left(v_{dc}^{ref} - v_{dc}\right) \tag{A1}$$

According to the linearized DC-link voltage dynamic equation, the transfer function from Δr_e to Δv_{dc} can be derived as:

$$G_1(s) = \frac{\Delta v_{dc}}{\Delta r_e} = \frac{-K_1}{Cs + K_2} \tag{A2}$$

where $K_1 = v_{gd}^2 \Big/ (v_{dc}^{ref} R_e^2)$, $K_2 = (v_{gd}^2 \Big/ (v_{dc}^{ref2} R_e)) + (1/R_L)$.

Then the open loop transfer function of voltage loop of REC can be described as:

$$G_{dcop}(s) = \frac{K_1 k_{pd} s + K_1 k_{id}}{Cs^2 + K_2 s} \tag{A3}$$

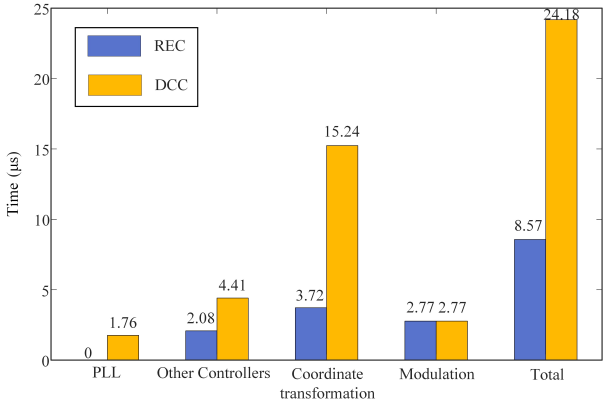

Fig. 19. Measured execution time of REC and DCC.

The open-loop amplitude-frequency characteristics can be calculated by substituting $s = j\omega$ into (A3):

$$G_{dcop}(j\omega_d) = \frac{K_1 k_{pd}\omega_d j + K_1 k_{id}}{-C\omega_d{}^2 + K_2\omega_d j} = a + bj \tag{A4}$$

The open-loop amplitude-frequency characteristics $G(j\omega_d)$ can also be expressed as:

$$G(j\omega_d) = r\cos\theta + jr\sin\theta \tag{A5}$$

where $r = |G(j\omega_d)| = 1, \theta = \gamma - 180°$ and γ is the phase margin. Based on A(4) and A(5), k_{pd} and k_{id} can be solved

as:

$$\begin{cases} k_{pd} = \dfrac{(C^2\omega_d^4 + K_2^2\omega_d^2)(K_2\cos\theta - C\omega_d\sin\theta)}{K_1K_2^2\omega_d^2 + C^2K_1\omega_d^4} \\ k_{id} = \dfrac{-(C^2\omega_d^4 + K_2^2\omega_d^2)(C\omega_d\cos\theta + K_2\sin\theta)}{K_1K_2^2\omega_d^2 + C^2K_1\omega_d^3} \end{cases} \tag{A6}$$

2) AC Control Loop of DCC: In the AC control loop, a PI current controller eliminating the dq cross coupling with PCC voltage feedforward is designed as:

$$\mathbf{v}_{ref}^c = -(k_{pa} + \frac{k_{ia}}{s})(\mathbf{i}_{ref} - G_{v2}\mathbf{i}^c) - j\omega_g L G_{v2}\mathbf{i}^c + G_{v1}\mathbf{E}^c \tag{A7}$$

where G_{v1} and G_{v2} are first-order low-pass feedforward filter of current sampling and PCC voltage sampling, respectively.

According to [10], $k_{pa} = \omega_{ci}L$, ω_{ci} is the bandwidth of current loop and $\omega_{ci} = 0.05\omega_{sw}$, where ω_{sw} is the angular switching frequency. And a small k_{ia} is employed to remove the steady-state impact of mismatch between actual and model inductances.

3) DC Control loop of DCC: In the direct-voltage control loop, a PI voltage controller is employed:

$$i_{dref} = \underbrace{\left(k_{pd} + \frac{k_{id}}{s}\right)}_{F_{dc}} \frac{(v_{dc}^*)^2 - v_{dc}^2}{2} \tag{A8}$$

k_{pd} and k_{id} can be determined by DC-link voltage loop bandwidth ω_d and phase margin. The open-loop transfer function can be written as (the closed-loop transfer function of the current loop $G_{ci} \approx 1$):

$$G_{dcop} = \frac{k_{pd}E_0R_Ls + k_{id}E_0R_L}{R_LCs^2 + 2s} \tag{A9}$$

The open-loop amplitude frequency characteristics can be calculated by substituting $s = j\omega$ into (A9):

$$G_{dcop}(j\omega_d) = \frac{k_{pd}E_0R_L\omega_d j + k_{id}E_0R_L}{-R_LC{\omega_d}^2 + 2\omega_d j} = a + bj \tag{A10}$$

Same as before, k_{pd} and k_{id} can be solved as:

$$\begin{cases} k_{pd} = \dfrac{\left(-R_L^2C^2\omega_d^3 + R_LC\omega_d^2 - 4\right)\cos\theta + 2R_LC\omega_d^2\sin\theta}{2E_0R_L\omega_d} \\ k_{id} = \dfrac{-\left(\cos\theta + 2\sin\theta\right)\left(R_L^2C^2{\omega_d}^3 + 4\omega_d\right)}{E_0R_L^3C^2\omega_d^2 + 4E_0R_L} \end{cases} \tag{A11}$$

4) Synchronization Loop (PLL) of DCC: In the synchronization loop, a PI controller is designed to output the instantaneous frequency deviation:

$$\Delta\omega = \underbrace{\left(k_{pp} + \frac{k_{ip}}{s}\right)}_{F_{PLL}} \Delta E_q \tag{A12}$$

The error angle $\Delta\theta$ can be derived as:

$$\Delta\theta = \underbrace{\frac{k_{pp}s + k_{ip}}{s^2 + E_0k_{pp}s + E_0k_{ip}}}_{G_{PLL}} \Delta E_q \tag{A13}$$

k_{pp} is selected as $k_{pp} = \omega_p/E_0$, ω_p is the bandwidth of the synchronization loop. ω_p is selected as $\omega_p \leq 0.1\omega_{ci}$ to reject PCC voltage harmonics.

B. Notations of DCC Admittance

$$y_{i1} = \frac{(1 - G_dG_{v1})(L_fs + G_dG_{v2}F_{ac})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} \tag{A14}$$

$$y_{i2} = \frac{i_q^0H_{PLL}(L_fs + G_dG_{v2}F_{ac})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} - \frac{\omega_gL_f(G_dG_{v2} - 1)(1 - G_dG_{v1} - i_d^0H_{PLL})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} \tag{A15}$$

$$y_{i3} = \frac{-\omega_gL_f(1 - G_dG_{v1})(1 - G_dG_{v2})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} \tag{A16}$$

$$y_{i4} = \frac{(sL_f + G_dG_{v2}F_{ac})(1 - G_dG_{v1} - i_d^0H_{PLL})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} - \frac{i_q^0\omega_gL_fH_{PLL}(1 - G_dG_{v2})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} \tag{A17}$$

$$g_{c1} = \frac{G_dF_{ac}(Ls + G_dG_{v2}F_{ac})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} \tag{A18}$$

$$g_{c2} = \frac{-\omega_gL_fG_dF_{ac}(1 - G_dG_{v2})}{\left(L_fs + G_dG_{v2}F_{ac}\right)^2 + \omega_g^2L_f^2\left(G_dG_{v2} - 1\right)^2} \tag{A19}$$

$$G_{dc}^d = -\frac{\frac{3}{4}(i_d^0 + (E_0 - L_fi_d^0s)y_{i1})}{\frac{1}{2}C_{dc}s + \frac{1}{R_L} + \frac{3}{4}(E_0 - L_fi_d^0s)g_{c1}F_{dc}} \tag{A20}$$

$$G_{dc}^d = -\frac{\frac{3}{4}(E_0 - L_fi_d^0s)y_{i2}}{\frac{1}{2}C_{dc}s + \frac{1}{R_L} + \frac{3}{4}(E_0 - L_fi_d^0s)g_{c1}F_{dc}} \tag{A21}$$

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