Regulated Cascode Current Mirror with Improved Voltage Swing

Vratislav Michal
STMicroelectronics, Imaging division, 12 rue Julles Horowitz, Grenoble, France
vratislav.michal@st.com

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***Abstract*—This paper presents a simple and easy-to-use method allowing to improve output swing of regulated cascode CMOS current mirror with short channel devices. It is based on matched offset voltage generators, implemented simultaneously at the input and output of the current mirror. These voltage generators translate the drain voltages of the reference and source transistors to the saturation voltage V_{DSAT}, *i.e.* to minimal level, ensuring high output resistance of the cascode. The design aims to provide a nanosecond current generator for optical laser source, with fast short channel devices facilitating the integration. This paper presents a concept of circuit implementation, a mathematical description of the optimal value of voltage offset, and simulation results in 40nm process.**

Keywords—CMOS current mirror, high-swing cascode, regulated cascode, fast current pulse generator.

I. Introduction

Recent trends in the custom IC integration cover hybrid implementation of the analog and digital VLSI circuits in sub-µm process, allowing to reduce area and power consumption of digital blocks. However, it involves complicated designs of analog circuits and may result in declining analog performances. This occurs mainly due to poor DC analog performances of sub-µm devices.

Typical sub-µm CMOS process contains several voltage-rated devices. GO1 (GO states for gate oxide thickness) are fast short-channel and low voltage devices, whereas GO2 are larger medium voltage devices designed to implement analog functions. Generally, GO2 transistor have better analog performances, except for parasitic capacitances and thus the speed.

Using transistors with several tens of nm channel length results in very fast operations, but typically poor DC performances. Transistor output resistance r_{DS} is particularly affected by short channel. It is well known that the channel length modulation $\lambda[V^{-1}]$ is responsible for limited output resistance of an MOSFET transistor in saturation [1]. It is inversely proportional to the channel length L:

$$\lambda \approx \frac{\Delta L}{V_E L} \tag{1}$$

where V_E is the approximation of Early voltage, L is the channel length and ΔL is the length of pinch-off region. Small signal output resistance r_{DS} can be expressed from λ:

$$r_{DS} = \frac{1}{\lambda I_D} \tag{2}$$

Low output resistance of the current mirror decreases accuracy of the output current. It creates a dependency between output current I_{OUT} and DC voltage V_{OUT}. Similarly,

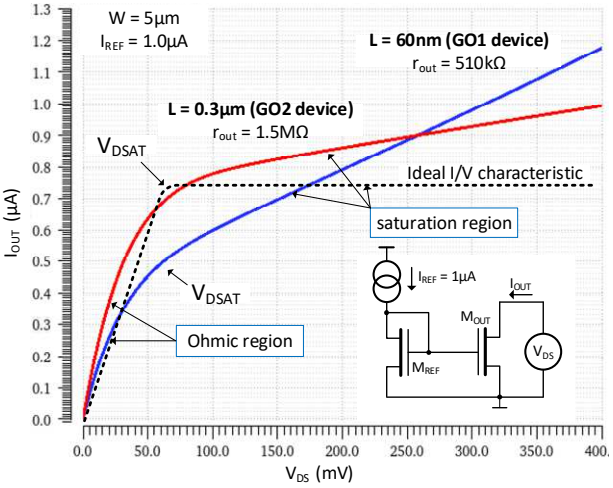

Fig. 1. Comparison of the output characteristic for a simple current mirror for GO1 and GO2 MOS transistors

limited r_{DS} reduces voltage gain of analog building blocks such as the comparators or operational amplifiers [1].

Output I/V characteristic of a simple non-cascoded current mirror with $W = 5\mu m$ is shown on example in *Fig. 1.* Output characteristic for transistors with $L = 0.3\mu m$ is relatively flat (high r_{out}), whereas it presents inconvenient high slope (low r_{out}) for short-channel device with $L = 60nm$. As we can see, transition between ohmic and saturation region for short channel device is ambiguous.

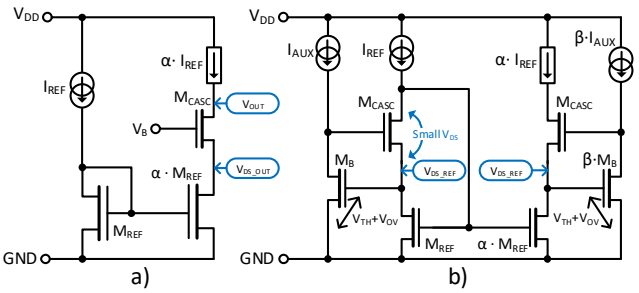

Fig. 2. a) standard "passive" cascode, b) regulated (Sackinger) cascode [2].

Increasing output impedance is typically provided either by increasing the channel length (1), (2), or by use of cascode structure. Whilst increase of the channel length allows to reach high output swing, it also presents poor AC performance related to excessive transistor area. On the other hand, standard "passive" cascode as shown in *Fig. 2. a)* increases output resistance r_{out} as given by a general cascode formula [1]:

$$r_{out} = r_{DS(casc)} + \underbrace{\left(1 + g_{m(casc)} r_{DS(casc)}\right)}_{>>1} r_{DS(ref)} \tag{3}$$

where g_m and r_{DS} are the transconductance and output

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resistances of respective transistors M_{CAS} and M_{REF}. In "passive" cascode shown in *Fig. 2 a*), M_{CASC} acts as a source follower and stabilizes the drain voltage of M_{REF}. It means that V_{DS_OUT} is maintained roughly constant by g_m of the cascode transistor. When considering an example of very low r_{DS} for 60nm device from *Fig. 1*, improvement (3) provided by "passive" cascode is insufficient, and the cascode presents non-negligible dependence between I_{OUT} on V_{OUT}.

With drain voltage stabilization realized by source follower *Fig. 2 a*) being insufficient for short-channel devices, an active loop regulating V_{DS} voltage of M_{REF} can provide very high stability. Regulating loop can be provided either by an OTA [1], or in a simple way by a regulated cascode [2] shown in *Fig. 2 b*). Circuit of regulated cascode can reach very high speed. This is mainly thanks to the simplicity, as well as to the use of short-channel devices in the feedback loop.

In the circuit of regulated cascode shown in *Fig. 2 b*), reference and source branches contain supplementary transistors M_B and small auxiliary bias currents I_{AUX}. Transistors M_B with current source I_{AUX} create a gain stage that regulates V_{DS} of M_{REF} to the value of gate-source voltage of M_B. This voltage is given by the geometry W/L of M_B and value of the bias current I_{AUX}:

$$V_{GS(B)} = V_{TH} + V_{OV} = V_{TH} + \sqrt{\frac{2I_{AUX}}{\mu_{n,p}C_{OX}}\frac{L}{W}} \qquad (4)$$

where V_{TH} is the threshold voltage, V_{OV} overdrive voltage $V_{OV} = V_{GS} - V_{TH}$, μ_n is the carrier mobility, C_{OX} the gate capacitance and W/L the aspect ratio of transistor M_B. Deviation from regulation target $V_{DS\_REF} \neq V_{GS(B)}$ is compensated by the feedback loop *via* gate voltage of M_{CASC}. It results that output impedance r_{out} of passive cascode (3) is amplified by the voltage gain of transistor M_B.

II. High-swing Regulated Cascode

In low voltage CMOS design, the target is to ensure operations of the current mirrors in a wide voltage range, namely towards low V_{DS} voltages. General approach to maximize the output voltage swing of the cascode *Fig. 2 a*) is to set voltage V_b to an optimal value allowing V_{DS} of M_{REF} to be equal to its saturated voltage V_{DSAT}. At this voltage, transistor operates between linear and saturated regions and reaches decent r_{DS}. Such performance can be achieved *e.g.* by Sooch cascode [3], Brooks - Rybicki cascode [4] or others known structures mentioned *e.g.* in [1].

By definition, $V_{DS} = V_{DSAT}$ places the transistor between linear (ohmic) and saturated regime. In first-order approximation V_{DSAT} is given by a simple formula:

$$V_{DSAT} = V_{GS} - V_{TH} \qquad (5)$$

Even though this equation is sufficient for long-channel devices, it is a rough approximation for short channel devices. On the other hand, definition of V_{DSAT} for short-channel devices is very ambiguous (see *Fig. 1*). It results that some acceptable inaccuracy have negligible impact on resulting r_{DS}. Compared to optimal V_{DSAT} of high-swing cascode from *Fig. 2 a*), drain voltage of regulated cascode *Fig. 2 b*) is high, because it contains full V_{TH} of transistor M_B.

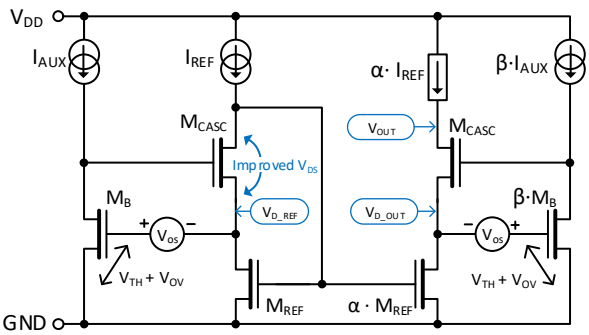

Fig. 3. Increasing output voltage swing of regulated cascode by setting $V_{DS(REF)}$ to V_{DSAT}. Voltage source V_{OS} are set to ~$V_{TH(B)}$.

This inconvenient biasing decreases output voltage swing by several hundreds of mV. In addition, high drain voltage of M_{REF}, and comparable drain voltage of M_{CASC} result in small V_{DS} of M_{CAS} of the left reference branch (see *Fig. 2 b*). Due to small V_{DS}, M_{CASC} can drop into ohmic regime, and thus decrease gain of the feedback loop of the regulated cascode.

A. Regulated Cascode with Improved Swing

An improvement of the voltage swing of regulated cascode is presented in [5]. It replaces the gain stage M_B - I_{AUX} in *Fig. 2 b*) by a self-biased inverter-based push-pool amplifier. Besides uncontrolled bias current, this solution allows to improve the voltage swing by decreasing V_{DS} of the reference transistor. Unfortunately, V_{DS} setting in [5] relies on matching of PMOS and NMOS transistors. Matching of PMOS and NMOS is process, supply voltage, and temperature sensitive, and results in inaccurate setting of M_{REF} V_{DS} voltage.

Similarly as previously discussed for passive high swing-cascode counterpart, the approach used in this paper is to accurately regulate the drain voltage of M_{REF} to V_{DSAT}. This is achieved by adding supplementary accurate voltage generator V_{OS} between the gate of M_B and drain of M_{REF}, as shown in *Fig. 3*. This technique allows to accurately control V_{DSAT} of M_{REF}, but also maintains M_{CAS} in saturation with large saturation margin.

Example of DC characteristic of *Fig. 3* modified cascode is shown in *Fig. 4* for various V_{OS}. Here, $V_{DS\_REF} > V_{DSAT}$ reaches decent r_{out} but limited output voltage swing, whereas $V_{DS} < V_{DSAT}$ results in poor output resistance due to M_{REF} operating in the ohmic region. It can be observed that $V_{DS} = V_{DSAT}$ is the best tradeoff to maximize r_{out} and voltage swing.

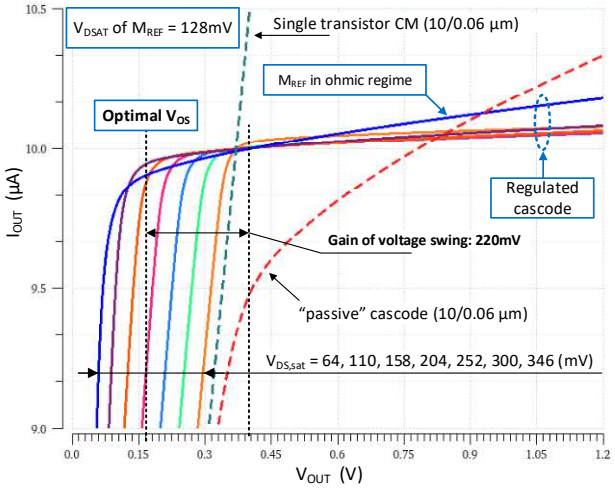

Fig. 4. Comparison of regulated cascode for various V_{OS}, comparison with single-transistor current mirror *Fig. 1* and "passive" cascode from *Fig. 2 a*).

B. V_{OS} Voltage Generator

In order to satisfy the condition $V_{DS\_REF} = V_{DSAT}$ over all PVT (process-voltage-temperature) variations, voltage generator V_{OS}, depending on the same physical parameters as V_{DSAT}, needs to be implemented.

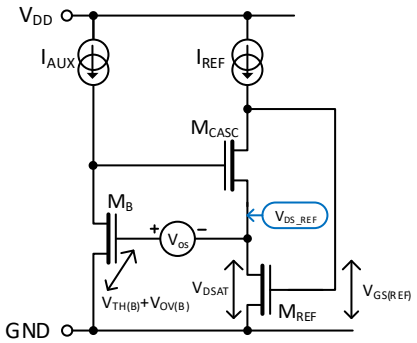

Fig. 5. Reference part of regulated cascode from *Fig. 2 b*) allowing to determine optimal value of the offset voltage V_{OS}.

Circuit shown in *Fig. 5* allows to determine the value of V_{OS} required to establish $V_{DS\_REF} = V_{DSAT}$. V_{GS} voltage of M_B can be written as a sum of the threshold voltage and overdrive voltage $V_{OV} = I_{AUX}/g_m$:

$$V_{GS(B)} = V_{TH(B)} + \frac{I_{AUX}}{g_{m(B)}} \tag{6}$$

And this gate voltage is equal to:

$$V_{GS(B)} = V_{DSAT(REF)} + V_{OS} \tag{7}$$

While $V_{DSAT(REF)}$ is equal to $I_{REF}/g_{m(ref)}$, V_{OS} can be written as:

$$V_{OS} = V_{TH(B)} + \frac{I_{AUX}}{g_{m(B)}} - \frac{I_{REF}}{g_{m(REF)}} \tag{8}$$

If geometry and bias currents are chosen in a way that transistors M_B and M_{REF} have identical V_{TH} and V_{OV}, last terms in (7) cancels and V_{OS} can be written as:

$$V_{OS} = V_{TH(B)} \tag{9}$$

This renders the desired value of V_{OS} allowing to set V_{DS_REF} to V_{DSAT} across PVT corners. Channel width W_B of transistor M_B can be found from general 1st order equation for transconductance g_m:

$$g_m = \sqrt{K_P I_D \frac{W}{L}} \tag{10}$$

where K_P is $\mu_{n,p}C_{OX}$. Considering identical channel length L_B and L_{REF}, V_{DS_REF} and V_{DS_OUT} can be set to V_{DSAT} by setting $V_{OS} = V_{TH(B)}$ (9) and channel width ratio:

$$\frac{W_{REF}}{W_B} = \frac{I_{REF}}{I_{AUX}} \tag{11}$$

Identical L_B and L_{REF} result from the requirement on identical V_T of transistors M_{REF} and M_B. This matching should be maintained regardless PVT condition. It means that short-channel device M_{REF} resulting from the high-speed requirement implies short channel device M_B. One can remark that using short channel M_B decreases the gain of the regulating loop due to reduced $r_{DS(MB)}$ (2). However, even relatively small gain of this loop provides an interesting improvement compared to cascode shown in *Fig. 2 a*).

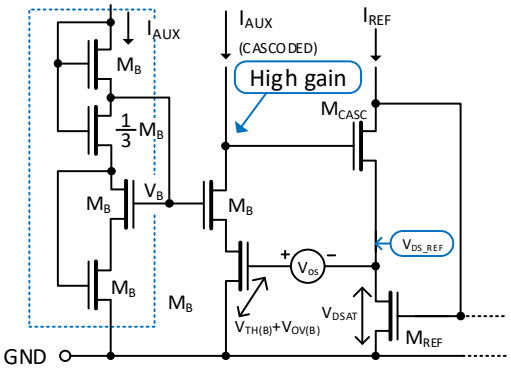

Fig. 6. Improving of the feedback-loop gain by cascading M_B transistor.

If gain enhancement obtained with short-channel M_B is insufficient, passive high swing cascode can be added to increase r_{DS} of M_B. This is conceptually shown in *Fig. 6* with example of Sooch cascode [3]. This additional cascode has very limited impact to overall speed but allows to increase gain of the regulated cascode loop by more than 20dB.

III. Implementation of Improved Regulated Cascode

$V_{OS} = V_{TH(B)}$ can be generated by an additional diode-mounted transistor M'_B driving very small current I_{OS}. Very small current in auxiliary transistor M'_B minimizes its overdrive voltage V_{OV} (4) in a way that $V_{DS} \approx V_{TH(B)}$ required by (9). Additionally, small I_{OS} reduces errors from I_{OS}, such as low r_{out}, limited output swing or temperature drift.

A. Regulated Cascode with Diode-mounted Transistors

A simple method to implement $V_{OS} = V_{TH(B)}$ is shown in *Fig. 7*. Here, diode mounted transistors M'_B are connected as V_{OS} voltage generators and are bypassed by C_{OS}. Voltage V_{OS} is generated by a very small offset current I_{OS} according to (4). Decoupling capacitors C_{OS} reduce impedance of V_{OS} voltage generator, allowing to maintain constant voltage even during transient events.

It is to be noted, that current I_{OS} biasing transistor M'_B is added to I_{REF} on the reference side, and simultaneously subtracted from I_{OUT} on the output of the cascode. In the case of unitary current-mirror ratio 1:1, this offset is cancelled, as it is present on both sides. If the cancellation cannot be achieved *e.g.* by appropriate scaling of right M'_B and I_{OS}, current offset can be compensated by bottom I'_{OS} current sink shown in *Fig. 7*. As V_{DS} of M_{REF} is voluntarily kept low, I'_{OS} current is subtracted from I_{REF} at the drain of transistor M_{CASC}. This slightly increases drain voltage of I'_{OS} that facilitates its implementation. Alternatively, right side I'_{OS} can be omitted if value of I_{OS} is negligible compared to I_{OUT}.

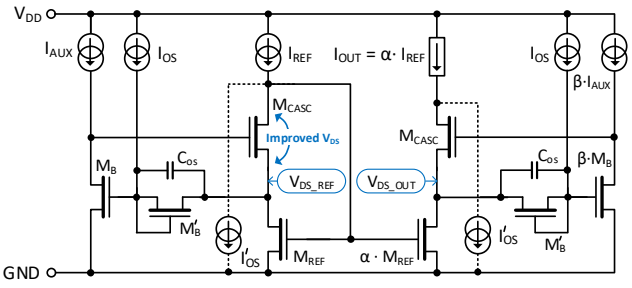

Fig. 7. Implementation of regulated cascode with improved swing. Diode-connected transistors act as V_{OS} voltage sources producing ~$V_{TH(B)}$ voltages.

B. *Current Conveyor with Resistive V_{OS} generators*

Using floating transistors M'_B, allowing to improve the output swing, is sufficient in majority of cases. However, to eliminate the bulk effect of M'_B, transistors M_B shall be implemented in isolated wells. This increases parasitic coupling to GND and slows the current-mirror transient response. If the speed limitation becomes dominant, transistors can be replaced by matched resistors biased by a CCII± current conveyor. This structure is shown in *Fig. 8*.

CCII± current conveyor reproduces input V_{OS} voltage from terminal Y to the voltage output terminal X. The current through reference resistor R_{OS} at terminal X is reproduced either in positive or negative polarity to the current outputs $Z_{\pm}$ [6]. These currents create matched voltage drops V_{OS} on R_{OS} in the structure of regulated cascode. Similarly to previous implementation, negative current sink I'_{OS} needs to be implemented only if the compensation of I_{OS} current in the structure is needed.

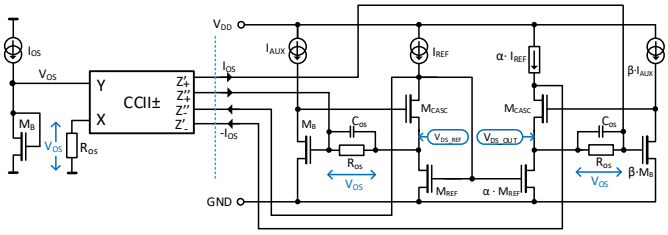

Fig. 8. Implementation of V_{OS} generator by CCII± and matched resistors.

IV. Simulation Results

Main purpose of the simulation is to verify that V_{DS} of M_{REF} is close to V_{DSAT} for expected PVT operating scenarios, and that output DC characteristic has maximal voltage swing and output resistance. This verification was done by DC simulations on regulated cascode with L = 60nm short-channel transistors and 10µA reference current. Simulation outcomes are shown for three PVT scenarios in *Fig. 9 a,b,c*) detailing output *I*/*V* characteristic. *Fig. 9 a*) corresponds to the typical operating condition at room temperature, *Fig. 9 b)* represents high temperature scenario where the transistor model parameters were adjusted to represent slow operating conditions, and *Fig. 9 c*) represents low temperature operations with fast adjustment of transistor models. In all cases, current mirror reaching optimal output swing vs. output resistance r_{out} can be observed.

Conclusion

This paper presents improvement of regulated cascode structure to maximize the output voltage swing across a wide range of operating conditions. The presented circuit allows to use fast GO1 short-channel devices and therefore to optimize the transient response speed of the current mirror. Optimization is achieved by introducing accurate offset to the feedback loop of regulated cascode. This permits to translate regulated V_{DS} voltage of the reference transistor to the optimal value V_{DSAT}. Demonstrated good stability of V_{DSAT}, across PVT corners enable employment of the structure in high-performances circuits, such as the nanosecond laser current source for optical communications.

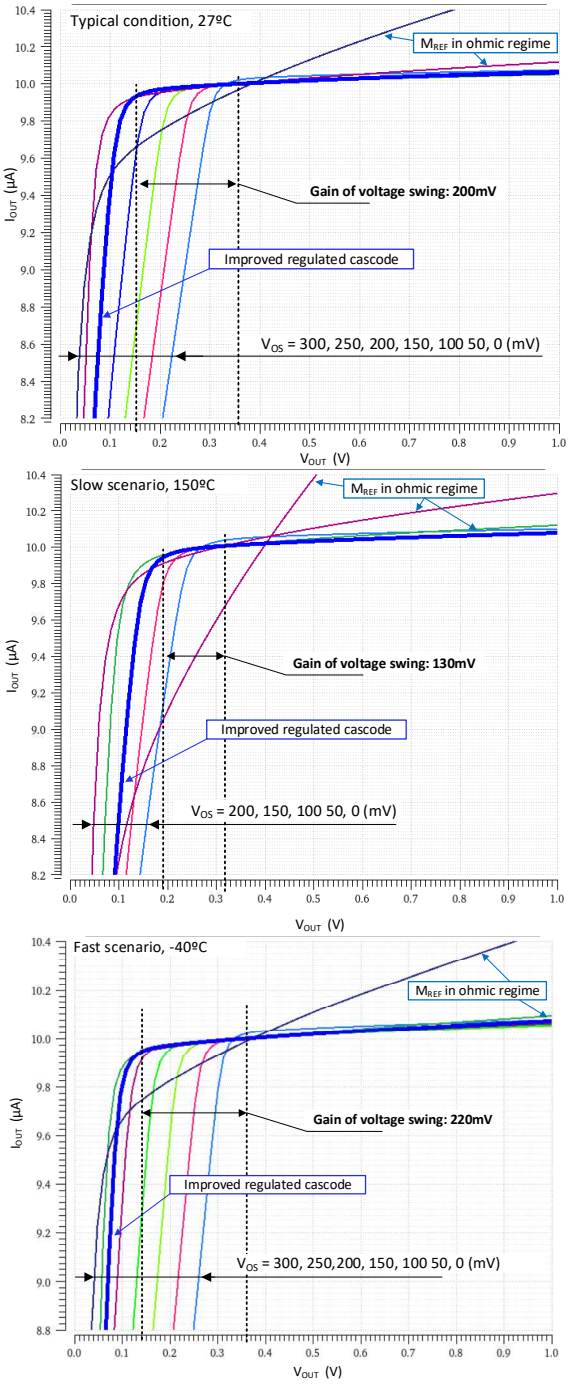

Fig. 9. Comparison of the output characteristic for modified regulated cascode with I_{REF} = 10µA, I_{OS} = 50nA, I_{AUX} = 2µA and $L_{B,REF}$ = 60nm.

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