Precise Model of the Effective Threshold Voltage Changes in the DLS MOSFETs for Different Gate Angles Compared with Measured Data

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Abstract—**This paper presents an interesting phenomenon related to the effective threshold voltage changes ($\delta V_{th,eff}$) in the diamond layout shape MOS transistors (DLS MOSFETs). Besides it, its analytical expression is presented here for the first time. The analytical approximative expression has been defined based on the results of the 3-D TCAD simulations for the different effective aspect ratio ($(W/L)_{eff}$) and different angle α of DLS MOSFET. The effective aspect ratio has been set to 2.0, 1.5, 1.0, 0.5 with the angle α varied from 180° to 80° with the step 20°. Furthermore, for purpose to verify the 3-D TCAD simulation results and measurement results, 1 124 samples were fabricated, which were proportionally divided into rectangle layout shape (RLS) MOSFETs and DLS MOSFETs with the angles α equal to 120°, 100°, and 80°. All the samples have been fabricated in the 160 nm BCD technology process. The mentioned phenomenon described by the proposed expression fits the measured data with a very high level of accuracy equal to 99.995 %. Thus, the presented analytical expression proves its quality. Thanks to the high level of the expression quality, the given expression is recommended to use for the analog designs with high-level precision requests and DLS MOSFET components.**

***Keywords*—BCD Technology, Diamond Layout Shape MOS Transistor, Effective Threshold Voltage, Rectangular Layout Shape MOS Transistor**

I. Introduction

THRESHOLD voltage (V_{th}) of the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [1], is a crucial electrical parameter, which defines the MOSFET turn on voltage and influence the transfer between the linear and saturation region [2]. Therefore, the threshold voltage plays a key role in the semiconductor industry, and any unpredictable behavior or its high sensitivity causes problems during front-end analog design [3]. Such as, in the case of the high-precise voltage references [5]. These unpredictable behaviors and V_{th} high sensitivities are present, for example, in the caseof a hump effect [6], TID effect [7], etc., but also in the case of the DLS MOSFET (Fig. 1), which is the subject of this article. The unpredictable behavior of DLS MOSFET has not been described yet, and therefore this article focuses on it.

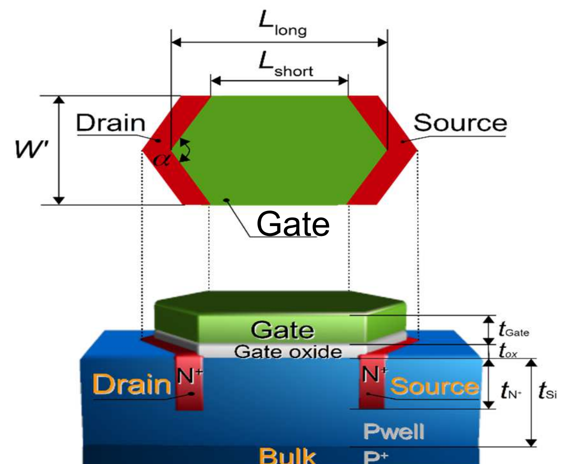

Fig. 1. A 2-D and 3-D top-view of the general N channel MOSFET structure with the Diamond Layout Shape [4]

Generally, the V_{th} is the value of the MOSFET gate-source voltage V_{GS} that will cause the interface potential to be equal in magnitude and opposite in sign to the substrate potential Φ_p [8]. Physically, for the N-channel MOSFET, it means that there would now be a concentration of mobile electrons at the surface equal in magnitude to a concentration of mobile holes in the P-substrate.

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In common, the threshold voltage equals to the sum of the flatband voltage V_{FB}, twice the bulk potential Φ_p and the voltage across the oxide [9], such it is described in [10] by the following expression:

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + \gamma\sqrt{2(-\phi_{\mathrm{p}})} - 2\phi_{\mathrm{p}} \tag{1}$$

where the V_{FB} is the flatband voltage, the Φ_p is a workfunction of a substrate, and the γ is a body effect. After a routine operation, we will get the following expression with basic technology parameters:

$$V_{\mathrm{th}} = \frac{T\log\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right)k_{\mathrm{B}}}{q} - \frac{T\log\left(\frac{N_{\mathrm{D}}}{n_{\mathrm{i}}}\right)k_{\mathrm{B}}}{q} + \frac{2\sqrt{\frac{T\log\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right)k_{\mathrm{B}}}{q}}\,t_{\mathrm{ox}}\sqrt{qN_{\mathrm{A}}\varepsilon_{\mathrm{Si}}}}{\varepsilon_{\mathrm{ox}}} \tag{2}$$

where the T is the temperature, k_B is the Boltzmann constant ($k_B = 1.38\cdot10^{23}$ J K^{-1}), and q is the magnitude of the electron charge ($q = 1.602\cdot10^{-19}$ C). N_A is the net ionized acceptor density, N_D is the donor impurity density in silicon, and n_i is the intrinsic doping concentration of silicon (n_i = $1.45\cdot10^{10}$ cm^{-3} at T = 300 K). ε_{Si} is the permittivity of silicon, and ε_{ox} is the permittivity of oxide.

As we can see, the final expression (2) does not consider the geometry settings of the MOSFETs. In the case of DLS MOSFETs, it could be a problem in terms of circuits accuracy. For this reason, we present an innovative expression of the changes in the effective threshold voltage based on simulation data, which are compared with measured data with excellent results.

In this work, the sub-threshold drain current method [11] has been used to extract the effective threshold voltage. This method is a function of gate-source voltage below the threshold voltage and plotted as log(I_{DS}) versus V_{GS} [12]. All measurements have been adjusted for the four-points measurement approach [13]. The measurements have been performed in the linear region with drain voltage set to 0.05 V and with the gate voltage step size of 10 mV.

II. Experimental Results and Discussion

A. Simulated Structures

In this research, the gate areas of MOSFETs have been set to A = 10 µm^2 with effective aspect ratios $(W/L)_{eff}$ varied from 0.5 to 2.0 with a step equal to 0.5. The DLS MOSFET's effective aspect ratio is described in [14] by the following expression:

$$\left(\frac{W}{L}\right)_{\mathrm{eff}} = \frac{2}{\frac{2L_{\mathrm{short}}}{W'} - 7.10^{-5}\left(90-\frac{\alpha}{2}\right)^2 + 1.57.10^{-2}\left(90-\frac{\alpha}{2}\right) - 2.10^{-3}} \tag{3}$$

where an angle α is in degrees and is accurate to within 1 percent provided $2L_{short}/W' > 1.4$. A L_{short} is a shorter parallel side of the trapezoid, and a W' is a geometrical width of the trapezoid.

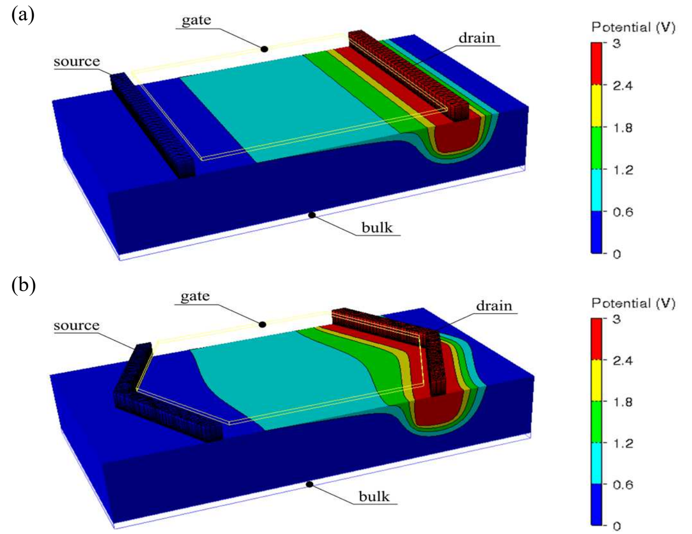

Fig. 2: Potential examples of the RLS, and DLS MOS transistor structures: (a) RLS MOSFET (b) DLS MOSFET [18]

The technological parameters of the DLS MOSFET (Fig. 1) have been set as follows, a gate polysilicon thickness t_{gate} is equal to 0.2 µm, a gate oxide thickness t_{ox} is equal to 8.5 nm, drain/source thicknesses t_{N+} is equal to 0.4 µm, and a silicon thickness t_{Si} has been set to 1.0 µm. A Pwell and N$^+$ drain/source doping concentrations have been set to $1\cdot10^{16}$ cm^{-3} and $1\cdot10^{20}$ cm^{-3}, respectively.

The Atlas, 3-D TCAD device simulation tool [15] from Silvaco company, has been used to realize and simulate the DLS MOSFETs considering the same effective aspect ratio $(W/L)_{eff}$ with the same gate area A for any angle α. The 3-D numerical simulations were run with a lateral electric field-dependent model, a concentration-dependent mobility model, Selberherr impact ionization model, and Shockley-Read-Hall model for generation-recombination processes [16]. In the TCAD simulations, the mesh grid has a direct effect on the accuracy and time of simulations. To find the proper grid is essential, and it has been considered for our simulations. In section III, the correct setting of the grid has also been proved by measurements.

Tab. 1: The simulated effective threshold voltage changes ($\delta V_{th,eff,TCAD}$) of DLS MOSFETs for different effective aspect ratios $(W/L)_{eff}$

α (°)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff}$ = 2.0 (%)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff}$ = 1.5 (%)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff}$ = 1.0 (%)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff}$ = 0.5 (%)
180	0.00	0.00	0.00	0.00
160	-0.11	-0.07	0.01	-0.03
140	-0.30	-0.17	-0.04	-0.07
120	-0.63	-0.33	-0.13	-0.10
100	-1.16	-0.59	-0.23	-0.15
80	-1.92	-0.92	-0.39	-0.19

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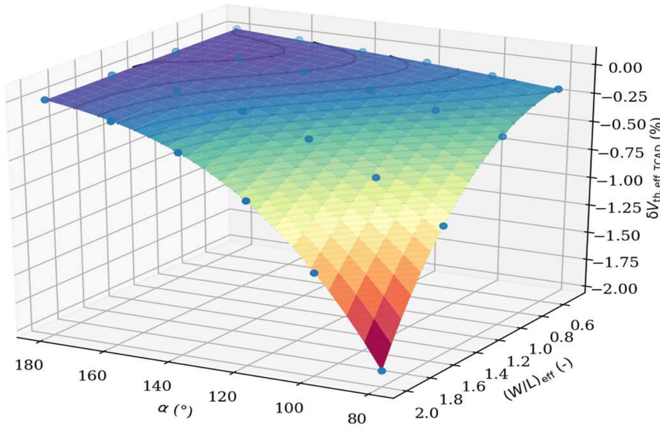

Fig. 3: Comparison of the effective threshold voltage decreasing for DLS MOSFETs with the different effective aspect ratio $(W/L)_{eff}$

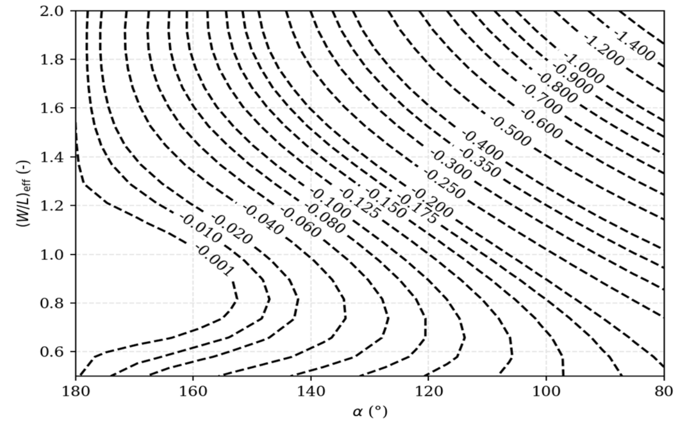

Fig. 4: Contour plot of effective threshold voltage variation $(\delta V_{th,eff,approx})$ as a function of angle α and effective aspect ratio $(W/L)_{eff}$

The examples of the simulated structures are depicted in Fig. 2., and all their inputs and outputs data are shown in Tab. 1 and illustrated in Fig. 3.

The Tab. 1 presents simulated changes in the effective threshold voltage $(\delta V_{th,eff,TCAD})$ calculated by the following expression:

$$\delta V_{th,eff,TCAD} = \left(\frac{V_{th,eff,TCAD,DLS} - V_{th,TCAD,RLS}}{V_{th,TCAD,RLS}} \cdot 100\right) \qquad (4)$$

where $V_{th,TCAD,RLS}$ is a threshold voltage of conventional rectangular layout shape MOSFET, and the $V_{th,eff,TCAD,DLS}$ is an effective threshold voltage of DLS MOSFETs.

The Fig. 3 illustrates the comparison of the changes in the effective threshold voltage for RLS and DLS MOSFET devices. It has been studied at different effective aspect ratios $(W/L)_{eff}$ equal to 2.0, 1.5, 1.0, and 0.5. As we can see, the simulated effective threshold voltage $(V_{th,eff,TCAD})$ decreases if the angle α of the DLS MOSFETs decreases, too. And moreover, if the effective aspect ratio $(W/L)_{eff}$ increases, the $V_{th,eff,TCAD}$ decreases more significantly. It is an interesting point that can be useful for the effective threshold voltage trimming of MOSFET devices in integrated circuits (ICs).

$$\begin{aligned}\delta V_{th,eff,approx} = & -1.349 + \alpha\, 7.57\cdot 10^{-2} + \left(\frac{W}{L}\right)_{eff} 5.244 \\ & - \alpha \left(\frac{W}{L}\right)_{eff} 0.387 - \alpha^2 1.62\cdot 10^{-3} + \alpha^2 \left(\frac{W}{L}\right)_{eff} 9.2\cdot 10^{-3} \\ & - \alpha^2 \left(\frac{W}{L}\right)^2_{eff} 1.39\cdot 10^{-2} - \left(\frac{W}{L}\right)^2_{eff} 7.09 + \alpha \left(\frac{W}{L}\right)^2_{eff} 0.554 \\ & + \left(\alpha^3 1.052 - \alpha^3 \left(\frac{W}{L}\right)_{eff} 6.152 + \alpha^3 \left(\frac{W}{L}\right)^2_{eff} 9.573\right)\cdot 10^{-5} \\ & - \alpha^3 \left(\frac{W}{L}\right)^3_{eff} 3.614\cdot 10^{-5} - \left(\frac{W}{L}\right)^3_{eff} 5.232 \\ & + \alpha \left(\frac{W}{L}\right)^3_{eff} 6.702\cdot 10^{-3} + \alpha^2 \left(\frac{W}{L}\right)^3_{eff} 3.832\cdot 10^{-3} \end{aligned} \qquad (5)$$

In the case of trimming effective threshold voltage, there is important to know how much the $V_{th,eff}$ will be changed. Therefore, in this article, we have simulated $V_{th,eff}$ variation $\delta V_{th,eff,TCAD}$ (Fig. 3), which has been approximated by the third order polynomial fitting function (5). It describes the decreases of the effective threshold voltage as a function of angle α and effective aspect ratio $(W/L)_{eff.}$ This trend is valid independently on MOSFET physical characteristics such as a gate material, a gate oxide thickness, and so on, because it defines just a variation of the effective threshold voltage of DLS relative to RLS. In case of needs, an absolute value of the DLS MOSFET effective V_{th} can be derived from (4), where $V_{th,TCAD,RLS}$ is close to V_{th} $(V_{th,TCAD,RLS} \doteq V_{th})$ defined by the analytical expression (2). It could be also important in analog design with DLS MOSFETs [17]. The final expression fits the simulated data with excellent results, where RMSE parameter is equal to 0.00307,and R-squared parameter is equal to 0.99995. The innovative expression (5) is illustrated in Fig. 3 as a 3-D surface plot and its contour plot is illustrated in Fig. 4.

B. Measured Structures

The measured test structures for this study are N-channel DLS MOSFET devices with 1.8V operating voltages fabricated in a 160 nm BCD technology process [18] with a triple well isolation [19]. A 2-D top-view and 3-D front-view of the general N-channel DLS MOSFET is depicted in Fig. 1, and an example of the measured sample is depicted in Fig. 5.

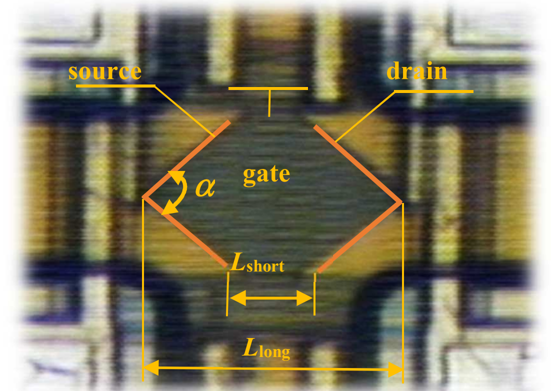

Fig. 5. Photography of the DLS NMOS transistor with the angle α = 100° [5]

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For this study, 1 124 samples were fabricated, which were proportionally divided into four different structures

. The first structures are reference conventional rectangular layout shape (RLS) MOS transistors (α = 180°) and the other structures are DLS MOS transistors with the angles α equal to 120°, 100°, and 80°. All the fabricated devices have a similar area equal to 500 μm^2, and effective aspect ratio $(W/L)_{eff}$ equal to 2.004 (α = 180°; RLS MOSFET), 1.892 (α = 120°), 1.834 (α

Tab. 2: The measured effective threshold voltage changes ($\delta V_{th,eff,meas}$) of DLS MOSFETs for different effective aspect ratios (W/L)

α (°)	W' (μm)	L_{short} (μm)	L_{long} (μm)	A (μm^2)	$\delta V_{th,eff,meas}$ @ $(W/L)_{eff}$ = 2.0 (%)
180	31.62	15.81	15.81	500	0.00
120	28.24	9.28	25.24	487	-0.63
100	26.34	7.68	29.28	487	-1.16
80	23.94	6.42	34.22	486	-1.94

= 100°), and 1.758 (α = 80°).
The

presents measured threshold voltage changes ($\delta V_{th,eff,meas}$) calculated by the following expression:

$$\delta V_{th,eff,meas} = \left(\frac{V_{th,eff,meas,DLS} - V_{th,meas,RLS}}{V_{th,meas,RLS}}\right) \cdot 100 \quad (6)$$

where $V_{th,meas,RLS}$ is a measured threshold voltage of conventional RLS MOSFET, and $V_{th,eff,meas,DLS}$ is a measured effective threshold voltage of DLS MOSFETs. Both $V_{th,meas,RLS}$, and $V_{th,eff,meas,DLS}$ have been measured by sub-threshold drain current extraction method [11]. This method is a common practice reference method for a long time, and it has been sequentially applied on RLS MOSFETs (α = 180°), and DLS MOSFETs with angle α equal to 120°, 100°, and 80°.

All the measured data of the experimental devices and their details are depicted in plots, Fig. 6 and Fig. 7, respectively. The Fig. 6 and Fig. 7 illustrate the measured data (solid lines), the sub-threshold drain current extraction data (dashed lines), and the constant drain-source current level $I_{DS,RLS}$ (dot line). The extracted threshold voltage of the RLS MOSFET ($V_{th,RLS}$) defines $I_{DS,RLS}$. Both, the extracted values are in accordance with the technological process data, and thus they confirm the correctness of the method used. To maintain the same $I_{DS,RLS}$ level also for DLS MOSFETs, the lower gate-source voltage level, i.e. $V_{th,eff,DLS,}$ is required. If the angle α of DLS MOSFETs decreases, the effective threshold voltage decreases, too. This means that in order to achieve the same drain-source current level for both RLS and DLS MOSFETs, the required effective threshold voltage is lower for DLS MOSFETs than for RLS MOSFETs.

The examples of measured data and post-processed results are independently depicted in Fig. 8 – Fig. 11. There are shown transfer characteristics and detail of the transfer

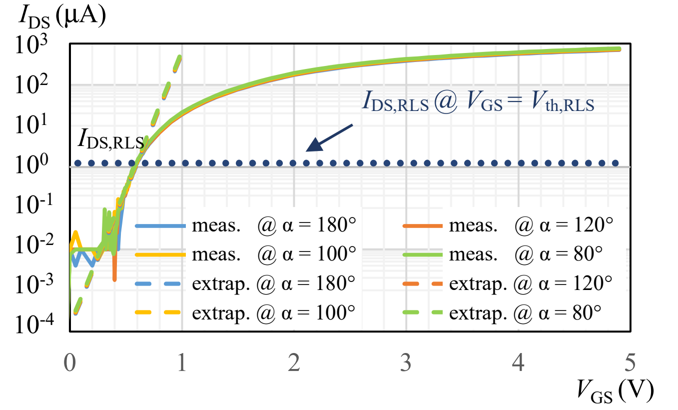

Fig. 6: Transfer characteristics of DLS MOSFETs with angle α = 180° (blue), 120° (brown), 100° (orange), and 80° (green)

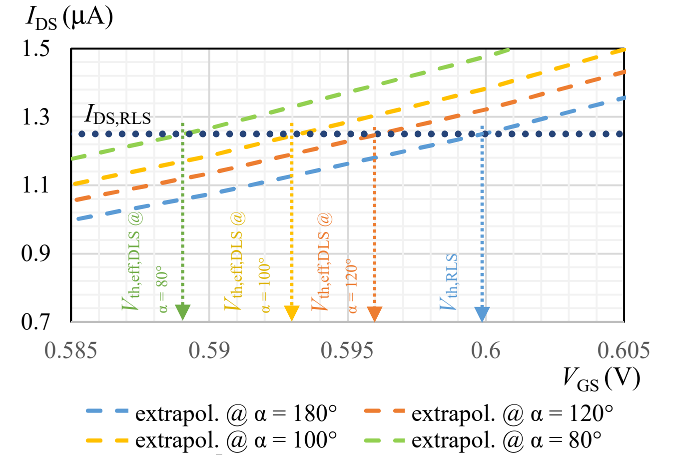

Fig. 7: Transfer characteristics of DLS MOSFETs with angle α = 180° (blue), 120° (brown), 100° (orange), and 100° (green) – in details

characteristics for the RLS MOSFET and DLS MOSFET with angle α equal to 80°.

III. Experimental Results Comparison & Discussion

The following Tab. 3 summarizes $\delta V_{th,eff,TCAD}$, $\delta V_{th,eff,approx}$, and $\delta V_{th,eff,meas}$ data with the excellent conformity depicted in Fig. 12. All the results fit very well together, and therefore, in the case of the IC analog design with DLS MOSFETs, it is recommended to use the innovative expression (5). Only in this way we can ensure the high accuracy level of the calculated drain-source current.

Tab. 3: Summary of the effective threshold voltage changes

α (°)	$\delta V_{th,eff,TCAD}$ @ $(W/L)_{eff}$ = 2.0 (%)	$\delta V_{th,eff,approx}$ @ $(W/L)_{eff}$ = 2.0 (%)	$\delta V_{th,eff,meas}$ @ $(W/L)_{eff}$ = 2.0 (%)
180	0.000	0.000	0.000
160	-0.11	-0.11	-
140	-0.30	-0.30	-
120	-0.62	-0.63	-0.63
100	-1.16	-1.16	-1.16
80	-1.91	-1.95	-1.94

The threshold voltage variation, which has been confirmed by the measurement, is relatively small. But due to a quadratic dependence of the drain-source current on V_{th} in the above-

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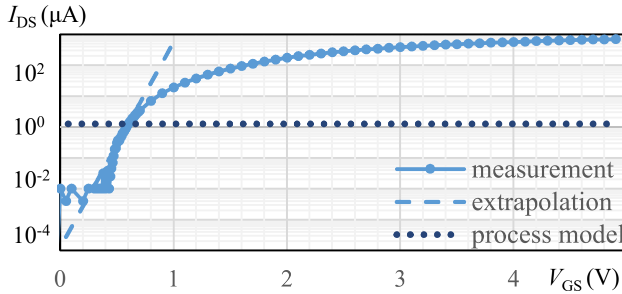

Fig. 8: Transfer characteristic of DLS MOSFET with angle α = 180°

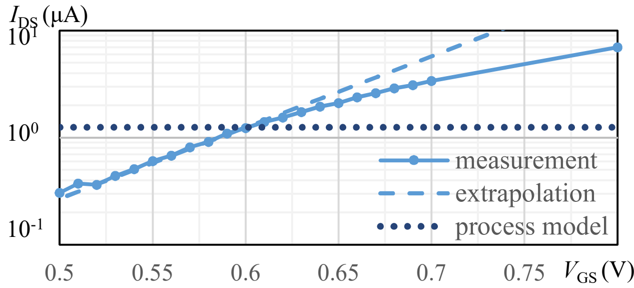

Fig. 9: Transfer characteristic of DLS MOSFET with angle α = 180° (detail)

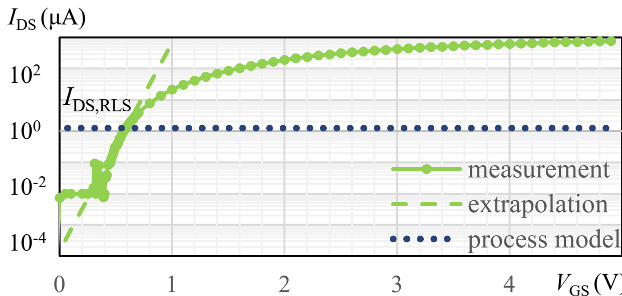

Fig. 10: Transfer characteristic of DLS MOSFET with angle α = 80°

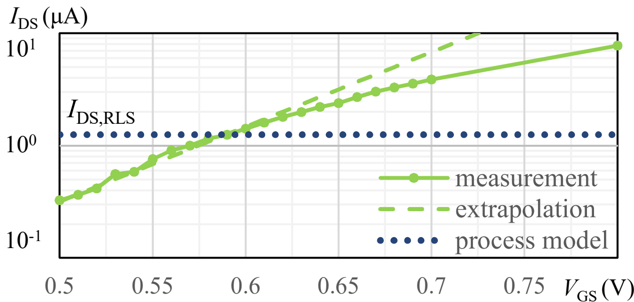

Fig. 11: Transfer characteristic of DLS MOSFET with angle α = 80° (detail)

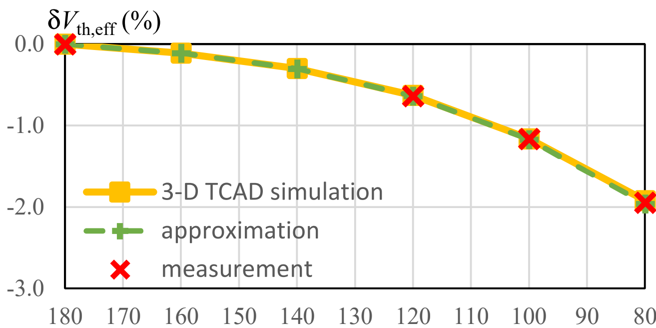

Fig. 12: A Comparison of changes threshold voltage given by TCAD simulation, analytical approximation, and measurement

threshold region and exponential dependence of the drain-source current on V_{th} in the sub-threshold region, each V_{th} modification should be considered. Moreover, in the case where the V_{GS} is close to V_{th}, the consequence of the V_{th} variation is even more significant. This is the case, when the circuits operate in an ultra-low voltage domain, such as operating voltage below 1.0 V, and low temperatures [20]. In the case when the angle α is set to 80° and respecting [20], the V_{th} variation may be up to 18 mV, which is a relatively a lot. The presented possibility to change V_{th} can help to complete the design comfortably.

In the case of drain-source current calculation, we also should respect different hole and electron mobility ($\mu_{0,P}$, $\mu_{0,N}$) in MOSFETs affected by the different MOSFET channel orientation [21]. In [22], the drain-source current can be varied up to 42 % dependently on the channel and silicon orientation. In the case of this article, there has been used CMOS standard (100) silicon wafers [23] and N-channel DLS MOSFETs have a top and bottom edge of the channel aligned with <110> direction. Crystalline orientations in channel area varied dependently on the geometry settings of DLS MOSFET due to curved current trajectory. For the drain-source current calculation of N-channel DLS MOSFET devices, the following fitting function (7) should be used. In this way, we can respect different channel orientations and electron mobility.

$$\mu_{0,N,eff} = (-9.8235\cdot 10^{-4}\,\alpha^2 + 1.9913\cdot 10^{-1}\,\alpha - 3.0154)\,\mu_{0,N} \quad (7)$$

where $\mu_{0,N,eff}$ is effective electron mobility as a function of angle α of DLS MOSFET devices and electron mobility for N-channel RLS MOSFET devices $\mu_{0,N}$.

The presented effective threshold voltage phenomenon could be explained such as consequence of the multi-threshold transistor consists of infinitive numbers of curved narrows MOSFETs with different channel lengths [24].

To have the above-mentioned DLS MOSFETs' advantages, it is essential to respect conditions in which the DLS MOSFETs can work. The first one is to avoid using the DLS MOSFET with small geometric sizes, because it may cause a high peak field and current concentration at the local angle region of the DLS MOSFET topology. The second condition is using the DLS MOSFET in low-voltage and low-power applications which is a trend of nowadays ICs. In this way, we can reduce the total die area up to 36.9 % compared to the same circuit using the conventional MOSFETs [17]. These conditions are typically requested in real applications [25]. Moreover, in this case, another non-conventional MOSFET shape topology with sharp angles has been successfully used as well [25].

Furthermore, this approach is very useful in terms of V_{th} modification for the selectively requested components. In general, the V_{th} can be changed by process modification (2), as an example modification of the gate insulator's thickness. Nevertheless, in this case, this approach modifies the effective V_{th} of one type of component and not selectively, such as the presented approach enables it.

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IV. Conclusion

This paper presents the changes in the effective threshold voltage of the DLS MOSFET devices dependently on its shapes. For this reason, the DLS MOSFET structures have been simulated in 3-D Silvaco TCAD simulator as well as they have been verified by measurement on samples. Moreover, the described phenomenon has been for the first time numerically approximated by the expression with a very high accuracy level equal to 99.995 %.

There has been observed, if the angle α of the DLS MOSFETs decreases, the effective threshold voltage $V_{th,eff,DLS}$ decreases too. In additional, if the effective aspect ratio $(W/L)_{eff}$ of DLS MOSFETs increases, the effective threshold voltage decreases more significantly.

In both measurement and simulation cases, the effective threshold voltage for the DLS MOSFET with the effective aspect ratio $(W/L)_{eff}$ equal to 2.0, and angle α set to 80° has been decreased close to by -2 %.

This article apprises us about the interesting phenomena in IC DLS MOSFETs that can be used for both effective threshold voltage trimming as well as for the analog ICs design using DLS MOSFETs.

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