Investigation on Threshold Voltage Instability Under Sweeping and DC Gate Bias Stressing of SiC Symmetrical and Asymmetrical Double-trench MOSFETs

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Abstract

In this paper, measurements on gate threshold voltage drift by sweeping the gate voltage and both with positive and negative DC gate stressing are performed on symmetrical and asymmetrical double-trench SiC MOSFETs with comparison to SiC planar MOSFET at a range of temperatures. For the sweeping stress, the impact of sweeping speed on SiC MOSFET characteristics is also presented. In the experiments of DC gate stressing, the mobility degradation and threshold voltage drift values are obtained. Comparisons for threshold voltage drift in regard to temperature rise is made between different gate-structured SiC MOSFETs.

1 Introduction

Gate stressing has raised a major reliability issue on SiC MOSFETs. As a consequence of electron or hole capture by traps on the gate oxide under the impact of gate voltage applied, threshold voltage drift is induced. Unlike Silicon MOSFET, SiC MOSFET is more sensitive to gate stressing because there is Carbon presented at the oxide-channel interface which are potential origins for the traps as well as its wide band-gap property makes traps of more energy level involved in the trapping/de-trapping of electrons [1, 2]. Therefore, with the same oxide thickness, SiC MOSFET shows more threshold voltage shift than Silicon MOSFET [3, 4]. The threshold voltage drift closely affects the circuit operation. For example, positive threshold voltage drift causes higher on-state conduction loss and negative threshold voltage drift increases the likelihood of parasitic turn-ON. In recent publications of threshold voltage stability on SiC MOSFET [5, 6, 7], the devices studied mainly focuses on the planar MOSFET. However, with the introduction of double-trench structured SiC MOSFET to the market, it has become a competitor to the conventional planar MOSFET as its double-trench structure allows high channel-density design thus enables lower on-state loss and faster switching [8, 9]. Three cross-sectional schematics for planar structure, symmetrical and asymmetrical double-trench SiC MOSFETs are shown in Fig. 1. In this paper, the threshold voltage stability under gate sweeping at different rate and gate DC bias are investigated and compared for three devices shown in Fig. 1 at a range of temperatures.

2 Experiments

Three devices have been under test representing different structures as Planar SiC MOSFET (SCT2160), Symmetrical double-trench SiC MOSFET (SCT3160) and Asymmetrical double-trench SiC MOSFET (IMW120R140M1H). All three devices under test (DUTs) are packaged in TO-247. Both stressing and measurement are performed by using the source measure unit B2902A. Change of temperature is achieved by attaching a heating block to DUT with a temperature controller.

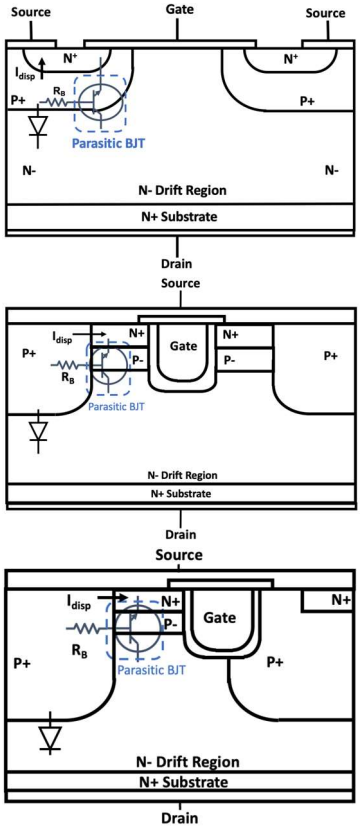

Fig. 1. Cross-sectional schematic of Planar MOSFET, Symmetrical double-trench MOSFET and Asymmetrical Double-trench MOSFET.

2.1 Sweeping Stress

The extraction of threshold voltage on MOSFET is requires a voltage sweeping on the gate [10, 11]. However, in SiC

MOSFET, the sweeping itself is able to make the interface traps out of equilibrium thus causes error to threshold readout [12, 13]. Therefore, in this section, the DUTs are placed under sweepings of different speed ranged from 500 V/s to 10 V/s to extract the threshold voltage reading. Then multiple sweepings of identical sweeping speed are consecutively applied to the MOSFET to investigate the accumulative effect of sweepings on the threshold reading. During sweeping, a small constant voltage is applied on the drain-source to measure the drain-source current to gate-source voltage (I_D-V_{GS}) trace. Temperature ranges from 25°C to 175°C.

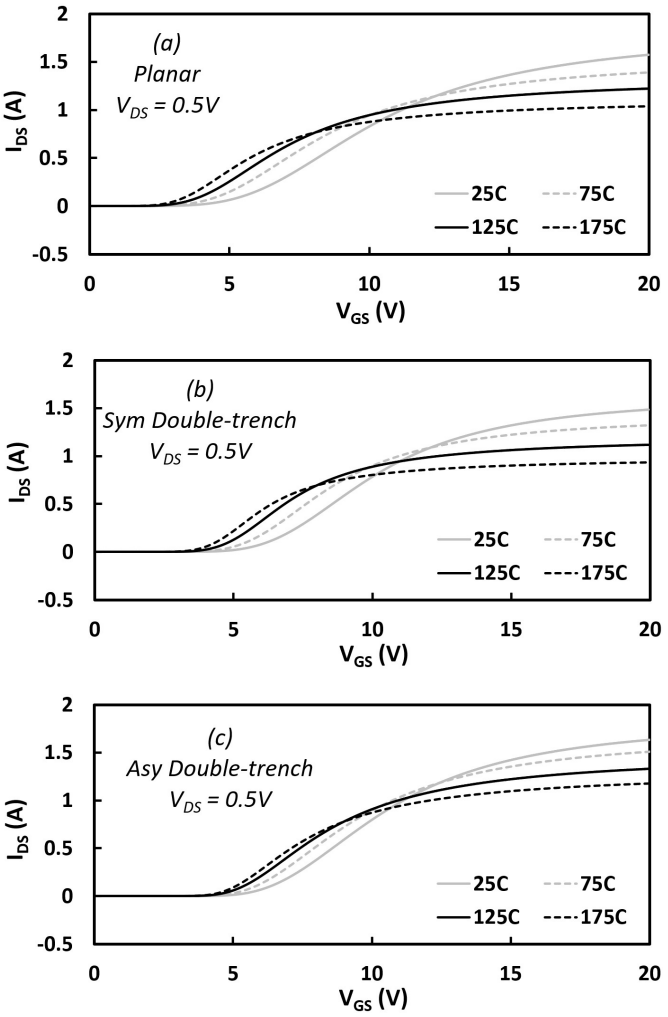

Fig. 2. The I_{DS}-V_{GS} sweeping up to 20 V under different temperature of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET and (c) Asymmetrical double-trench SiC MOSFET.

General comparison of I_D-V_{GS} sweeping up to 20 V for each DUT under different temperature is shown in Fig. 2. The turning point for the curve happens at low V_{GS} because the threshold drops at high temperature as a result of intrinsic carrier density increase. Since the device is driven in linear region, as the V_{GS} further increases, channel resistance is not dominated but the parasitic resistance which has positive temperature coefficient, hence, the I_{DS} stabilizes at lower level. Therefore, the impact of gate stress on the I_D-V_{GS} trace will only be visible when I_D is in a ramp before leveling out.

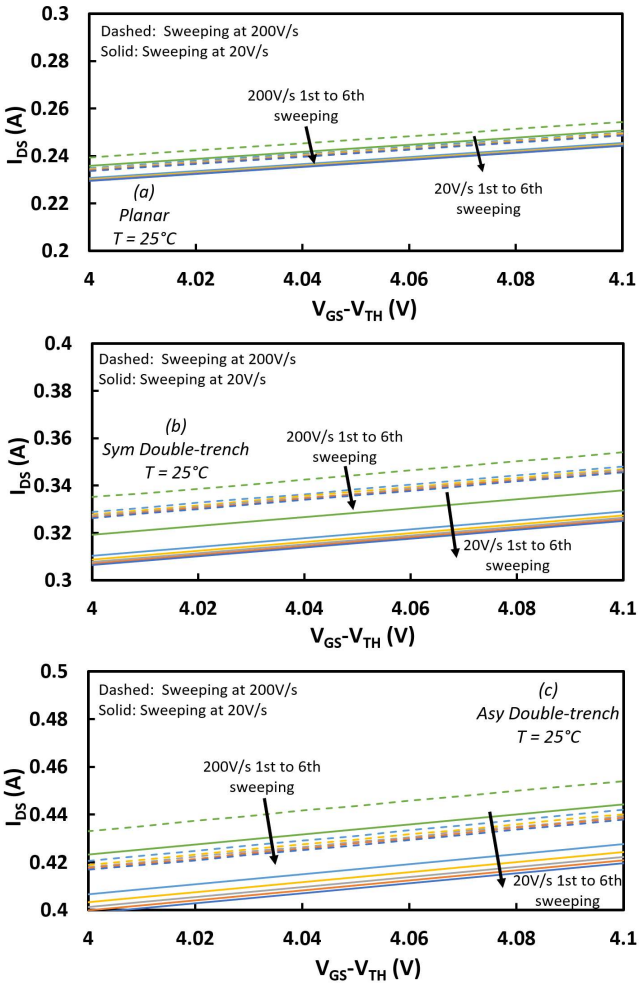

Fig. 3. Zoomed-in view of individual I_{DS}-V_{GS} sweeping curves at 20 V/s and 200 V/s under 25°C of (a) Planar MOSFET, (b) Symmetrical double-trench MOSFET & (c) Asymmetrical double-trench MOSFET.

The I_{DS}-V_{GS} sweeping trace under 25°C and 175°C for each individual sweep of two sweeping speed is shown in Fig. 3 and Fig. 5 respectively with zoomed-in view for V_{GS} above threshold V_{TH} by 4 V for a fair comparison. It can be seen that a trace at slow sweeping rate causes more downwards shift than faster rate which is expected because slow sweeping itself would exert longer time stress on the gate. Consecutive sweeping adds accumulative effect for further drift, but for both sweeping rates, the first sweeping is already enough for the shifting effect to approach saturation so that it makes the most significant shift than the following sweepings. The shift in planar SiC MOSFET is the least significant which shows the least sensitivity to sweeping speed.

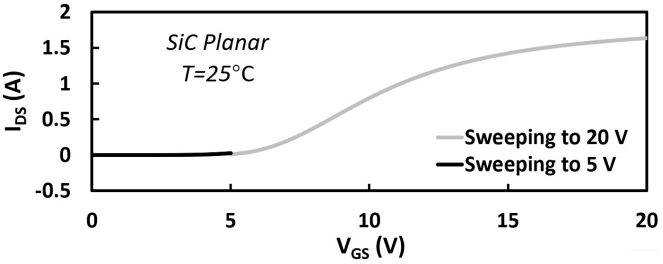

Fig. 4. Threshold voltage can normally be extracted by sweeping to 5V. Determination of threshold voltage IV sweeping to 20V leads to slight drift of readout as the sweeping voltage constitutes gate stress.

Although sweeping up to 20 V could give more information about on-state resistance and overall performance of the MOSFET at actual applied gate-source voltages, usually in range of 15 to 20 V, to accurately extract the value of threshold voltage of a SiC MOSFET, it is usually sufficient to limit the *IV* sweeping voltage to 5 V. This is because as shown in Figures 4 and 5, sweeping to 20 V specially at high sweeping rates would lead to minor drift of threshold voltage, as it constitutes as gate stress, while sweepings at only 5 V will be shown to induce less variation with repeat of sweeping. Therefore, in the following measurements on the impact of sweeping stress, only sweeping up to 5 V is implemented.

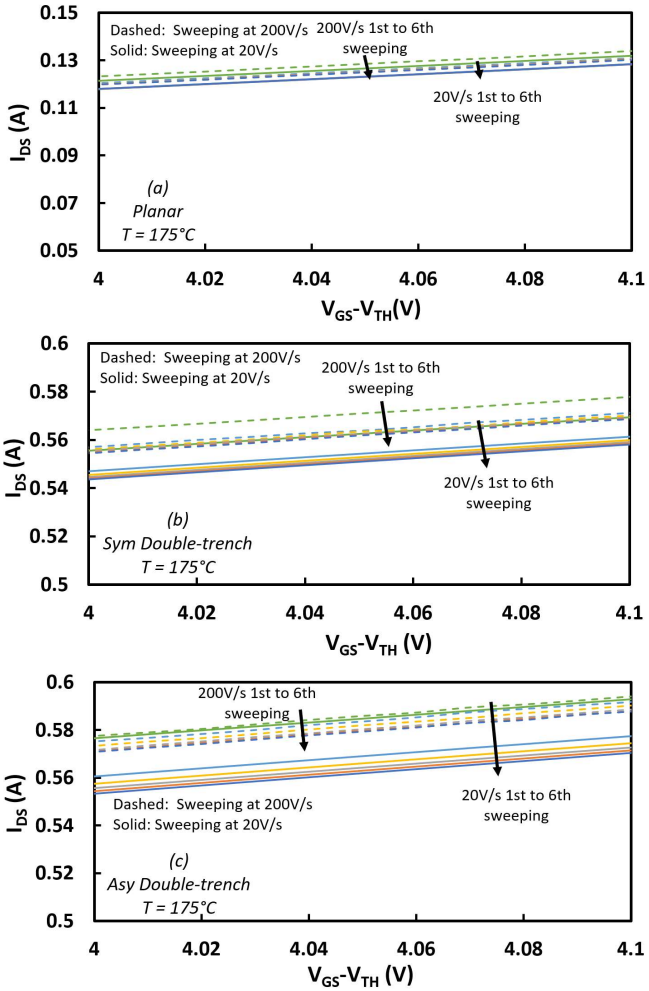

Fig. 5. Zoomed-in view of I_{DS}-V_{GS} sweeping at 20 V/s & 200 V/s at 175°C of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET & (c) Asymmetrical double-trench SiC MOSFET.

Methods for threshold voltage definition is discussed on [6]. To provide a clearer comparison, the constant current method is also selected to be provided in this paper, in which the threshold voltage defined as the gate-source voltage when drain-source current is equal to 1 mA. The variation of threshold reading with reference to the fastest sweeping speed (500 V/s) is also plotted on Fig. 6 under 25°C and 175°C. It can be noticed that a low sweeping speed would result in higher readout in threshold than higher sweeping speeds, because the slow sweeping speeds mean longer positive voltage applied equivalent to a small positive DC gate stressing, applying on gate prior to threshold readout.

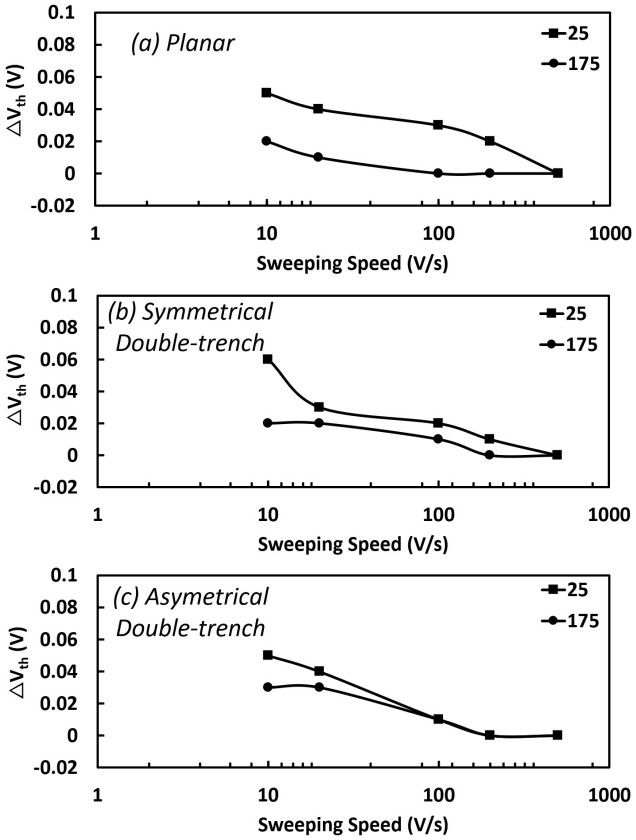

Fig. 6. Threshold voltage reading variation with reference to 500 V/s at different sweeping speed under temperature of 25°C and 175°C.

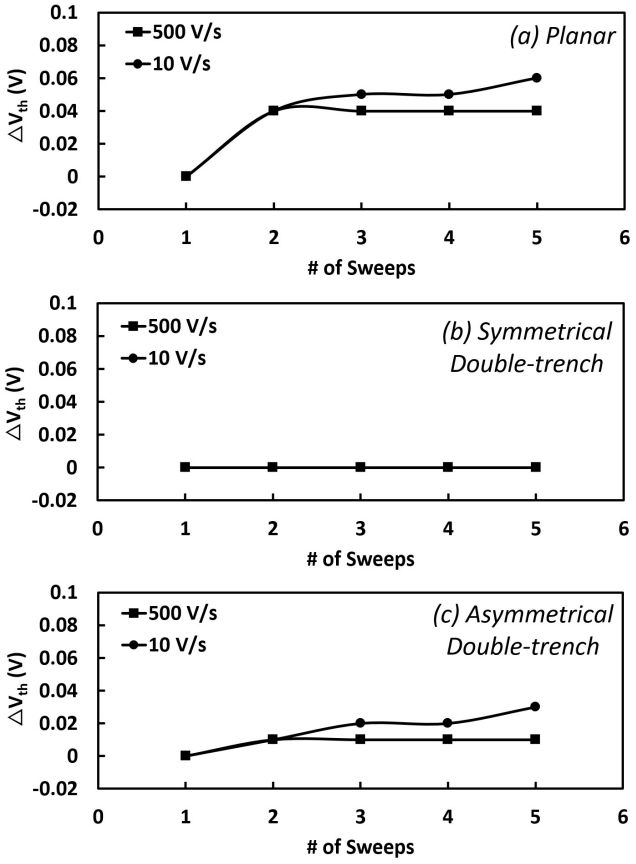

Fig. 7. Threshold voltage reading variation with reference to the first sweep at different sweeping speed under 25°C.

It must be noted that sweeping of voltage on gate to determine the threshold voltage by itself alters the precise value of threshold voltage, i.e. the readout is not the actual definite value for the threshold voltage. Repeating the sweeping at higher voltages, i.e. to 20 V, at successive measurements will also have a profound impact on the readout of the threshold voltage, and this varies for different gate structures. At the slowest sweeping case, the deviation could be nearly 60 mV. As the temperature increases to 175°C, such deviations by slowing down the sweeping speed is minimized. In theory, high temperature would cause more traps generated in the oxide layer [4] which yield more threshold voltage drift. However, the Constant Current method is the industrial approach to extract the threshold voltage that fits the I_D to V_{GS} equation of MOSFET in the linear region thus the mobility degradation with temperature rise would increase the required V_{GS} to reach the current value as in V_{TH} definition.

The results for applying consecutive five sweepings on DUT under 25°C is shown in Fig. 7. The threshold voltage reading variation is referenced to the readout from the first sweep. It can be seen that symmetrical double-trench SiC MOSFET has no further variation of threshold drift at increasing number of sweeping applied which means that one sweep at both speed is enough to push the device to saturation state. In the other two devices, accumulative effect of multiple sweeps is visible, in the slower sweeping speed case, the saturation of threshold readout is reached earlier while there is more steady increase on variation as more sweeps applied

2.2 Positive DC Bias Stress

The DC bias stress experiment is implemented on a measure-stress-measure (MSM) manner with procedure demonstrated in Fig. 8. Readout on threshold voltage is performed by interrupting the stressing and sweeping the gate-source voltage up to 5 V with 0.5 V of drain-source voltage applied. Between the DC stress and sweeping, there is a delay of 0.5 sec which is the internal limitation of equipment. Positive DC bias stress is applied to each DUTs with stressing voltage selected to be 18 V, this is within the recommended operation range for all three DUTs. Drain-source voltage is grounded while stressing.

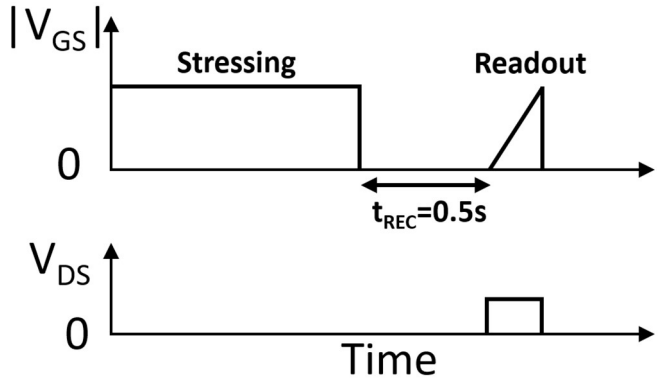

Fig. 8. DC bias stressing experiment procedure demonstration.

The $I_{DS} - V_{GS}$ trace at sweeping for threshold voltage readout not only contains the information of threshold voltage but also the mobility [14, 15]. The sweeping curve for different stressing time is shown in Fig. 9 at 175°C because temperature rise reduces threshold voltage which gives larger measured maximum current for better demonstration under the same sweeping range of V_{GS}. From the equation for MOSFET drain-source current in linear region, the threshold voltage determines the knee point of $I_{DS} - V_{GS}$ trace while mobility determines the gradient of the subsequent current rise. To investigate the impact of stressing periods on the gradient of I_D-V_{GS} curve, the threshold drift is excluded by plotting graphs of I_D against $(V_{GS} - V_{TH})$, as shown in Fig. 10. It can be seen that the overlapping of pre-stress curve on 1 ks stress curve is good on planar and symmetrical double-trench but a slight deviation is seen in asymmetrical double-trench.

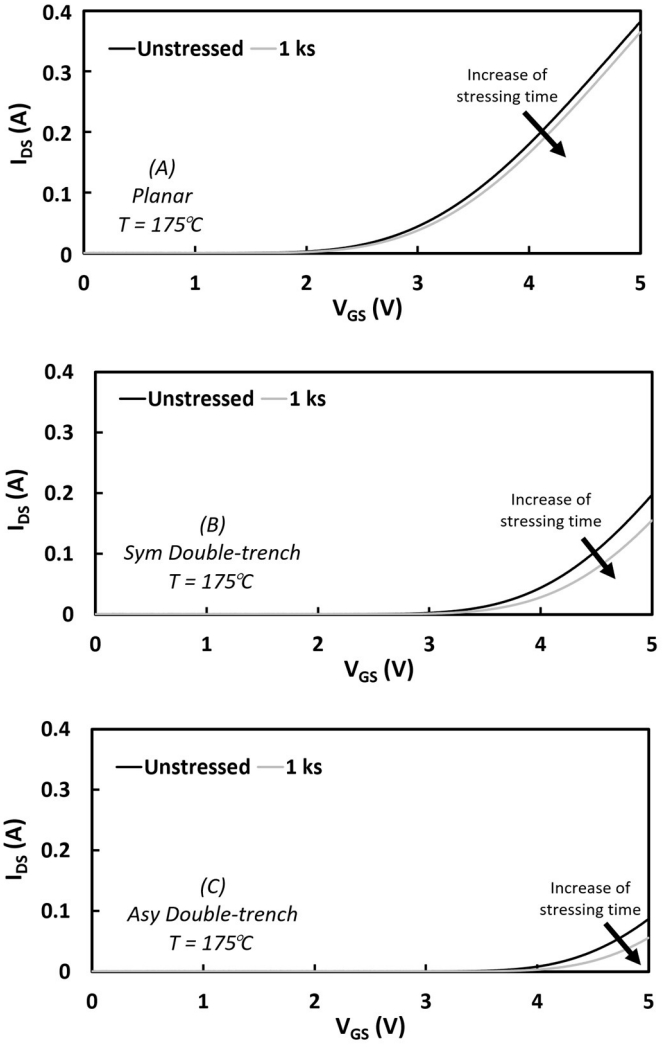

Fig. 9. The $I_{DS} - V_{GS}$ trace for 18 V positive DC stressing under 175°C of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET & (c) Asymmetrical Double-trench SiC MOSFET.

Threshold voltage drift is calculated by subtracting the initially measured threshold voltage before any stress applied from the readout at the interruption of stressing. Fig. 11 shows the results for all three DUTs at four different temperatures up to the highest allowed operating temperature 175°C. As the stressing time is increasing, there is more threshold drift as expected. It can be seen that all three DUTs follow a logarithm time behaviour, among which two double-trenched devices

show larger threshold voltage drift than the planar one. A common feature that has been observed for three DUTs is that rise of temperature damps the threshold drift. Such effect has been explained by the reduction of interface traps' capture time constant so that during the delay between removal of stress and threshold voltage measurement, the threshold drift recovered and not captured by measurement as proposed in [16]. It also shows that such damping effect of increasing temperature soon approaches saturation so that the decrease of threshold drift after the same stressing time for temperature above 75°C is not that significant as that from 25°C. This suggests that approximately 50°C rise from room temperature is sufficient to reduce the capture time constant on the interface traps.

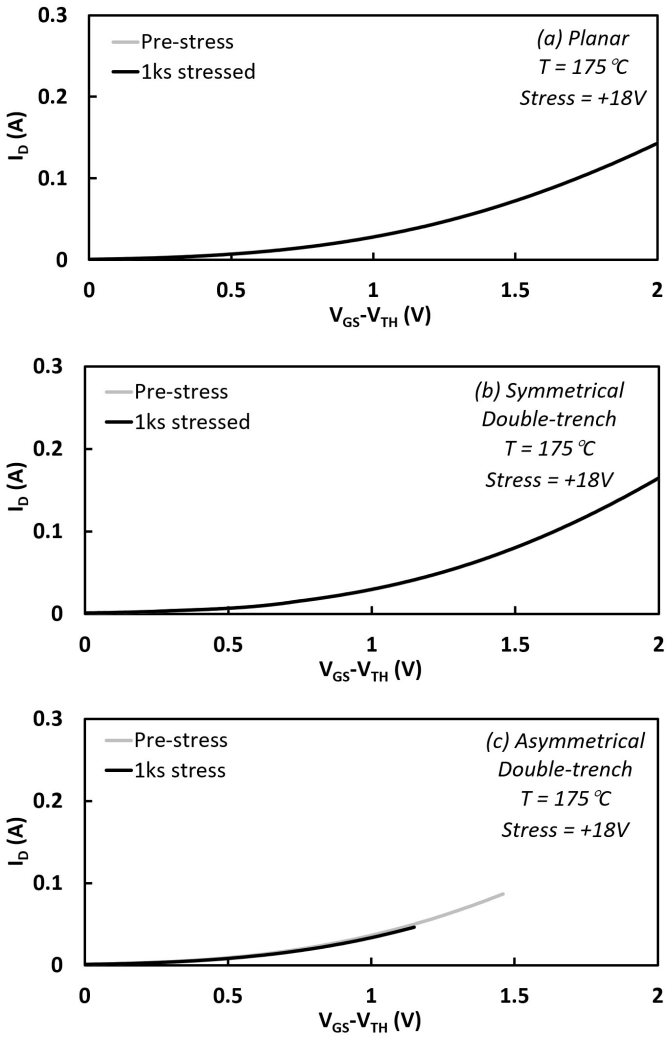

Fig. 10. $I_{DS} - (V_{GS}\text{-}V_{TH})$ trace for 18 V positive DC stressing under 175°C of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET & (c) Asymmetrical Double-trench SiC MOSFET.

The damping effect is the most noticeable as observed on two double-trenched devices especially on symmetrical double-trench MOSFET where the threshold drift is almost identical as temperature increases from 75°C to 175°C.

2.3 Negative DC Bias Stress

Negative DC voltage is applied to the gate of DUTs with the value selected to be -5V which is within the recommended operating range since SiC MOSFET could only bears a small magnitude of negative gate voltage. The experiment procedure is the same as demonstrated in Fig. 8, except the stressing voltage in this case is negative instead of positive. Fig. 12 shows the $I_{DS} - V_{GS}$ trace at sweeping for threshold voltage readout when the temperature is 175°C while Fig. 13. shows the gradient comparison on $I_{DS} - V_{GS}$ trace at sweeping by amending the x-axis to $(V_{GS} - V_{TH})$ instead of V_{GS}. The temperature is selected to be 175°C for the same reason that the measured maximum current is larger for the same sweeping range due to decline of threshold voltage.

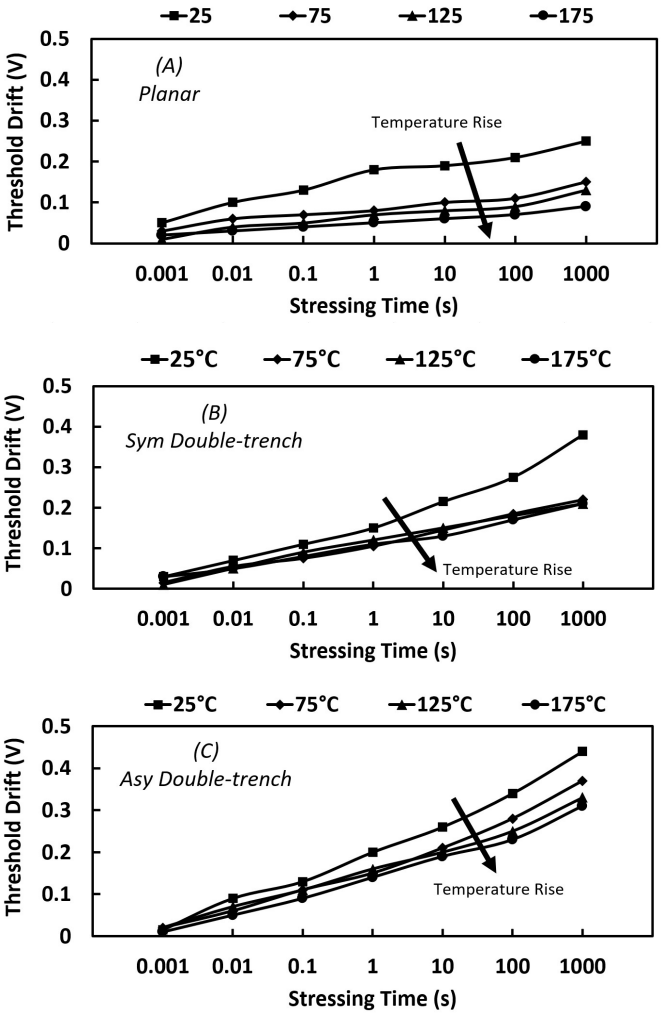

Fig. 11. Threshold voltage drift under 18 V DC bias stressing of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET and (c) Asymmetrical Double-trench SiC MOSFET.

Fig. 12 demonstrates the trace against the threshold voltage value, as the stressing time increase, the $I_{DS} - V_{GS}$ trace is shifting towards left as a consequence of electron emission and hole capture [1] yielding a threshold voltage drop. However, an intersection point between pre-stress and post-stress curve can be seen in the asymmetrical double-trench MOSFET at around 4.3 V. To better demonstrate this, Fig. 13 provides a fairer and clearer comparison by removing the impact of the different threshold voltages. As the stressing time increase, unlike the case in +18V stressing, all three devices see a milder gradient after stressing, but planar has the least extent and it is

more significant in symmetrical and asymmetrical double-trench SiC MOSFETs. Since electrons would be released from interface traps in negative gate stressing, this would increase the carrier-carrier scattering level which is the main mechanism that leads to carrier mobility degradation. This in-turn impacts the severity of potential crosstalk [17, 18] as well.

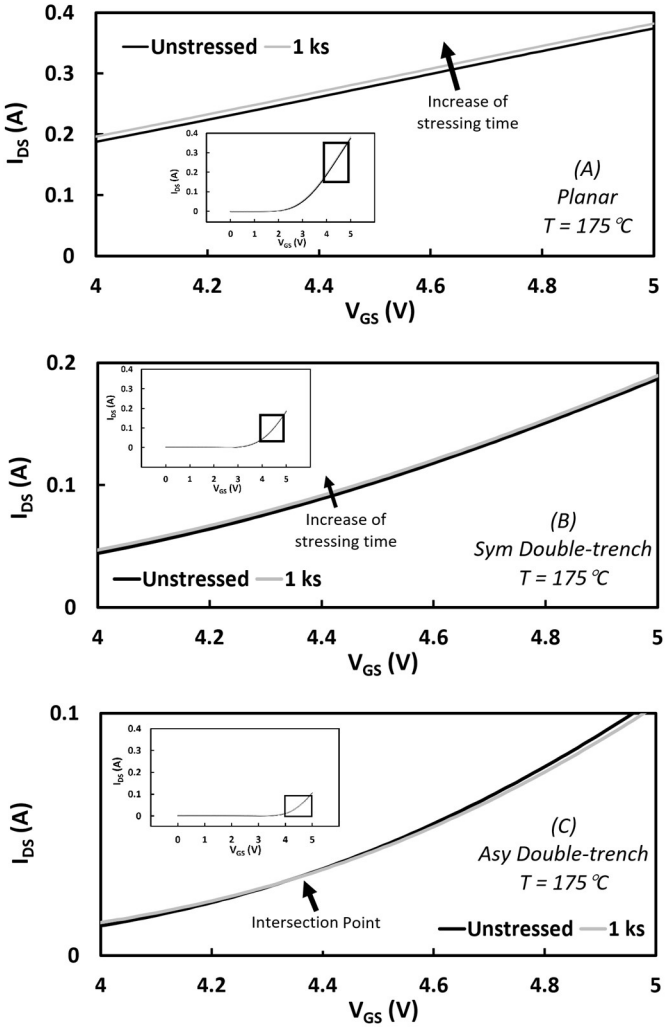

Fig. 12. The I_{DS}–V_{GS} trace for -5V negative DC stressing under 175°C of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET and (c) Asymmetrical Double-trench SiC MOSFET.

Fig. 14 shows the threshold voltage drift under -5V gate stressing at a range of temperature up to 175°C. In this case, the drift reaches saturation very fast within 1 second for planar and asymmetrical double-trench SiC MOSFET, but there is sustaining decrease of threshold voltage drift for symmetrical double-trench SiC MOSFET. In regard to the response to temperature change, planar and asymmetrical double-trench SiC MOSFET have similar trend that there is less threshold drift at higher temperature. As for planar SiC MOSFET, there is a significantly reduced threshold voltage at temperature rise to 75°C, and for the further increase, the impact of temperature reaches saturation so that there is little difference for threshold voltage drift under different temperature while the impact of temperature is more uniform across the full range up to 175°C.

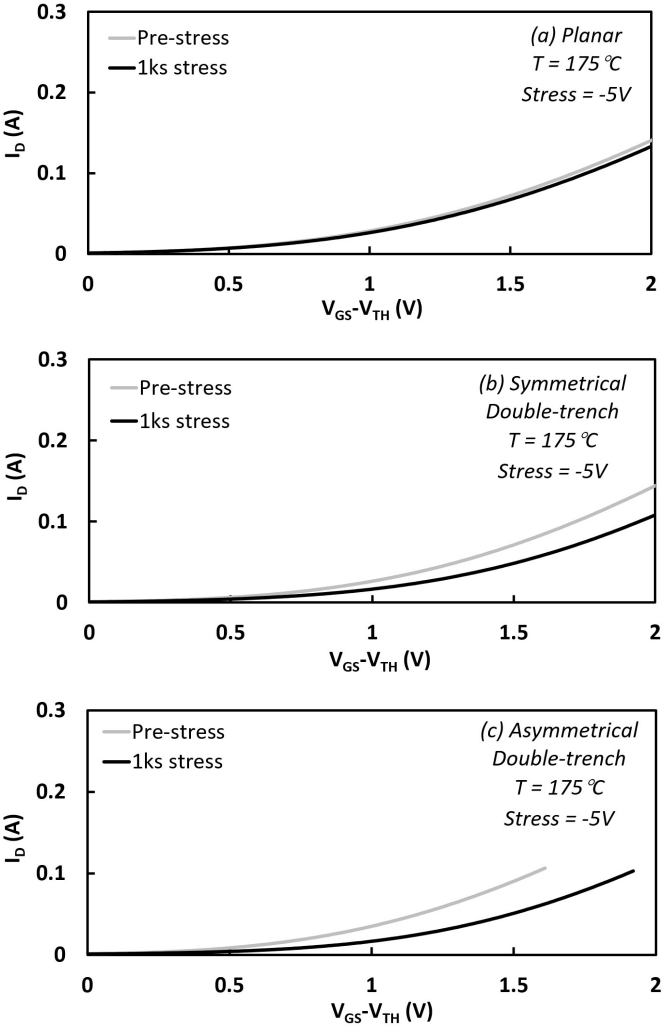

Fig. 13. The I_{DS} – (V_{GS}-V_{TH}) trace for -5V negative DC stressing under 175°C of (a) Planar SiC MOSFET, (b) Symmetrical double-trench SiC MOSFET and (c) Asymmetrical Double-trench SiC MOSFET.

The trend is opposite in symmetrical double-trench SiC MOSFET, temperature rise enables more threshold drift. As explained in [16], traps with small emission time constant also have small capture time constant, therefore, similar to the case of positive gate stressing, the reason for the observation of threshold drift to temperature on these three DUTs is that planar and asymmetrical double-trench SiC MOSFET has sufficiently small low capture and emission time constant on traps, thus at higher temperature, the threshold is easily to be shifted and recovered. As for asymmetrical double-trench SiC MOSFET, based on the same explanation given in [16], the proposed reason is that the reduction of capture and emission time constant is not balanced at increase of temperature, the emission time constant drops so that for the same stressing time the more traps contributing to more threshold drift, capture time constant, though drops as well, but not that significant as emission, so there is a net increase of the gate threshold voltage drift.

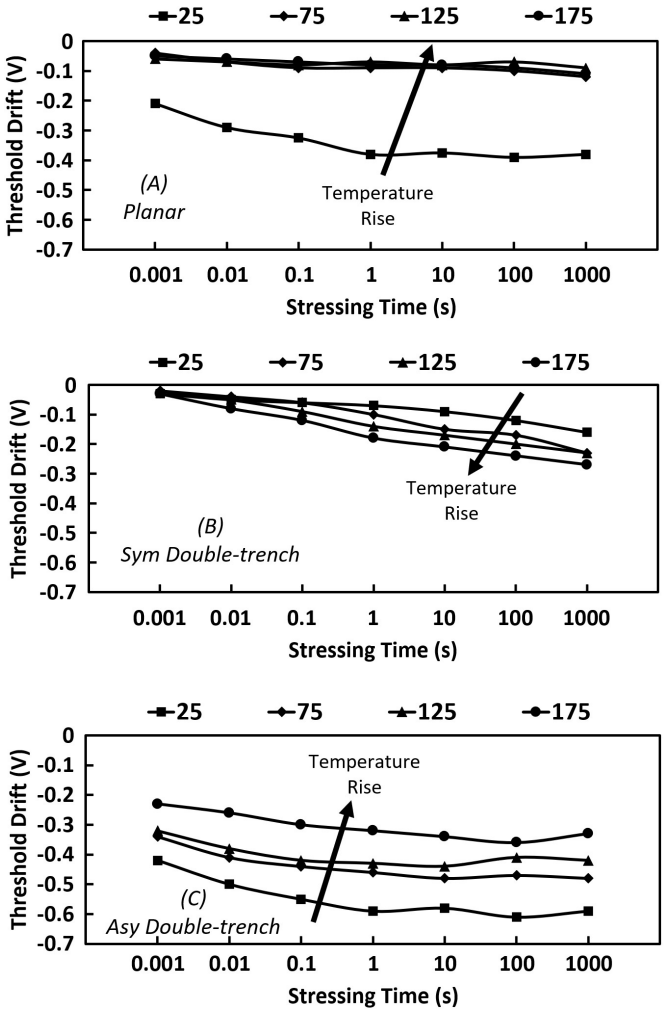

Fig. 14. Threshold voltage drift under -5V DC bias stressing of (a) Planar SiC MOSFET (b) Symmetrical double-trench SiC MOSFET and (c) Asymmetrical Double-trench SiC MOSFET.

3 Conclusion

Measurements are done on SiC planar MOSFETs together with the symmetrical and asymmetrical double trench SiC MOSFETs on their threshold voltage drift under both positive and negative DC gate voltage stressing and sweeping. In the case of positive DC gate biasing, the two double-trench SiC MOSFETs exhibit more threshold voltage drift than the planar SiC MOSFET, while temperature increase reduces the measured threshold drift for all devices. In the case of negative DC gate biasing, the device that has the most threshold drift is different at different temperatures because their response of threshold drift to temperature is distinct. It can also be seen that mobility degradation is more severe in negative gate stressing than positive gate stressing. Under positive +18 V gate stressing, only asymmetrical double-trench SiC MOSFET exhibits evident mobility degradation while on -5 V negative gate stressing measurements, all three devices exhibit mobility degradations with the least effect on the planar one.

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